# About Me

But there is more too engineering that just the physical and concrete. We are the creators of the future, so our actions today not only affect the lives of those around us, but also the lives

of those who will succeed us. We must design and build a world that reflects the best in humanity, and pass down a sustainable legacy that can grow and evolve with the needs of the times.

With this in mind, I want to help usher in the future. I am a hardware engineer at a stealth startup aiming to democratize hardware design for the masses. We are building a modular and customizable hardware and software solution that allows for the rapid bring-up of ASIC-like designs without the multi-million dollar costs or year-long design schedules. As the Lead Digital Design Engineer, it is my responsibility to create a system that is scalable, accessible, and resilient. Our product will ease the development of everything from small form-factor wearables such as biometric sensor rings to mission critical control systems like autonomous driving vehicle hardware arrays. There is still a lot of work ahead of us, but the challenge is exciting and fun.

If you like to learn more about me or my company, please feel free to contact me. Thank you for visiting my website.

# Experience

I graduated from Cornell University with a Bachelors in Electrical and Computer Engineering in the Winter of 2011. My first job out of college was at Intel in Oregon, where I worked as a Formal Verification Engineer on the Haswell/Broadwell architecture, validating hardware virtualization and the Uncore System Agent. This eventually transitioned to a Validation Engineer role on the Input/Output Memory Management Unit, a modular and scalable Soft-IP for VT-d and SVM that is used internally in all Intel architectures ranging from mobile to HPC.

In 2015, I move to the Bay Area and transferred internally to Intel’s Server division. There, I was a Design Engineer on Cannonlake Server and owned both Core Hard-IP integration and System Agent VT-d Design using the IOMMU. With respect to Core HIP Integration, I coordinated a multi-site design and validation team across the US, India, and Israel to insure that the CNX Core was properly validated and integrated on schedule.

In 2016, I decided to leave Intel and pursue other opportunities. I wanted to see what else was out there, and to see what it was like working in a smaller, more agile environment. Hence, I am now working in a stealth startup developing a product which targets both the IoT market and smaller companies without the budget for full scale hardware design divisions. Having put on multiple hats within the company, I have learned a lot and have been exposed to a lot more than I would have at Intel since joining. I have basically owned the full front-end design stack, from architecture, design, and validation to synthesis, timing, analog interfacing, backend interfacing, and FPGA prototyping. Though I definitely do miss the support that a big company offers, I love having the freedom of tackling a design problem without being burdened by bureaucracy.

Since moving to California, I decided to continue my education to broaden my perspective in the semiconductor industry as well as learn more about IoT and software design. As such, I’ve enrolled in Stanford’s Honor’s Coop Program, a part-time graduate program that allows me to pursue my Masters in Electrical Engineering while still working full-time. I will be finished by the Spring of 2017, with a EE focus in Hardware and Software System Design.