

Mi primer proyecto con el Microchip Curiosity Nano PIC18F57Q43 empleando XC8 PIC Assembler

Por Kalun Lau
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El Curiosity Nano PIC18F57Q43 de Microchip

Documentación:

- Part number: DM164150
- Product page: <https://www.microchip.com/en-us/product/PIC18F57Q43#>
- Datasheet: <https://ww1.microchip.com/downloads/aemDocuments/documents/MCU08/ProductDocuments/DataSheets/PIC18F27-47-57Q43-Data-Sheet-40002147F.pdf>
- Curiosity Board for PIC18F57Q43: <http://ww1.microchip.com/downloads/en/DeviceDoc/PIC18F57Q43-Curiosity-Nano-HW-UserGuide-DS40002186B.pdf>
- PIC18F57Q43 Curiosity Nano Hardware User Guide: <https://onlinedocs.microchip.com/pr/GUID-5D38BF5C-8481-46C4-BD08-1B8F4C7289B2-en-US-2/index.html>

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El Curiosity Nano PIC18F57Q43 de Microchip

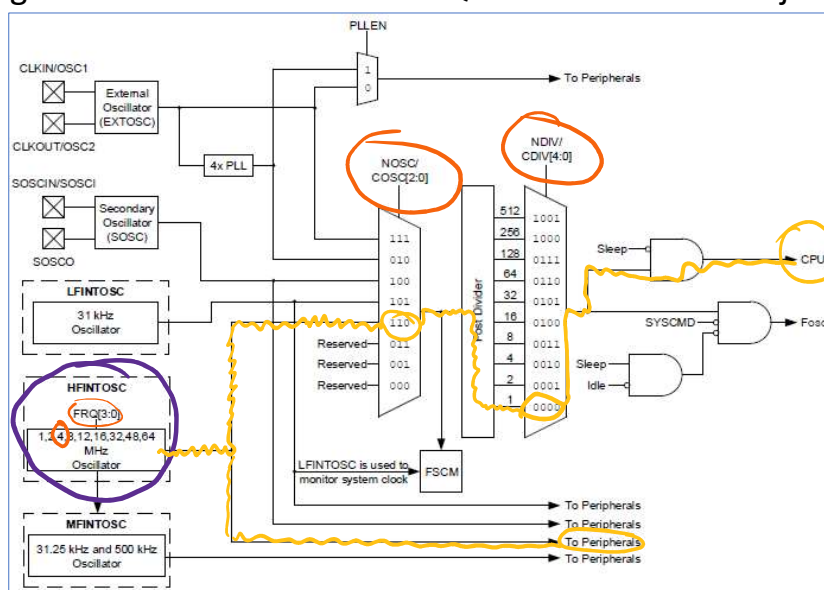
- Configuración inicial del PIC18F57Q43: Los bits de configuración

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x300000	CONFIG1	7:0		RSTOSC[2:0]				FEXTOSC[2:0]		
0x300001	CONFIG2	7:0			FCMEN		CSWEN		PR1WAY	CLKOUTEN
0x300002	CONFIG3	7:0	BOREN[1:0]		LPBOREN	IVT1WAY	MVECEN	PWRTS[1:0]		MCLRRE
0x300003	CONFIG4	7:0	XINST		LVP	STVREN	PPS1WAY	ZCD	BORV[1:0]	
0x300004	CONFIG5	7:0		WDTE[1:0]				WDTCP5[4:0]		
0x300005	CONFIG6	7:0				WDTCC5[2:0]			WDTCWS[2:0]	
0x300006	CONFIG7	7:0			DEBUG	SAFEN	BBEN	BBSIZE[2:0]		
0x300007	CONFIG8	7:0	WRTAPP				WRTSAF	WRTD	WRTC	WRTB
0x300008	CONFIG9	7:0								
0x300009	CONFIG10	7:0								CP

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- Configuración inicial del PIC18F57Q43: La fuente de reloj



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El Curiosity Nano PIC18F57Q43 de Microchip

- Estructura de la memoria de programa del PIC18F57Q43:
 - 128Kbyte de capacidad (000000H-01FFFFH)
 - Data EEPROM (1Kbyte) se encuentra mapeado en 380000H

Address	Device		
	PIC18Fx5Q43	PIC18Fx6Q43	PIC18Fx7Q43
00 0000h to 00 3FFFh	Program Flash Memory (16 KW) ⁽¹⁾	Program Flash Memory (32 KW) ⁽¹⁾	Program Flash Memory (54 KW) ⁽¹⁾
00 4000h to 00 7FFFh			
00 8000h to 00 FFFFh			
01 0000h to 01 FFFFh	Not Present ⁽²⁾	Not Present ⁽²⁾	Not Present ⁽²⁾
02 0000h to 1F FFFFh	User IDs (32 Words) ⁽²⁾		
20 0000h to 20 003Fh	Reserved		
20 0040h to 2B FFFFh	Device Information Area (DIA) ^(3,4)		
2C 0000h to 2C 00FFh	Reserved		
2C 0100h to 2F FFFFh	Configuration Bytes ⁽⁵⁾		
30 0000h to 30 0009h	Reserved		
30 000Ah to 37 FFFFh	Data EEPROM (1024 Bytes)		
38 0000h to 38 00FFh	Reserved		
38 0100h to 3B FFFFh	Device Configuration Information ^(3,4,6)		
3C 0000h to 3C 0009h	Reserved		
3C 000Ah to 3F FFFFh	Revision ID (1 Word) ^(3,4,6)		
3F 0000h to 3F FFFFh	Device ID (1 Word) ^(3,4,6)		

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- Estructura de la memoria de datos del PIC18F57Q43:
 - A diferencia del PIC18F45K50, la memoria RAM esta mapeada a partir del Bank 5 (500H) y los registros de funciones especiales (SFR) se encuentran entre Bank 0 y Bank 4
 - Tener en cuenta que la RAM de datos es de 8Kbyte

Bank	BSR add[13:8]	add[7:0]	PIC18F	
			x5Q43	x6Q43
0	'b00 0000	0x00-0xFF		
1	'b00 0001	0x00-0xFF		
2	'b00 0010	0x00-0xFF		
3	'b00 0011	0x00-0xFF		
4	'b00 0100	0x00-0xFF		
5	'b00 0101	0x00-0xFF		
6	'b00 0110	0x00-0xFF		
7	'b00 0111	0x00-0xFF		
8	'b00 1000	0x00-0xFF		
9	'b00 1001	0x00-0xFF		
10	'b00 1010	0x00-0xFF		
11	'b00 1011	0x00-0xFF		
12	'b00 1100	0x00-0xFF		
13	'b00 1101	0x00-0xFF		
14	'b00 1110	0x00-0xFF		
15	'b00 1111	0x00-0xFF		
16	'b01 0000	0x00-0xFF		
17	'b01 0001	0x00-0xFF		
18	'b01 0010	0x00-0xFF		
19	'b01 0011	0x00-0xFF		
20	'b01 0100	0x00-0xFF		
21	'b01 0101	0x00-0xFF		
22	'b01 0110	0x00-0xFF		
23	'b01 0111	0x00-0xFF		
24	'b01 1000	0x00-0xFF		
25	'b01 1001	0x00-0xFF		
26	'b01 1010	0x00-0xFF		
27	'b01 1011	0x00-0xFF		
28	'b01 1100	0x00-0xFF		
29	'b01 1101	0x00-0xFF		
30	'b01 1110	0x00-0xFF		
31	'b01 1111	0x00-0xFF		
32	'b10 0000	0x00-0xFF		
33	'b10 0001	0x00-0xFF		
34	'b10 0010	0x00-0xFF		
35	'b10 0011	0x00-0xFF		
36	'b10 0100	0x00-0xFF		
37	'b10 0101	0x00-0xFF		
38	'b10 0110	0x00-0xFF		
39	'b10 0111	0x00-0xFF		
40	'b10 1000	0x00-0xFF		
41	'b10 1001	0x00-0xFF		
42	'b10 1010	0x00-0xFF		
43	'b10 1011	0x00-0xFF		
44	'b10 1100	0x00-0xFF		
45	'b10 1101	0x00-0xFF		
46	'b10 1110	0x00-0xFF		
47	'b10 1111	0x00-0xFF		
48	'b11 0000	0x00-0xFF		
49	'b11 0001	0x00-0xFF		
50	'b11 0010	0x00-0xFF		
51	'b11 0011	0x00-0xFF		
52	'b11 0100	0x00-0xFF		
53	'b11 0101	0x00-0xFF		
54	'b11 0110	0x00-0xFF		
55	'b11 0111	0x00-0xFF		
56	'b11 1000	0x00-0xFF		
57	'b11 1001	0x00-0xFF		
58	'b11 1010	0x00-0xFF		
59	'b11 1011	0x00-0xFF		
60	'b11 1100	0x00-0xFF		
61	'b11 1101	0x00-0xFF		
62	'b11 1110	0x00-0xFF		
63	'b11 1111	0x00-0xFF		

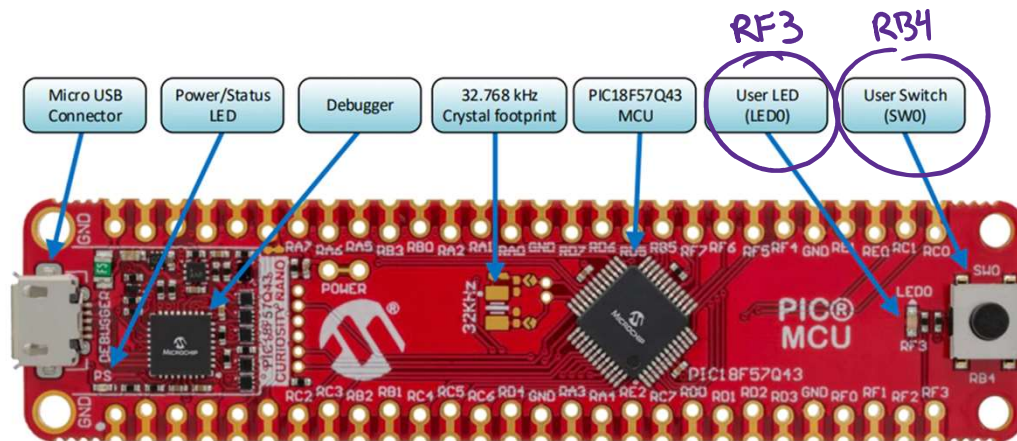
Virtual Access Bank
Access RAM 0x00-0x5F
Fast SFR 0x60-0xFF

GPR
SFR
Buffer RAM
Unimplemented

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El Curiosity Nano PIC18F57Q43 de Microchip

- Primer ejemplo: Un negador lógico de un bit empleando el pulsador y el LED integrados en el Curiosity Nano



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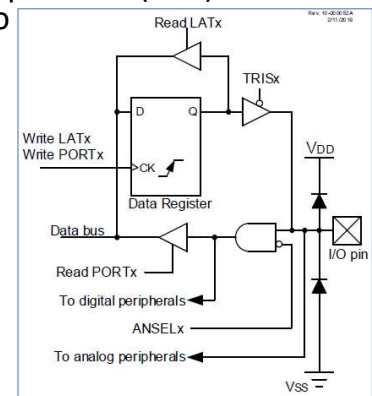
El Curiosity Nano PIC18F57Q43 de Microchip

Configuraciones iniciales

- Reloj: Se usará el HFINTOSC a 4MHz para alimentar al CPU
 - OSCCON1 = 60H para que HFINTOSC sea la fuente y divisor sea 1:1
 - OSCFRQ = 02H para que HFINTOSC sea de 4MHz
 - OSCCON.6 = 1 para que se habilite HFINTOSC

- Puertos de E/S: Tener en cuenta que tanto LED (RF3) como pulsador (RB4) integrados en el Curiosity Nano son del tipo activos en bajo

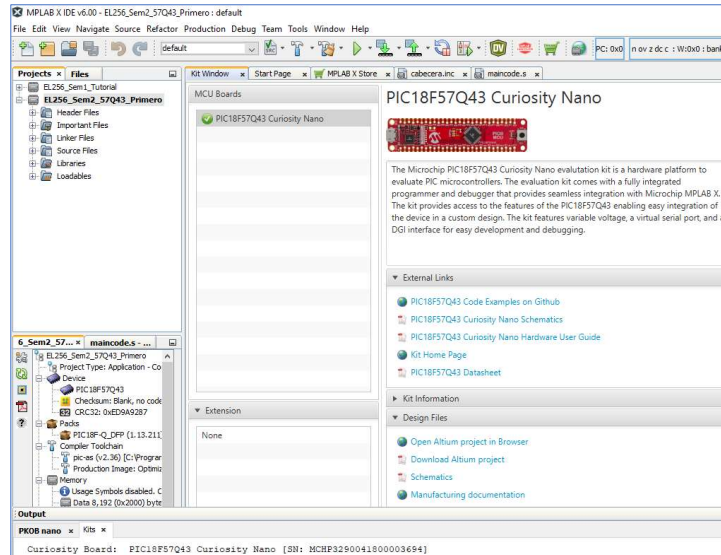
- TRISB.4 = 1 para que sea una entrada
- ANSELB.4 = 0 para que sea digital
- WPUB.4 = 1 para activar resistencia interna de pull-up
- TRISF.3 = 0 para que sea una salida
- ANSELF.3 = 0 para que sea digital



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El Curiosity Nano PIC18F57Q43 de Microchip

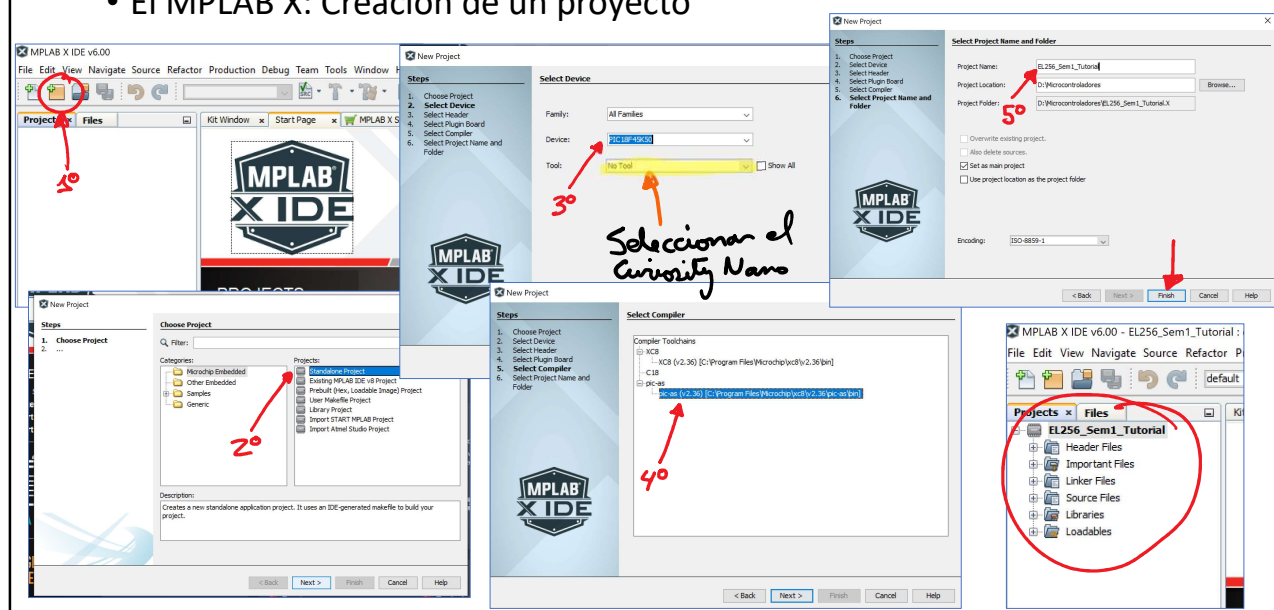
- El MPLAB X: Al conectar el Curiosity Nano



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El Curiosity Nano PIC18F57Q43 de Microchip

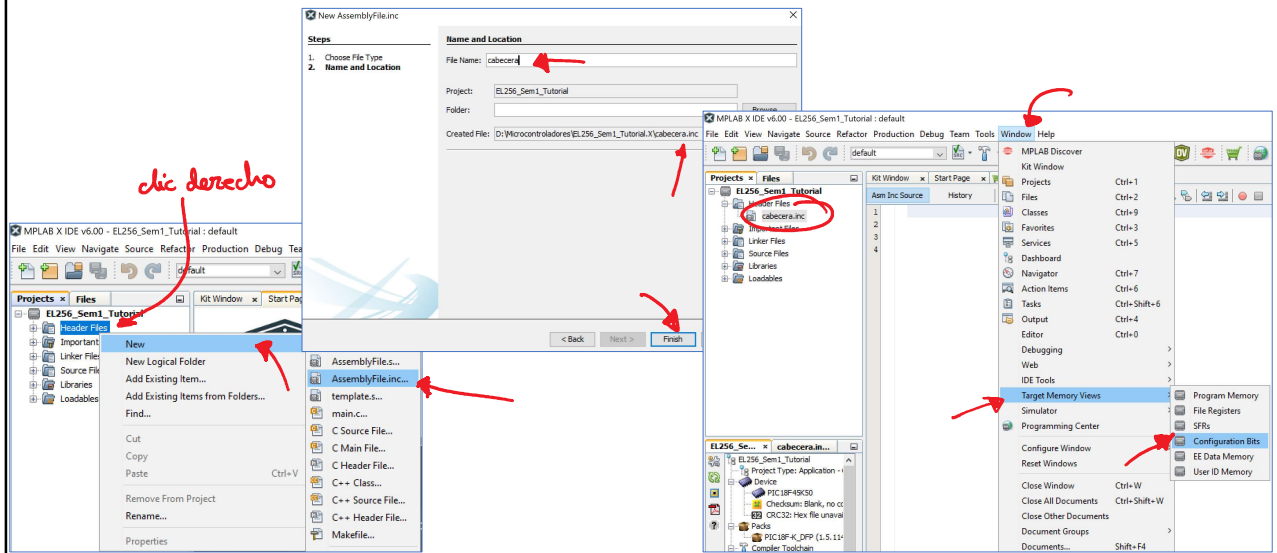
- El MPLAB X: Creación de un proyecto



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El Curiosity Nano PIC18F57Q43 de Microchip

- Creación de cabecera.inc



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El Curiosity Nano PIC18F57Q43 de Microchip

- El MPLAB X: Configuration bits

Address	Name	Value	Field	Option	Category	Setting
300000	CONFIG1	FF	-	-	-	-
		7	FEXTOSC	ECH	External Oscillator Selection	EC (external clock) above 8 MHz
		7	RSTOSC	EXTOSC	Reset Oscillator Selection	EXTOSC operating per FEXTOSC bits (device manufacturing default)
300001	CONFIG2	FF	-	-	-	-
		1	CLKROUTEN	OFF	Clock out Enable bit	CLKROUT function is disabled
		1	PRIMWAY	ON	PRLOCKED One-Way Set Enable bit	PRLOCKED bit can be cleared and set only once
		1	CSWEN	ON	Clock Switch Enable bit	Writing to WOSC and WDIV is allowed
		1	PCMEN	ON	Fail-Safe Clock Monitor Enable bit	Fail-Safe Clock Monitor enabled
300002	CONFIG3	FF	-	-	-	-
		1	MCLRRE	EXTMCLR	MCLR Enable bit	If LVP = 0, MCLR pin is MCLR; If LVP = 1, RE3 pin function is MCLR
		3	PWRTS	PWRT_OFF	Power-up timer selection bits	PWRT is disabled
		1	MVECEN	ON	Multi-vector enable bit	Multi-vector enabled, Vector table used for interrupts
		1	IVTLOCK	ON	IVTLOCK bit One-way set enable bit	IVTLOCKED bit can be cleared and set only once
		1	LPF0REN	OFF	Low Power BOR Enable bit	Low-Power BOR disabled
		3	BORREN	SBORDIS	Brown-out Reset Enable bits	Brown-out Reset enabled, SBORREN bit is ignored
300003	CONFIG4	FF	-	-	-	-
		1	BORV	VBOR_IP9	Brown-out Reset Voltage Selection bits	Brown-out Reset Voltage (VBOR) set to 1.9V
		1	ZCD	OFF	ZCD Disable bit	ZCD module is disabled. ZCD can be enabled by setting the ZCDSEN bit of ZCDCON
		1	PFSLOCK	ON	PFSLOCK bit One-Way Set Enable bit	PFSLOCKED bit can be cleared and set only once; PFS registers remain locked after one clear/set cycle
		1	STVREN	ON	Stack Full/Underflow Reset Enable bit	Stack full/underflow will cause Reset
		1	LVP	ON	Low Voltage Programming Enable bit	Low voltage programming enabled; MCLR/VPP pin function is MCLR. MCLRRE configuration bit is ignored
		1	WINTST	OFF	Extended Instruction Set Enable bit	Extended Instruction Set and Indexed Addressing Mode disabled
300004	CONFIG5	FF	-	-	-	-
		1F	WDTCPR	WDTCPRS_31	WDT Period selection bits	Divider ratio 1:65536; software control of WDTFS
		3	WDTE	ON	WDT operating mode	WDT enabled regardless of sleep; SWDTEN is ignored
300005	CONFIG6	FF	-	-	-	-
		7	WDTCS	WDTCS_7	WDT Window Select bits	window always open (100%); software control; keyed access not required
		7	WDTCS	SC	WDT input clock selector	Software Control
300006	CONFIG7	FF	-	-	-	-
		7	BBSIZE	BBSIZE_512	Boot Block Size selection bits	Boot Block size is 512 words
		1	BREN	OFF	Boot Block enable bit	Boot block disabled
		1	SAFEN	OFF	Storage Area Flash enable bit	SAF disabled
		1	DEBUG	OFF	Background Debugger	Background Debugger disabled
300007	CONFIG8	FF	-	-	-	-
		1	WRWB	OFF	Boot Block Write Protection bit	Boot Block not Write protected
		1	WRWC	OFF	Configuration Register Write Protection bit	Configuration registers not Write protected
		1	WRWD	OFF	Data EEPROM Write Protection bit	Data EEPROM not Write protected
		1	WRWSAF	OFF	SAF Write protection bit	SAF not Write Protected
		1	WRWAPP	OFF	Application Block write protection bit	Application Block not write protected
300009	CONFIG10	FF	-	-	-	-
		7	CP	OFF	FPN and Data EEPROM Code Protection bit	FPN and Data EEPROM code protection disabled

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El Curiosity Nano PIC18F57Q43 de Microchip

- El MPLAB X: Configuration bits
 - Habilitar power-up timer a 16ms
 - Deshabilitar Brown-out reset
 - Deshabilitar LVP
 - Deshabilitar watchdog timer

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El Curiosity Nano PIC18F57Q43 de Microchip

- El MPLAB X: El contenido final del archivo header o cabecera (extensión *.inc)

```

2  ; PIC18F57Q43 Configuration Bit Settings
3
4  ; Assembly source line config statements
5
6  ; CONFIG1
7  CONFIG FEXTOSC = OFF      ; External Oscillator Selection (Oscillator not
8  CONFIG RSTOSC = EXTOSC    ; Reset Oscillator Selection (EXTOSC operating p
9
10 ; CONFIG2
11 CONFIG CLKOUTEN = OFF      ; Clock out Enable bit (CLKOUT function is disab
12 CONFIG PRIWAY = ON         ; PRLOCKED One-Way Set Enable bit (PRLOCKED bit
13 CONFIG CSWEN = ON          ; Clock Switch Enable bit (Writing to WOSC and N
14 CONFIG FCMEN = ON          ; Fail-Safe Clock Monitor Enable bit (Fail-Safe
15
16 ; CONFIG3
17 CONFIG MCLR = EXTMCCLR     ; MCLR Enable bit (If LVP = 0, MCLR pin is MCLR;
18 CONFIG PWRTS = PWRT_16    ; Power-up timer selection bits (PWRT set at 16ms
19 CONFIG MVECEN = ON         ; Multi-vector enable bit (Multi-vector enabled,
20 CONFIG IVT1WAY = ON        ; IVTLOCK bit One-way set enable bit (IVTLOCKED
21 CONFIG LPBORN = OFF        ; Low Power BOR Enable bit (Low-Power BOR disabl
22 CONFIG BOREN = OFF         ; Brown-out Reset Enable bits (Brown-out Reset d
23
24 ; CONFIG4
25 CONFIG BORV = VBOR_1P9     ; Brown-out Reset Voltage Selection bits (Brown-
26 CONFIG ZCD = OFF           ; ZCD Disable bit (ZCD module is disabled. ZCD d
27 CONFIG PPS1WAY = ON        ; PPSLOCK bit One-Way Set Enable bit (PPSLOCKED
28 CONFIG STVREN = ON         ; Stack Full/Underflow Reset Enable bit (Stack f
29 CONFIG LVP = OFF           ; Low Voltage Programming Enable bit (HV on MCLR
30 CONFIG XINST = OFF         ; Extended Instruction Set Enable bit (Extended
31
32 ; CONFIG5
33 CONFIG WDTCP5 = WDTCP5_31  ; WDT Period selection bits (Divider ratio 1:655
34 CONFIG WDTE = OFF          ; WDT operating mode (WDT Disabled; SWDTEN is ig
35
36 ; CONFIG6
37 CONFIG WDTWNS = WDTWNS_7   ; WDT Window Select bits (window always open (10
38 CONFIG WDTCCS = SC         ; WDT input clock selector (Software Control)

```

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El Curiosity Nano PIC18F57Q43 de Microchip

- El MPLAB X: El archivo source o fuente (extensión *.s)

```

1 ;Este es un comentario
2 ;Ejemplo hecho por Kalun ps
3 PROCESSOR 18F57Q43 ;modelo de micro
4 #include "cabecera.inc" ;llamada a cabecera
5
6
7 PSECT upcino, class=CODE, reloc=2, abs ;program section
8 upcino: ;etiqueta upcino
9 ORG 000000H ;vector de reset
10 goto configuro ;salto a etiqueta configuro
11
12 ORG 000020H ;zona de prog de usuario
13 configuro: ;etiqueta configuro
14 ;aqui van los registros de conf para el reloj
15 movlb 0H ;bank0 al access bank
16 movlw 60H
17 movwf OSCCON1 ;HFINTOSC con divisor a 1:1
18 movlw 02H
19 movwf OSCFREQ ;HFINTOSC a 4MHz
20 bsf OSCEN, 6 ;HFINTOSC habilitado
21 ;aqui van los registros de conf para las E/S
22 movlb 4H ;bank4 al access bank
23 bsf TRISE, 4 ;RB4 como entrada
24 bcf ANSELB, 4 ;RB4 como digital
25 bsf WPUB, 4 ;RB4 activado su pull-up
26 bcf TRISF, 3 ;RF3 como salida
27 bcf ANSELF, 3 ;RF3 como digital
28
29 loop: ;etiqueta loop
30 ;programa de usuario
31 btfs PORTB, 4 ;pregunto si RA0 es uno
32 goto nah ;F a la preg anterior, salta a etiqueta nah
33 bcf LATF, 3 ;V a la preg anterior, RC0 a cero
34 goto loop ;salto a etiqueta loop
35 nah:
36 bsf LATF, 3 ;RC0 a uno
37 goto loop ;salto a etiqueta loop
38 end upcino ;fin de program section

```

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El Curiosity Nano PIC18F57Q43 de Microchip

- El MPLAB X: Compilación del proyecto y grabado del microcontrolador

no compile *compilar y grabar el dispositivo*

The screenshot shows the MPLAB X IDE interface. The 'Projects' window on the left lists the project 'EL256_Sem2_57Q43_Primer0'. The 'Output' window on the right shows the build process, including the generation of the production.hex file and the connection to the Curiosity Nano board for programming. The 'Output' window also shows the 'make' command being executed, which builds the project and programs the device.

```

make -f nbproject/Makefile-default.mk SUBPROJECTS= .build-conf
make[1]: Entering directory 'D:/Microcontroladores/EL256_Sem2_57Q43_Primer0'
make -f nbproject/Makefile-default.mk dist/default/production
make[2]: Entering directory 'D:/Microcontroladores/EL256_Sem2_57Q43_Primer0'
make[2]: 'dist/default/production/EL256_Sem2_57Q43_Primer0.X.production.hex' is up to date.
make[2]: Leaving directory 'D:/Microcontroladores/EL256_Sem2_57Q43_Primer0.X'
make[1]: Leaving directory 'D:/Microcontroladores/EL256_Sem2_57Q43_Primer0.X'

BUILD SUCCESSFUL (total time: 291ms)
Loading code from D:/Microcontroladores/EL256_Sem2_57Q43_Primer0.X/dist/default/production/EL256_Sem2_57Q43_Primer0.X.production.hex...
Program loaded with pack, PIC18F-Q_DFP, 1.13.211, Microchip
Loading completed
Connecting to programmer...
Programming target...
Programming completed
Running target...

```

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El Curiosity Nano PIC18F57Q43 de Microchip

- Pruebas en físico:

