R3 - Hardware Training 2

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7.4.2 Astable Operation

If the circuit is connected as shown in Figure 14 (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

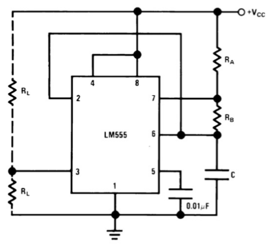
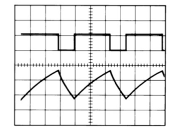


Figure 14. Astable

timer runs on a V_{cc} from 5^V-15^V standard.

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Device Functional Modes (continued)



V_{CC} = 5 V
TIME = 20μs/DIV.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 μF

Top Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

Figure 15. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693 (R_A + R_B) C \quad (1)$$

And the discharge time (output low) by:

$$t_2 = 0.693 (R_B) C \quad (2)$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693 (R_A + 2R_B) C \quad (3)$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2 R_B) C} \quad (4)$$

Figure 16 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B} \quad (5)$$

since R_A is neglegeable

$T = 1.386 R_B C$

$T = 1s \Rightarrow \boxed{C = \frac{0.7215}{R_B}}$

for 50% duty $R_A \ll R_B$

$\Rightarrow D \approx \frac{R_B}{2R_B} = 50\%$

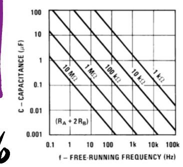


Figure 16. Free Running Frequency

We want Astable configuration for a constant clock pulse.

about 100x

↳ To make R_A negleable but still usable (won't blow) we can make it $R_A = 1k\Omega$ with it's counterpart $R_B = 100^{k\Omega}$

This makes $D = 49.8\%$ which is tolerable for this application

↳ Now that we have our duty matched, we need 1s uptime for the LED

$\Rightarrow$ high for 50% a period, so $T = 2s$ gives us this desired value

$$C \approx \frac{0.7215}{150k\Omega} = 4.81\mu F$$

∴ this is not a commonly rated capacitor, so we will use a 4.7μF/6.3V electrolytic capacitor instead.

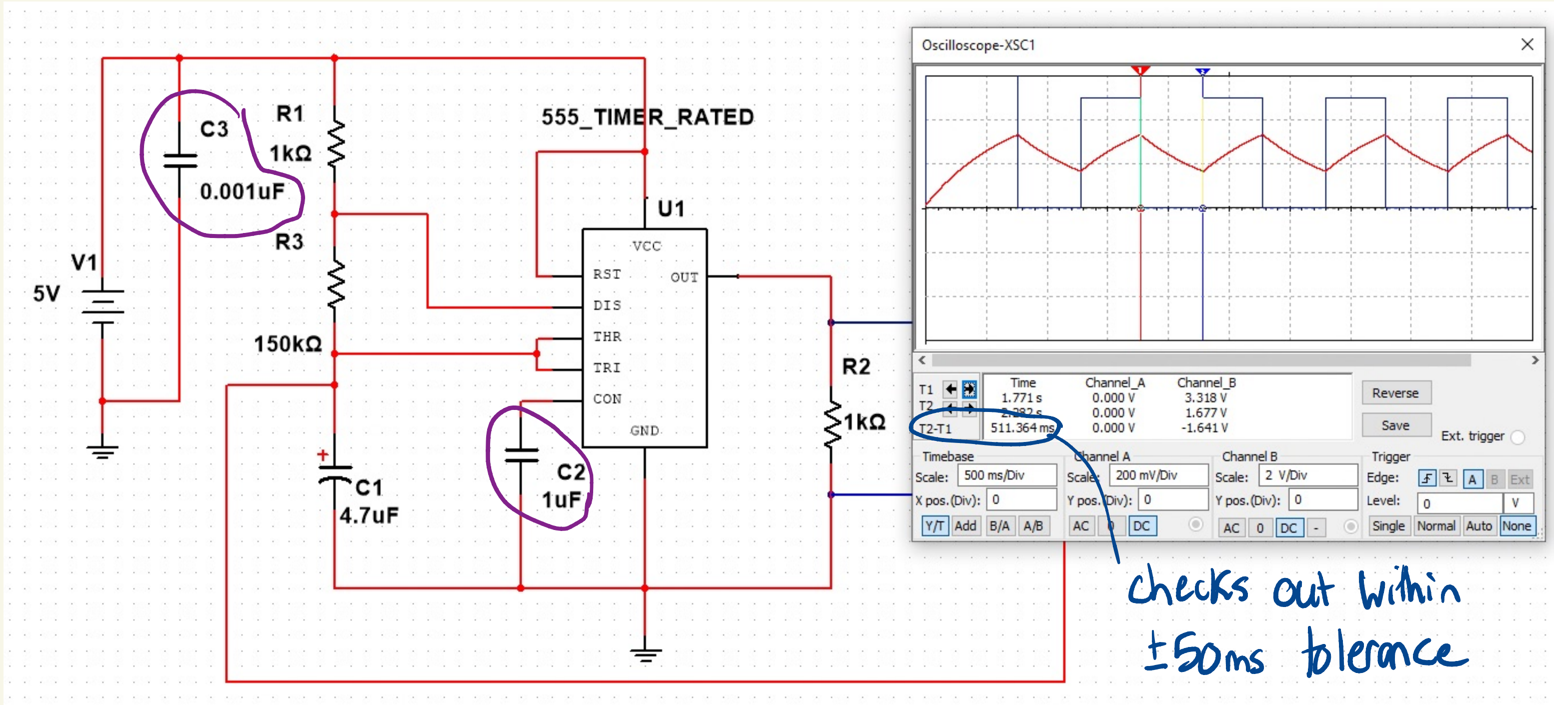
↳ This capacitor yields a

$T = 0.693(1k + 300k)4.7\mu F$

$= 0.9804s$

$\Rightarrow$ 0.49s on time

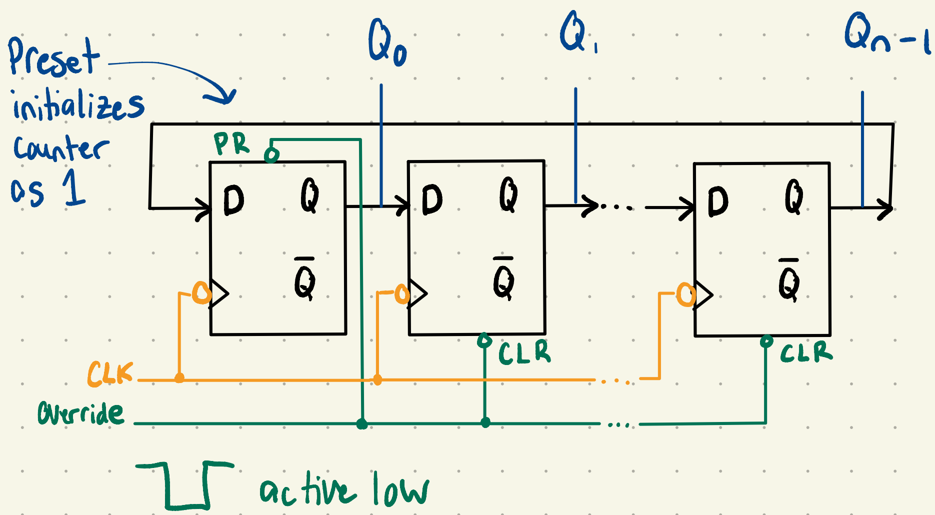
↳ I verified these values on Multisim and everything worked, but was not consistent until I added C_2 & C_3.



C_2 minimizes the noise in the circuit (as depicted by datasheet)

C_3 limits overpulling current from V_{cc}, more consistent

Dual channel FF has +7V max V_{cc}. Limit it to 5.0V



Ring Counter, the schematic provided isn't 100% correct