DESIGN AND INVESTIGATION OF 3D FinFET USING SENTAURUS TCAD

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DECLARATION

"DESIGN AND INVESTIGATION OF
3D FinFET USING SENTAURUS TCAD TOOL"

We declare that the art on display is mostly comprised of our own ideas and work, expressed in our own words. Where other people's thoughts or words were used, we properly cited and noted them in the reference materials. We have followed all academic honesty and integrity principles.

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ABSTRACT

This report provides a comprehensive analysis of 12nm FinFET technology using Sentaurus TCAD (Technology Computer-Aided Design) software. The primary goal is to evaluate the performance and scalability of FinFET devices at the 12nm node. By leveraging Sentaurus TCAD tools—specifically Sentaurus structure editor, Sentaurus Device and SVisual—this study simulates key device characteristics, optimizes performance metrics, and assesses the effects of process variations. Results indicate that FinFET technology offers substantial advantages over traditional planar transistors, including enhanced drive currents, reduced leakage currents, and improved overall performance.

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CHAPTER

1

INTRODUCTION

In the ever-evolving field of semiconductor technology, the continuous push towards smaller technology nodes presents both opportunities and challenges. The transition from planar transistors to FinFETs (Fin Field-Effect Transistors) represents a significant advancement in addressing these challenges. As devices approach the 12nm node, planar MOSFETs face increasing difficulties, including elevated leakage currents and diminished electrostatic control. FinFETs offer a promising alternative by providing improved control over the channel due to their three-dimensional structure.

This report focuses on the utilization of Sentaurus TCAD software to simulate and optimize 12 nm FinFET devices. Sentaurus TCAD, developed by Synopsys, is a suite of powerful tools designed to model semiconductor devices and processes. By leveraging Sentaurus Device for electrical simulations and Sentaurus Process for process simulations, this study aims to thoroughly evaluate the performance of 12nm FinFETs and identify key factors influencing their behavior. Through detailed simulations, this report aims to provide insights into the effectiveness of FinFET technology and its advantages over traditional planar transistors.

CHAPTER

2

FinFET Technology

2.1 History and Evolution

The FinFET technology was introduced to address the limitations inherent in planar MOSFETs as transistor sizes continued to shrink below the 20nm node. As the demand for faster and more efficient transistors grew, traditional planar MOSFETs began to exhibit severe short-channel effects and leakage currents that hindered performance.

- Early 2000s: The initial concept of FinFETs was proposed as a potential solution to the scaling challenges faced by planar transistors. Researchers recognized that a 3D gate structure could offer improved electrostatic control and reduced leakage.
- 2006: Intel became one of the first companies to incorporate FinFET technology into its 45nm process node, marking a significant advancement in semiconductor technology.
- 2012: The widespread adoption of FinFETs in the 22nm and 14nm process nodes demonstrated the technology's effectiveness in enhancing device performance and scaling to smaller nodes.

The evolution of FinFET technology underscores its role as a pivotal development in semiconductor design, providing a viable path for continued miniaturization and performance improvement.

2.2 Structure and Operation

FinFETs (Fin Field-Effect Transistors) are a type of transistor that has become increasingly important in semiconductor technology due to their superior performance and reduced power consumption compared to traditional planar transistors. Here's a detailed look at their structure and operation:

Structure of FinFET :

1. Fin Structure:

- The name "FinFET" comes from the "fin" structure that is a key component. In a FinFET, the channel is formed in a thin, vertical fin-shaped structure that extends above the substrate.
- The fin is usually made of a semiconductor material like silicon and is designed to be thin and tall, which allows for better control of the channel compared to planar devices.

2. Gate:

- The gate wraps around the fin on three sides (the two vertical sides and the top), providing improved electrostatic control over the channel.
- This 3D gate structure enhances the gate’s ability to control the flow of current through the channel, reducing leakage currents and improving performance.

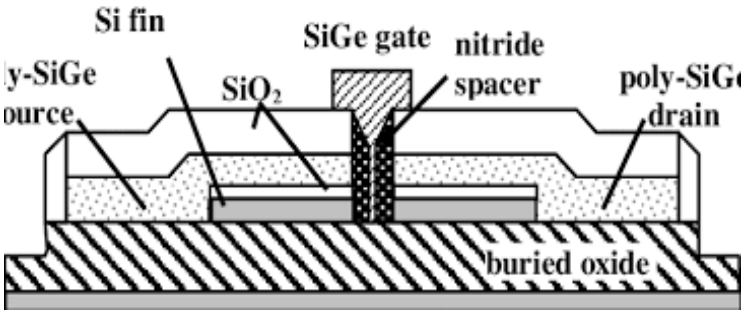

Figure 1: FinFET Device Structure

3. Source and Drain:

- The source and drain regions are located at the ends of the fin. These are doped regions that allow for the injection and extraction of current.
- The source and drain contacts are typically formed by ion implantation and subsequent annealing processes.

4. Channel Region:

- The channel is the region of the fin where current flows between the source and drain. It is controlled by the gate voltage.
- The channel's thin, vertical nature ensures that the gate can control it effectively, minimizing short-channel effects and leakage currents.

5. Dielectric Layer:

- An insulating dielectric layer separates the gate from the underlying substrate and source/drain regions. This layer prevents current from flowing through unintended paths.

Operation of FinFET:

1. Gate Control:

- In a FinFET, the gate voltage controls the current flow through the fin channel by creating an electric field that modulates the channel's conductivity.

- Because the gate wraps around the fin on three sides, it provides a strong electrostatic control over the channel, effectively turning the transistor on or off.

2. On-State (Conducting Mode):

- When a positive voltage is applied to the gate (relative to the source), an electric field is generated that attracts electrons towards the channel region, allowing current to flow between the source and drain.

- The channel becomes conductive, and the transistor is in the "on" state.

3. Off-State (Non-Conducting Mode):

- When the gate voltage is zero or negative (relative to the source), the electric field repels electrons away from the channel, effectively blocking current flow between the source and drain.

- The channel is non-conductive, and the transistor is in the "off" state.

4. Subthreshold Operation:

- In the subthreshold region, the transistor operates with a gate voltage below the threshold voltage. Here, current flow is exponentially dependent on the gate voltage.

- FinFETs are particularly advantageous in this region due to their improved control over leakage currents compared to planar devices.

5. Short-Channel Effects:

- FinFETs are designed to mitigate short-channel effects, which are issues that arise when transistors are scaled down to smaller sizes. The 3D structure of the FinFET provides better control of the channel, reducing issues like drain-induced barrier lowering (DIBL) and threshold voltage roll-off.

6. Drive Current and Performance:

- The fin structure allows for higher drive currents and better performance at lower power consumption levels. This is due to the increased gate control and reduced leakage currents.

2.3 Advantages of FinFETs

FinFET technology offers several notable advantages over traditional planar MOSFETs, making it a preferred choice for advanced semiconductor applications:

- Reduced Leakage Currents: The 3D gate structure provides better electrostatic control, significantly reducing leakage currents that are common in planar devices. This is particularly important for low-power applications where leakage can lead to significant power loss.
- Improved Drive Current: Enhanced gate control enables higher drive currents, which translates to better performance in terms of speed and efficiency. The improved drive current allows for faster switching and higher performance in digital circuits.
- Scalability: FinFET technology supports continued scaling to smaller nodes, making it suitable for advanced semiconductor technologies. The ability to maintain performance while shrinking the device size is crucial for meeting the demands of modern electronics.

2.4 Challenges and Limitations

Despite its advantages, FinFET technology also faces several challenges and limitations:

- Fabrication Complexity: The 3D structure of FinFETs introduces additional complexity to the fabrication process. This increased complexity can lead to higher manufacturing costs and requires advanced techniques to achieve precise control over the device structure.
- Short-Channel Effects: While FinFETs reduce short-channel effects compared to planar devices, they are not entirely eliminated. Designers must carefully manage these effects to ensure optimal device performance and reliability.

Addressing these challenges requires ongoing research and development to refine fabrication techniques and improve the overall performance of FinFET devices.

CHAPTER

3

Sentaurus Software Overview

3.1 Introduction

Sentaurus TCAD is a comprehensive suite of simulation tools developed by Synopsys for modeling and optimizing semiconductor devices and processes. The software is widely used in the semiconductor industry to predict device behavior, optimize design parameters, and evaluate the impact of process variations.

3.2 Key Features

Sentaurus TCAD provides several specialized modules designed to handle different aspects of semiconductor device modeling and simulation. Among these, SDE (Sentaurus Device), SDevice, and SVisual are key components that play crucial roles in the simulation process. Here's an in-depth look at each:

3.2.1 Sentaurus Structure Editor (SDE):

Sentaurus Structure Editor (SDE) is a graphical tool within the Sentaurus TCAD suite used for the creation, manipulation, and visualization of semiconductor device structures. Its main functions and features include:

1. **Device Structure Design:** SDE allows users to construct complex semiconductor device geometries using a user-friendly graphical interface. It supports a range of device structures, from simple planar devices to intricate 3D geometries like FinFETs and 3D NAND flash.

2. **Layer and Material Definition:** Users can define multiple layers and materials within a device structure, specifying their dimensions, doping profiles, and material properties. This includes creating custom layer configurations and specifying the precise composition of each layer.

3. **Graphical Editing:** The editor provides tools for interactive graphical editing, including drawing, resizing, and modifying device geometries. Users can visualize and adjust the layout in 2D or 3D views, facilitating intuitive design and modifications.

4. **Mesh Generation:** SDE includes features for generating computational meshes that discretize the device structure for simulation. Users can control mesh density and refinement to balance accuracy and computational efficiency.

5. **Import and Export:** The tool supports importing and exporting device structures from/to various file formats, allowing for integration with other design tools and workflows. This includes compatibility with CAD formats and other TCAD tools.

6. **Visualization:** SDE provides visualization capabilities for inspecting the device structure, including cross-sections, 3D views, and graphical overlays. This helps users ensure that the device design meets specifications before proceeding to simulation.

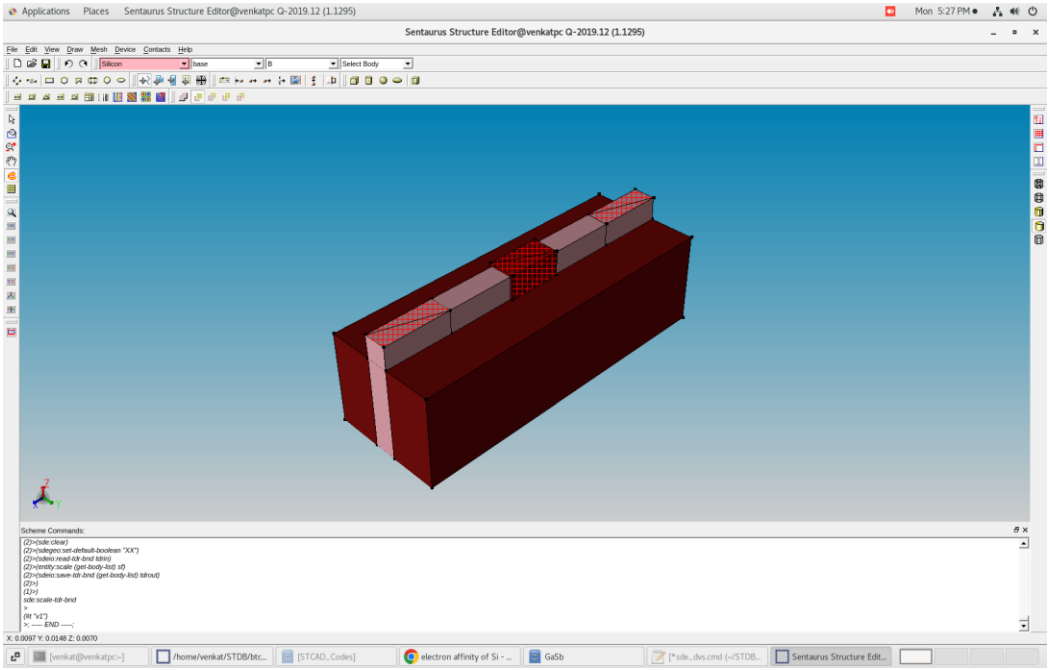

Fig 3.1 3D FinFET structure from Synopsys Sentaurus screen capture. The unit of length is nm

3.2.2 SDEVICE (Sentaurus Device):

Sentaurus Device (SDE) is a core module within the Sentaurus TCAD suite focused on device simulation. It offers comprehensive capabilities for modeling the electrical behavior of semiconductor devices with high accuracy.

1. **Advanced Device Physics**: SDE incorporates a range of sophisticated physical models to simulate the behavior of various semiconductor devices. It includes models for carrier transport (drift-diffusion, Monte Carlo), recombination, impact ionization, and quantum effects, among others.

2. **Multiscale Simulation:** The tool supports simulations across multiple scales, from atomic-level details to macroscopic device performance. This includes handling complex phenomena like strain effects in advanced materials or processes.

3. **Customization:** Users can define and integrate custom physical models or modify existing ones to address specific research or development needs. This flexibility allows for simulation of novel or experimental device structures.

4. **Performance Analysis:** SDE can be used to analyze various performance metrics of semiconductor devices, including threshold voltage, subthreshold slope, drive current, and switching characteristics.

5. **Process-Device Interaction:** It integrates with process simulation modules to evaluate how fabrication steps impact device performance. This is essential for understanding how variations in manufacturing affect the final device characteristics.

3.2.3 SVisual :

SVisual is a powerful visualization tool integrated with Sentaurus TCAD for analyzing and presenting simulation results. It enhances the ability to interpret complex data generated by simulations:

1. **Comprehensive Visualization**: SVisual provides extensive visualization capabilities, including 2D and 3D plots. Users can visualize device structures, electric fields, carrier concentrations, current densities, and more.

2. **Interactive Analysis**: The tool offers interactive features that allow users to explore and analyze simulation data dynamically. This includes zooming, panning, and rotating 3D structures to gain insights into different aspects of the simulation results.

3. **Data Extraction and Presentation** : Users can extract and present data in various formats, including graphical plots and tabular data. SVisual supports customized data extraction and presentation tailored to specific analysis needs.

4. **Integration with Simulation Results** : It seamlessly integrates with the results from SDE and SDevice, providing a unified interface for analyzing and interpreting the data. This integration ensures that users can efficiently move from simulation setup to result analysis.

5. **Reporting :** SVisual can generate detailed reports and visualizations that are useful for documentation and presentation purposes. This includes the ability to create publication-quality figures and plots.

SDE (Sentaurus Device) and SDevice are integral parts of the Sentaurus TCAD suite, focusing on detailed and efficient device simulation with advanced physical modeling and process integration capabilities. SVisual complements these tools by providing advanced visualization and analysis features, allowing users to interpret and present simulation data effectively. Together, these components offer a comprehensive solution for semiconductor device design, optimization, and analysis, supporting both practical engineering tasks and advanced research.

3.3 Importance in Semiconductor Design

Sentaurus TCAD tools are vital for semiconductor design due to their ability to provide accurate predictions and optimizations:

1.**Predicting Device Behavior**: Accurate modeling of device behavior under various conditions helps in understanding how devices will perform in real-world applications. This includes assessing factors such as drive current, leakage, and switching speed.

2.**Optimizing Design Parameters**: Sentaurus TCAD allows for fine-tuning of design parameters to achieve optimal performance. By adjusting parameters such as gate length and doping concentrations, engineers can enhance device performance and reliability.

3.Evaluating Process Variations: The software enables the assessment of how variations in the fabrication process affect device performance. This is crucial for ensuring that devices meet performance specifications despite variations in manufacturing conditions.

Overall, Sentaurus TCAD provides the necessary tools for effective semiconductor design and optimization, supporting the development of high-performance and reliable devices.

3.4 Source code

SDE CODE:

```
;------------------ (1) parameter -----------------------;
 (define nm 1e-3)
 (define Fw 5)
 (define Fh 5)
 (define Lg 15)
 (define LSDC 15)
 (define LSD 15)
 (define Tox 0.5)
 (define x1 LSDC)
 (define x2 (+ x1 LSD))
 (define x3 (+ x2 Lg))
 (define x4 (+ x3 LSD))
 (define x5 (+ x4 LSDC))
 (define y1 Fw)
 (define y2 (+ y1 Tox))
 (define y3 (+ y2 10))
 (define z1 Fh)
 (define z2 (+ z1 Tox))
 (define C_Doping @C_Doping@)
 ;(define C_Doping 1e11)
 (define SD_Doping @SD_Doping@)
 (define SDC_Doping @SDC_Doping@)
 ;(define B_Doping 1e15)
 (define B_Doping @B_Doping@)
```

```
;---------------------- (2) Structure ----------------------;
"ABA"
 ;--- Source contact and Source ---;
(sdegeo:create-cuboid (position 0 0 0 )  (position x1 y1 z1 )  "Silicon" "SourceC")
 (sdegeo:create-cuboid (position x1 0 0 )  (position x2 y1 z1)  "Silicon" "Source")

 ;--- Gate oxide ---;
 (sdegeo:create-cuboid (position x2 (- Tox) 0 )  (position  x3 y2 z2 )  "SiO2" "Gateoxide")

 ;--- Channel ---;
(sdegeo:create-cuboid (position x2 0 0 )  (position x3 y1 z1 )  "Silicon" "Channel")

 ;--- Drain contact and Drain---;
(sdegeo:create-cuboid (position x3 0 0 )  (position x4 y1 z1 )  "Silicon" "Drain")
 (sdegeo:create-cuboid (position x4 0 0 )  (position x5 y1 z1 )  "Silicon" "DrainC")

 ;--- Buried oxide ---;
 (sdegeo:create-cuboid (position 0 (- 10) (- 20) )  (position x5 y3 0 )  "SiO2" "Box")

 "ABA"
 ;--- Si Body ---;
(sdegeo:create-cuboid (position 0 0 (- 20) )  (position x5 y1 0 )  "Silicon" "Body")

 ;---------------------- (3) Contact ------------------;
;----- Source -----;
(sdegeo:define-contact-set "S" 4.0  (color:rgb 1.0 0.0 0.0 ) "##" )
 (sdegeo:set-current-contact-set "S")
 (sdegeo:set-contact-faces (find-face-id (position 1 1 z1)))

;----- Drain -----;
(sdegeo:define-contact-set "D" 4.0  (color:rgb 1.0 0.0 0.0 ) "##" )
 (sdegeo:set-current-contact-set "D")

(sdegeo:set-contact-faces (find-face-id (position (+ x4 1) 1 z1 )))

;----- Front Gate -----;
(sdegeo:define-contact-set "G" 4.0  (color:rgb 1.0 0.0 0.0 ) "||" )
 (sdegeo:set-current-contact-set "G")
 (sdegeo:set-contact-faces (find-face-id (position (+ x2 1) (- Tox) 1 )))

;----- Top Gate -----;
(sdegeo:define-contact-set "G" 4.0  (color:rgb 1.0 0.0 0.0 ) "||" )
 (sdegeo:set-current-contact-set "G")
 (sdegeo:set-contact-faces (find-face-id (position (+ x2 1) 1  z2 )))

;----- Back Gate -----;
 (sdegeo:define-contact-set "G" 4.0  (color:rgb 1.0 0.0 0.0 ) "||" )
 (sdegeo:set-current-contact-set "G")
 (sdegeo:set-contact-faces (find-face-id (position (+ x2 1) y2 1 )))

;----- Body -----;
(sdegeo:define-contact-set "B" 4.0  (color:rgb 1.0 0.0 0.0 ) "##" )
 (sdegeo:set-current-contact-set "B")
```

```
(sdegeo:set-contact-faces (find-face-id (position (* 0.5 x5) (* 0.5 y1) (- 20) )))

;------------------------ (4) Doping ------------------------;
;----- Channel -----;
(sdedr:define-constant-profile "dopedC" "BoronActiveConcentration" C_Doping )
 (sdedr:define-constant-profile-region  "RegionC" "dopedC" "Channel" )

 ;----- Source -----;
(sdedr:define-constant-profile "dopedS" "ArsenicActiveConcentration" SD_Doping )
 (sdedr:define-constant-profile-region  "RegionS" "dopedS" "Source" )
(sdedr:define-constant-profile "dopedSC" "ArsenicActiveConcentration" SDC_Doping )
 (sdedr:define-constant-profile-region  "RegionSC" "dopedSC" "SourceC" )

 ;----- Drain ------;
(sdedr:define-constant-profile "dopedD" "ArsenicActiveConcentration" SD_Doping )
 (sdedr:define-constant-profile-region  "RegionD" "dopedD" "Drain" )
 (sdedr:define-constant-profile "dopedDC" "ArsenicActiveConcentration" SDC_Doping )
 (sdedr:define-constant-profile-region  "RegionDC" "dopedDC" "DrainC" )

 ;----- Si Body -----;
(sdedr:define-constant-profile "dopedB" "BoronActiveConcentration" B_Doping )
 (sdedr:define-constant-profile-region  "RegionB" "dopedB" "Body" )

 ;---------------------- (5) Mesh ----------------------;

;--- AllMesh ---;
(sdedr:define-refinement-size "Cha_Mesh" 5 5 5 1 1 1)
 (sdedr:define-refinement-material "channel_RF" "Cha_Mesh" "Silicon" )

 ;--- ChannelMesh ---;
(sdedr:define-refinement-window "multiboxChannel" "Cuboid"
 (position x1 0 0)
 (position x4 y1 z1))
 (sdedr:define-multibox-size "multiboxSizeChannel"  2 2 2 2 2 2)
 (sdedr:define-multibox-placement "multiboxPlacementChannel" "multiboxSizeChannel"
"multiboxChannel")
 (sdedr:define-refinement-function "multiboxPlacementChannel" "DopingConcentration"
"MaxTransDiff" 1)

 ;-----------  (6) Save (BND and CMD and rescale to nm) -----------;
(sde:assign-material-and-region-names (get-body-list) )
 (sdeio:save-tdr-bnd (get-body-list) "n@node@_nm.tdr")
 (sdedr:write-scaled-cmd-file "n@node@_msh.cmd" nm)
(define sde:scale-tdr-bnd
 (lambda (tdrin sf tdrout)
 (sde:clear)
 (sdegeo:set-default-boolean "XX")
(sdeio:read-tdr-bnd tdrin)
 (entity:scale (get-body-list) sf)
 (sdeio:save-tdr-bnd (get-body-list) tdrout)
 ))
 (sde:scale-tdr-bnd "n@node@_nm.tdr" nm "n@node@_bnd.tdr")
```

SDEVICE CODE:

```
File
{
 Grid="@tdr@"
 Plot="@tdrdat@"
 Current="@plot@"
 Output="@log@"
 }

Electrode
 {
 { name="S"    Voltage=0.0 }
 { name="D"     Voltage=0.0 }
 { name="G"      Voltage=0 WorkFunction=@WK@}
 { name="B"     Voltage=0.0 }
 }

Physics
{
 Mobility( DopingDep HighFieldSaturation Enormal )
 EffectiveIntrinsicDensity( OldSlotboom )
 Recombination( SRH(DopingDep) )
 }

Math
{
 Extrapolate
 Derivatives
 * Avalderivatives
 RelErrControl
Digits=5

ErRef(electron)=1.e10
 ErRef(hole)=1.e10
Notdamped=50
 Iterations=20
 *Newdiscretization
 Directcurrent
 Method=ParDiSo
 Parallel= 2
 *-VoronoiFaceBoxMethod
 NaturalBoxMethod
 }
```

```
Plot
{
 eDensity hDensity
  eCurrent hCurrent
 TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
 eMobility hMobility
 eVelocity hVelocity
 eEnormal hEnormal
 ElectricField/Vector Potential SpaceCharge
 eQuasiFermi hQuasiFermi
 Potential Doping SpaceCharge
 SRH Auger
AvalancheGeneration
 DonorConcentration AcceptorConcentration
 Doping
 eGradQuasiFermi/Vector hGradQuasiFermi/Vector
eEparallel hEparalllel
 BandGap
BandGapNarrowing
 Affinity
ConductionBand ValenceBand
 }

Solve
{
 NewCurrentFile=""
Coupled(Iterations=100){ Poisson }
 Coupled(Iterations=100){ Poisson Electron Hole }
 Coupled{ Poisson Electron Hole }
 Quasistationary(
 InitialStep=0.01 Increment=1.35
 MinStep=1e-5 MaxStep=0.2
 Goal{ Name="D" Voltage= @Vd@ }
 ){ Coupled{ Poisson Electron Hole } }
 Quasistationary(
 InitialStep=1e-3 Increment=1.35
 MinStep=1e-5 MaxStep=0.05
 Goal{ Name="G" Voltage= @Vg@ }
 ){ Coupled{ Poisson Electron Hole} }
 }
```

3.5 Simulation Methodology of 3D FinFET

Device Configuration

The simulation of a 12nm FinFET device involves configuring several key parameters to accurately model its behavior. The device configuration includes the following elements:

- Gate Length: Set to 12nm, the gate length is a critical dimension that influences the device's performance. Shorter gate lengths typically result in higher drive currents but may also increase leakage currents.

- Fin Height: Configured at 40nm, the fin height is essential for ensuring adequate channel formation and electrostatic control.

- Fin Width: Set to 10nm, the fin width is a key parameter affecting the balance between drive current and leakage. Narrower fins enhance electrostatic control but may reduce drive current.

- Gate Dielectric: High-k dielectric materials are used to reduce leakage currents and improve gate control. This choice of dielectric material is critical for enhancing the performance of the FinFET at the 12nm node.

- Doping Profile: The doping concentrations for the source and drain regions are carefully selected to optimize carrier injection and extraction. Typical doping profiles are n-type for the source and p-type for the drain.

3.5.1 Device Simulation

Sentaurus Device is used to simulate the electrical characteristics of the FinFET:

- Id-Vg Characteristics: The drain current (Id) versus gate voltage (Vg) curves are simulated to evaluate the device’s switching behavior.

These curves provide insights into the device's performance, including its drive current and threshold voltage.

- Subthreshold Slope: This parameter indicates how effectively the device transitions between the off and on states. A subthreshold slope close to 60mV/decade is desirable as it signifies strong electrostatic control and minimal leakage.
- Drain-Induced Barrier Lowering (DIBL): DIBL measures the impact of drain voltage on the threshold voltage, reflecting how well the gate controls the channel under varying drain voltages. A lower DIBL indicates better short-channel control.

3.5.2 Parameter Settings

The simulations are conducted by varying key parameters to understand their impact on device performance:

- Gate Length: Adjusted to study the effects on drive current and leakage.
- Fin Height and Width: Varied to optimize electrostatic control and performance.
- Doping Concentrations: Modified to assess their impact on device characteristics such as Id-Vg curves and threshold voltage.

CHAPTER

4

Simulation Result

Device Characteristics

The simulation results reveal significant improvements in device characteristics for the 12nm FinFET compared to planar transistors:

- **Id-Vg Curves**: The drain current (Id) increases substantially with gate voltage (Vg) for the FinFET, showing improved drive current compared to planar devices. The curves are steep, indicating effective switching behavior and reduced leakage.

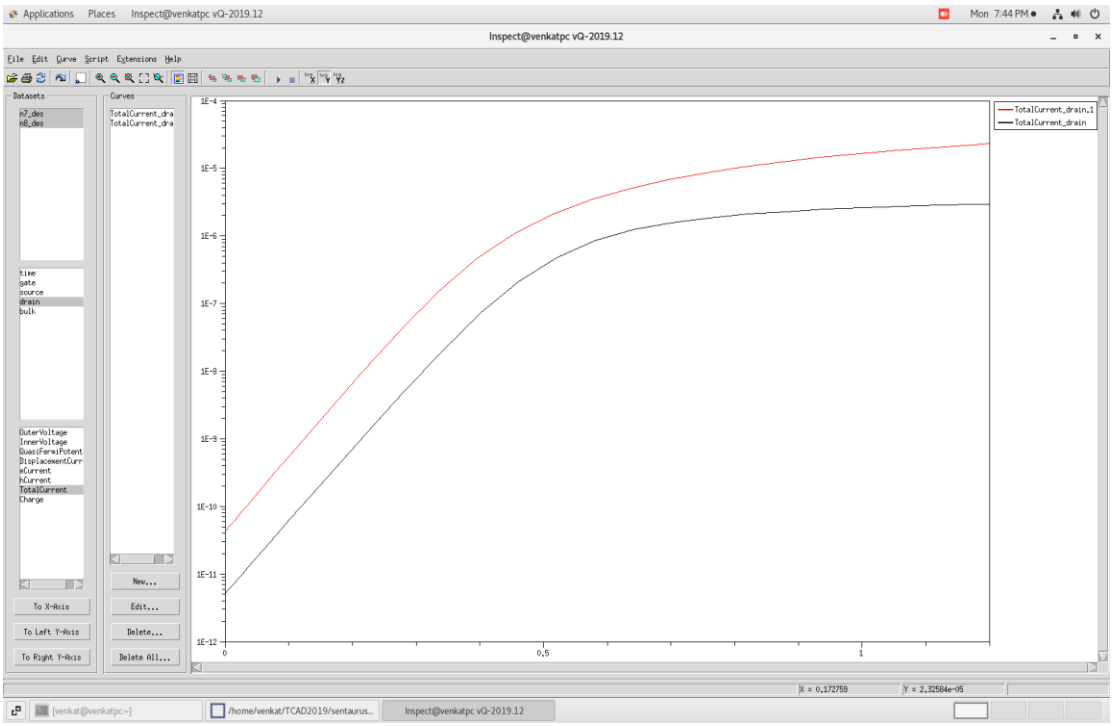

Figure 3.3: Id-Vg Curve for 12nm FinFET

- **Doping Concentration Profile:**

  Source/Drain Doping**:** High doping in the source and drain reduces resistance and enhances current flow but must be managed to avoid increased capacitance and reliability issues.

  Channel Doping**:** Proper channel doping is critical for controlling Vth and mitigating short-channel effects like DIBL and threshold voltage roll-off, ensuring stable device operation.

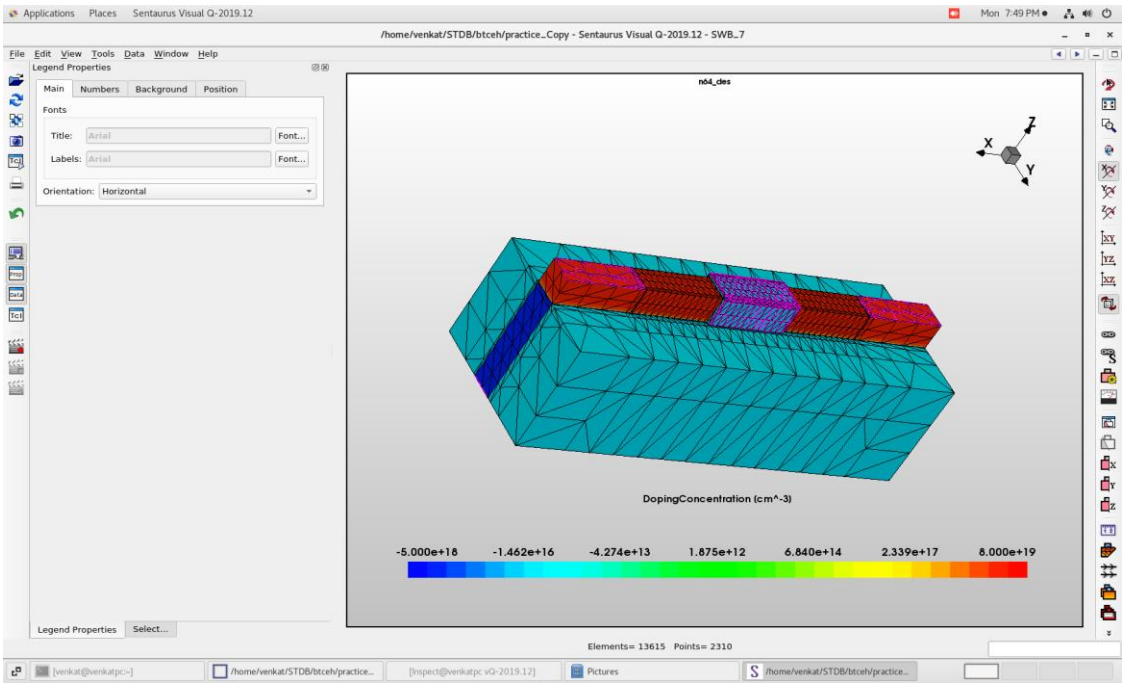

Fig. 3.4 Electron concentration distribution of 3D nFinFET simulation

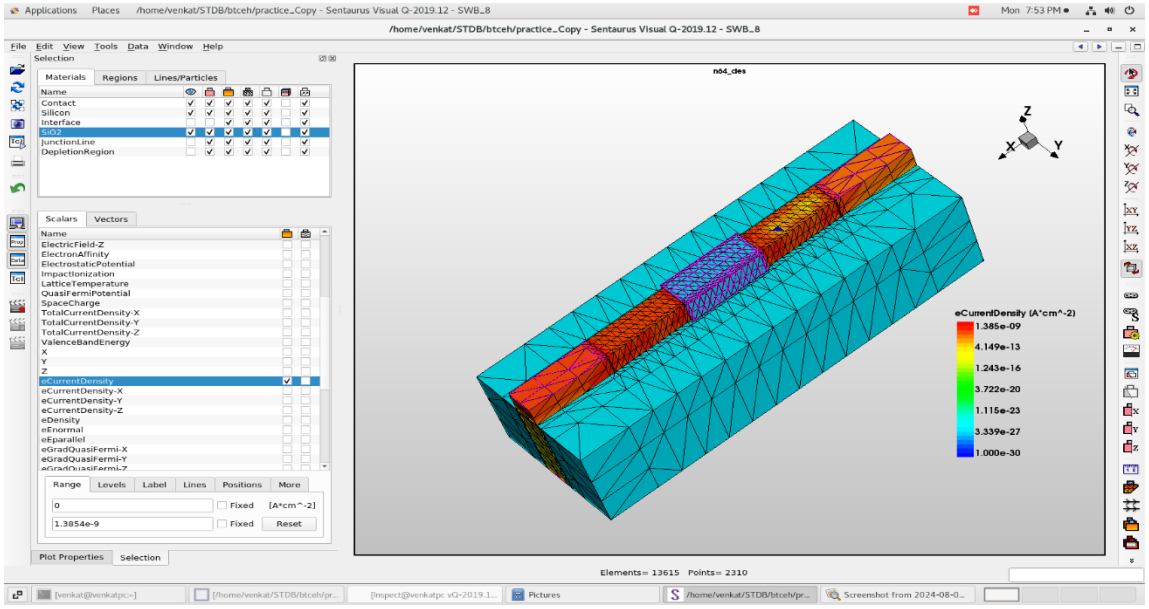

Fig. 3.5 Electron Current density distribution of 3D nFinFET simulation

- **Electrostatic Potential:** The electrostatic potential along the channel influences the energy barrier for carriers, affecting current flow. A well-designed potential profile ensures effective gate control, facilitating efficient switching and minimizing leakage.This distribution reflects the control over the channel by the gate, crucial for minimizing short-channel effects and maintaining overall device performance.

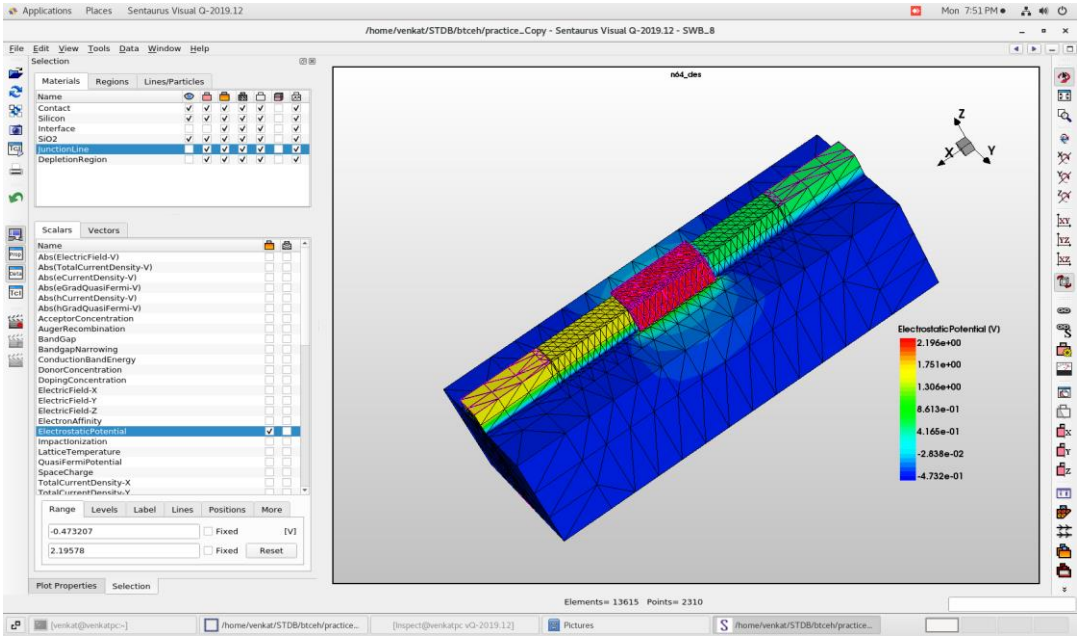

Fig. 3.6 Electric potential distribution of 3D nFinFET simulation

Performance Metrics

- Subthreshold Slope: The 12nm FinFET achieves a subthreshold slope of approximately 60mV/decade. This value is indicative of effective electrostatic control, which helps in reducing leakage currents and improving switching performance.

- Threshold Voltage: The device exhibits a well-defined threshold voltage, showing minimal variability. This stability is crucial for reliable operation across different conditions.

- Drain-Induced Barrier Lowering (DIBL): The DIBL effect is minimized, demonstrating that the FinFET provides better gate control and reduced short-channel effects compared to planar devices.

3.6 Optimization and Analysis

3.6.1 Optimization Techniques

Several optimization techniques are employed to enhance the performance of the 12nm FinFET:

- Fin Width Optimization: Adjusting the fin width to find the optimal balance between drive current and leakage. Narrower fins improve electrostatic control but may reduce drive current, so a trade-off must be found.
- Gate Length Optimization: Fine-tuning the gate length to achieve desired performance metrics. Shorter gate lengths increase drive current but may lead to higher leakage currents, necessitating careful optimization.

3.6.2 Sensitivity Analysis

Sensitivity analysis helps identify which parameters most significantly affect device performance.

- Fin Height Sensitivity: Variations in fin height have a considerable impact on electrostatic control and drive current. This parameter is crucial for achieving optimal performance and minimizing short-channel effects.

- Gate Length Sensitivity: Adjustments to gate length affect both drive current and leakage. Sensitivity analysis helps determine the optimal gate length for balancing these factors.

3.6.3 Trade-offs and Recommendations

Trade-offs between performance metrics such as drive current and leakage are discussed. Recommendations for optimizing the 12nm FinFET include:

- Balancing Fin Dimensions: Selecting appropriate fin height and width to optimize electrostatic control and drive current while minimizing leakage.
- Choosing Dielectric Materials: Using high-k dielectric materials to reduce leakage currents and improve gate control.

By carefully considering these trade-offs, designers can achieve a well-balanced performance for the 12nm FinFET.

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Future work

The 12nm FinFET technology, simulated using the Sentaurus TCAD tool, has demonstrated promising performance metrics, including optimized threshold voltage (Vth), subthreshold swing (SS), high on/off current ratio (Ion/Ioff), and low leakage current. However, further research and optimization are necessary to enhance device performance, reliability, and power efficiency. This report outlines key areas for future work to advance 12nm FinFET technology.

1. **Advanced Doping Profile Optimization:**

- Source/Drain Engineering: Refine the doping concentration in the source and drain regions to further reduce series resistance while avoiding excessive junction capacitance.Utilize advanced doping techniques such as ion implantation and rapid thermal annealing to achieve precise control over the doping profile. Investigate the impact of different dopant species and concentrations on device performance and reliability.

- Channel Doping Enhancement: Optimize channel doping to mitigate short-channel effects (SCEs) such as drain-induced barrier lowering (DIBL) and threshold voltage roll-off. Explore alternative doping profiles, including retrograde and super-steep retrograde doping, to improve electrostatic control and maintain a stable Vth. Analyze the trade-offs between doping concentration, SCE suppression, and mobility degradation.

2. Advanced Device Architectures and Materials:

- Gate-All-Around (GAA) FETs: Explore the potential of GAA structures for further scaling beyond 12nm. Simulate GAA FETs using Sentaurus TCAD to evaluate their electrostatic control, scalability, and performance compared to FinFETs. Analyze the challenges and benefits of transitioning to GAA technology.

- Alternative Channel Materials: Investigate new channel materials, such as silicon germanium (SiGe) or III-V semiconductors, to enhance carrier mobility and device performance.Model the integration of these materials into the FinFET structure and evaluate their impact on key performance metrics, including drive current, leakage, and thermal stability.

The 12nm FinFET technology presents significant potential for advanced semiconductor applications, but ongoing optimization is essential to fully realize its capabilities. Future work will focus on refining doping profiles, managing electric fields and current density, enhancing thermal stability, and exploring new device architectures and materials. These efforts, leveraging the powerful simulation capabilities of the Sentaurus TCAD tool, will contribute to the continued advancement of FinFET technology and its application in next-generation electronic devices.

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Conclusion

After diving into the 12nm FinFET simulations with Sentaurus TCAD, it's clear that this technology has significant potential for the future of semiconductors. Key metrics, including threshold voltage (Vth), subthreshold swing (SS), on/off current ratio (Ion/Ioff), and leakage currents, all look promising, indicating that the FinFET is both efficient and high-performing.

To advance further, we should focus on several areas. First, fine-tuning the doping profiles in the source, drain, and channel regions will help reduce resistance and address short-channel effects. Managing electric fields is another priority; we need to explore LDD structures and new gate designs to avoid peak field issues and ensure a uniform distribution. Optimizing current density by working on thermal management and adjusting fin geometry is crucial to handle electron current density effectively and prevent overheating. Additionally, improving electrostatic potential through different gate dielectrics and multi-gate structures can enhance control and reduce leakage. Finally, investigating advanced architectures such as Gate-All-Around (GAA) FETs and alternative channel materials like SiGe and III-V semiconductors will push the boundaries of performance.

By addressing these areas with the insights gained from Sentaurus TCAD simulations, we can tackle scaling challenges and enhance the performance, power efficiency, and reliability of 12nm FinFETs, setting the stage for next-generation electronic devices and fully leveraging the exciting potential of this technology.

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THANK YOU