Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India

(Autonomous College Affiliated to University of Mumbai)

End Semester Examination

April / May 2018

Max. Marks: 100 **Duration: 180 Min**
Class: S.E. **Semester: IV**
Course Code: CE44 / IT42 **Branch: Computer / IT**
Name of the Course: Computer Organization and Architecture

Instruction:
(1) All questions are compulsory
(2) Draw neat diagrams
(3) Assume suitable data if necessary

Q No.		Max. Marks	CO
Q.1 (a)	Differentiate between Computer Organization and Computer Architecture.	05	CO1
Q.1 (b)	Compare Programmed I/O and Interrupt-driven I/O.	05	CO5
Q.1 (c)	What are the types of ROM? Write each in brief.	05	CO4
Q.1 (d)	Differentiate Harvard model and Von Neumann model.	05	CO1
Q.2 (a)	Solve following using Recoded Multiplier Method. i) (+14) X (-5) ii) (-13) X (-20) **OR** Draw the flowchart and Perform 25 x (-16) using Booth's multiplication algorithm.	10 10	CO2 CO2
Q.2 (b)	Draw the flowchart of Non-Restoring Division method. Solve following example with using non-restoring method. Dividend = 23 Divisor = -5	10	CO2
Q.3 (a)	What are the different design methods for Hardwired Control Units? Explain any one method in detail. **OR** How is the Wilkes microprogrammed control unit works? Write advantages and disadvantages of it.	10 10	CO3 CO3
Q.3 (b)	What are the features of RISC and CISC processors?	10	CO3
Q.4 (a)	What are the different cache memory mapping techniques? Consider a cache consisting of 256 line of 16 words each, for a total of 4096 words and assume that the main memory is addressable by 16-bit address and it consists of 4 blocks. How many bits are there in each of the Tag, Line/Set and Word field of different cache memory mapping techniques? (Assume 2 way Set - Associative) **OR**	10	CO4

Q.4 (a)	Find miss ratio and hit ratio using LRU and FIFO page replacement policy for the following referencing stream – 7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1 . Consider i) Frame size = 3 ii) Frame size =4	10	CO4
Q.4 (b)	Explain the High order interleaving and Low order interleaving memory techniques.	10	CO4
Q.5 (a)	Give the Working of ARM architecture.	10	CO1
Q.5 (b)	What is Instruction pipelining and it's advantages? What are the types of pipeline hazards and Discribe any one in detail. **OR** Why Flynn's Classification is required? Give the working of each and write the advantages and disadvantages of it.	10 10	CO6 CO6