Qualcomm Technologies, Inc.

QCA4020 Dual-Band Wi-Fi, BT5 and 802.15.4 SOC

Device Specification

80-YA501-1 Rev. B

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Revision history

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
A	February 2018	Initial release. This document only contains specifications for the QCA4020 device. For QCA4024 specifications, see *QCA4024 BLE and IEEE 802.15.4 Device Specification*, 80-YA502-1.
B	March 2018	Updates to the following sections: ■ Section 2.2, "Ball descriptions" on page 23 ■ Section 3.2, "Recommended operating conditions" on page 33 ■ Section 4.3, "Device ordering information" on page 40

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1 Introduction

1.1 Document updates

See the Revision history for details on the changes included in this revision.

1.2 Documentation overview

This document contains technical information for the QCA4020 and is organized as follows:

Chapter 1 Gives a high-level functional description of the device, lists the device features, and defines marking conventions, terms, and acronyms used throughout this document.

Chapter 2 Defines the device pin assignments.

Chapter 3 Defines the device electrical characteristics, including absolute maximum ratings and recommended operating conditions.

Chapter 4 Provides IC mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics.

Chapter 5 Describes carrier, storage and handling information of the QCA4020.

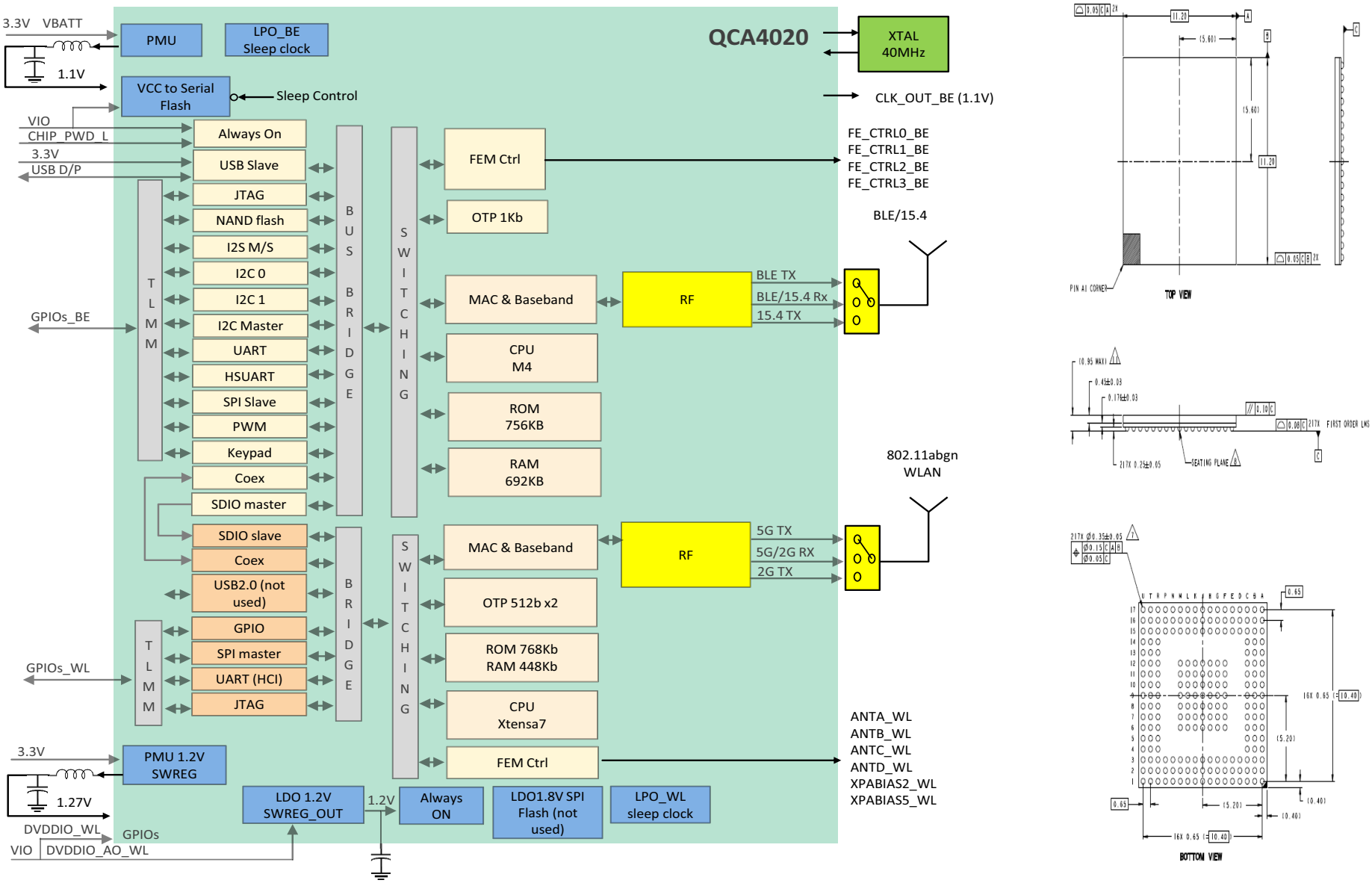
Chapter 6 Presents procedures and specifications for mounting the QCA4020 onto printed circuit boards (PCBs).

Additional reference documents are listed in Table 1-1.

Table 1-1 Reference documents

Document Number	Title
80-YA501-121	*QCA4020 Module (M20) Product Specification*

1.3 Chip-level block diagram



1.4 Device description

The QCA4020 is a single package wireless local area network (WLAN), Bluetooth (BT) Low Energy and 802.15.4 combo solution to support dual-band 1 × 1 IEEE 802.11a/b/g/n WLAN standards, BT 5 and 802.15.4, thereby supporting virtually seamless integration of WLAN/BT Low Energy and 802.15.4 technology.

1.4.1 Key features

The QCA4020 contains three processors:

- The first processor, an ARM Cortex-M4F at up to 128 MHz is used as the application processor. It runs the Qualcomm Technologies networking stack as well as OEM application code. Customer software runs under an RTOS such as ThreadX or FreeRTOS, and so on
- Second processor, an ARM Cortex-M0 at 64 MHz, which is utilized as the connectivity processor for the BLE and 802.15.4 subsystems.
- Third processor, CPU which is a dedicated processor to run the Wi-Fi dual band function.

The QCA4020 implements three wireless subsystems in a single package:

- Dual band 1x1 802.11 a/b/g/n Wi-Fi function
- Bluetooth Low Energy (BLE) compliant to the SIG v5 specification
- IEEE 802.15.4 compliant to the v2006 specification and also featuring Coordinated Sample Listing (CSL), from the 802.15-2015 specification

Other Interfaces

- Up to 2 of I^2C, Up to 1x HS and 1x 2-wire UART, Up to 2x SPI, QSPI, Sensor ADC (up to 8 channels, 12-bit, 1 Msps), Up to 8 PWM optimized for LED lighting applications, SDIO 2.0 device only, I^2S, a rich set of programmable General Purpose IOs (GPIOs), JTAG debug port.

Security

- QCA4020 implements secure boot (authentication of firmware images) for firmware loaded from flash for the M4F, M0 and WLAN XTENSA processors. Additionally, mechanisms exist to protect the execution environments of the aforementioned processors from potential external attackers. In addition to this, facilities exist to support maintaining secure communication channels between QCA4020 and external servers. A crypto accelerator subsystem supports application-level AES encryption and the image authentication hash function (SHA256)

Power Management

- QCA4020 implements an advanced power management scheme to minimize power dissipation for each use case.
- Fine-grain power island partitioning with aggressive power gating
- Dynamic Voltage and Frequency Control

- Configurable memory retention for minimizing deep sleep power per application

1.5 Product feature details

The QCA4020 is an intelligent platform for the Internet of Things that contains a low-power Wi-Fi, BLE and 15.4 connectivity protocols along with SSL, enabling a low-cost, low-complexity system to obtain full-featured Internet connectivity and reliable information exchange.

NOTE Some of the hardware features integrated within the QCA4020 must be enabled by software. Refer to the latest revision of the applicable software release notes to identify the enabled QCA4020 features.

Triple processors

The QCA4020 contains three processors. The first is an ARM Cortex-M4F, used as the application, or host processor. It runs the Qualcomm Technologies networking stack as well as OEM application code. Customer software runs under an RTOS such as ThreadX or FreeRTOS, and so on. Processor and memory subsystem attributes are as follows:

- ARM Cortex-M4F at up to 128 MHz
- ARM v7-M ISA (Thumb/Thumb-2)
- Single-precision floating point
- SRAM is available for customer applications. The banks are further subdivided physical regions that are designed to allow each region's storage array to be either retained or power collapsed during deep sleep mode, giving maximum flexibility on power savings for specific applications.
- Memory-mapped, cached view of external Quad SPI flash (QSPI). A 32 KB, 4-way set associative cache is used to achieve zero wait state operation under hit.

The second processor is an ARM Cortex-M0, which is used as the connectivity control processor for the BLE and 802.15.4 subsystems (CNSS). Processor and memory subsystem attributes are as follows:

- ARM Cortex-M0 running up to 64 MHz
- ARM v6-M ISA (subset of Thumb/Thumb-2)
- No wait state ROM – Runs Secure Primary Boot Load (PBL) and general FW related to BLE and 15.4 controller functions

The third processor is XTENSA7 running at 130 MHz, which is a dedicated processor to run the Wi-Fi dual band function.

There are multiple advantages to the multiple processor configuration:

- Qualcomm Wi-Fi, BLE and 15.4 code has a known execution environment without generating competition for processor resources from customer code.
- The customer maintains flexibility to choose the operating system for their code.

- The execution environment of Qualcomm Technologies code is easier to separate from customer code from a security perspective.

Wireless interfaces

The QCA4020 implements three wireless subsystems on-chip, and supports a master and slave configuration:

- 1x1 dual band 802.11abgn Wi-Fi function
- Bluetooth Low Energy (BLE) compliant to the SIG v5.0 specification.
- IEEE 802.15.4 compliant to the v2006 specification and also featuring Coordinated Sample Listing (CSL) from the 802.15-2015 specification.

WI-Fi Link

Wi-Fi link is a full-featured, dual-band, single stream 802.11n solution. The Wi-Fi link is highly integrated, and includes an energy efficient on-board power amplifier and LNA. The QCA4020:

- Green Tx power saving mode
- Low power listen mode
- Data rates up to 150 Mbps
- Full security support: WPS, WPA, WPA2, WAPI, WEP, TKIP

System cost optimization

The QCA4020 is optimized for low system cost, and minimizes the number and cost of any components required to achieve a reliable:

- Highly-Integrated Wi-Fi solution
- matching components to complete the RF link
- Integrated IPv4/IPv6 TCP/IP stack
- Integrated Network services such as HTTP, DNS, FTP
- 11.2 x 11.2 mm, 0.65 mm pitch 217-ball VFBGA package
- QCA4020 patch firmware is stored and automatically loaded from a low cost serial flash memory

Manufacturing interface

- USB 2.0 device interface, providing a simplified, high-speed, and scalable manufacturing test and configuration interface for QCA4020-based systems, using an integrated controller and PHY

Other Interfaces

The following additional I/O interfaces are provided by QCA4020.

- Up to 2 of I2C interface
- Up to 1 of SPI Master and 1 of SPI Slave interface

- Up to 1 of SDIO2.0 Slave interface
- Up to 1 of SD master for memory card interface
- Up to 2 of high speed UART interface
- Up to 6 of Sensor ADC (up to 8-channels, 12-bit, 1Msps) for sensor application
- Up to 6 of PWM for LED lighting application
- Key PAD interface
- JTAG debug port

NOTE Some of the above interfaces have dedicated pins while most are configurable using the programmable GPIOs. This allows various configurations covering a wide range of applications while maintaining a small footprint.

Security

The QCA4020 implements secure boot (authentication) on firmware loaded from external flash and intended to run on the M4F, M0 and XTENSA processors. Additionally, mechanisms exist to protect the execution environments of these processors from external attackers. Facilities exist to maintain secure communication channels between QCA4020 and external servers. Two on-chip hardware crypto accelerator subsystems support application-level AES encryption/decryption and image authentication hash function (for example, SHA256). A Public Key hardware accelerator is also included to accelerate operations for public key algorithms such as RSA. A HW ECC engine is provided to accelerate TLS/SSL certificate validation. To maximize the protection during key generation, a True Random Number Generator (TRNG) is included.

1.6 GPIO

QCA4020 GPIO pins are fully configurable. They are shared with other interfaces, such as I2C, SPI, and serial flash. Chapter 2 provides the set of pin configurations options.

Each of the GPIO pins supports this configuration option:

- Internal pull-up/down options

1.7 Serial interface

QCA4020 includes two high-speed Universal Asynchronous Receiver/Transmitter (UART) interfaces, which may be configured to serve as either a host interface link or a debug message console.

1.8 Power transition

The QCA4020 provides integrated power management and control functions and extremely low power operation for maximum battery life across all operational states by:

- Gating clocks for logic when not needed.

- Shutting down unneeded high speed clock sources
- Reducing voltage levels to specific blocks in some states

1.9 System clocking

1.9.1 Low-speed clocking

The QCA4020 has eliminated the need for an external sleep clock source thereby reducing system cost. Instead, an internal ring oscillator is used to generate a low frequency sleep clock. It is also used to run the state machines and counters related to low power states.

1.9.2 Sense ADC

The QCA4020 includes a 1.8V IO of dedicated of 12-bit ADC, up to 1Msps with 8 channels single-ended input or 4 channels differential-ended inputs. If sense ADC is used, the chip requires to use single 1.8V VIO only.

- Digital power supply is from 1.1V of SWREG_BE
- Analog power support is from both 1.1V of SWREG_BE and 1.8V of VDDIO_BE4
- Voltage input of single-ended is 0V to 1.75V
- Voltage input of differential is -1.75V to +1.75V.
- Common mode voltage is 0.875V

1.10 Front end control

For applications that use external front-end components, the QCA4020 provides the ability to control them with four antenna switch control outputs named:

- ANTA
- ANTB
- ANTC
- ANTD

A programmable switch table indexed by transceiver state offers flexibility for various front-end configurations. The QCA4020 supports antenna sharing with another wireless chip in all power states by using ANTD to control the shared antenna switch.

1.11 MAC block

The QCA4020 Wireless MAC consists of these major blocks:

- Host interface unit (HIU) for bridging to the AHB for bulk data accesses and APB for register accesses
- 10 queue control units (QCU) for transferring Tx data
- 10 DCF control units (DCU) for managing channel access
- Protocol control unit (PCU) for interfacing to baseband
- DMA receive unit (DRU) for transferring Rx data
- Supports Rx diversity

1.12 Baseband block

The QCA4020 baseband (BB) module is the physical layer controller for the 1x1 802.11abgn air interface. It is responsible for modulating data packets in the transmit direction, and detecting and demodulating data packets in the receive direction. It has a direct control interface to the radio to enable hardware to adjust analog gains and modes dynamically.

1.13 Bootstrap modes and pins

Certain pins in the QCA4020 are sampled at startup, and these sampled values are used to select among various bootstrap modes and chip configurations.

GPIO9_BE	GPIO25_BE	GPIO18_BE	JTAG Interface
0	0	0	No JTAG
0	0	1	JTAG in GPIO[53:50]_BE
0	1	0	JTAG in GPIO[11:8]_BE
0	1	1	JTAG in GPIO[27:24]_BE
1	x	x	Not Allow

GPIO22_BE	GPIO9_BE	Force to enter USB Boot Mode
0	0	Force M4 to load image from flash memory
1	0	Force M4 to boot in EDL (Emergency Download Mode)

GPIO23_BE	XTAL 40 MHz or 26 MHz Selection
0	Crystal 40MHz
1	Not Allow

GPIO21_BE	GPIO20_BE	32.768 KHz Source Selection
0	0	Chip Internal LPO
0	1	External Crystal 32.768 KHz (Not Used)
1	0	External 32.768 KHz TCXO Clock connected to GPIO48_BE (Not Used)
1	1	Not allowed

GPIO0_WL	GPIO2_WL	Host Mode Selection
0	0	No Allowed
0	1	No Allowed
1	0	No Allowed
1	1	SDIO

GPIO20_WL	XTAL 40 MHz or 26 MHz
0	26 MHz (Not Support)
1	40 MHz

GPIO13_WL	SWREG Selection
0	SWREG_WL switching regulator
1	Not Allowed

GPIO11_WL	GPIO4_WL	EJTAG Selection
0	X	Normal Operation
1	0	SoC JTAG (Not Allowed)
1	1	EJTAG : WLAN CPU JTAG

1.14 GPIO mapping

Table 1-2 GPIO names

GPIO #	Chip Internal PU/PD	Primary Function	SPI or I2C or QSPI	SDIO	SD Memory Card	UART	JTAG	PWMADC or SenseADC	KeyPAD1	KeyPAD2	Codec	PTA
GPIO4_BE	PD	WL_WKUP_ BE										
GPIO5_BE	X	GPIO_5								KEY_ COL_0		BT_ ACTIVE
GPIO6_BE	X	GPIO_6								KEY_ COL_1		WLAN_ ACTIVE
GPIO7_BE	X	GPIO_7								KEY_ COL_2		BT_ PRIORITY
GPIO8_BE	PU	GPIO_8				M0&M4_ UART0_RX	JTAG1_BE_ TCK		KEY_ COL_4	KEY_ COL_3		
GPIO9_BE	PD	GPIO_9				M0&M4_ UART0_TX	JTAG1_BE_ TDO		KEY_ ROW_4	KEY_ ROW_0		
GPIO10_BE	PU	GPIO_10	I2C0_Master_ SCL				JTAG1_BE_ TMS		KEY_ COL_5	KEY_ ROW_1		
GPIO11_BE	PU	GPIO_11	I2C0_Master_ SDA				JTAG1_BE_ TDI		KEY_ ROW_5	KEY_ ROW_2		
GPIO12_BE	X	GPIO_12						pwm_out_0	KEY_ COL_6	KEY_ ROW_3		
GPIO13_BE	X	GPIO_13						pwm_out_7	KEY_ ROW_6	KEY_ COL_4		
GPIO14_BE	X	GPIO_14				HS_UART0_ DM_CTS			KEY_ COL_0	KEY_ COL_5		
GPIO15_BE	X	GPIO_15				HS_UART0_ DM_TXD			KEY_ COL_1	KEY_ COL_6		
GPIO16_BE	X	SPI0_CS2_N	I2C1_Master_ SCL			HS_UART0_ DM_RFR			KEY_ ROW_0	KEY_ COL_7		BT_ ACTIVE
GPIO17_BE	X	SPI0_CS1_N	I2C1_Master_ SDA			HS_UART0_ DM_RXD			KEY_ ROW_1	KEY_ ROW_4		WLAN_ ACTIVE

Table 1-2 GPIO names (cont.)

GPIO #	Chip Internal PU/PD	Primary Function	SPI or I2C or QSPI	SDIO	SD Memory Card	UART	JTAG	PWMADC or SenseADC	KeyPAD1	KeyPAD2	Codec	PTA
GPIO18_BE	PD	GPIO_18	SPI_Slave_ CLK	SDIO_Slave_ CLK	SD_ Master_ CLK (O)	HS_UART1_ DM_CTS		pwm_out_6		KEY_ ROW_5		
GPIO19_BE	X	GPIO_19	SPI_Slave_ CS_N	SDIO_Slave_ CMD	SD_ Master_ CMD (B)	HS_UART1_ DM_TXD		pwm_out_1	KEY_ COL_3	KEY_ ROW_6		
GPIO20_BE	PD	GPIO_20	SPI_SLAVE_ MISO	SDIO_Slave_ DATA_0	SD_ Master_ DATA_0 (B)	HS_UART1_ DM_RXD		pwm_out_2	KEY_ ROW_2	KEY_ ROW_7		
GPIO21_BE	PD	GPIO_21		SDIO_Slave_ DATA_1	SD_ Master_ DATA_1 (B)			pwm_out_4	KEY_ ROW_3			
GPIO22_BE	PD	GPIO_22		SDIO_Slave_ DATA_2	SD_ Master_ DATA_2 (B)			pwm_out_3				
GPIO23_BE	PD	GPIO_23	SPI_SLAVE_ MOSI	SDIO_Slave_ DATA_3	SD_ Master_ DATA_3 (B)	HS_UART1_ DM_RFR		pwm_out_5				
GPIO24_BE	PU	GPIO_24	SPI0_ Master_CS_N			M0&M4_ UART2_RX	JTAG2_BE_ TCK		KEY_ COL_7			
GPIO25_BE	PD	GPIO_25	SPI0_ Master_CLK			M0&M4_ UART2_TX	JTAG2_BE_ TDO		KEY_ ROW_7			
GPIO26_BE	PU	GPIO_26	SPI0_ Master_MOSI				JTAG2_BE_ TMS		KEY_ COL_2			
GPIO27_BE	PU	GPIO_27	SPI0_ Master_MISO				JTAG2_BE_ TDI					
GPIO28_BE	X	GPIO_28									I2S_ BCLK	
GPIO29_BE	X	GPIO_29									I2S_ RXD	
GPIO30_BE	X	GPIO_30									I2S_ TXD	

Table 1-2 GPIO names (cont.)

GPIO #	Chip Internal PU/PD	Primary Function	SPI or I2C or QSPI	SDIO	SD Memory Card	UART	JTAG	PWMADC or SenseADC	KeyPAD1	KeyPAD2	Codec	PTA
GPIO31_BE	X	GPIO_31									I2S_ FSYNC	
GPIO32_BE	X	GPIO_32									I2S_ MCLK	
GPIO33_BE	PD	CHIP_PWD_ L_WL										
GPIO_41_ BE	X	PWR_STATUS										
GPIO42_BE	X	GPIO_42	QSPI_ Master_CLK									
GPIO43_BE	X	GPIO_43	QSPI_ Master_DAT0									
GPIO44_BE	X	GPIO_44	QSPI_ Master_DAT1									
GPIO45_BE	X	GPIO_45	QSPI_ Master_DAT2									
GPIO46_BE	X	GPIO_46	QSPI_ Master_DAT3									
GPIO47_BE	PU	GPIO_47	QSPI_ Master_CS_N									
GPIO48_BE	X	Ext_32K_IN										
GPIO49_BE	X	GPIO_49										
GPIO50_BE	PU	GPIO_50					JTAG3_BE_ TCK					
GPIO51_BE	X	GPIO_51					JTAG3_BE_ TDO					
GPIO52_BE	PU	GPIO_52					JTAG3_BE_ TMS					
GPIO53_BE	PU	GPIO_53					JTAG3_BE_ TDI					

Table 1-2 GPIO names (cont.)

GPIO #	Chip Internal PU/PD	Primary Function	SPI or I2C or QSPI	SDIO	SD Memory Card	UART	JTAG	PWMADC or SenseADC	KeyPAD1	KeyPAD2	Codec	PTA
GPIO54_BE	X	GPIO_54						SENSEADC 2				
GPIO55_BE	X	GPIO_55						SENSEADC 3				
GPIO56_BE	X	GPIO_56						SENSEADC 4				
GPIO57_BE	X	GPIO_57						SENSEADC 5				
GPIO58_BE	X	GPIO_58						SENSEADC 6				
GPIO59_BE	X	GPIO_59				HS_UART2_ DM_CTS (I)		SENSEADC 7				
GPIO60_BE	PD	GPIO_60				HS_UART2_ DM_TXD (O)						BT_ PRIORITY

Table 1-3 WLAN_GPIO names

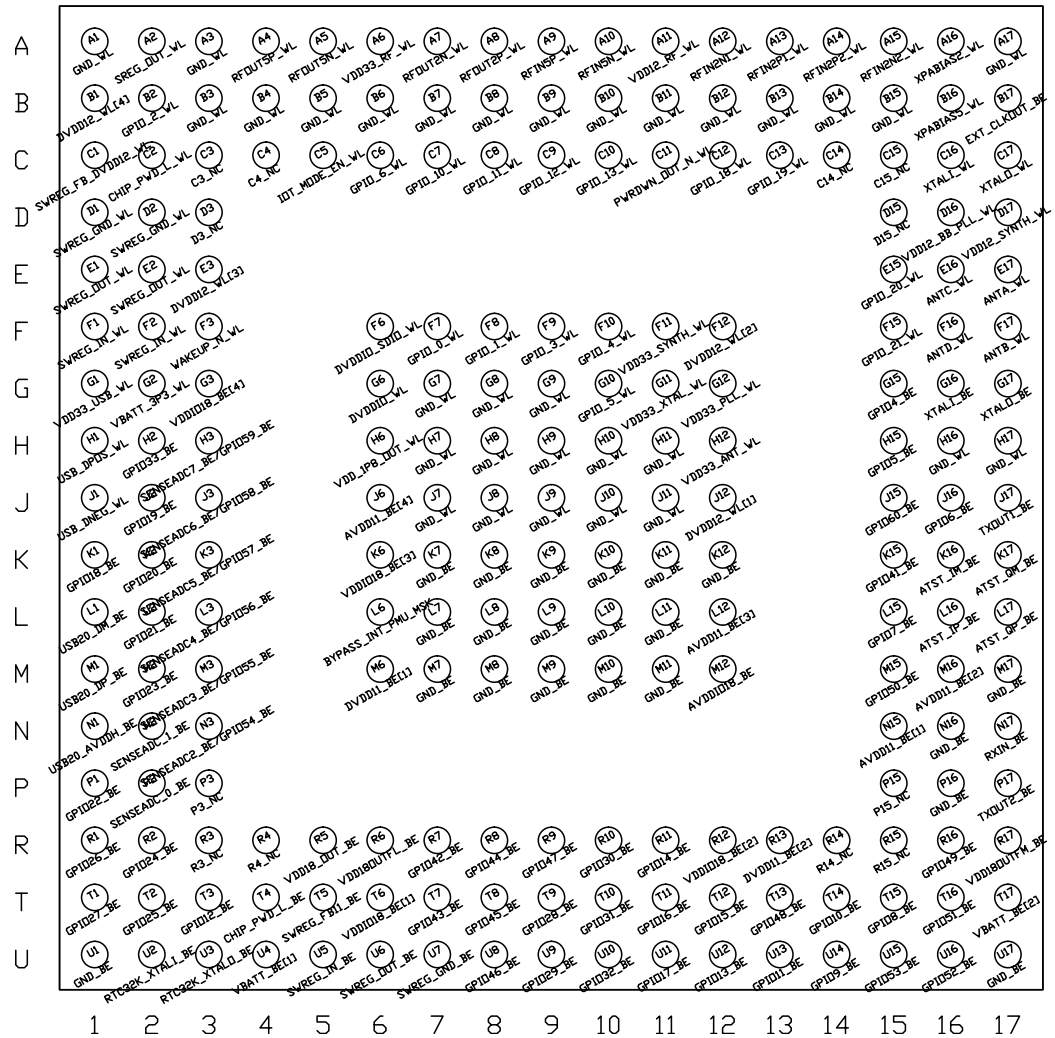
WLAN_GPIO #	PU/PD	GPIO or Others	Debug_UART	EJTAG_WLAN
GPIO_0_WL	X	INT_SDIO_CMD		
GPIO_1_WL		INT_SDIO_D3		
GPIO_2_WL	X	INT_SDIO_D2		
GPIO_3_WL	X	INT_SDIO_D1		
GPIO_4_WL		INT_SDIO_D0		
GPIO_5_WL	X	INT_SDIO_CLK		
GPIO_6_WL	X	GPIO_6_WL		EJTAG_WL_TDI
GPIO_10_WL		GPIO_10_WL	UART0_WL_RXD UART1_WL_RXD UART2_WL_RXD	EJTAG_WL_TMS
GPIO_11_WL	PD	GPIO_11_WL	UART0_WL_TXD UART1_WL_TXD UART2_WL_TXD	
GPIO_12_WL	X	GPIO_12_WL		EJTAG_WL_TCK
GPIO_13_WL	X	GPIO_13_WL	UART0_WL_CTS UART1_WL_CTS	EJTAG_WL_TDO
GPIO_18_WL		WL_WKUP_BE	UART0_WL_RTS UART1_WL_RTS UART2_WL_CTS	
GPIO_19_WL		GPIO_19_WL	UART0_WL_RTS UART0_WL_RXD	
GPIO_20_WL	PU	GPIO_20_WL	UART0_WL_TXD UART1_WL_TXD	
GPIO_21_WL		GPIO_21_WL	UART0_WL_RXD UART1_WL_RXD UART0_WL_RTS	

NOTE GPIO_x_WL are reserved for WLAN debug only. Use GPIOx_BE for the application.

2 Ball definitions

The QCA4020 is available in the 217-ball MSP package that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Chapter 4 for package details. A high-level view of the pin assignments is shown in the following figure.

The QCA4020 provides Wi-Fi, BLE and 15.4 in a 11.2 x 11.2 mm, 0.65 mm pitch 217-ball MSP package.



Top View

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output signal
GND	Ground
NC	No connection should be made to this pin
NP	No pull-up
OD	Digital output signal with open drain
P	Voltage supply
Pad pull details for digital I/Os	
PU	Input signals with weak internal pull-up, to prevent signals from floating when left open
PD	Input signals with weak internal pull-down, to prevent signals from floating when left open

2.2 Ball descriptions

I/Os are grouped according to their functionality and described in the following table.

Table 2-2 Ball descriptions

Pin	Signal Name	Type	Description
XTAL interface			
G16	XTALI_BE	AIO	Crystal 40 MHz.
G17	XTALO_BE	AIO	
B17	EXT_CLKOUT_BE	GND	1.1 Vpp Clock output same as crystal frequency.
C16	XTALI_WL	AIO	Connect directly to GND
C17	XTALO_WL	AIO	Connect XTALO_ WL from EXT_CLKOUT_BE with DC block capacitor.
U2	RTC32K_XTALI_BE	AIO	Optional 32.768 KHz crystal input. Can be No Connect (or floating).
U3	RTC32K_XTALO_BE	AIO	Optional 32.768 KHz crystal output. Can be No Connect (or floating).
Chip Power Down (or Reset) Control			

Table 2-2 Ball descriptions

Pin	Signal Name	Type	Description
T4	CHIP_PWD_L_BE	DI	M4 processor and BLE/15.4 subsystem reset signal (active low).
H2	GPIO33_BE	DO	An output of CHIP_PWD_L_WL (active low).
C2	CHIP_PWD_L_WL	DI	An input of Wi-Fi Reset signal (active low). External 10 kΩ pull down resistor is required.
Control Pins setup			
C5	IOT_MODE_EN_WL	DI	This signal requires 10K ohm pull-down.
F3	WAKEUP_N_WL	DI	This signal requires 10K ohm pull-up.
L6	BYPASS_INT_PMU_MSK	DI	This signal require a 10K ohm pull-down.
USB for manufacture test			
N1	USB20_AVDDH_BE	PS	3.3 V supply for USB 2.0
L1	USB20_DM_BE	AIO	USB D+/D- pins to be used.
M1	USB20_DP_BE	AIO	
SENSEADC Input (single 12-bit ADC with 8 MUX single-ended or 4 MUX differential-ended signals).			
P2	SENSEADC_0_BE	AI	ADC input. If used, VIO must be 1.8V; can be floating if not used.
N2	SENSEADC_1_BE	AI	ADC input. If used, VIO must be 1.8V; can be floating if not used.
N3	SENSEADC2_BE/GPIO54_BE	AI/DIO	Can be used either ADC or generic GPIO. VIO is same as VDDIO_BE[4] (Pin#G3), but chip can only support single VIO in either 1.8V or 3.3V only. When use as ADC, VIO must be 1.8V only. When used as generic GPIO, VIO can be either 1.8V or 3.3V, but ADC must be disabled by SW.
M3	SENSEADC3_BE/GPIO55_BE	AI/DIO	
L3	SENSEADC4_BE/GPIO56_BE	AI/DIO	
K3	SENSEADC5_BE/GPIO57_BE	AI/DIO	
J3	SENSEADC6_BE/GPIO58_BE	AI/DIO	
H3	SENSEADC7_BE/GPIO59_BE	AI/DIO	
Power supply			
U4	VBATT_BE[1]	PS	3.3V Supply input for BLE/15.4.
T17	VBATT_BE[2]	PS	3.3V Supply input for BLE/15.4.
VIO Voltage			
T6	VDDIO_BE[1]	PS	If SENSEADC is used, VIO=1.8V only; otherwise, VIO can be either 1.8V or 3.3V if SENSEADC is not used or disabled by SW.
R12	VDDIO_BE[2]	PS	
K6	VDDIO_BE[3]	PS	
G3	VDDIO_BE[4]	PS	
F6	DVDDIO_AO_WL	PS	
G6	DVDDIO_WL	PS	

Table 2-2 Ball descriptions

Pin	Signal Name	Type	Description
M12	AVDDIO_BE	PS	Analog input supply same as VIO voltage
Internal LDO or VIO on/off switch for BLE and 15.4			
R5	VDD18_OUT_BE	PS	1.8 V LDO output with maximum 40 mA. Can be used as 1.8 V VIO supply.
R17	VDD18OUTFM_BE	PS	1.8 V LDO output (100mA maximum) to support external 15.4/BLE RF Front-end. Floating if not used.
R6	VDD_OUTFL_BE	PS	SW On/Off switch of VIO output to external serial Flash. VIO voltage is based on VDDIO_BE[2].
Internal LDO for Wi-Fi			
A2	SREG_OUT_WL	PS	WLAN Always-on LDO (1.2 V) output, connect to 470pF only.
H6	VDD_1P8_OUT_WL	PS	Do not use. Floating only.
3.3 V input for WLAN			
G2	VBATT_3P3_WL	PS	Not used. VBATT_3P3_WL must be connected directly to GND for proper operation to avoid leakage current)
H12	VDD33_ANT_WL	PS	WLAN Analog 3.3 V input..
G12	VDD33_PLL_WL	PS	
A6	VDD33_RF_WL	PS	
F11	VDD33_SYNTH_WL	PS	
G1	VDD33_USB_WL	PS	
G11	VDD33_XTAL_WL	PS	
BLE/15.4 Switching Regulator (SWREG_BE) and 1.1V of both Digital and Analog.			
U5	SWREG_IN_BE	PS	SWREG_BE Voltage Input (3.3V)
U7	SWREG_GND_BE	GND	SWREG_BE Ground
U6	SWREG_OUT_BE	PS	SWREG_BE Output (1.1V)
T5	SWREG_FB11_BE	PS	SWREG_BE Feedback
M6	DVDD11_BE[1]	PS	Digital 1.1 V input supply
R13	DVDD11_BE[2]	PS	
N15	AVDD11_BE[1]	PS	Analog 1.1 V input supply
M16	AVDD11_BE[2]	PS	
L12	AVDD11_BE[3]	PS	
J6	AVDD11_BE[4]	PS	
WLAN Switching Regulator (SWREG_WL) and 1.2V of both Digital and Analog.			

Table 2-2 Ball descriptions

Pin	Signal Name	Type	Description
F1	SWREG_IN_WL	AI	SWREG_WL Voltage Input (3.3V)
F2	SWREG_IN_WL	AI	
D1	SWREG_GND_WL	GND	SWREG_WL Ground
D2	SWREG_GND_WL	GND	
E1	SWREG_OUT_WL	PS	SWREG_WL Output (1.2V)
E2	SWREG_OUT_WL	PS	
C1	SWREG_FB_DVDD12_WL	AI	SWREG_WL feedback
J12	DVDD12_WL[1]	PS	WLAN Digital 1.2V input
F12	DVDD12_WL[2]	PS	
E3	DVDD12_WL[3]	PS	
B1	DVDD12_WL[4]	PS	
D16	VDD12_BB_PLL_WL	PS	WLAN Analog 1.2V input
A11	VDD12_RF_WL	PS	
D17	VDD12_SYNTH_WL	PS	
GPIO			
G15	GPIO4_BE	DI	WoW input: Wake up on WLAN. WLAN to wake up M4 Processor system. Connect from GPIO_18_WL.
H15	GPIO5_BE	DIO	Generic GPIO
J16	GPIO6_BE	DIO	Generic GPIO
L15	GPIO7_BE	DIO	Generic GPIO
T15	GPIO8_BE	DIO	Generic GPIO
U14	GPIO9_BE	DIO	Generic GPIO
T14	GPIO10_BE	DIO	Generic GPIO
U13	GPIO11_BE	DIO	Generic GPIO
T3	GPIO12_BE	DIO	Generic GPIO
U12	GPIO13_BE	DIO	Generic GPIO
R11	GPIO14_BE	DIO	Generic GPIO
T12	GPIO15_BE	DIO	Generic GPIO
T11	GPIO16_BE	DIO	Generic GPIO
U11	GPIO17_BE	DIO	Generic GPIO
K1	GPIO18_BE	DIO	Generic GPIO
J2	GPIO19_BE	DIO	Generic GPIO
K2	GPIO20_BE	DIO	Generic GPIO
L2	GPIO21_BE	DIO	Generic GPIO
P1	GPIO22_BE	DIO	Generic GPIO

Table 2-2 Ball descriptions

Pin	Signal Name	Type	Description
M2	GPIO23_BE	DIO	Generic GPIO
R2	GPIO24_BE	DIO	Generic GPIO
T2	GPIO25_BE	DIO	Generic GPIO
R1	GPIO26_BE	DIO	Generic GPIO
T1	GPIO27_BE	DIO	Generic GPIO
T9	GPIO28_BE	DIO	Generic GPIO
U9	GPIO29_BE	DIO	Generic GPIO
R10	GPIO30_BE	DIO	Generic GPIO
T10	GPIO31_BE	DIO	Generic GPIO
U10	GPIO32_BE	DIO	Generic GPIO
K15	GPIO41_BE	DIO	Generic GPIO
R7	GPIO42_BE	DIO	Generic GPIO
T7	GPIO43_BE	DIO	Generic GPIO
R8	GPIO44_BE	DIO	Generic GPIO
T8	GPIO45_BE	DIO	Generic GPIO
U8	GPIO46_BE	DIO	Generic GPIO
R9	GPIO47_BE	DIO	Generic GPIO
T13	GPIO48_BE	DIO	Generic GPIO
R16	GPIO49_BE	DIO	Generic GPIO
M15	GPIO50_BE	DIO	Generic GPIO
T16	GPIO51_BE	DIO	Generic GPIO
U16	GPIO52_BE	DIO	Generic GPIO
U15	GPIO53_BE	DIO	Generic GPIO
J15	GPIO60_BE	DIO	Generic GPIO
WLAN GPIO : Do not recommend for other application. Use GPIO_BE first.			
F7	INT_CMD_GPIO_0_WL	DIO	Used for chip internal only, Do not use for other application.
F8	INT_D3_GPIO_1_WL	DIO	
B2	INT_D2_GPIO_2_WL	DIO	
F9	INT_D1_GPIO_3_WL	DIO	
F10	INT_D0_GPIO_4_WL	DIO	
G10	INT_CK_GPIO_5_WL	DIO	

Table 2-2 Ball descriptions

Pin	Signal Name	Type	Description
C6	GPIO_6_WL	DIO	Reserved for WL FW Debug. Not recommended to use in customer application.
C7	GPIO_10_WL	DIO	
C8	GPIO_11_WL	DIO	
C9	GPIO_12_WL	DO	
C10	GPIO_13_WL	DIO	Reserved for WL FW Debug. Not recommended to use in customer application.
C12	GPIO_18_WL	DIO	WoW output: Wake up on WLAN. WLAN to wake up M4 Processor system. Connect to GPIO_4_BE.
C13	GPIO_19_WL	DIO	Reserved for WL FW Debug. Not recommended to use in customer application.
E15	GPIO_20_WL	DIO	
F15	GPIO_21_WL	DIO	
RF Front-End External Switch Control signal for BLE and 15.4			
L16	FE_CTRL0_BE	AO	15.4/BLE RF Front-end control signal. VIO is same as AVDDIO_BE (Pin#M12)
K16	FE_CTRL1_BE	AO	
L17	FE_CTRL2_BE	AO	
K17	FE_CTRL3_BE	AO	
RF Front-End External Switch Control signal for Wi-Fi			
E17	ANTA_WL	DO	WLAN RF switch control (3.3V)
F17	ANTB_WL	DO	
E16	ANTC_WL	DO	
F16	ANTD_WL	DO	
A16	XPABIAS2_WL	AO	Bias for optional external power amplifier in 2.4 GHz
B16	XPABIAS5_WL	AO	Bias for optional external power amplifier in 5 GHz
Radio			
A12	RFIN2N1_WL	AI	WLAN RF primary 2.4GHz receiver differential input
A13	RFIN2P1_WL	AI	WLAN RF primary 2.4GHz receiver differential input
A15	RFIN2N2_WL	AI	WLAN RF Secondary 2.4GHz receiver differential input, Can be floating (or no connect) if not used.
A14	RFIN2P2_WL	AI	WLAN RF Secondary 2.4GHz receiver differential input, Can be floating (or no connect) if not used.

Table 2-2 Ball descriptions

Pin	Signal Name	Type	Description
A10	RFIN5N_WL	AI	WLAN RF 5GHz receiver differential input
A9	RFIN5P_WL	AI	
A7	RFOUT2N_WL	AO	WLAN RF 2.4GHz Transmitter differential output
A8	RFOUT2P_WL	AO	
A5	RFOUT5N_WL	AO	WLAN RF 5GHz Transmitter differential output
A4	RFOUT5P_WL	AO	
N17	RXIN_BE	AI	Both 15.4 and BLE RF receiver input (single- ended)
J17	TXOUT1_BE	AO	15.4 RF Transmitter output.
P17	TXOUT2_BE	AO	BLE RF Transmitter output.
Ground			
K7	GND_BE	GND	Ground
K8	GND_BE	GND	Ground
K9	GND_BE	GND	Ground
K10	GND_BE	GND	Ground
K11	GND_BE	GND	Ground
K12	GND_BE	GND	Ground
L7	GND_BE	GND	Ground
L8	GND_BE	GND	Ground
L9	GND_BE	GND	Ground
L10	GND_BE	GND	Ground
L11	GND_BE	GND	Ground
M7	GND_BE	GND	Ground
M8	GND_BE	GND	Ground
M9	GND_BE	GND	Ground
M10	GND_BE	GND	Ground
M11	GND_BE	GND	Ground
M17	GND_BE	GND	Ground
N16	GND_BE	GND	Ground
P16	GND_BE	GND	Ground
U1	GND_BE	GND	Ground
U17	GND_BE	GND	Ground
A1	GND_WL	GND	Ground
A3	GND_WL	GND	Ground
A17	GND_WL	GND	Ground
B3	GND_WL	GND	Ground
B4	GND_WL	GND	Ground

Table 2-2 Ball descriptions

Pin	Signal Name	Type	Description
B5	GND_WL	GND	Ground
B6	GND_WL	GND	Ground
B7	GND_WL	GND	Ground
B8	GND_WL	GND	Ground
B9	GND_WL	GND	Ground
B10	GND_WL	GND	Ground
B11	GND_WL	GND	Ground
B12	GND_WL	GND	Ground
B13	GND_WL	GND	Ground
B14	GND_WL	GND	Ground
B15	GND_WL	GND	Ground
G7	GND_WL	GND	Ground
G8	GND_WL	GND	Ground
G9	GND_WL	GND	Ground
H7	GND_WL	GND	Ground
H8	GND_WL	GND	Ground
H9	GND_WL	GND	Ground
H10	GND_WL	GND	Ground
H11	GND_WL	GND	Ground
H16	GND_WL	GND	Ground
H17	GND_WL	GND	Ground
J7	GND_WL	GND	Ground
J8	GND_WL	GND	Ground
J9	GND_WL	GND	Ground
J10	GND_WL	GND	Ground
J11	GND_WL	GND	Ground
No Connect			
C14	NC	NC	No Connect
C15	NC	NC	No Connect
C3	NC	NC	No Connect
C4	NC	NC	No Connect
D15	NC	NC	No Connect
D3	NC	NC	No Connect
P15	NC	NC	No Connect
P3	NC	NC	No Connect
R14	NC	NC	No Connect

Table 2-2 Ball descriptions

Pin	Signal Name	Type	Description
R15	NC	NC	No Connect
R3	NC	NC	No Connect
R4	NC	NC	No Connect
J1	NC	AIO	No Connect
H1	NC	AIO	No Connect
C11	NC	NC	No Connect.

3 Electrical characteristics

3.1 Absolute maximum ratings

Operating the QCA4020 under conditions beyond its absolute maximum ratings could damage the device. In the following table, the absolute maximum ratings are limiting values to consider individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, is not guaranteed or implied. Exposure could affect device reliability.

NOTE Maximum rating for signals follows the supply domain of the signals.

Symbol (Domain)	Description	Minimum	Maximum	Unit
VBATT_3P3_WL	WL High Voltage supply	-0.3	4.0	V
SWREG_IN_WL	WL Internal SWREG supply	-0.3	4.0	V
VDD33_WL				
VDD33_ANT_WL, VDD33_RF_WL, VDD33_XTAL_WL, VDD33_PLL_WL, VDD33_SYNTH_WL, VDD33_USB_WL	WL Analog High Voltage supply	-0.3	4.0	V
DVDDIO_AO_WL, DVDDIO_WL, VDDIO_BEx, AVDDIO_BE	VIO supply	-0.3	4.0	V
DVDD12_WL	WL Core Digital supply	-0.3	1.32	V
VDD12_BB_PLL_WL, VDD12_RF_WL, VDD12_SYNTH_WL	WL Core Analog supply	-0.3	1.32	V
SWREG_FB_DVDD12_WL	WL SWREG Feedback/DVDD12 supply	-0.3	1.32	V
VBATT_BE	BE Battery supply	-0.3	4.0	V
SWREG_IN_BE,	BE Internal SWREG supply	-0.3	4.0	V
DVDD11_BE	BE Core Digital supply	-0.3	1.25	V
AVDD11_BE	BE Core Analog supply	-0.3	1.25	V
V_{IH} MIN	Minimum Digital I/O Input Voltage for 1.8 V or 3.3 V I/O Supply	-0.3	–	V
3.3 V I/O V_{IH} MAX	Maximum Digital I/O Input Voltage for 3.3 V I/O Supply	–	Vdd+0.3	V
RF_{in}	Maximum RF input (reference to 50-Ω input)	–	+10	dBm
T_{store}	Storage Temperature	-45	125	°C
T_j	Junction Temperature	–	125	°C

Symbol (Domain)	Description	Minimum	Maximum	Unit
ESD-HBM	Electrostatic Discharge Tolerance under Human Body Model, all pins	-2000	+2000	V
ESD-CDM	Electrostatic Discharge under Charged Device Model, all pins except RF pins	-250	+250	
ESD-CDM-RF	Electrostatic Discharge under Charged Device Model, for the RFIN and RFOUT pins	-250	+250	

3.2 Recommended operating conditions

Operating conditions include parameters under user control, such as the power-supply voltage and ambient temperature. If the absolute maximum ratings have never been exceeded, the QCA4020 is designed to meet the performance specifications listed in Section 3.3 through the remainder of the chapter, when used within the operating conditions, unless otherwise noted in those sections.

Table 3-1 Recommended operating conditions

Symbol (Domain)	Parameter	Min.	Typ.	Max.	Unit
SWREG_IN_WL	WL Internal SWREG supply	3.14	3.3	3.46	V
VDD33_WL					
VDD33_ANT_WL, VDD33_RF_WL, VDD33_XTAL_WL, VDD33_PLL_WL, VDD33_SYNTH_WL, VDD33_USB_WL	WL Analog High Voltage supply	3.14	3.3	3.46	V
DVDD12_WL	WL Core Digital supply	1.2	1.26	1.32	V
VDD12_BB_PLL_WL, VDD12_RF_WL, VDD12_SYNTH_WL	WL Core Analog supply	1.2	1.26	1.32	V
SWREG_FB_DVDD12_WL	WL SWREG Feedback/DVDD12 supply	1.2	1.26	1.32	V
VBATT_BE	BE Battery supply	3.14	3.3	3.46	V
SWREG_IN_BE	BE Internal SWREG supply	3.14	3.3	3.46	V
DVDDIO_AO_WL, DVDDIO_WL, VDDIO_BEx, AVDDIO_BE	VIO = 1.8V	1.71	1.8	1.89	V
	VIO = 3.3V	3.14	3.3	3.46	V
DVDD11_BE	BE Core Digital supply	1.045	1.1	1.23	V
AVDD11_BE	BE Core Analog supply	1.045	1.1	1.23	V
V_{IH} MIN	Minimum Digital I/O Input Voltage for 1.8 V or 3.3 V I/O Supply	-0.3	–	–	V
3.3 V I/O V_{IH} MAX	Maximum Digital I/O Input Voltage for 3.3 V I/O Supply	–	–	V_{dd} +0.3	V
RF_{in}	Maximum RF input (reference to 50-Ω input)	–	–	+10	dBm
T_{store}	Storage Temperature	-45	25	125	°C
T_j	Junction Temperature	–	55	125	°C

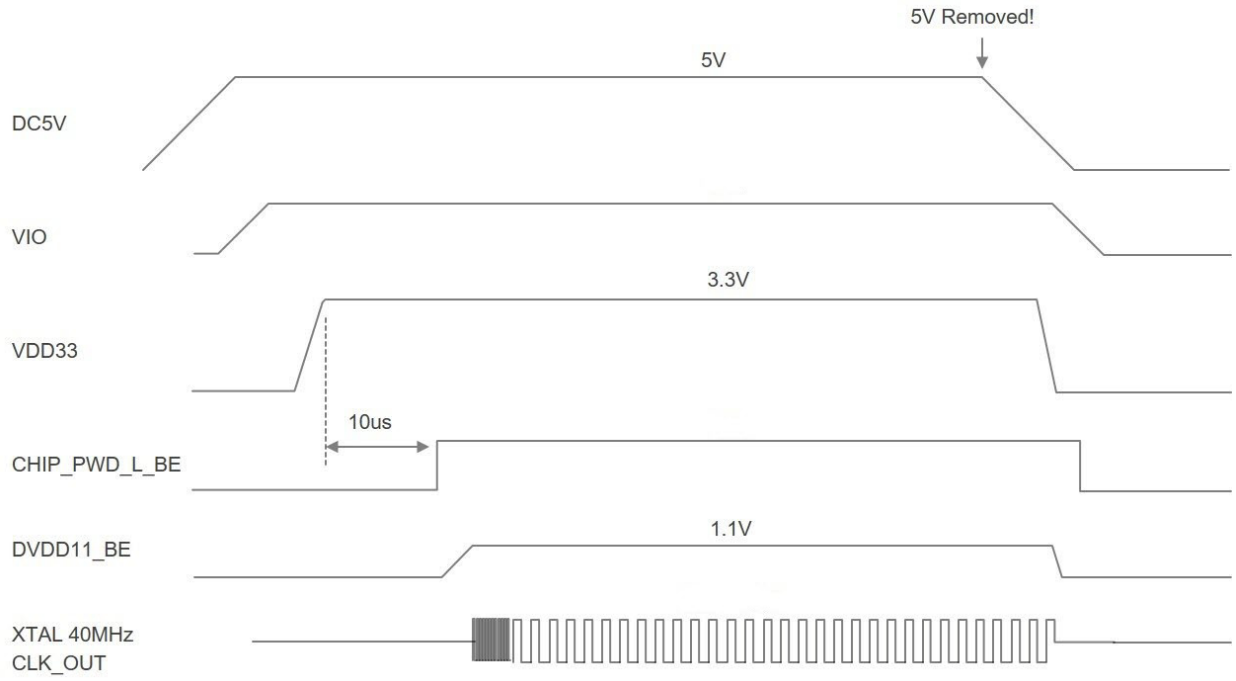
Table 3-1 Recommended operating conditions

Symbol (Domain)	Parameter	Min.	Typ.	Max.	Unit
T_{case}	Standard Case Temperature	0	–	85	°C
	Extended Case Temperature	-40 [1]	–	115	°C

1. Tcase=-40°C is tested at ambient temperature, but other Tcase data were tested at case temperature.

3.3 Power up/down sequencing

The CHIP_PWD_L_BE is the reset pin, and all supplies should be stable for a minimum of 10 µs before CHIP_PWD_L_BE is de-asserted (that is, is greater than V_{IL} for V_{IO}). If VIO = 3.3V, then VDD33 and VIO can share same 3.3V power rail.



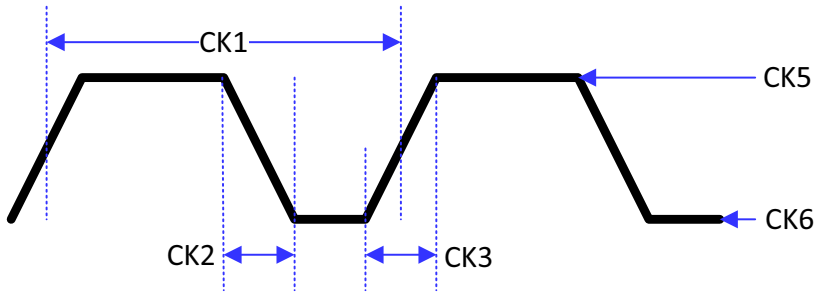
3.3.1 Power-on reset timing

Parameter	Description	Min	Max	Unit
t_R	Rise time of VDD33 to 90% of 3.3 V	–	25	ms
t_S	Minimum of 10 µS before CHIP_PWD_L is de-asserted	10	–	µs

3.4 Digital logic characteristics (3.3 V I/O operation)

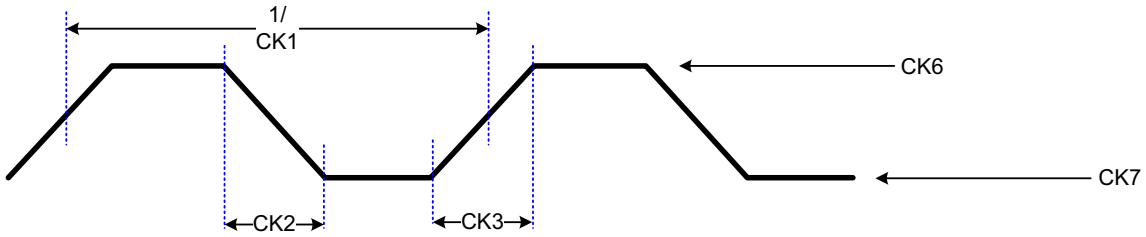
Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	2.4	–	3.6	V
V_{IL}	Low Level Input Voltage	-0.3	–	0.3	V
V_{OH}	High Level Output Voltage	3.0	–	3.6	V
V_{OL}	Low Level Output Voltage	-0.3	–	0.4	V
I_{IH}	High Level Input Current	–	–	60 (Rpd is ON) 0.1 (Rpd is OFF)	µA
I_{IL}	Low Level Input Current	–	–	60 (Rpd is ON) 0.1 (Rpd is OFF)	µA
I_{OH}	High Level Output Current	–	–	5 (x4 drive strength) 3.3 (x2 drive strength) 2 (x1 drive strength)	mA
I_{OL}	Low Level Output Current	–	–	6.7 (x4 drive strength) 4.4 (x2 drive strength) 2.6 (x1 drive strength)	mA
C_{IN}	Input Capacitance	–	5	–	pF

3.5 External 40 MHz reference clock timing



Symbol	Description	Min	Typ	Max	Unit
CK1	Frequency accuracy	-20	–	20	ppm
	Frequency	–	40	–	MHz
CK2	Fall time	–	–	0.1 x period	ns
CK3	Rise time	–	–	0.1 x period	ns
CK4	Duty cycle (high-to-low ratio)	40	–	60	%
CK5	Input high voltage	0.75	–	1.26	V
CK6	Input low voltage	-0.55	–	0.3	V

3.6 External 32.768 KHz sleep clock timing



Parameter	Description	Min	Typ	Max	Unit
CK1	Clock rate	–	32.768	–	KHz
CK2	Fall time	1	–	100	ns
CK3	Rise time	1	–	100	ns
CK4	Duty cycle (high to low ratio)	15	–	85	%
CK5	Frequency stability	-200	–	200	PPM
CK6	Input high voltage	0.8 * VIO	–	VIO	V
CK7	Input low voltage	-0.3	–	VIO	V

NOTE Power up VIO before the external sleep clock is required.

4 Mechanical and ordering information

4.1 Device physical dimensions

The QCA4020 device is available in the 11.2 x 11.2 mm, 0.65 mm pitch 217-ball MSP package that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. Pin A1 is located by an indicator mark on top of the package, and by the ball pattern when viewed from below. A simplified version of the 217 MSP package outline

Figure 4-1 shows a simplified view QCA4020 mechanical dimensions and top and bottom views.

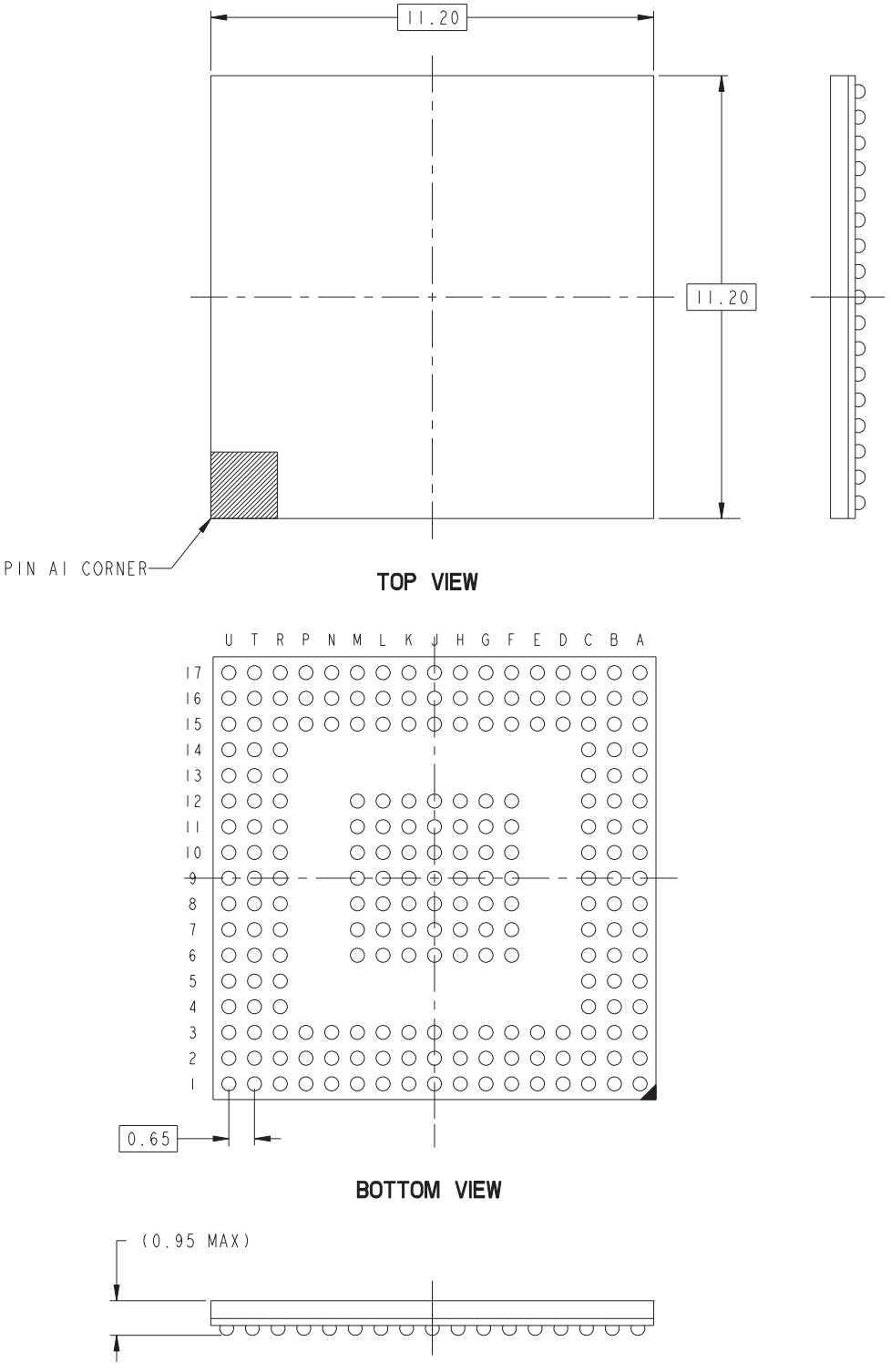


Figure 4-1 QCA4020 simplified package drawing (217 MSP)

4.2 MSP part marking

This device can be ordered using the identification code shown in Section 4.3.

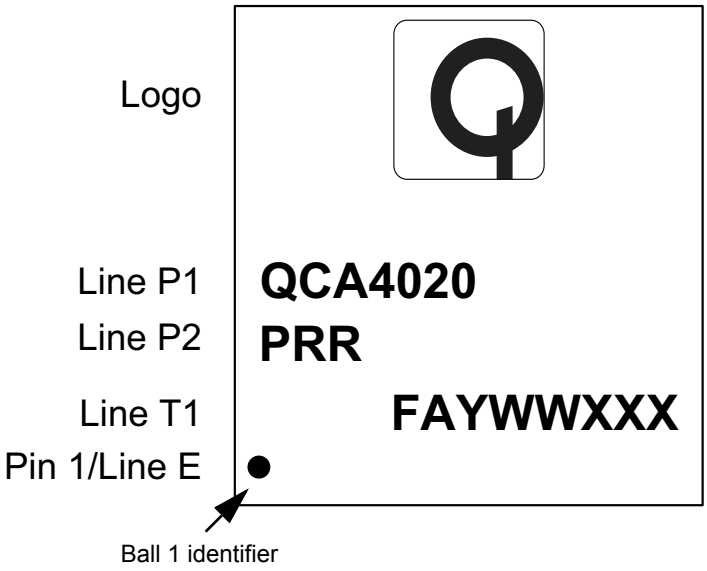


Figure 4-2 QCA4020 part marking (top view)

Table 4-1 MSP part configuration marking

Line	Marking	Description
Logo	Q	Qualcomm® name or logo
P1	QCA4020	Qualcomm product name
P2	PRR	P = Product configuration code RR = Product revision code
T1	FAYWWXXX	F = Source of supply code for wafer fab locations □ When F = F: Fabrication = TSMC A = Source of supply code for assembly site (ball drop) code □ When A = E: Fabrication = ASE □ When A = K: Fabrication = SPIL Y = Single/last-digit of year WW = Two-digit work week of current year XXX = 3 character lot code serial number
Pin 1/Line E		Ball 1 identifier

4.3 Device ordering information

This device can be ordered using the identification code shown in Figure 4-3, and explained below.

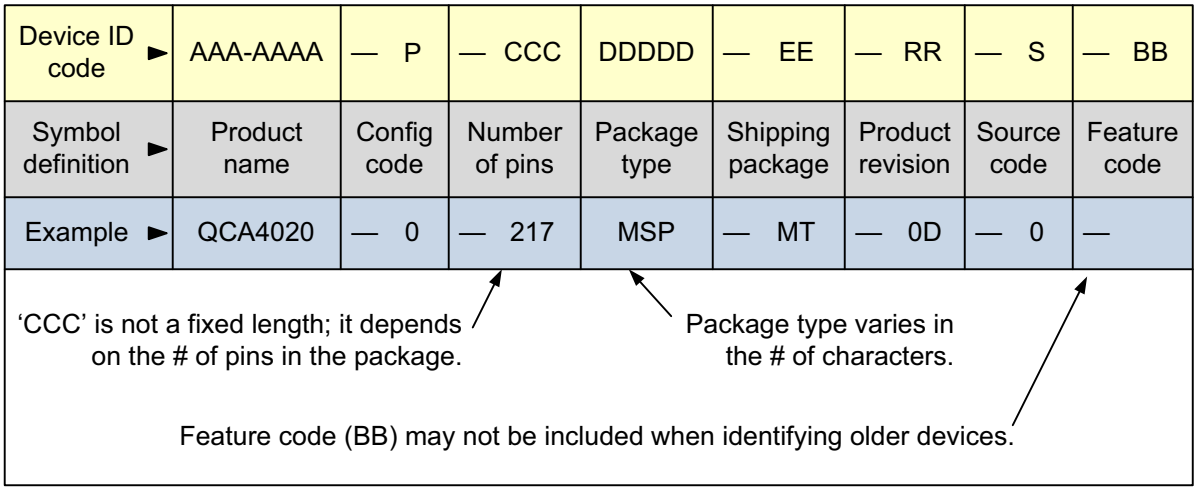


Figure 4-3 Device identification code

Table 4-2 Ordering information

Product Part Number	Temp	Ordering Number[1]	PRR	Product Type
QCA4020	C-temp	QCA-4020-0-217MSP-MT-0D-0	00D	CS
QCA4020	C-temp	QCA-4020-0-217MSP-TR-0D-0	00D	CS
QCA4020	I-temp	QCA-4020-1-217MSP-MT-0D-0	10D	CS
QCA4020	I-temp	QCA-4020-1-217MSP-TR-0D-0	10D	CS

1. MT – Matrix tray, TR —Tape and reel

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-3.

Table 4-3 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH;
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH, QCA4020 rating
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

Qualcomm Technologies, Inc. (QTI) follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The QCA4020 is classified as MSL3; the qualification temperature is 30ºC.*** This qualification temperature (30°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.5 Device thermal characteristics

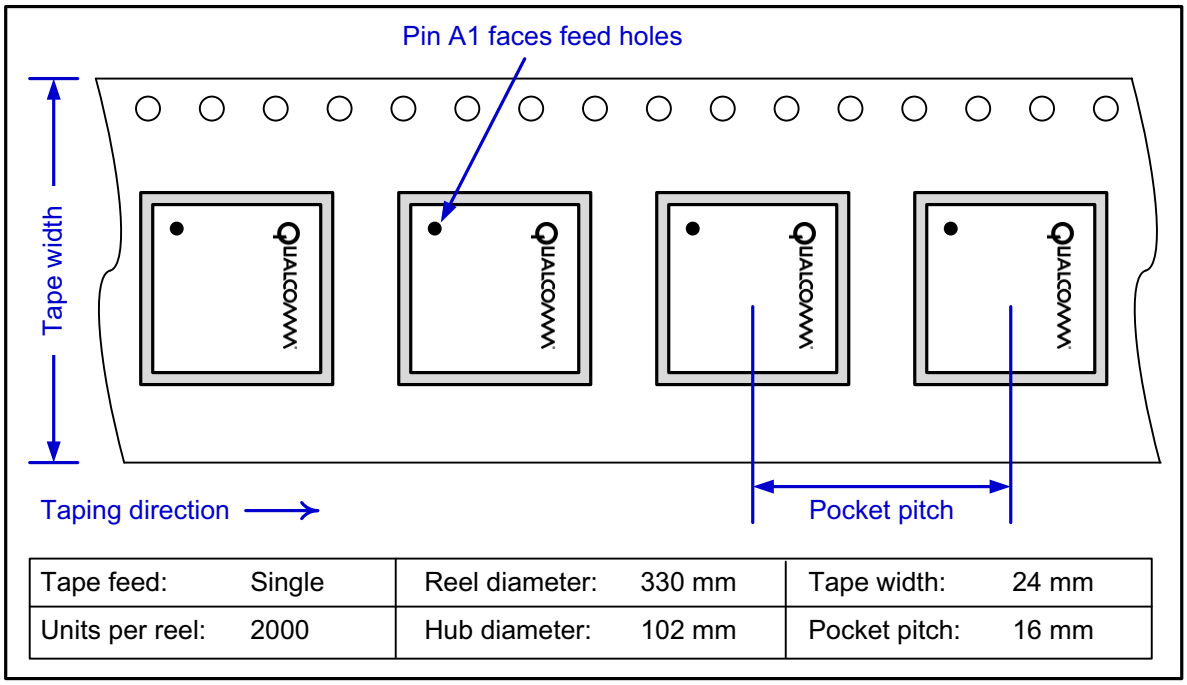
Parameter	Comments	Comments	Typ
θ_{JA}	Thermal resistance, J-to-A	Junction-to-ambient (still air)[1]	26.8
ψ_{JT}	Thermal resistance, J-to-T	Junction-to-ambient (still air)[1]	0.1
θ_{JA}	Thermal resistance, J-to-C	Junction-to-ambient (still air)[1]	5.6
θ_{JA}	Thermal resistance, J-to-B	Junction-to-ambient (still air)[1]	8.5

1. Junction-to-ambient thermal resistance ($\theta_{JAa)}$ is calculated with ambient temperature = 30.8 ºC.

5 Carrier, storage, & handling information

5.1 Tape and reel information

A simplified sketch of the QCA4020 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	102 mm	Pocket pitch:	16 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

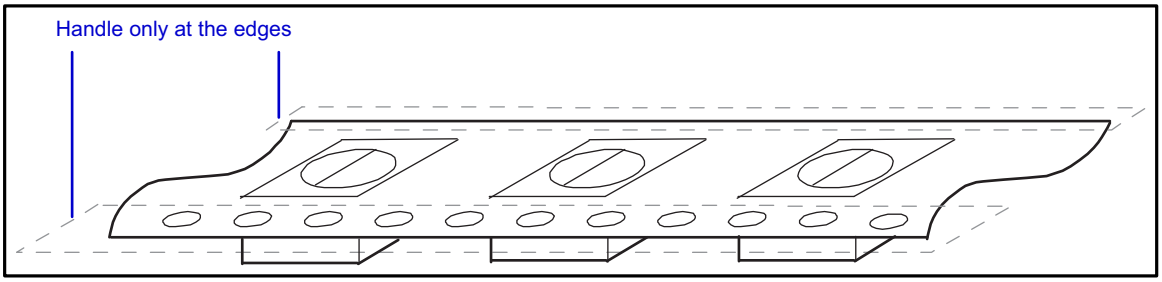


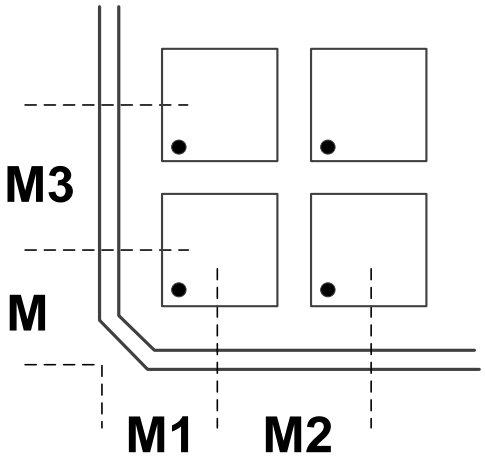
Figure 5-2 Tape handling

5.2 Matrix tray information

The device pin 1 is oriented to the chamfered corner of the matrix tray.

Each tray of the QCA4020 contains up to 168 devices. Production orders of the QCA4020 that are shipped in matrix tray carriers will be in [5 + 1, 10 + 1] tray stacks of [840, 1680] units. The stacking configuration and quantity for sample orders will vary.

See Figure 5-3 for matrix-tray key attributes and dimensions.



Key Dimensions	
Array	8 x 21 (168 units)
M	11.95 mm
M1	11.00 mm
M2	14.65 mm
M3	16.00 mm

Figure 5-3 Matrix-tray key attributes and dimensions

5.3 Storage

5.3.1 Bagged storage conditions

QCA4020 delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags.

5.3.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating as described in Section 4.4.

5.4 Handling

Tape handling was described in Section 5.2. Other (IC-specific) handling guidelines are presented in the following subsections.

5.4.1 Baking

It is **not necessary** to bake the QCA4020 if the conditions specified in Section 5.3.1 and Section 5.3.2 have **not been exceeded**.

It is **necessary** to bake the QCA4020 if any condition specified in Section 5.3.1 or Section 5.3.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.4.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

6 PCB mounting guidelines

6.1 RoHS compliance

The device is lead-free and RoHS-compliant. Its SnAgCu solder balls use SAC125/Ni composition.

6.2 SMT parameters

The information presented in this section describes Qualcomm Technologies board-level characterization process parameters. It is included to assist customers when starting their SMT process development; it is not intended to be a specification for customer SMT processes.

NOTE Qualcomm Technologies recommends that customers follow their solder paste vendor recommendations for the screen-printing process parameters and reflow profile conditions.

Qualcomm Technologies characterization tests attempt to optimize the SMT process for the best board-level reliability possible. This is done by performing physical tests on evaluation boards, which may include:

- Drop shock
- Temperature cycling
- Bend cycle (optional)

6.2.1 Land pad and stencil design

Qualcomm Technologies recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile **prior to PCB production**. Optimizing the solder stencil-pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

6.2.2 Reflow profile

Reflow profile conditions typically used by Qualcomm Technologies for SnPb and lead-free systems are given in Table 6-1.

Table 6-1 Qualcomm Technologies typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Lead-free (high temperature condition limits)
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Dry out and flux activation	150 to 190°C	60 to 120 sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C[1]	50 to 70 sec
Cool down	Cool rate – ramp-to-ambient	< 220°C	6°C/sec max

1. During the reflow state, the peak temperature should not exceed 245°C. This temperature should not be confused with the peak temperature reached during MSL testing.

Figure 6-1 shows the typical SMT reflow profile.

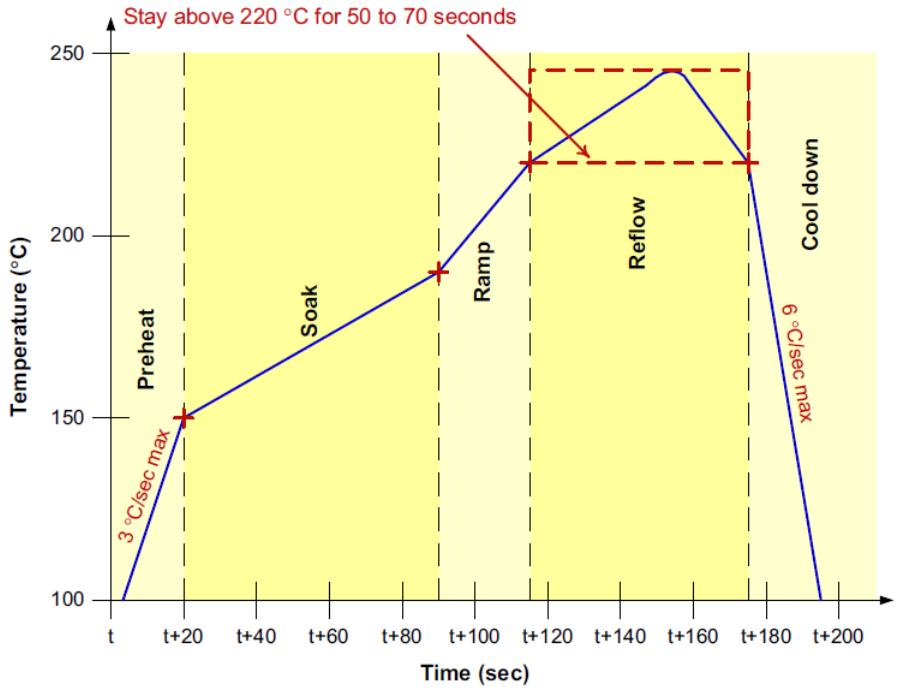


Figure 6-1 Typical SMT reflow profile

6.2.3 SMT peak package-body temperature

During a production board's reflow process, the temperature for the package must be controlled. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more).

Although the solder-paste manufacturer's recommendations for optimum temperature and duration for solder reflow must be followed, the Qualcomm Technologies recommended limits must not be exceeded.

6.2.4 SMT process verification

Qualcomm Technologies recommends verification of the SMT process prior to high-volume PCB fabrication, including:

- Electrical continuity
- X-ray inspection of the package installation for proper alignment, solder voids, solder balls, and solder bridging
- Visual inspection
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume

6.3 Board-level reliability

Qualcomm Technologies conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- (Optional) Cyclic bend testing (JESD22-B113)

A Terminology and Usage

A.1 Terms and acronyms

Table A-1 defines terms and acronyms commonly used throughout this document.

Table A-1 Terms and acronyms

Term	Definition
π/4 DQPSK	π/4 rotated differential quadrature phase shift keying
8DPSK	8-state differential phase shift keying
16QAM	16-state quadrature amplitude modulation
64QAM	64-state quadrature amplitude modulation
ADC	Analog-to-digital converter
AoA	Angle of arrival
BER	Bit error rate
BLE	Bluetooth low energy
DAC	Digital-to-analog converter
DBS	Dual-band simultaneous
EDR	Enhanced data rate
EIA	Electronic Industries Alliance
GPIO	General-purpose input/output
HS	High Speed (for Bluetooth)
JESD	JEDEC standards
kbps	kilobits per second
MSL	Moisture Sensitivity Level (for PCBs)
PA	Power amplifier
PDET	Power detector
PM	Power management
RDBS	Radio Broadcast Data System (USA)
RDS	Radio Data System (Europe)
RSSI	Received signal strength indicator
RH	Relative humidity
RoHS	Restriction of Hazardous Substances
SMT	Surface mount technology

Table A-1 Terms and acronyms (cont.)

Term	Definition
SnPb	Tin-Lead (for solder)
SoC	System-on-chip (single die)
SRO	Solder resistant opening
UART	Universal asynchronous receiver transmitter
WLAN	Wireless local area network
WLPSP	Wafer Level Pico Scale Package
WSI	WLAN to Serial interface (proprietary Qualcomm interface)

A.2 Special marks

Table A-2 defines special marks used in this document.

Table A-2 Special marks

Mark	Definition
( )	Brackets (( )) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, SDC1_DATA(7:4) may indicate a range that is 4 bits in length, or DATA(7:0) may refer to all eight DATA pins.
_N	A suffix of _N indicates an active low signal. For example, RESIN_N.
0x0000	Hexadecimal numbers are identified with an x in the number (for example, 0x0000). All numbers are decimal (base 10) unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number; for example, 0011 (binary).
|	A blue vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.