
STM32
CubeMX

1. Description

1.1. Project

Project Name	firmware
Board Name	NUCLEO-G474RE
Generated with:	STM32CubeMX 6.3.0
Date	11/01/2021

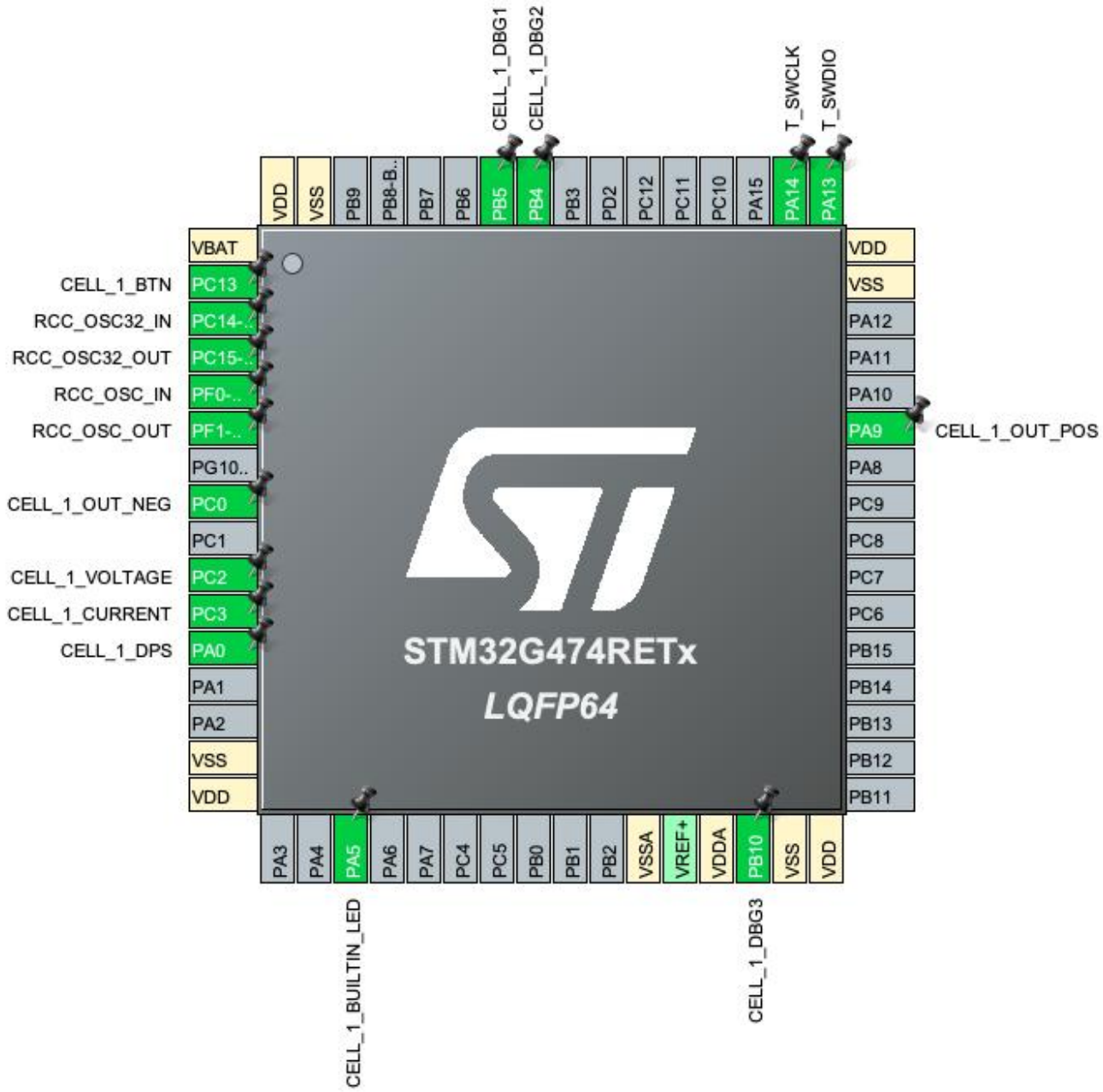
1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x4
MCU name	STM32G474RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	ARM Cortex-M4

2. Pinout Configuration

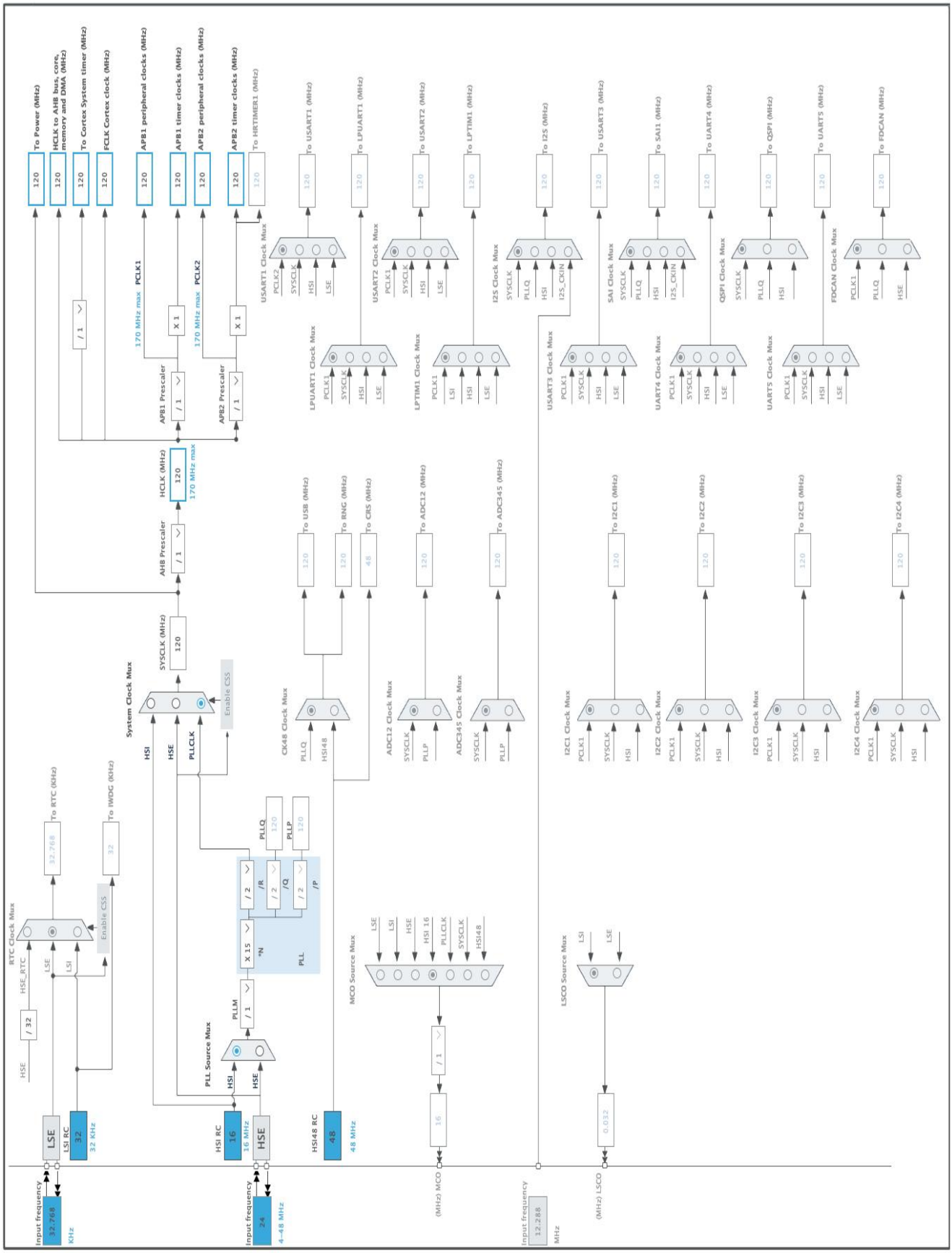


3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	CELL_1_BTN
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
8	PC0 *	I/O	GPIO_Output	CELL_1_OUT_NEG
10	PC2	I/O	ADC1_IN8	CELL_1_VOLTAGE
11	PC3	I/O	ADC2_IN9	CELL_1_CURRENT
12	PA0	I/O	GPIO_EXTI0	CELL_1_DPS
15	VSS	Power		
16	VDD	Power		
19	PA5 *	I/O	GPIO_Output	CELL_1_BUILTIN_LED
27	VSSA	Power		
29	VDDA	Power		
30	PB10 *	I/O	GPIO_Output	CELL_1_DBG3
31	VSS	Power		
32	VDD	Power		
43	PA9 *	I/O	GPIO_Output	CELL_1_OUT_POS
47	VSS	Power		
48	VDD	Power		
49	PA13	I/O	SYS_JTMS-SWDIO	T_SWDIO
50	PA14	I/O	SYS_JTCK-SWCLK	T_SWCLK
57	PB4 *	I/O	GPIO_Output	CELL_1_DBG2
58	PB5 *	I/O	GPIO_Output	CELL_1_DBG1
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	firmware
Project Folder	/Users/rfeijoo/Documents/OneDrive/CubeMX/firmware
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_G4 V1.4.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_TIM1_Init	TIM1
4	MX_ADC1_Init	ADC1
5	MX_ADC2_Init	ADC2
6	MX_ADC5_Init	ADC5
7	MX_TIM2_Init	TIM2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x4
MCU	STM32G474RETx
Datasheet	DS12288_Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

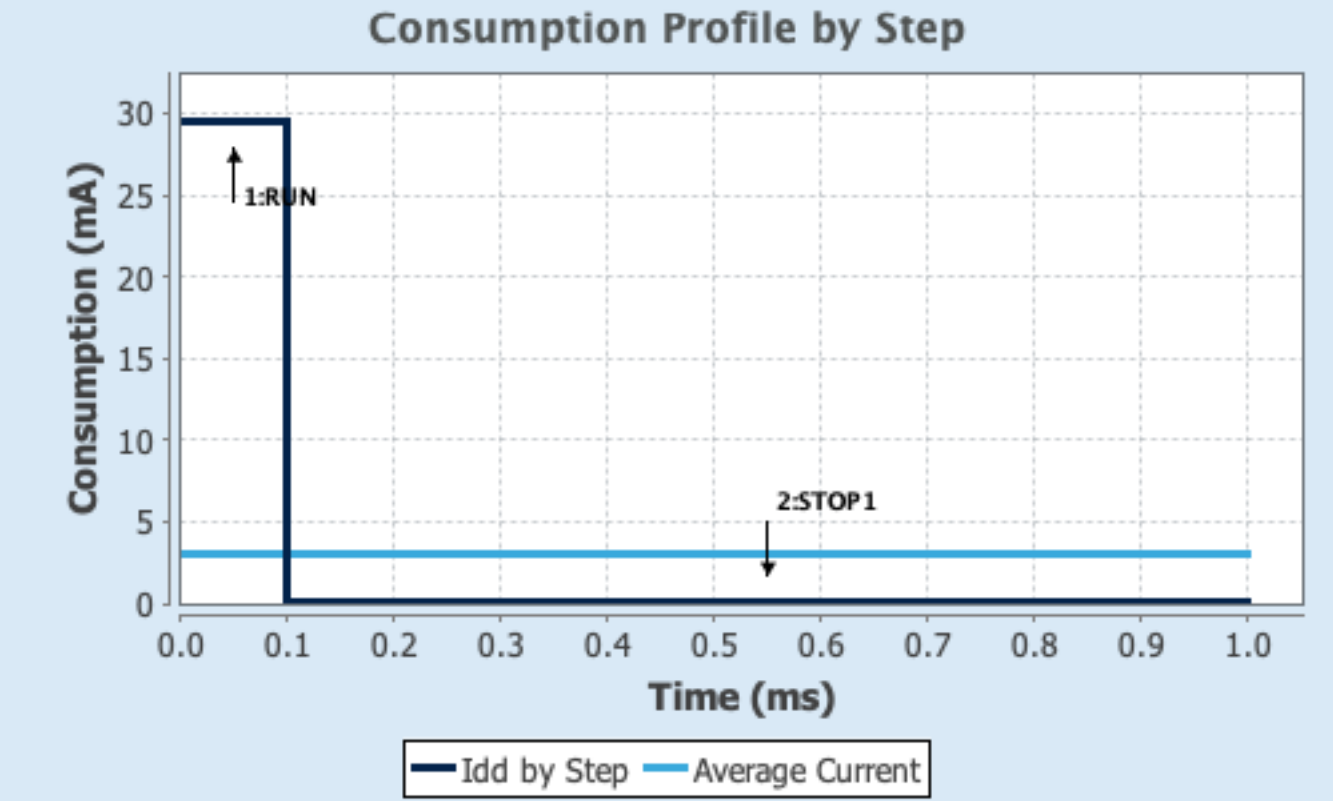
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP1
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Boost	NoRange
Fetch Type	FLASH/DualBank/ART	NA
CPU Frequency	170 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	29.5 mA	80.5 µA
Duration	0.1 ms	0.9 ms
DMIPS	213.0	0.0
Ta Max	124.25	129.98
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	3.02 mA
Battery Life	1 month, 16 days, 9 hours	Average DMIPS	212.5 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
30
25
20
15
10
5
0
1:RUN
2:STOP1
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

IN8: IN8 Single-ended

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	**Dual regular simultaneous mode only ***
DMA Access Mode	DMA access mode disabled
Delay between 2 sampling phases	1 Cycle

ADC_Settings:

Clock Prescaler	Synchronous clock mode divided by 2
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Gain Compensation	0
Scan Conversion Mode	Disabled
End Of Conversion Selection	**End of sequence of conversion ***
Low Power Auto Wait	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
Overrun behaviour	Overrun data preserved

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 8
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. ADC2

IN9: IN9 Single-ended

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	**Dual regular simultaneous mode only ***
DMA Access Mode	DMA access mode disabled
Delay between 2 sampling phases	1 Cycle

ADC_Settings:

Clock Prescaler	Synchronous clock mode divided by 2
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Gain Compensation	0
Scan Conversion Mode	Disabled
End Of Conversion Selection	**End of sequence of conversion ***
Low Power Auto Wait	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
Overrun behaviour	Overrun data preserved

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
Rank	1
Channel	Channel 9
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.3. ADC5
mode: Temperature Sensor Channel
mode: Vrefint Channel

7.3.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Synchronous clock mode divided by 2
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Gain Compensation	0
Scan Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Low Power Auto Wait	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
Overrun behaviour	Overrun data preserved

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel Temperature Sensor
Sampling Time	**640.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator
Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	3 WS (4 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

Peripherals Clock Configuration:

Generate the peripherals clock configuration	TRUE

7.5. SYS

Debug: Serial Wire
Timebase Source: SysTick
mode: save power of non-active UCPD - deactive Dead Battery pull-up

7.6. TIM1

Clock Source : Internal Clock

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**119 ***
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**1041 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

7.7. TIM2

Clock Source : Internal Clock

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**11999 ***
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 32 bits value)	**10000 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC2	ADC1_IN8	Analog mode	No pull-up and no pull-down	n/a	CELL_1_VOLTAGE
ADC2	PC3	ADC2_IN9	Analog mode	No pull-up and no pull-down	n/a	CELL_1_CURRENT
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	T_SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	T_SWCLK
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	CELL_1_BTN
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CELL_1_OUT_NEG
	PA0	GPIO_EXTI0	**External Interrupt Mode with Rising/Falling edge**	No pull-up and no pull-down	n/a	CELL_1_DPS
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CELL_1_BUILTIN_LED
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CELL_1_DBG3
	PA9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CELL_1_OUT_POS
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CELL_1_DBG2
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CELL_1_DBG1

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line0 interrupt	true	0	0
ADC1 and ADC2 global interrupt	true	0	0
TIM1 update interrupt and TIM16 global interrupt	true	0	0
TIM2 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
ADC5 global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM15 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM17 global interrupt	unused		
TIM1 capture compare interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
EXTI line0 interrupt	false	true	true
ADC1 and ADC2 global interrupt	false	true	true
TIM1 update interrupt and TIM16 global interrupt	false	true	true
TIM2 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true
ADC5 global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00431551.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00355726.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00500968.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00074240.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00083249.pdf
Application note	http://www.st.com/resource/en/application_note/DM00121475.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00311483.pdf
Application note	http://www.st.com/resource/en/application_note/DM00355687.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00442716.pdf

Application note	http://www.st.com/resource/en/application_note/DM00442720.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00605707.pdf
Application note	http://www.st.com/resource/en/application_note/DM00607955.pdf
Application note	http://www.st.com/resource/en/application_note/DM00610467.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625282.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf