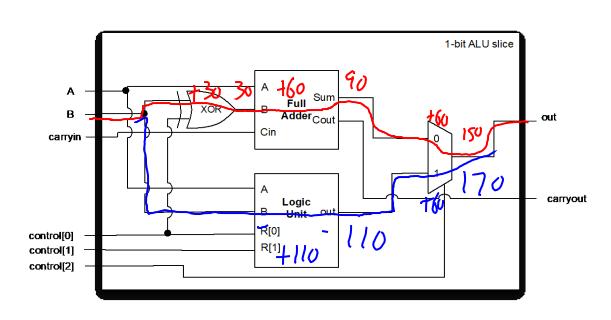
Computing components from ALU1 iclicker.





What is the worst cas€ propagation delay from B to out? (consider both arithmetic and logic operations)

A: 120ps

B: 150ps

C: 160ps

D: 170ps

E: 190ps

| XOR | In | Out | Delay |
|-------|-----|------|-------|
| gate | A,B | out | 30ps |
| | | | |
| Full | In | Out | Delay |
| Adder | A,B | Sum | 60ps |
| | Cin | Sum | 30ps |
| | A,B | Cout | 90ps |
| | Cin | Cout | 60ps |
| | | | |

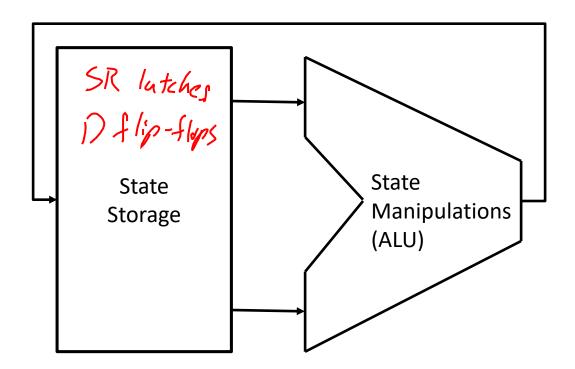
| .ogic | In | Out | Delay | |
|-------|-------------|-----|-------|--|
| Unit | A, <u>B</u> | out | 110ps | |
| | R | out | 10ps | |

| 2-to-1 | In | Out | Delay | |
|-------------|-----|-----|-------|--|
| Multiplexor | 0,1 | out | 60ps | |
| | S | out | 80ps | |

Exam 2 content Starts today
Finite State Machines Happy job fairing Honor's section lecture + HW post tonight

State – the central concept of computing

How do we generate control signals for circuits? Finite State Machines



Today's lecture

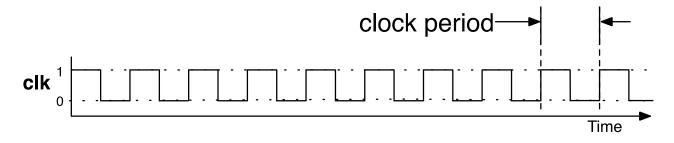
- Goal: Build a sequential circuit from a state diagram
 - Step 0: Problem specification
 - Step 1: Build the state diagram
 - Setp 2: Build the state table
 - Step 3: Build the sequential circuit using D flip-flops
- Timing diagram
- Another example: Sequence recognizer

If a combinational logic circuit is an implementation of a Boolean function, then a sequential logic circuit can be considered an implementation of a finite state machine.

Synchronous Design

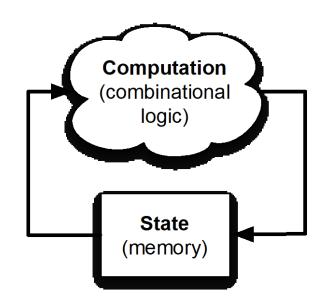
- The easiest (and most common) way to build computers
- All state elements get updated at the same time
 - Using a clock signal

- Clock signal
 - A square wave with a constant period

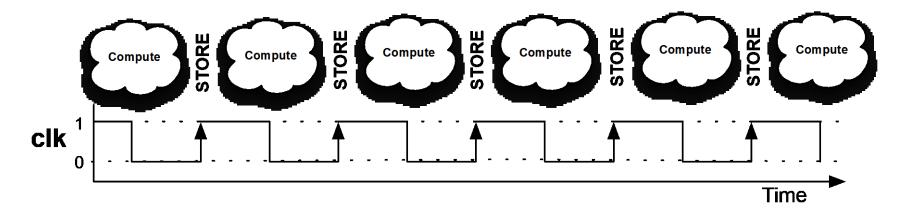


- We always update state at the same point in wave
 - E.g., the rising edge

Synchronous Design, cont.

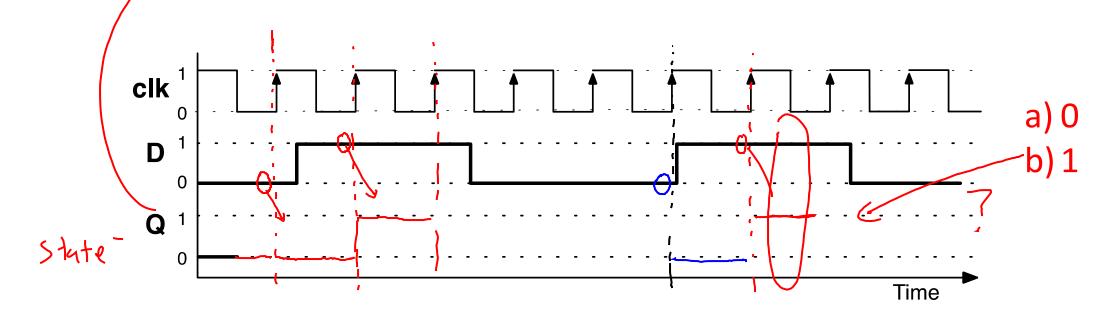


• Alternate between computation and updating state.



The state element that we really want...

- The D flip flop
 - Holds 1 bit of state
 - Output as Q.
 - Inputs
 - Copies D input into state on rising edge of clock.



Next-State Output Logic Outputs Inputs State Logic nextA X $Clk \overline{Q}$ nextB $Clk \overline{Q}$

Step 0: Problem Specification

- We have a candy machine that dispenses candies that cost 15-cents
 - Accepts
 - nickels (5-cents)
 - dimes (10-cents)
 - Dispenses a candy if the balance is ≥ 15-cents
 - When the customer overpays
 - the machine does not return change, but
 - keeps the balance for future transactions



Step 1: Build the State Diagram

Inputs

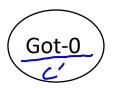
Ouputs

State identification

| d n | |
|-----|---|
| C | no money inserted nickel "I dime "I not possible |
| 0 | no candy candy |

Step 1: Build the State Diagram

Outputs: candy or candy'





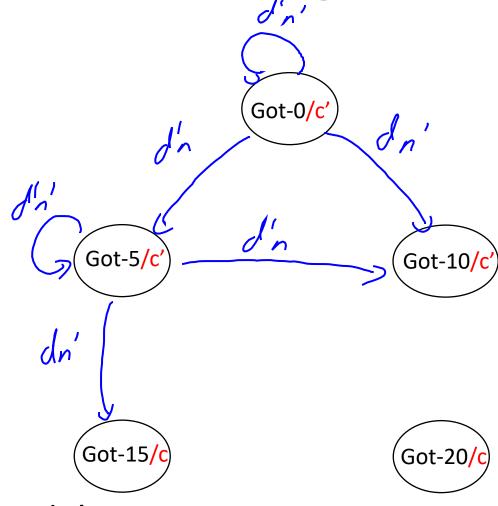






- a) candy
- b) candy'

Step 1: Build the State Diagram



Inputs: d'n', d'n, dn'

Step 1: Build the State Diagram iclicker.

What are the transitions for state Got-15?

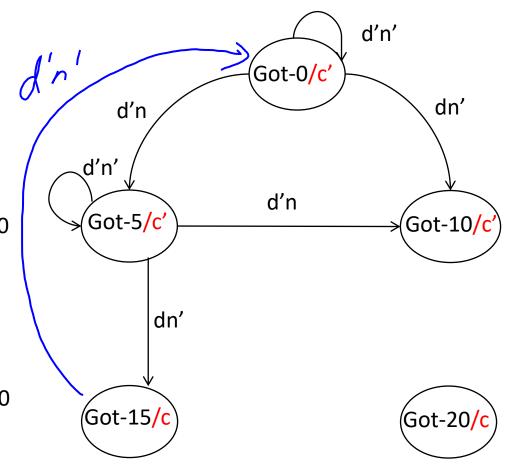
A: d'n': Got0; d'n: Got20; dn': Got20

B: d'n': Got0; d'n: Got0; dn': Got0

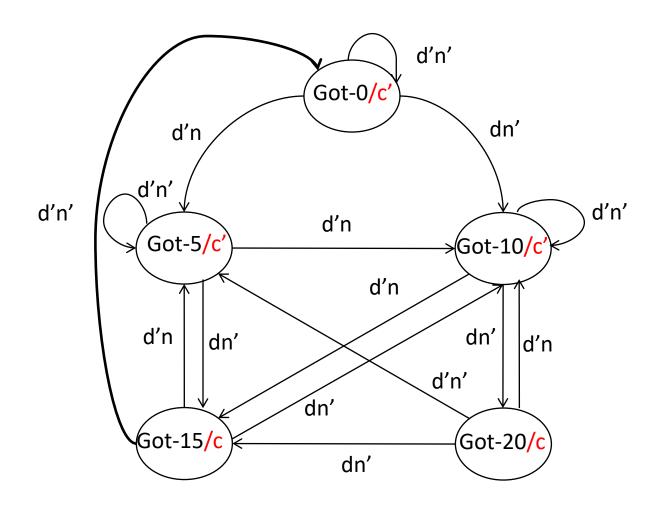
C: d'n': Got0; d'n: Got5; dn': Got10

D: d'n': Got15; d'n: Got5; dn': Got10

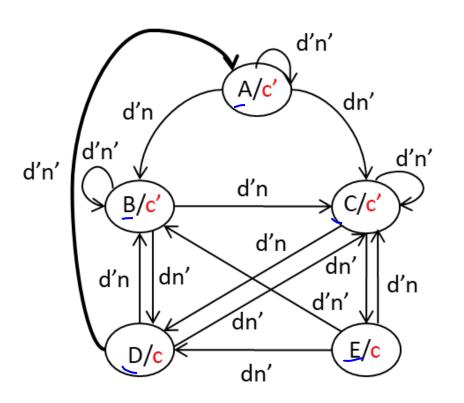
Inputs: d'n', d'n, dn'



Final State Diagram



Step 2: Build a State Table

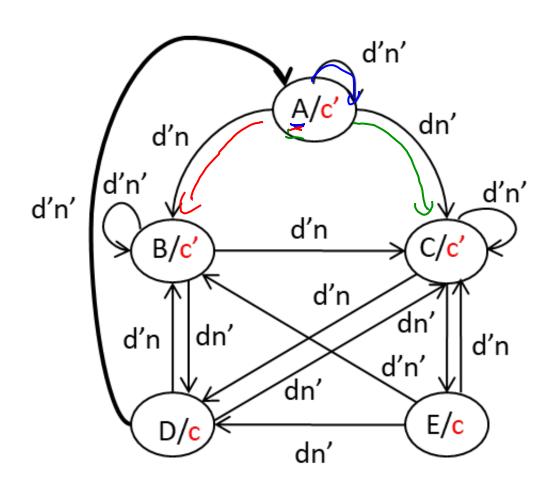


| Current State | Output candy |
|------------------|---------------|
| А | \mathcal{O} |
| В | 0 |
| С | 0 |
| D | 1 |
| E | (|

Candy = D+E

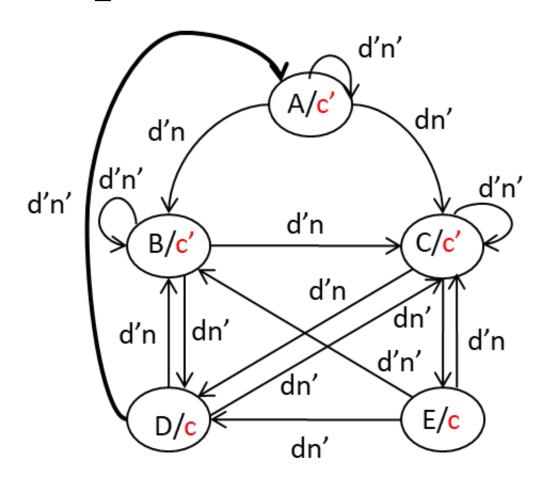
In a 'Moore machine', the outputs are a function only of the current state.

Step 2: Build a Next-State Table iclicker.



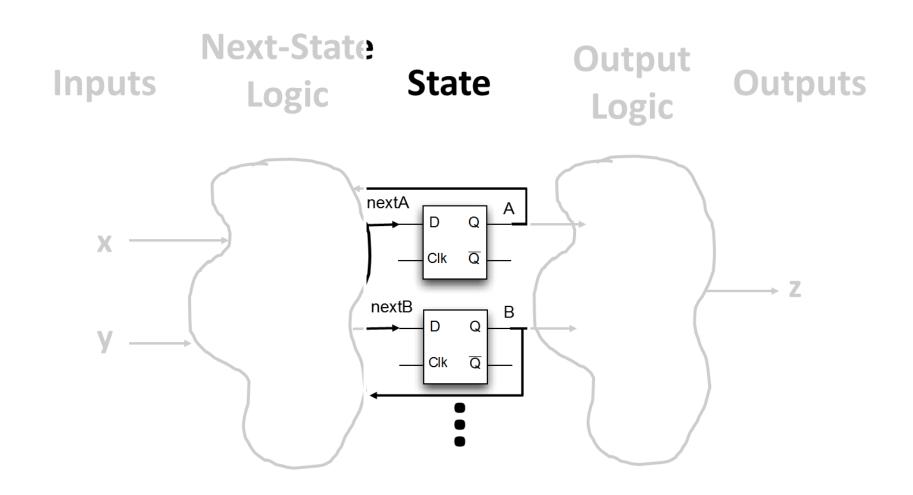
| | | | _ | | | | |
|------------------|-------|---------------|---|---|---|---|---|
| Current State | Input | Next State | | | | | |
| Α | d'n' | A | | | | | |
| Α | ďn | B | | | | | |
| A | _dn′ | C | A | В | С | D | E |
| В | ď'n' | | Α | В | В | В | С |
| В | d'n | | В | С | С | D | D |
| В | dn' | | С | D | Е | Α | Е |
| С | ď'n' | | | | | | |
| С | d'n | | | | | | |
| С | dn' | | | | | | |
| D | d'n' | | | | | | |
| D | ďn | | | | | | |
| D | dn' | | | | | | |
| Е | d'n' | | | | | | |
| Е | ďn | | | | | | |
| Е | dn' | | | | | | |

Step 2: Build a Next-State Table



Why do we need sequential logic to build this circuit?

| Current State | Input | Next State |
|------------------|-------|---------------|
| А | d'n' | А |
| Α | d'n | В |
| А | dn' | С |
| В | d'n' | В |
| В | ďn | С |
| В | dn' | D |
| С | d'n' | С |
| С | d'n | D |
| С | dn' | E |
| D | ďn' | А |
| D | d'n | В |
| D | dn' | С |
| E | d'n' | В |
| E | d'n | С |
| E | dn' | D |



| Current State | Input | Next State |
|------------------|-------|---------------|
| А | ďn' | А |
| А | d'n | В |
| А | dn' | С |
| В | ďn' | В |
| В | d'n | С |
| В | dn' | D |
| С | d'n' | С |
| С | ďn | D |
| С | dn' | E |
| D | d'n' | А |
| D | d'n | В |
| D | dn' | С |
| E | d'n' | В |
| E | d'n | С |
| E | dn' | D |

State Encoding:

5 states: How many bits?

| Current State | Input | Next State |
|------------------|-------|---------------|
| А | ďn' | А |
| А | d'n | В |
| А | dn' | С |
| В | d'n' | В |
| В | d'n | С |
| В | dn' | D |
| С | ďn' | С |
| С | d'n | D |
| С | dn' | E |
| D | d'n' | А |
| D | ďn | В |
| D | dn' | С |
| E | d'n' | В |
| E | ďn | С |
| E | dn' | D |

One hot encoding

ABCDE

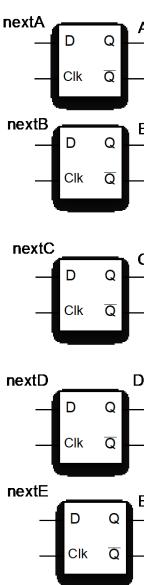
State A = 10000

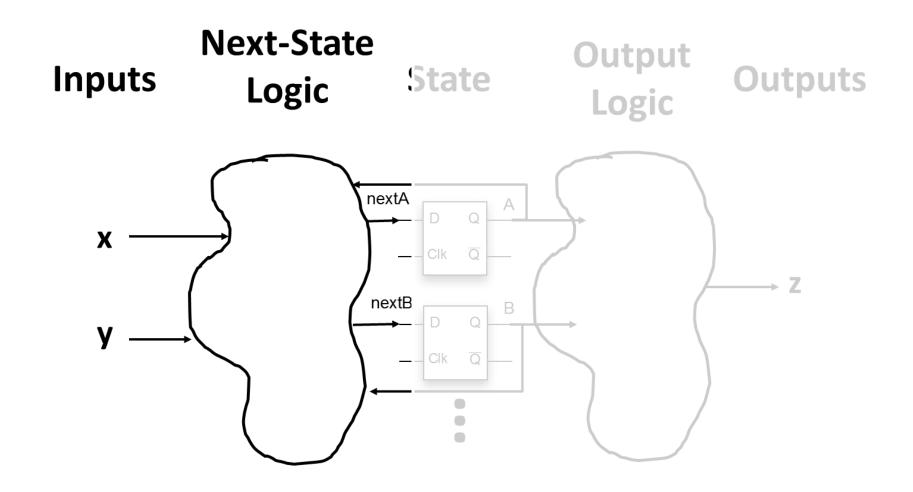
State B = 01000

State C = 00100

State D = 00010

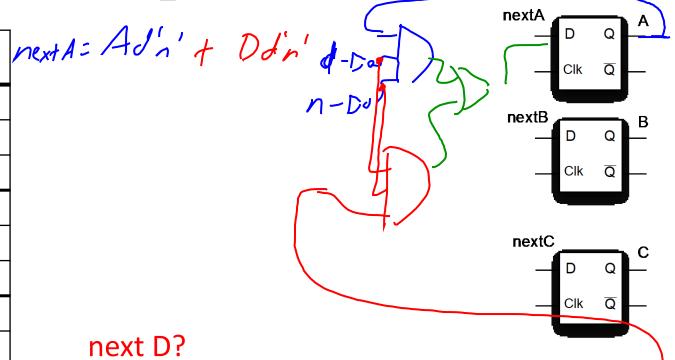
State E = 00001





Step 3: Build Sequential Circuit iclicker.

| t |
|--------|
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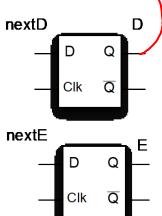
A: nextD = Ad'n' + Dd'n'

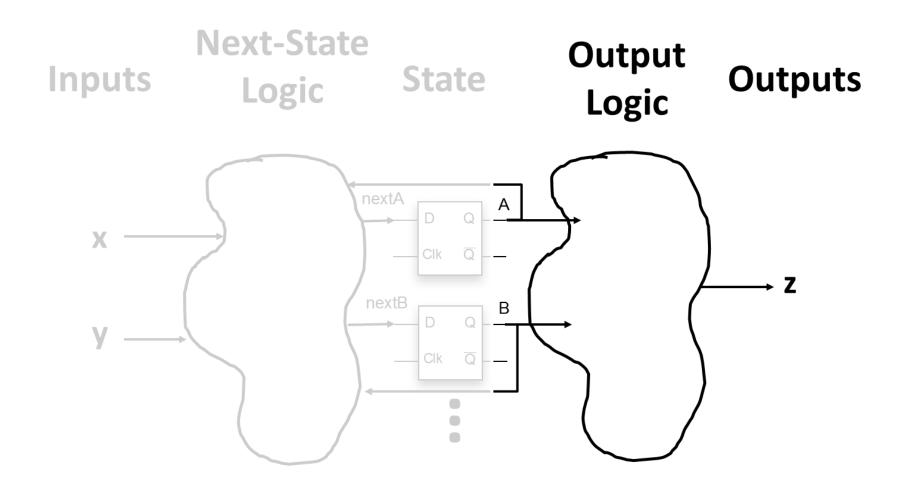
B: nextD= Ad'n + Bd'n' + Dd'n

C: nextD = Bdn' + Cd'n + Edn'

D: nextD = Ad'n' + Bd'n + Cdn'

E: nextD = 1





| Current State | Input | Next State | Output |
|------------------|-------|---------------|--------|
| А | d'n' | А | 0 |
| А | d'n | В | 0 |
| А | dn' | С | 0 |
| В | ďn' | В | 0 |
| В | d'n | С | 0 |
| В | dn' | D | 0 |
| С | ďn' | С | 0 |
| С | d'n | D | 0 |
| С | dn' | E | 0 |
| D | ďn' | А | 1 |
| D | d'n | В | 1 |
| D | dn' | С | 1 |
| E | ďn' | В | 1 |
| E | d'n | С | 1 |
| E | dn' | D | 1 |

```
nextA = Ad'n'+ Dd'n'

nextB = Ad'n + Bd'n' + Dd'n + Edn'

nextC = And' + Bd'n + Cd'n' + Ddn' + Ed'n

nextD = Bdn' + Cd'n + Edn'

nextE = Cdn'
```

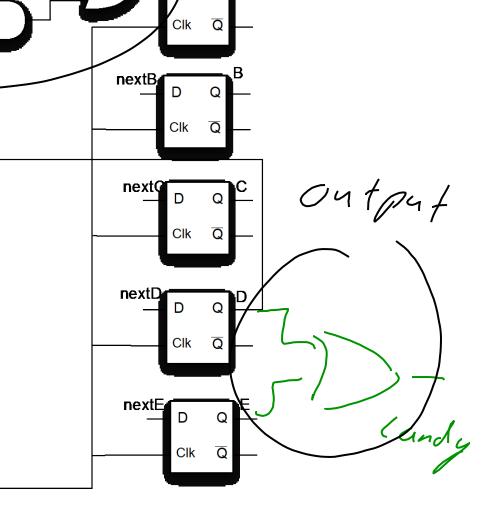
Output: Candy = D + E

Step 3: Sequential circuit with D flip-

flops

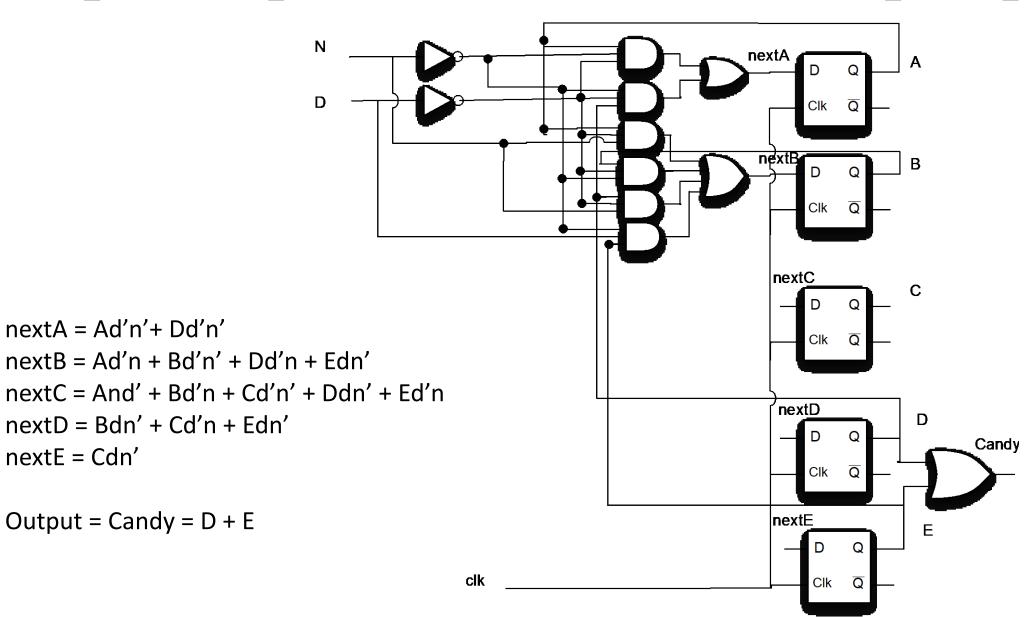
nextA = Ad'n'+ Dd'n' nextB = Ad'n + Bd'n' + Dd'n + Edn' nextC = And' + Bd'n + Cd'n' + Ddn' + Ed'n nextD = Bdn' + Cd'n + Edn' nextE = Cdn'

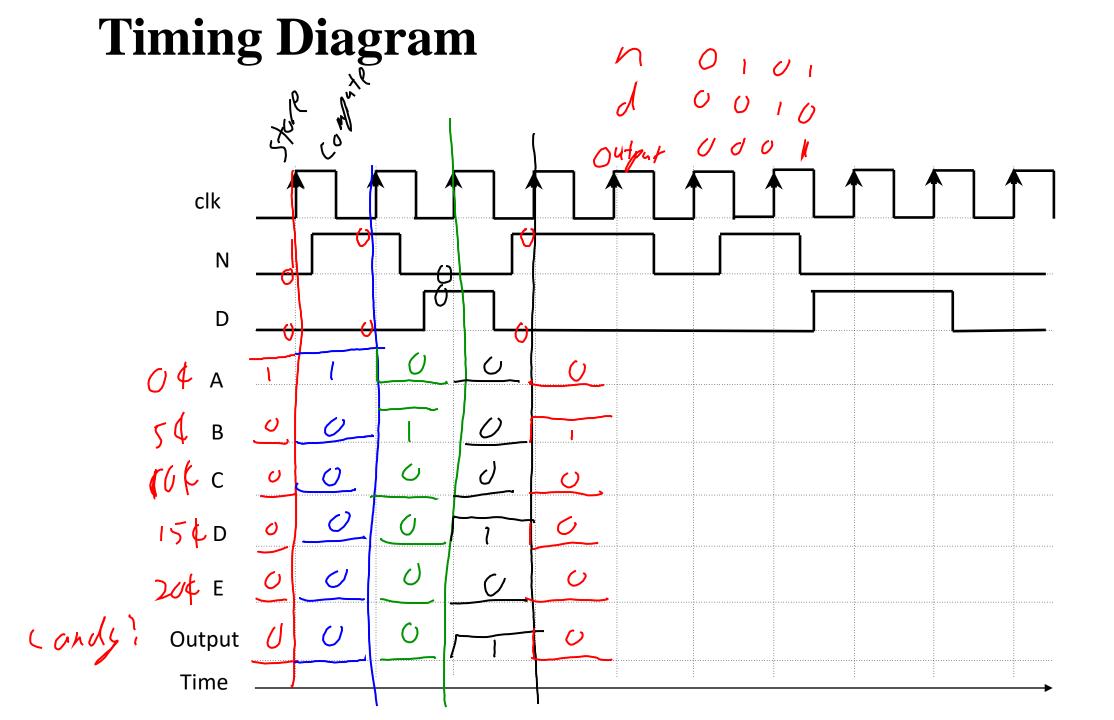
Output: c = D + E



nextA

Step 3: Sequential circuit with D flip-flops





Timing Diagram

