GATE

Computer Science & Information Technology

Computer Organization & Architecture

DPP 01

Cache Organization

Q1 The memory cycle time of a memory is 500nsec. The maximum rate with which the memory can be accessed?
Note: Consider memory as byte addressable.
(A) 500 Bytes / Sec
(B) 2000 Bytes / Sec
(C) 2 Mbytes / Sec
(D) 2 GBytes / Sec

Q2 The address bus width of a memory of size 4096×8 bits is ____ bits?

Q3 Consider a byte addressable memory which has 0.2GBPS writing rate. The memory access time is ___ nanoseconds?

Q4 Consider a word addressable memory of total capacity of 4GB. The memory is accessed using a minimum of 29 bits address bus. The word size per address in this memory is ____ bytes?

Q5 Consider a memory with maximum size of X bytes. Memory is word addressable with word size of W bytes. The size of the address bus of the processor is at least _____ bits?
(A) $Log_2(X/W$
(B) $2^{(X/W)}$
(C) X/W
(D) $Log_2(X)$

Q6 A DRAM chip of 64M × 16 bits has 128K rows of cells with y cells in each row. If DRAM takes x-ns for 1 refresh then total refresh time of the DRAM is _____ Microseconds, if $x = 2 * \log_2 y$?
(A) 1200
(B) 2304
(C) 3202
(D) 5444

Q7 A 32-bits wide main memory unit with a capacity of 16GB is built using 8-bits RAM chips. If there are x-horizontal arrangements of chips are there, with y number of chips in each horizontal arrangement then the value of 10x+y is?

Q8 A cache is used to reduce the effective memory access time of 200ns without cache to 65ns with cache. If cache access time is 50ns, then cache hit rate is _____%?

Q9 A computer system has a cache with cache access time Tc = 10ns, hit ratio of 80% and average memory access time of Tm = 20ns. The access time for physical memory Tp is _____ ns?

Q10 A cache line has 128 bytes. The main memory has addressing latency 64ns and access bandwidth 1GB/s. The time required to fetch the entire cache line from the main memory is _____ ns?

Q11 Consider a system using a cache. The cache is having 70% hit ratio and is 9 times faster than main memory. The average memory access time then increased due to some program execution and the new average access time becomes 40% more than older one of 340ns. The hit ratio of new cache design is ____%?

Q12 Consider a memory hierarchy which takes 500 nanoseconds for access when there is a miss in cache and takes 100 nanoseconds for access when there is a hit in cache. Assume if among all

memory references 90% of the references are having a hit on cache then average memory access time is _____ nanoseconds?

Q13 A system has a write through cache with access time of 100ns and hit ratio of 90%. The main memory access time is 1000ns. 70% of memory references are for read operations. Average memory access time for read-write operations both and effective hit rate(in %) are?

(A) 433, 90% (B) 433, 63%

(C) 190, 90% (D) 190, 63%

Q14 Consider a write through cache which can provide only 63.75% of effective hit rate. If among all memory references 75% references are for read, then the hit ratio of cache for only read operations ____%?

Q15 Consider a write through cache which can provide only 61.92% effective hit rate. If among all memory references 28% references are for write, then the hit ratio of cache for only read operations is _____?

GATE

Answer Key

Q1	(C)
Q2	12~12
Q3	5~5
Q4	8~8
Q5	(A)
Q6	(B)
Q7	324~324
Q8	90~90
Q9	60~60
Q10	192~192
Q11	53~53
Q12	140~140
Q13	(B)
Q14	85~85
Q15	86~86

Hints & Solutions

Q1 Text Solution:

Memory cycle time means memory take 500nanoseconds for read or write on one address.

Here memory is byte addressable hence on 1 address 1 byte content is stored.

In 500 nanoseconds, data accessed from memory = 1 byte

In 1 second, data accessed from memory = 1 byte / 500 nanoseconds

= 0.002

gigabytes per second

= 2

megabytes per second

Q2 Text Solution:

Number of cells in memory = 4096 = 2^{12}

Hence address size for memory = 12 bits

Q3 Text Solution:

For 0.2 GB data, time taken = 1 second

For 1 byte data, time taken = 1 second / 0.2 G

= 5 nanoseconds

Q4 Text Solution:

Address size = 29 bits, hence Number of cells in memory = 2^{29}

Number of cells in memory = total capacity / word size

4GB = 2^{29} / word size

Word size = 4GB / 2^{29}

= $2^{32}/2^{29}$ bytes

= 2^3 bytes

= 8 bytes

Q5 Text Solution:

Number of cells in memory = total capacity / word size

= X/W

Address size of memory = $\log_2(X/W)$

Q6 Text Solution:

Number of cells in memory as given = 64M

128K * cells per row = 64M

Cells per row = 64M / 128K = 2^9

Hence y = 2^9

Hence x = 2 * $\log_2 y$ = 2 * $\log_2 2^9$ = 18 nanoseconds

DRAM refresh time = number of rows of cells * 1 refresh time

= 128K * 18 nanoseconds

= 2304 microseconds

Q7 Text Solution:

32-bits wide main memory means for each address, demanded data is 32 bites = 4 bytes

Number of words in memory = 16GB / 4bytes = 4 G

Hence memory can be represented as 4G 4 bytes

1 chip capacity = 8-bits = 1 byte

Number of chips required = total capacity / 1 chip capacity

(4G 4) / (1)

Here for such memory 32 vertically arranged, 4 chip horizontal arrangements are needed.

Hence x = 32 and y = 4

Value of 10x + y = 10*32 + 4 = 324

Q8 Text Solution:

Without cache memory access time = only main memory access time = 200ns

With cache, memory access time = average memory access time

65 = H * 50 + (1–H) × 200

H = 0.9

H = 90%

Q9 Text Solution:

Average memory access time = 0.8 * 10 + 0.2 * T_p

20 = 0.8 *10 + 0.2* T_p

T_p = 60ns

Q10 Text Solution:

For 1 GB data, memory access time = 1 sec

For 128 bytes data, memory access time = (1sec * 128Bytes) / 1 GBytes

= 128 nanoseconds

The time required to fetch the entire cache line from the main memory is

= Latency time + block access time from memory

= 64 + 128

= 192 ns

Q11 Text Solution:

Main memory access time = 9 * cache memory access time

Old average memory access time = 340ns

340 = 0.7 *Tcm + 0.3*Tmm

340 = 0.7 * Tcm + 0.3 * 9 * Tcm

340 = 3.4 * Tcm

Tcm = 340/3.4 = 100ns

Hence Tmm = 9 * 100 = 900 ns

New average memory access time = 1.4 * 340 = 476

476 = H * 100 + (1-H) * 900

476 = 100 H + 900 – 900H

800 H = 424

H = 424 / 800 = 0.53 = 53 %

Q12 Text Solution:

Here is information given about time required when there is hit and miss, hence general conceptual formula must be used. (Cache and main memory access times are not given explicitly)

Average memory access time = 0.9 * 100 + 0.1 * 500

= 90 + 50

= 140ns

Q13 Text Solution:

Average memory access time for read operations = 0.9 * 100 + 0.1 * 1000 = 90 + 100 = 190ns

Average memory access time for write operations = Main memory access time = 1000ns

Average memory access time for both = 0.7*190 + 0.3 * 1000 = 433 ns

Effective hit rate = Hit rate for read * % of read operations

= 0.9 * 0.7

= 0.63

= 63%

Q14 Text Solution:

Effective hit rate = Hit rate for read * % of read operations

0.6375 = Hit rate for read * 0.75

Hit rate for read = 0.6375 / 0.75 = 0.85 = 85%

Q15 Text Solution:

% of read operations = 100 – 28 = 72 %

Effective hit rate = Hit rate for read * % of read operations

0.6192 = Hit rate for read * 0.72

Hit rate for read = 0.86 = 86%