CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Basics of COA

Lecture No.- 03

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Recap of Previous Lecture

Topic CPU Registers

Topic Memory Access

Topic Memory Addressing

Topics to be Covered

Topic Micro operations

Topic Instructions

Topic : Micro Operation

- The operations executed on values stored in registers
- Symbolic Notation to describe the micro-ops: Register Transfer Language (RTL)

Topic : Micro Operation

R1 = 8 R2 = 8

- Register Transfer: $R1 \leftarrow R2$ or $R2 \rightarrow R1$
- Comma: $IR \leftarrow DR$, $PC \leftarrow PC + 1$
- Memory Transfer:

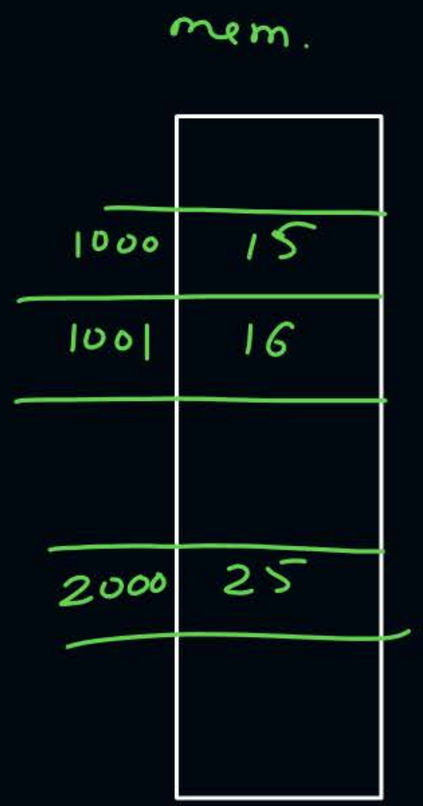
Read :- $DR \leftarrow M[address]$ | $DR \leftarrow M[500]$, $DR \leftarrow M[AR]$

write :- $M[Address] \leftarrow DR$

R1 = ~~5~~ ~~13~~ ~~38~~ 54

R2 = ~~8~~ ~~25~~ 16

R3 = ~~1000~~ 1001



$R1 \leftarrow R1 + R2$

$R2 \leftarrow M[2000]$

$R1 \leftarrow R1 + R2$

$R3 \leftarrow R3 + 1$

$R2 \leftarrow M[R3]$

$R1 \leftarrow R1 + R2$

Value of R1 = 54 ?

[NAT]

Ans = 25

#Q. Consider the following program segment. Here R1 and R2 are the general purpose register. Assume that the content of memory location 2000 is 37. All numbers are in decimal. After the execution of this program the value of memory location 2000 is?

Instructions	Operations
MOV R1, #12	R1 ← #12
MOV R2, (2000)	R2 ← M[2000]
SUB R2, R1	R2 ← R2 – R1
MOV (2000), R2	M[2000] ← R2
HALT	Stop

R1 = 12

R2 = ~~37~~ 25

[NAT]

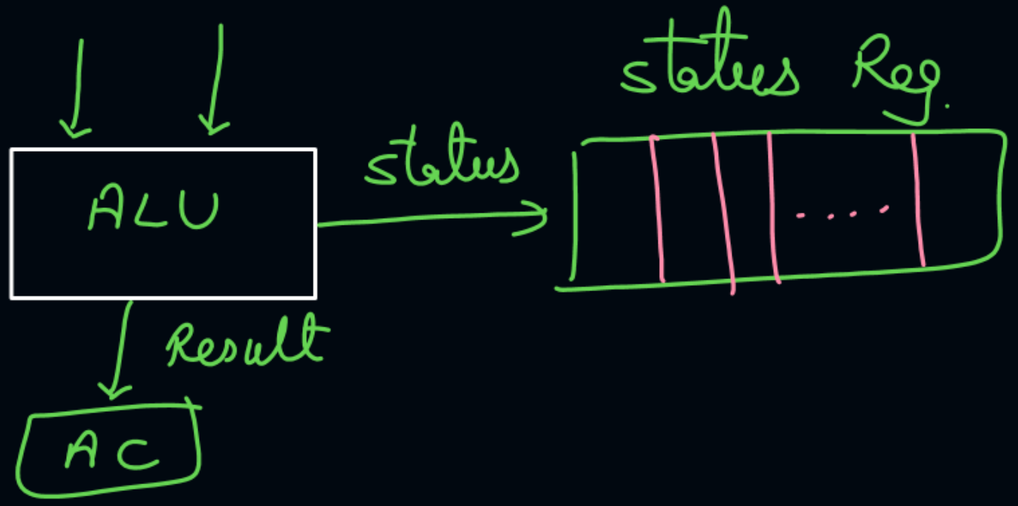
Ans = 140

#Q. Consider the following program segment. Here R1 and R2 are the general purpose register. Assume that the content of memory location 3000 is 13. All numbers are in decimal. After the execution of this program the value of memory location 3000 is?

Instructions	Operations
MOV R1, #7	R1 ← #7
MOV R2, (3000)	R2 ← M[3000]
ADD R2, R1	R2 ← R2 + R1
MUL R1, R2	R1 ← R1 * R2
MOV (3000), R1	M[3000] ← R1
HALT	Stop

R1 = ~~7~~ 140

R2 = ~~13~~ 20


ALU
status
status Reg.
Result
AC

[NAT]

Ans = 52

#Q. Consider the following program segment. Here R1 and R2 are the general-purpose register. Assume that the content of memory location 1000 is 9. All the numbers are in decimal.

	Instructions	Operations
	MOV R1, (1000)	R1 ← M[1000]
	MOV R2, #7	R2 ← #7
LOOP:	ADD R2, R1	R2 ← R2 + R1
	DEC R1	R1 ← R1 – 1
	BNZ LOOP	Branch on not zero
	HALT	Stop

0 1 2 3 4

R1 = 9 8 7 6 5

R2 = 7 16 24 31 37 42 46 49 51 52

The value of R2 at the end of program execution is?

[MCQ] GATE- 2007

#Q. Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

mem add. for word addressable mem.

	Instruction	Operation	Instruction Size (no. of words)	
1000	MOV R1, (3000)	R1 ← M[3000]	2 = 2*4 = 8B	1000
1008 LOOP:	MOV R2, (R3)	R2 ← M[R3]	1 = 4B	1002
1012	ADD R2,R1	R2 ← R1 + R2	1	1003
1016	MOV (R3),R2	M [R3] ← R2	1	1004
1020	INC R3	R3 ← R3 + 1	1	1005
1024	DEC R1	R1 ← R1 – 1	1	1006
1028	BNZ LOOP	Branch on not zero	2	1007
1036	HALT	Stop	1	1009

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. The number of memory reference for accessing the data in executing the program completely is

A 10

B 11

C 20

D 21

Solution

	Operation
LOOP:	R1 ← M[3000]
	R2 ← M[R3]
	R2 ← R1 + R2
	M [R3] ← R2
	R3 ← R3 + 1
	R1 ← R1 – 1
	Branch on not zero
	Stop

R3 = ~~2000~~ ~~2001~~ ~~2002~~ ... 2010

R1 = ~~10~~ ~~9~~ ~~8~~ ... 0

R2 = ~~100~~ ~~110~~ ~~100~~ ~~109~~ ~~100~~ ~~108~~ ~~100~~ 107

No. of mem. references = $2x + 1 \Rightarrow 21$

x = no. of times loop runs $\Rightarrow x = 10$

Memory

1000	Instns
2000	~~100~~ 110
2001	~~100~~ 109
2002	~~100~~ 108
2003	~~100~~ 107
2004	~~100~~ 106
2005	~~100~~ 105
2006	~~100~~ 104
2007	~~100~~ 103
2008	~~100~~ 102
2009	~~100~~ 101
2010	100
3000	10

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.
Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is:

A ✓ 100

B 101

C 102

D 110

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occurs during the execution of the instruction "INC R3", what return address will be pushed on the stack?

A 1005

B 1020

C 1024

D 1040

Ques) in prev. questⁿ, mem. is word addressable, then what return address is pushed onto stack.

Ans = 1006

[NAT] GATE- 2021

#Q. Consider the following instruction sequence where registers R1, R2 and R3 are general purpose and MEMORY [X] denotes the content at the memory location X.

1000

1004

Instruction	Semantics	Instruction Size (bytes)
MOV R1, (5000)	R1 ← MEMORY[5000]	4
MOV R2, (R3)	R2 ← MEMORY[R3]	4
ADD R2, R1	R2 ← R1 + R2	2
MOV (R3), R2	MEMORY[R3] ← R2	4
INC R3	R3 ← R3 + 1	2
DEC R1	R1 ← R1 – 1	2
BNZ 1004	Branch if not zero to the given absolute address	2
HALT	Stop	1

Assume that the content of the memory location 5000 is 10, and the content of the register R3 is 3000. The content of each of the memory locations from 3000 to 3010 is 50. The instruction sequence starts from the memory location 1000. All the numbers are in decimal format. Assume that the memory is byte addressable.

After the execution of the program, the content of memory location 3010 is 50 ?

True/False

Accumulator is used to store result of ALU only? → false

True/False

Size of IR is always equal to size of AC? → false

IR → 'instⁿ

AC → operand or result of ALU

True/False

Size of PC is always equal to size of AR? → True

PC → mem. add.

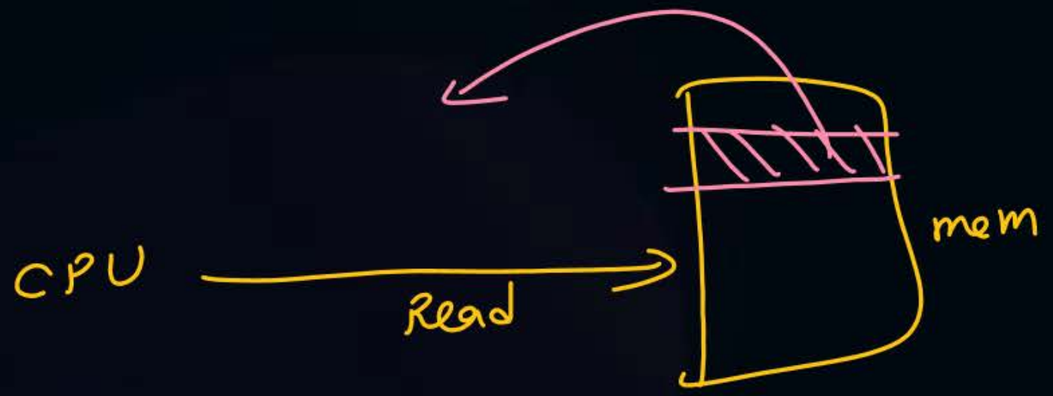
AR → mem. add.

True/False

Control bus is fully bidirectional? → false

True/False

Read control Signal is unidirectional from memory to CPU? → false



True/False

CPU Design is given along with Computer Architecture? → True

True/False

Having 2 set of all buses (address, data and control bus) can enable CPU to access instruction and data from single memory chip simultaneously? → false

[MCQ] GATE- 2023 H.W. [2023 : 2M]

#Q. Consider the given C-code and its corresponding assembly code, with a few operands U1–U4 being unknown. Some useful information as well as the semantics of each unique assembly instruction is annotated as inline comments in the code. The memory is byte-addressable.

```
//C-code
int a[10], b[10], i;
// int is 32-bit
for (i=0; i<10;i++)
a[i] = b[i] * 8;
```

```
;assembly-code (; indicates comments)
;r1-r5 are 32-bit integer registers
;initialize r1=0, r2=10
;initialize r3, r4 with base address of a, b
L01: jeq r1, r2, end      ;if(r1==r2) goto end
L02: lw r5, 0(r4)         ;r5 <- Memory[r4+0]
L03: shl r5, r5, U1       ;r5 <- r5 << U1
L04: sw r5, 0(r3)         ;Memory[r3+0] <- r5
L05: add r3, r3, U2       ;r3 <- r3+U2
L06: add r4, r4, U3
L07: add r1, r1, 1
L08: jmp U4               ;goto U4
L09: end
```

Continue to Next Slide...

Which of the following options is a correct replacement for operands in the position (U1, U2, U3, U4) in the above assembly code?

A (8, 4, 1, L02)

B (3, 4, 4, L01)

C (8, 1, 1, L02)

D (3, 1, 1, L01)

2 mins Summary

Topic Micro operations

Topic Instructions

Happy Learning

THANK - YOU