CS & IT ENGINEERING

Computer Organization Architecture

IO Organization

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#Q. 8-bit characters are transmitted using a synchronous mode of transmission with 1 start bit, 8 data bits and 1 stop bit. The efficiency of the transmission line is ___?

Total bit sent for one character = 1 start-bit + 8 character bits + 1 stop bit

$$\Rightarrow 1 + 8 + 1 = 10 \text{ bits.}$$

Effuceny of transmission of line = (bit Per character) / bit transmitted Percharact

$$\Rightarrow 8/10 = \underline{0.8}$$

#Q. 8-bit characters are transmitted using a parity synchronous mode of transmission with 1 start bit, 8 data bits, 2 stop bits and 1 parity bit. If the transfer rate of the line is 3000 bits per second, then effective transfer rate is _____ bytes per second?

Total bit sent for one character = 1 start bit + 8 character bit + 2 stop bit + 1 parity bit

$$= 1 + 8 + 2 + 1 = 12 \text{ bit}$$

Efficiency of transmission $\bar{\eta} = \dfrac{(\text{bit per character})}{(\text{bit transmitted})} = \dfrac{8}{12} = \dfrac{2}{3}$

Efficien Rate $\Rightarrow 2/3 \times 3000 = 2000$ bit per second

$2000/8 = \boxed{250} \text{ byte}$

#Q. Consider a CPU which takes 0.05 microseconds as interrupt overhead time when a device generates interrupt for CPU, and CPU accepts it. After that CPU takes 5 cycles to service the interrupt. If CPU runs on 10MHz clock rate then total time CPU spends for interrupt service is _____ microseconds (rounded upto 2 decimal places)?

CPU cycle time = $\frac{1}{10}$ MHz = 0.1 micros.

Total interrupt-service time = interrupt-overhead time + interrupt-service time

= 0.05 + 5 × 0.1

= 0.55

#Q.   Which of the following is connected to CPU directly?

A Keyboard

B Hard-disk

C RAM

D Camera

only Memory is the other component of computer ——— CPU.

#Q.   Which of the following is/are true?
1.   Data format used in IO devices may differ from CPUs format
2.   IO devices are slower than CPU
3.   IO devices are slower than main memory

A   Only 1

B   Only 1 & 2

C   Only 1 & 3

D   All 1, 2 & 3

#Q. Which of the following is true regarding IO mapped IO as compared to memory mapped IO?

1. ALU operation cannot be performed on IO data directly
2. IO devices have their own address space
3. Less number of Instructions to access IO
4. Less number of IO devices connected

Own address

Less no. of

A Only 2 & 3

B Only 2 & 4

C Only 2, 3 & 4

D All 1, 2, 3 & 4

#Q.   Which of the following is true regarding memory mapped IO as compared to IO mapped IO?

1.   ALU operation cannot be performed on IO data directly

2.   IO devices do not have their own address space

3.   Some memory wastage

4.   More number of IO devices connected

✗ ALU operations Can
be performed I o
directly.

A   Only 2 & 3

B   Only 2 & 4

C   Only 2, 3 & 4

D   All 1, 2, 3 & 4

#Q. Consider a device operating on 8MBPS speed and transferring the data to memory using cycle stealing mode of DMA. If it takes 250 nanoseconds to transfer 16 bytes data to memory when it is ready/prepared. Then percentage of time CPU is blocked due to DMA is ____ % (rounded upto 1 decimal place)?

8mb data - pt in Io = 1s

1 by data pt in Io = 1/8 m = 0.125 ms = 125 ns

16 byte data pt in Io = 16 × 125 = 2000 ns

% of time CPU = (250/2000) × 100 = 12.5%

#Q. Consider a device operating on cycle stealing mode of DMA and transfer the data to memory in 20nanoseconds when 8 bytes data is ready or prepared. If the DMA blocks 0.1 fraction of CPU time for this transfer, then the transfer rate of the device is _____ megabytes per second?

fraction of time CPU is blocked due to DMA

$$0.1 = 20/PT$$

$$PT = 200\,nS$$

In 200 nanosecond device can prepare date = 8 bytes

In 1 nano secon ——— $8 bytes/200.$

$$= 8000 \; bytes / 200$$

$$= 40 \, M \, by$$

Interrupt service time = 1.2 − 0.4 = 0.8 ns

#Q. Consider a CPU which takes 0.4 nanoseconds as interrupt overhead time when a device generates interrupt for CPU, and CPU accepts it. After that CPU takes 4 cycles to service the interrupt. The total time CPU spends for interrupt service is 1.2 nanoseconds. If the same CPU has average CPI of 4 then in the MIPS count of the CPU is _____?

$0.8 \text{ ns} = 4 \times \text{cycle time}$

$\Rightarrow \text{Cycle time} = \dfrac{0.8}{4} = 0.2 \text{ ns}$

$\text{Clock rate} = \dfrac{1}{0.2} = 5 \text{ GHz}$

$\text{MIPS count} = \dfrac{\text{clock rate}}{CPI}$

$= \dfrac{5 \text{ GHz}}{4 \times 10^6} = \dfrac{5000}{4}$

$= 1250$

#Q. A device with data transfer rate 5 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 2 CPU cycles. The byte transfer time between the device interface register and CPU or memory is negligible. The minimum performance gain of operating the device under interrupt mode over operating it under program-controlled mode is 20. The CPU has average CPI of 5, then the average instruction execution time in CPU is _____microseconds?

$\rightarrow$ Int IO time = 10 μs

1 Byte, time = $\dfrac{1}{5K}$ = 200 μs

1 cycle time = $\dfrac{10}{2}$ = 5 μs

$PG = \dfrac{Pro.\ IO\ time}{Int\ IO\ time}$

Avg inst exe time = CPI × cycle time

= 5 × 5 μs

$\rightarrow$ 20 = $\dfrac{200\ \mu s}{Int\ IO\ time}$

= 25 μs

THANK - YOU