GATE

Computer Science & Information Technology

Computer Organization & Architecture

Basics of COA

DPP: 1

Q1 In a microprocessor, the register which holds address of the next instruction to be fetched?
(A) Accumulator
(B) Program Counter
(C) Stack Pointer
(D) Instruction Register

Q2 The following register holds the instruction before it goes for decode?
(A) Data Register
(B) Accumulator
(C) Address Register
(D) Instruction Register

Q3 Which of the following 2 registers are used to access the memory?
(A) Instruction Register and Program counter
(B) Address Register and Program counter
(C) Program counter and Stack Pointer
(D) Address register and data register

Q4 In a CPU which of the following pair of registers should have same capacity of storage?
(A) Instruction Register and Program counter
(B) Address Register and Program counter
(C) Program counter and Stack Pointer
(D) Address register and Data register

Q5 Which is not a CPU architecture?
(A) Single Accumulator architecture
(B) General Register architecture
(C) Base Register architecture
(D) Stack architecture

Q6 Which of the following is included in the architecture of computer?
1. Addressing Modes, Design of CPU
2. Instruction Set, Data Format
3. Secondary Memory, Operating System

(A) 1 and 2 (B) 2 and 3
(C) 1 and 3 (D) 1, 2 and 3

Q7 Consider the following statements:
1. A computer will have a multiply instruction
2. Multiply instruction will be implemented by a special multiplication unit

Which of the following is correct?
(A) Both 1 and 2 are not architectural design issues.
(B) Both 1 and 2 are not organizational issues.
(C) 1 is an architectural design issue while 2 is an organizational issue.
(D) 1 is an organizational issue while 2 is an architectural design issue

Q8 A CPU has 24-bits instruction. A program starts at address 600 (in decimal). Which of the following is a legal program counter value?
(A) 700 (B) 800
(C) 900 (D) 950

Q9 Consider a computer which has 2-word instructions. 1 word size is 2 bytes. In main memory an instruction is stored at location 628 (decimal). The decimal value of PC when this instruction will be execution in CPU?
(A) 628 (B) 630
(C) 632 (D) None

Q10 Consider the following program segment. Here R1, R2 and R3 are the general-purpose register. Assume that the content of memory location 3000 is 50 and location 2000 is 25. Content of

register R2 is 12. All numbers are in decimal. After the execution of this program the value of memory location 2000 is?

Instructions	Operations
MOV R1, #15	R1 ← #15
MOV (2000), R1	M[2000] ← R1
ADD R2, (2000)	R2 ← R2 + M[2000]
MOV(3000), R2	M[3000] ← R2
MOV R3, R1	R3 ← R1
ADD R3, (3000)	R3 ← R3 + M[3000]
MOV (2000), R3	M[2000]← R3
HALT	Stop

Q11 Consider the following program segment. Here R1 and R2 are the general-purpose register. Assume that the content of memory location 3000 is 27 and location 2000 is 13. Content of register R2 is 10. All numbers are in decimal. After the execution of this program the value of R2 is?

	Instructions	Operations
	MOV R1, #7	R1 ← #7
X:	DEC R1	R1 ← R1 – 1
	JNZ Y	Jump to Y on Non-Zero
	ADD R2, (3000)	R2← R2 + M[3000]
	JMP Z	Jump to Z
Y:	ADD R2, (2000)	R2 ← R2 + M[2000]
	JMP X	Jump to X
Z:	HALT	Stop

Q12 Consider a computer system with word addressable memory. The word size is 4 bytes. The system has a memory capacity of 256GBytes. The address bus width of the computer system must be atleast _____ bits?

Q13 Consider a digital computer with 29 bits wide address bus. The computer supports word addressable memory with each word size of 32 bits. The maximum capacity of memory the computer can support is _____ GBytes?

Q14 Consider a system with 512Mbytes of memory capacity. The memory has 28 lines address bus. The word addressable memory can have maximum word size _____ bits?

GATE

Answer Key

Q1	(B)	Q8	(C)
Q2	(D)	Q9	(C)
Q3	(D)	Q10	42~42
Q4	(B, C)	Q11	115~115
Q5	(C)	Q12	36~36
Q6	(A)	Q13	2~2
Q7	(C)	Q14	16~16

Hints & Solutions

Q1 **Text Solution:**
The program counter, also known as the instruction pointer or simply PC, is a fundamental component of a computer's central processing unit (CPU). It is a special register that keeps track of the memory address of the next instruction to be executed in a program.

Q2 **Text Solution:**
When the CPU fetches an instruction from memory, it is temporarily stored in the IR.

Q3 **Text Solution:**
Address register is used to send address to memory, on which the memory is accessed. And data register is to send data to memory (for memory write) and to receive data from memory (for memory read).

Q4 **Text Solution:**
Address register, program counter and stack pointers store memory addresses. Hence their sizes must be same, to store addresses. Data register size may be different than these registers, as it stores data. And same for instruction register, as it stores instruction word.

Q5 **Text Solution:**
Base register architecture is not a type of architecture. Other 3 are types of architecture of CPU based on how ALU takes input operands.

Q6 **Text Solution:**
In CPU architecture following are specified:
1. Detailed CPU design
2. Instruction set
3. Addressing modes supported
4. Data format to be processed

Q7 **Text Solution:**
Which instruction is supported by a CPU, this decision is made during architecture design of Computer. But how an instruction is implemented for execution, this decision is made during organization.

Q8 **Text Solution:**
Instruction size = 24 bits = 3 bytes, which means each instruction is stored on 3 locations in memory, Given in question that first instruction is stored in memory from address 600, then it will be completed stored on 600, 601 and 602 addresses. So next instruction starts from 603 and next after that starts from address 606 and so one.
Program counter (PC) stores starting address of instruction hence it possible stores 600 then 603 then 606 for sequential program execution. Hence any address PC will store will be multiple of 3, which suggests valid PC value is 900 from given options.

Q9 **Text Solution:**
Instruction size = 2 words = 2*2 bytes. Which means each instruction is stored on 4 locations in memory.
When instruction from address 628 is fetched then PC increments by size of instruction (which is 4). Hence when the instruction is in execution then PC value will be 628+4 = 632

Q10 **Text Solution:**
Given R2 = 12,
memory location 3000 is 50

Operation	Register or memory values
R1 ← #15	R1=15
M[2000] ← R1	Memory location 2000 stores value 15
R2 ← R2 + M[2000]	R2 = 12 + 15 = 27
M[3000] ← R2	Memory location 3000 stores value 27
R3 ← R1	R3=15
R3 ← R3 + M[3000]	R3=15+27 = 42

M[2000]← R3	Memory location 2000 stores value 42
Stop	

Memory location 2000 has value 42 after execution.

Q11 **Text Solution:**

Value at memory location 2000 = 13

Value at memory location 3000 = 27

R2 = 10

R1 is decremented before jump condition hence the jump to Y and then X (this loop) are repeated exactly 6 times, until R1 becomes 0. And every time value of memory location 2000 is added in value of R2.

Hence R2 = R2 + 6 × M[2000] = 10 + 6 × 13 = 88

After that when JNZ Y condition is false then Value of memory location 3000 is added in R2.

Hence

R2 = 88 + 27 = 115

Q12 **Text Solution:**

Number of cells in memory = 256GBytes / 4 bytes = 64 G = 2^{36}

Hence number of bits in memory address = 36 bits

Q13 **Text Solution:**

Number of cells in memory = 2^{29}

Memory capacity = 2^{29} * 32 bits

= 2^{29} * 4 bytes {as answer is asked in bytes}

= 2^{31} bytes

= 2Gbytes

Q14 **Text Solution:**

Number of cells in memory = 2^{28}

Word size = 512Mbytes / 2^{28}

= 2^{29} bytes / 2^{28}

= 2 bytes

= 16 bits