CS & IT ENGINEERING

Computer Organization Architecture

Cache Organization

DPP- 01

Discussion Notes

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[MCQ]

#Q. The memory cycle time of a memory is 500nsec. The maximum rate with which the memory can be accessed?

Note: Consider memory as byte addressable.

A 500 Bytes / Sec

B 2000 Bytes / Sec

C 2 Mbytes / Sec

D 2 GBytes / Sec

in 500 nsec, data transferred = 1 B

1 ns, —— " —— = $\frac{1B}{500\,ns}$

1 sec, —— " —— = $\frac{1\,B}{500 * 10^{-9}\,sec}$

$= \frac{10^9\,B}{500\,sec}$

$= \frac{1000}{500} * 10^6\,B/sec$

$= 2\,MB/sec$

[NAT]

#Q. The address bus width of a memory of size 4096×8 bits is ___ bits?

no. of cells = 4096 = 2^{12}

add. size = $(\log_2 2^{12})$ bits

= 12 bits Ans.

[NAT]

#Q. Consider a byte addressable memory which has 0.2 GBPS writing rate. The memory access time is __ nanoseconds?

0.2 GB, access time = 1 sec

1 B, —||— $= \frac{1\,sec * 1B}{0.2\,GB}$

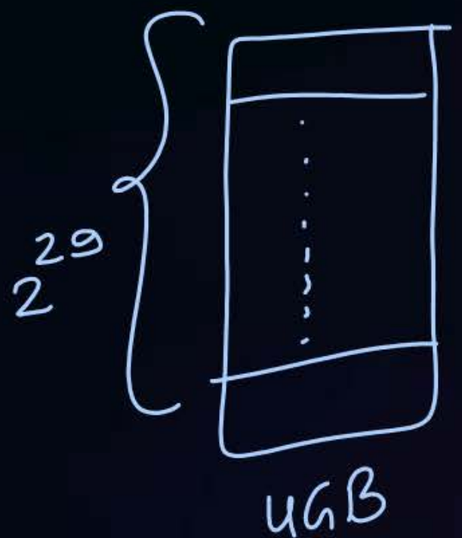
$= 5\,nsec$ Ans

[NAT]

Ans = 8B

#Q. Consider a word addressable memory of total capacity of 4GB. The memory is accessed using a minimum of 29 bits address bus. The word size per address in this memory is ___ bytes?

no. of cells $= 2^{29}$



$$\text{no. of cells} = \frac{4GB}{1 \text{ word size}}$$

$$1 \text{ word size} = \frac{4GB}{2^{29}} = \frac{2^2 \cdot 2^{30}}{2^{29}} B$$

$$= 2^3 B = 8B$$

[MCQ]

#Q. Consider a memory with maximum size of X bytes. Memory is word addressable with word size of W bytes. The size of the address bus of the processor is at least ____ bits?

A $Log_2(X/W)$

B $2^{(X/W)}$

C X/W

D $Log_2(X)$

$$\text{no. of cells in mem.} = \frac{\text{Mem. Size}}{\text{word size}}$$

$$= \frac{X \text{ bytes}}{W \text{ bytes}}$$

$$= \frac{X}{W}$$

$$\text{add. size} = \log_2\left(\frac{X}{W}\right) \text{ bits} = \left(\log_2 X - \log_2 W\right) \text{ bits}$$

[MCQ]

no. of cells

#Q. A DRAM chip of 64M × 16 bits has 128K rows of cells with y cells in each row. If DRAM takes x-ns for 1 refresh then total refresh time of the DRAM is ____ microseconds, if $x = 2 \times \log_2 y$?

no. of rows of cells * 18 nsec

= 128 k * 18 nsec

= 128 * 18 usec

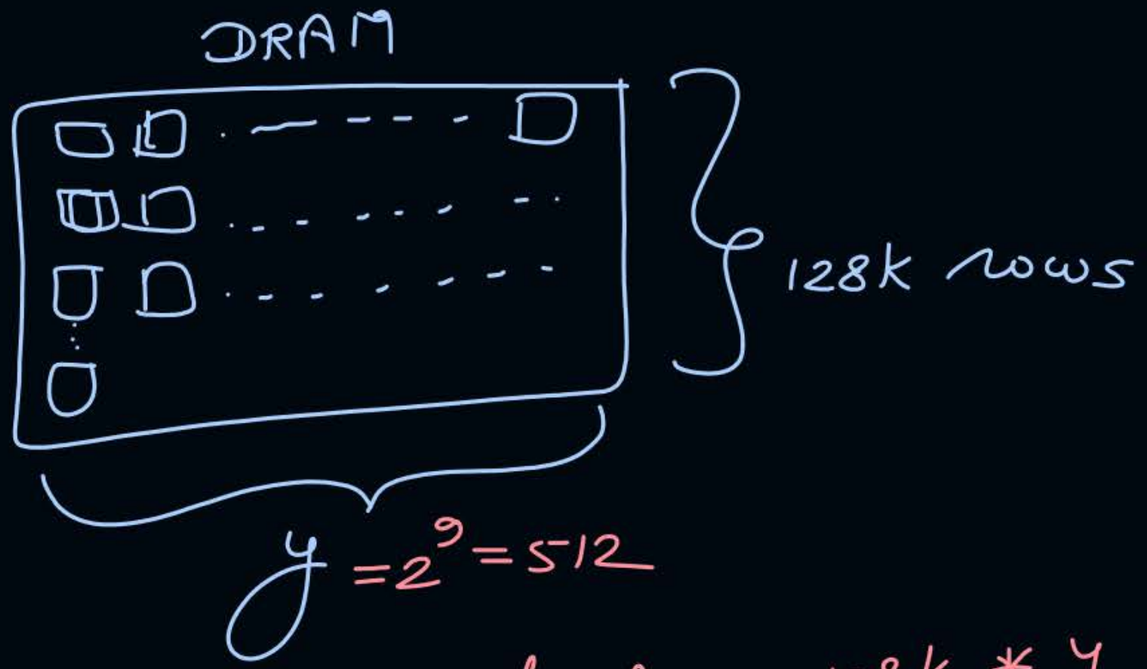
= 2304 usec

A 1200

B 2304

C 3202

D 5444



$$x = 2 * \log_2 y$$

$$= 2 * \log_2 2^9$$

$$= 18$$

no. of cells = $128k * y$

$$64M = 128k * y$$

$$y = \frac{64M}{128k} = \frac{2^6 * 2^{20}}{2^7 * 2^{10}} = \frac{2^{26}}{2^{17}} = 2^9$$

[NAT]

Ans = 324

#Q. A 32-bits (4B) wide main memory unit with a capacity of 16GB is built using 128M×8-bits RAM chips. If there are x-horizontal arrangements of chips are there, with y number of chips in each horizontal arrangement then the value of 10x + y is?

no. of addresses in expected mem. = $\frac{16GB}{4B} = 4G = 2^{32}$

expected mem = 4G × 4B = 4G × 32 bits

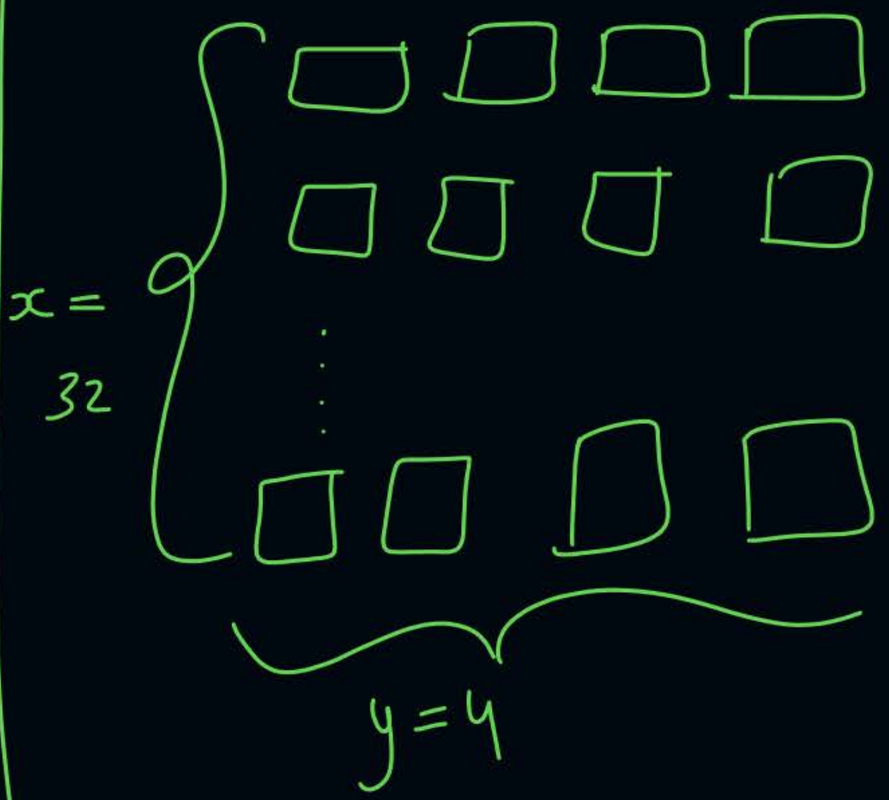
$$\text{no. of chips} = \frac{4G \times 32 \text{ bits}}{128M \times 8 \text{ bits}}$$

$$= \frac{2^{5} \times 4}{2^{27}} \text{ bits}$$

$$= 32 * 4$$

$$= 128 \text{ chips}$$

arrangement of chips



$10x + y = 10 * 32 + 4$

$= 324$

[NAT]

#Q. A cache is used to reduce the effective memory access time of 200ns without cache to 65ns with cache. If cache access time is 50ns, then cache hit rate is _____%?

$t_{mm} = 200\,ns$

$t_{avg} = 65\,ns$

$t_{cm} = 50\,ns$

$65 = H * 50 + (1-H)\,200$

$H = \underline{\underline{90\%}}$ Ans.

[NAT]

#Q. A computer system has a cache with cache access time Tc = 10ns, hit ratio of 80% and average memory access time of Tm = 20ns. The access time for physical memory Tp is _____ ns?

↳ main

$T_{cm} = 10$ ns

$H = 80\%$

$T_{avg} = 20$ ns

$T_{mm} = ?$

$20 = 0.8 * 10 + 0.2 * t_{mm}$

$t_{mm} = \frac{12}{0.2}$ ns

$= 60$ ns Ans.

[NAT]

#Q. A cache line (block) has 128 bytes. The main memory has addressing latency 64ns and access bandwidth 1GB/s. The time required to fetch the entire cache line from the main memory is _____ ns?

= 1 Latency + 128 bytes read time

64 ns + 128 ns = 192 ns Ans.

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for 1GB, time = 1 sec

1 B, —11— = $\frac{1\text{sec}}{1G}$ = 1ns

128 B, —11— = 128 * 1ns = 128ns

[NAT]

Ans = 53%

#Q. Consider a system using a cache. The cache is having 70% hit ratio and is 9 times faster than main memory. The average memory access time then increased due to some program execution and the new average access time becomes 40% more than older one of 340ns. The hit ratio of new cache design is ___%?

$t_{cm} = \frac{t_{mm}}{9} \Rightarrow t_{mm} = 9 * t_{cm}$

$H = 0.7$

$t_{avg} = 340\,ns$

new

$t_{avg} = 340 + 340 * 40\% = 340 + \frac{340 * 40}{100}$

$= 1.4 * 340 = 476\,ns$

$H = ?$

Old execution :-

$$340 = 0.7 * t_{cm} + 0.3 * 9\, t_{cm}$$

$$340 = 3.4\, t_{cm}$$

$$t_{cm} = 100 \text{ ns}$$

$$t_{mm} = 9 * 100 = 900 \text{ ns}$$

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new execution :-

$$476 = H * 100 + (1-H)\, 900$$

$$476 = 100H + 900 - 900H$$

$$800H = 424$$

$$H = \frac{424}{800} = 0.53 = 53\%$$

[NAT]

#Q. Consider a memory hierarchy which takes 500 nanoseconds for access when there is a miss in cache and takes 100 nanoseconds for access when there is a hit in cache. Assume if among all memory references 90% of the references are having a hit on cache then average memory access time is _____ nanoseconds?

$= 0.9 * 100 + 0.1 * 500$

$= 90 + 50$

$= 140$ ns Ans.

[MCQ]

#Q. A system has a write through cache with access time of 100ns and hit ratio of 90%. The main memory access time is 1000ns. 70% of memory references are for read operations. Average memory access time for read-write operations both and effective hit rate(in %) are?

A 433, 90%

B 433, 63%

C 190, 90%

D 190, 63%

$T_{avg\ read} = 0.9 * 100 + 0.1 * 1000 = 190\ ns$

$T_{avg\ write} = 1000\ ns$

$T_{avg} = 0.7 * 190 + 0.3 * 1000$

$= 433\ nsec$

Effective hit rate $= 0.7 * 0.9 = 0.63 = 63\%$

[NAT]

#Q. Consider a write through cache which can provide only 63.75% of effective hit rate. If among all memory references 75% references are for read, then the hit ratio of cache for only read operations 85 %?

$$0.6375 = 0.75 * H$$

$$H = \frac{0.6375}{0.75} = 0.85 = 85\% \quad \text{Ans.}$$

[NAT]

#Q. Consider a write through cache which can provide only 61.92% effective hit rate. If among all memory references 28% references are for write, then the hit ratio of cache for only read operations is ____?%

$0.6192 = 0.72 * H$

$H = 0.86 = 86\%$

THANK - YOU