CS & IT ENGINEERING

Operating System

Memory Management

Lecture -4

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Recap of Previous Lecture

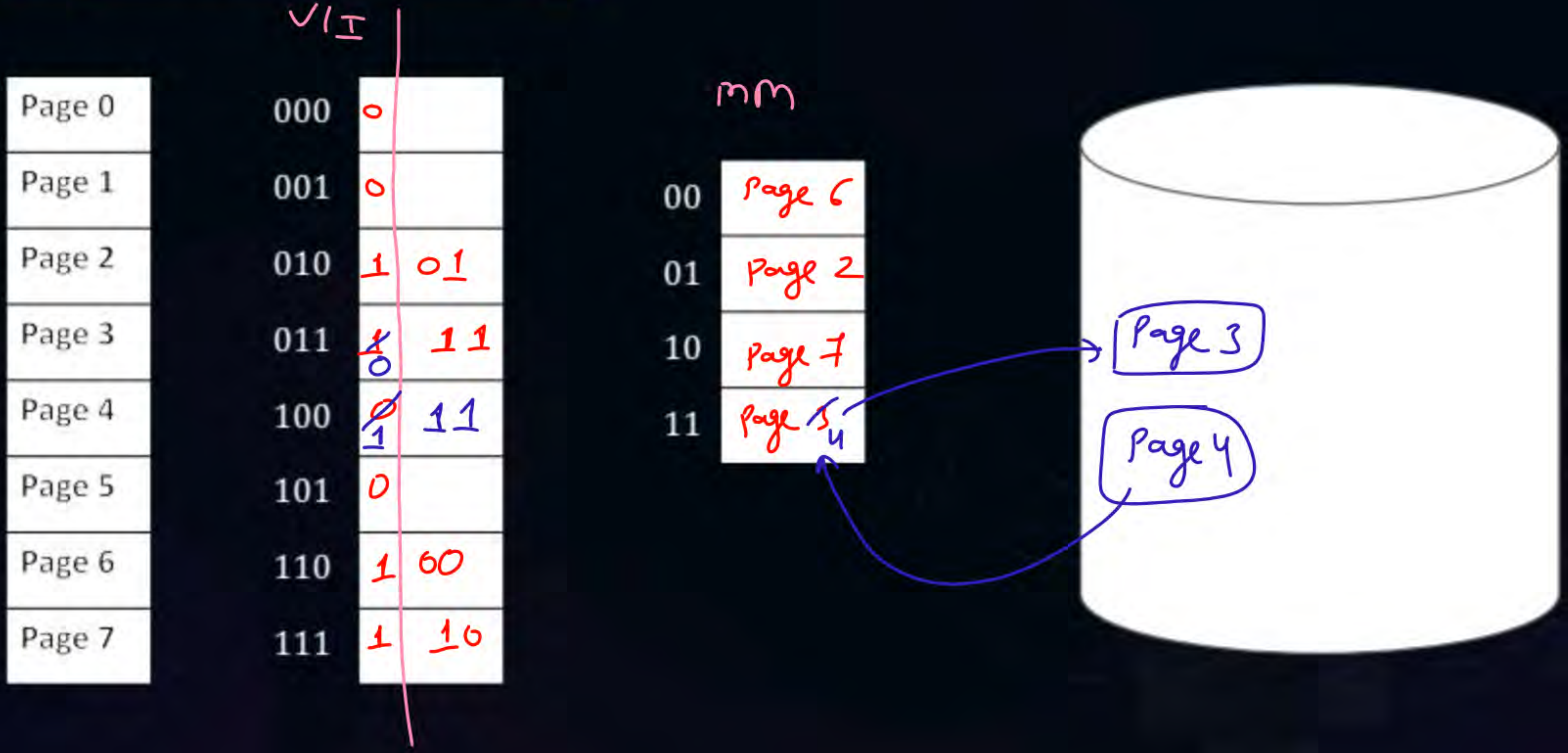
Topic TLB Mapping

Topic Segmentation

Topics to be Covered

- **Topic** Virtual Memory
- **Topic** Effective Memory Access Time

Topic : Virtual Memory

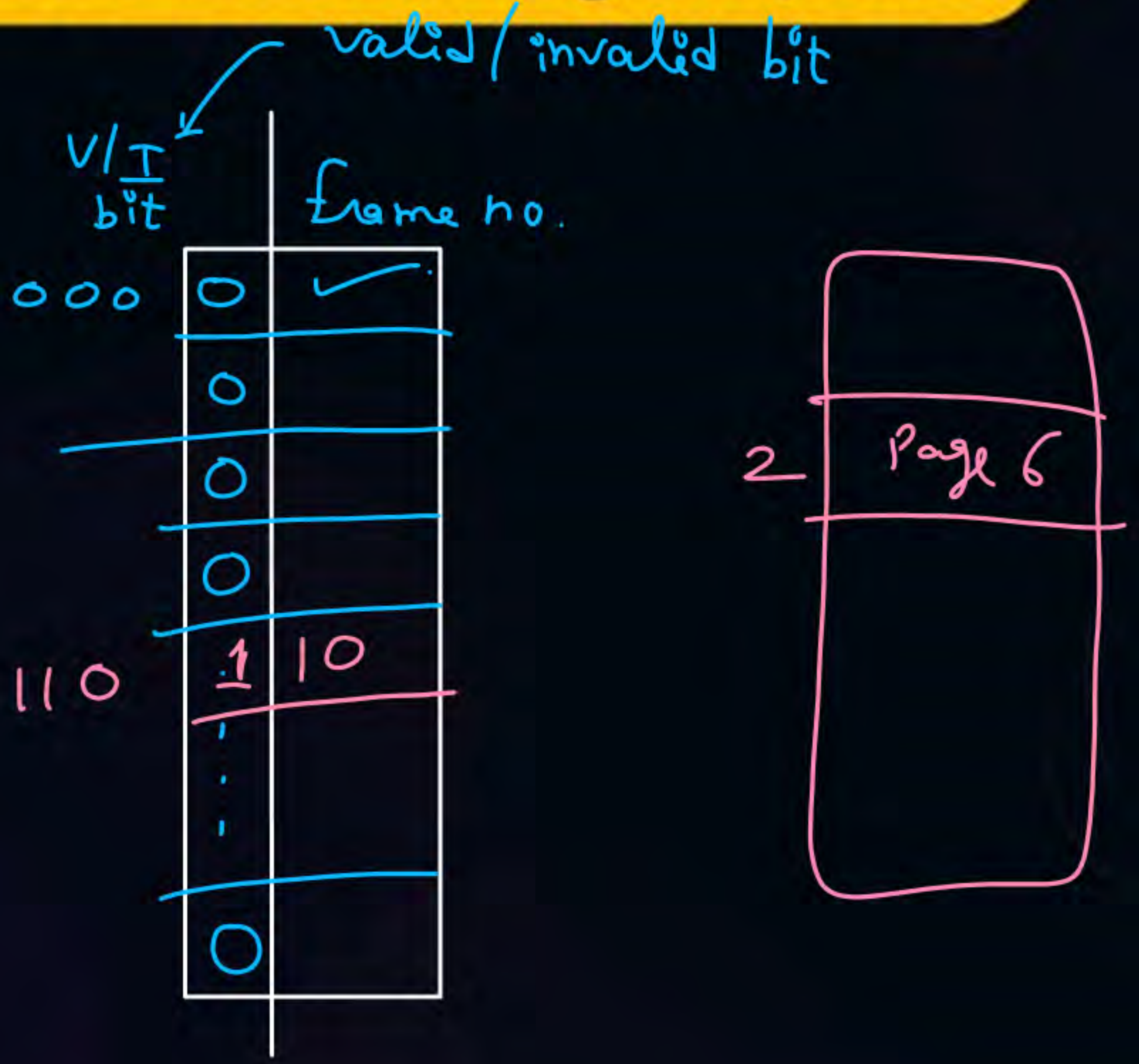


		V/I	
Page 0	000	0	
Page 1	001	0	
Page 2	010	1	01
Page 3	011	~~1~~ 0	11
Page 4	100	~~0~~ 1	11
Page 5	101	0	
Page 6	110	1	00
Page 7	111	1	10

MM

00	Page 6
01	Page 2
10	Page 7
11	Page ~~3~~ 4

Topic : How to Check Page Hit/Fault



Topic : Saving Page Swap Time

dirty bit used / modified bit

- 0 page directly replaced
- 1 page must be saved to disk before replacement

P.T.

f	V/I	d	R/W

R/W → Page access has read only or write also for process

Topic : Effective Memory Access Time

assume page fault rate is $\Rightarrow p$

page hit rate $= (1-p)$

E.M.A.T. without TLB $= (1-p) *$ mem. access time when page hit $+ \; p *$ mem. access time when page fault

GATE- 2018

#Q. Consider a process executing on an operating system that uses demand paging. The average time for a memory access in the system is M units if the corresponding memory page is available in memory, and D units if the memory access causes a page fault. It has been experimentally measured that the average time taken for a memory access in the process is X units.

Which one of the following is the correct expression for the page fault rate experienced by the process.

A (D – M)/ (X – M)

B [✓ (X – M) / (D – M)]

C (D – X) / (D – M)

D (X – M)/(D – X)

$$X = p * D + (1-p) m$$

$$X = pD + m - pM$$

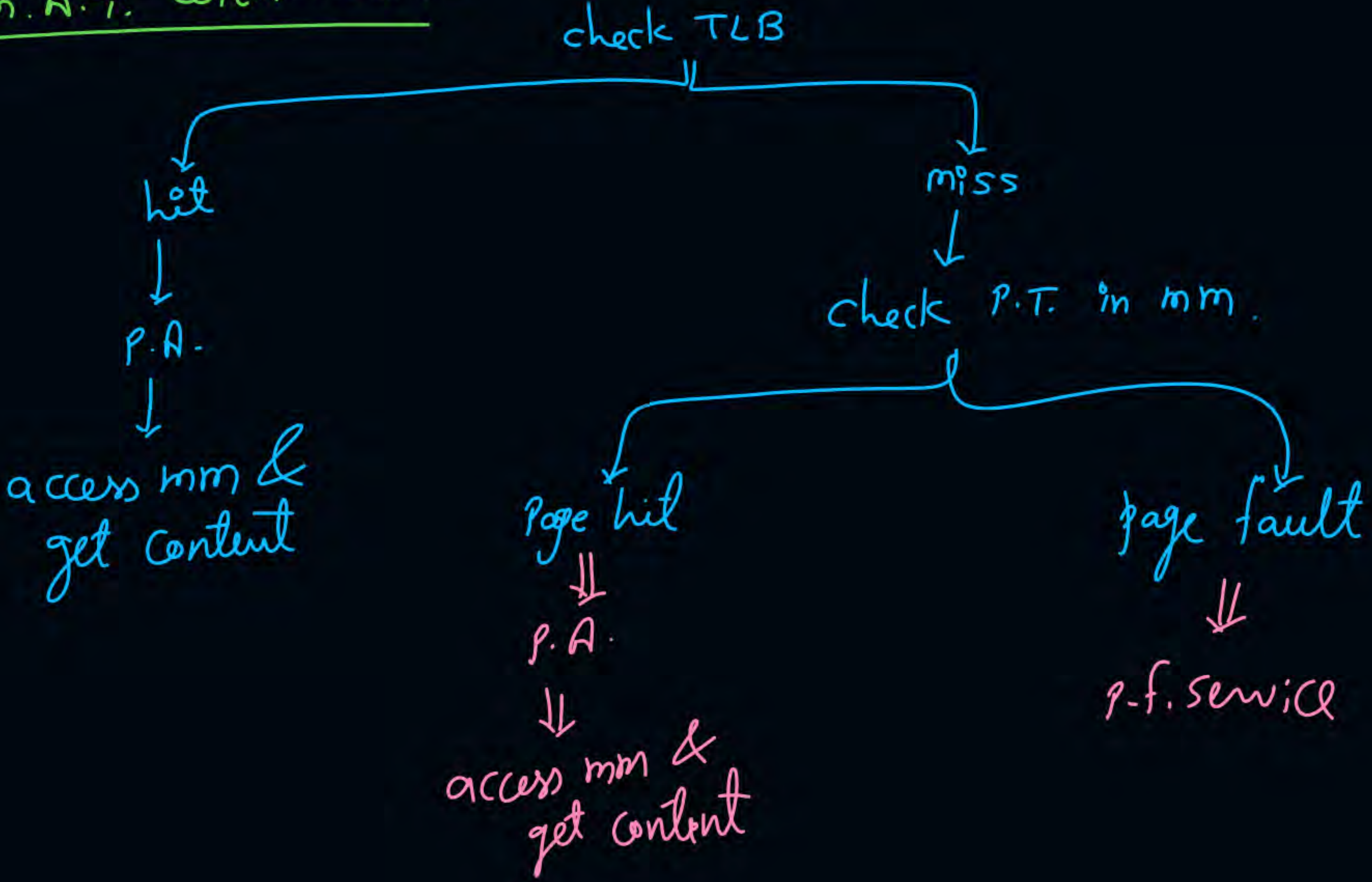
$$X - m = p(D-m)$$

$$p = \frac{X-m}{D-m}$$

E.M.A.T. w/o TLB and with page fault

$$= (1-p) * 2t_{mm} + p * \left[\underbrace{t_{mm}}_{\text{for checking P.T.}} + \underbrace{\text{page fault service time}}_{\text{To bring faulted page from disk to mem \& P.T. update}}\right]$$

E.M.A.T. with TLB :-



check TLB

hit

P.A.

access mm & get content

miss

check P.T. in mm.

Page hit

P.A.

access mm & get content

page fault

p.f. service

E.M.A.T. with TLB :-

$$E.M.A.T. = H * \left[\underset{\text{for checking TLB \& getting P.A.}}{t_{TLB}} + \underset{\text{for content}}{\underline{t_{mm}}} \right] + (1-H) \left[\overset{\text{checking TLB \& getting miss}}{t_{TLB}} + \overset{\text{for checking P.T.}}{t_{mm}} + (1-p) * \overset{\text{for content}}{t_{mm}} + \underline{p} * p.f.s.T. \right]$$

Topic : Question

TLB hit = 90%

TLB access time = 10 n sec

mm access time = 200 n sec

Page fault rate = 1 %

p.f. service time = 10000 nsec

E. M. A. T. = 239.8 n sec.

$$EMAT = 0.9 * (10 + 200)$$

$$+ 0.1 (10 + 200 + 0.99 * 200 + 0.01 * 100000)$$

$$= 239.8$$

Topic : Dirty Bit Included (Without TLB)

$$= t_{mm} + (1-p)t_{mm} + p * \left[m * \underset{\text{for dirty page}}{p.f.s.T.} + (1-m) * \underset{\text{for non-dirty page}}{p.f.s.T.} \right]$$

Topic : Question

P = 2%

M = 5%

T_{mm} = 100 n sec

P. F .S.T. when page dirty = 20 μ sec

P. F .S.T. when not dirty = 10 μ sec

E. M. A. T. = ___408___ n sec.

$$= 100 + 0.98 * 100 + 0.02 \left[0.05 * 20000 + 0.95 * 10000 \right]$$

$$= 408 \text{ ns}$$

Topic : Dirty Bit with TLB

$$\begin{aligned} &= H * \left(t_{TLB} + t_{mm}\right) \\ &\quad + (1-H)\left[t_{TLB} + t_{mm} + (1-p)\,t_{mm} + p\left(m * \underset{\substack{\text{for}\\ \text{dirty}\\ \text{page}}}{\text{p.f.s.T.}} + (1-m) * \underset{\substack{\text{for}\\ \text{non-dirty}\\ \text{page}}}{\text{p.f.s.T.}}\right)\right]\end{aligned}$$

m = fraction of page which are replaced and modified

Topic : Question

$H = 85\%$

$t_{TLB} = 20$ n sec

$t_{mm} = 200$ n sec

$P = 1\%$

$M = 2\%$

P.F.S.T. with dirty page = 50 μ sec $= 50000 ns$

P.F.S.T. without dirty page = 20 μ sec $= 20000 ns$

E. M. A. T. = $\underline{280.6 ns}$?

$$= 0.85 * (20+200)$$

$$+ 0.15 \left[20+200 + 0.99 * 200 + 0.01 \left(0.98 * 20000 + 0.02 * 50000 \right) \right]$$

$$= 280.6 ns$$

P.f.S.T. for dirty page = Time to write back replaced page from mm to disk + time to bring faulted page from disk to mm + P.T. updation time in mm

P.f.S.T. for non-dirty page = time to bring faulted page from disk to mm + P.T. updation time in mm

Topic : Question

TLB Hit = 90%

t_{TLB} = 15 n sec

T_{mm} = 120 n sec

P = 2%

M = 10%

Time taken to transfer a page b/w mm & sm = 10000 n sec

E.M.A.T. = ___169___?

P.f.S.T. for dirty page = 10000+10000 + 120 = 20120 ns

p.f.s.T. for non-dirty = 10000 + 120 = 10120 ns

$$EMAT = 0.9 * (15+120) + 0.1 \left[15 + 120 + 0.98 * 120 + 0.02 (0.1 * 20120 + 0.9 * 10120) \right]$$

= 169 ns

Topic : Question

H.W.

[GATE-2020]

#Q. Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. Each page transfer to/from the disk takes 5000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. Assume that for 20% of the total page faults, a dirty page has to be written back to disk before the required page is read from disk. TLB update time is negligible. The average memory access time in ns (round off to 1 decimal places) is________.

Topic : Cache with TLB

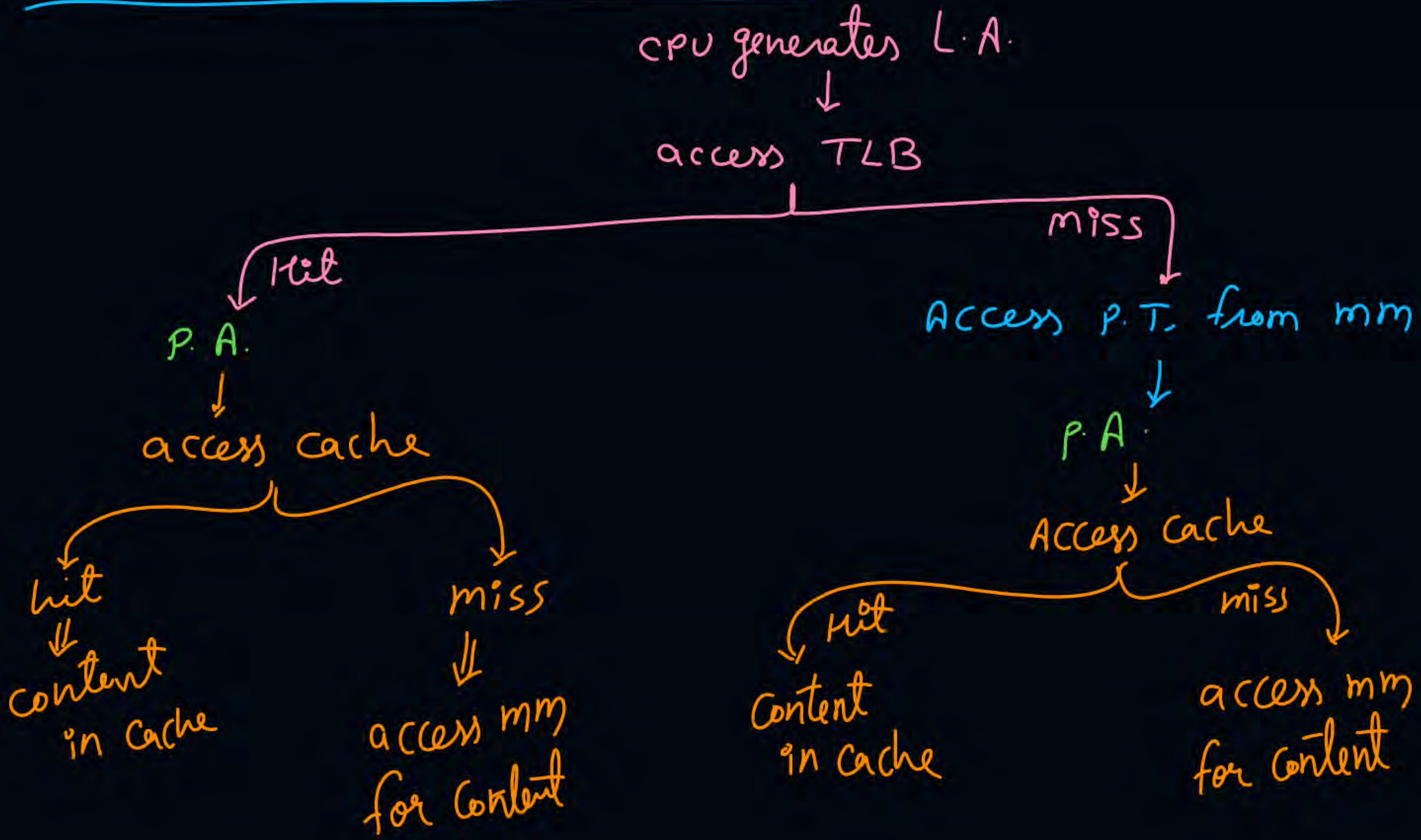
↓

physically addressed cache

H_c = Hit rate of cache

Content access time with physical add. (t_{CA}) $= (H_c * t_{cm}) + (1-H_c)(t_{cm}+t_{mm})$

Cache & TLB w/o p.f. :-



CPU generates L.A.

access TLB

Hit

P.A.

access cache

hit

content in cache

miss

access mm for content

miss

Access P.T. from mm

P.A.

Access cache

Hit

Content in cache

miss

access mm for content

$$E.M.A.T. = H * \left(t_{TLB} + \underset{\substack{\uparrow \\ \text{for content}}}{\underline{t_{cA}}}\right) + (1-H)\left(t_{TLB} + \underset{\substack{\uparrow \\ \text{for} \\ \text{P.T.}}}{\underline{t_{mm}}} + \underset{\substack{\uparrow \\ \text{for content}}}{\underline{t_{cA}}}\right)$$

Ques) $H_c = 80\%$

$t_{cm} = 10 ns$

$t_{mm} = 200 ns$

$t_{TLB} = 5 ns$

$H_{TLB} = 90\%$

E.M.A.T. = $\underline{\ 75\ }$ ns

$t_{cA} = 0.8 * (10) + 0.2 * (10 + 200)$

$= 8 + 42$

$= 50ns$

$EMAT = 0.9 * (5 + 50) + 0.1 (5 + 200 + 50)$

$= 75$ ns

Topic : Question

H. W.

#Q. A processor uses 1–level page table for virtual to physical address translation. Page table is stored in the main memory. Further, the processor has a translation look-aside buffer (TLB), with a hit rate of 96%. The TLB caches recently used virtual page numbers and the corresponding physical page numbers. The processor also has a physically addressed cache with a hit rate of 90%. Main memory access time is 10 ns, cache access time is 2 ns, and TLB access time is also 1 ns.

Assuming that no page faults occur, the average time taken to access a virtual address is approximately?

Topic : Page Replacement Policies

1. First In First Out (FIFO)
2. Optimal Policy
3. Least Recently Used (LRU)
4. Last in First Out (LIFO)
5. Most Recently Used (MRU)
6. Least Frequently Used (LFU)
7. Most Frequently Used (MFU)

} frequency based

Topic : First In First Out (FIFO)

Assume:

- Number of frames = 3 (All empty initially)
- Page reference sequence: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5

no. of page faults = 9

page fault rate = $\frac{9}{12}$

page hit rate = $\frac{3}{12}$

1	2	3	4	1	2	5	1	2	3	4	5
1	1	1	4	4	4	5			5	5	
	2	2	2	1	1	1			3	3	
		3	3	3	2	2			2	4	
✓	✓	✓	✓	✓	✓	✓	✗	✗	✓	✓	✗

Topic : First In First Out (FIFO)

Assume:

- Number of frames = 4 (All empty initially)
- Page reference sequence: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5

✓ ✓ ✓ ✓ ✗ ✗ ✓ ✓ ✓ ✓ ✓ ✓

1	1	1	1	5	5	5	5	4	4
	2	2	2	2	1	1	1	1	5
		3	3	3	3	2	2	2	2
			4	4	4	4	3	3	3

no. of page faults = 10

Topic : Belady's Anomaly

↓

FIFO suffers from it

for some page reference sequences, increasing no. of frames may increase no. of page faults.

Topic : First In First Out (FIFO)

Advantages:

1. Simple and easy to implement.
2. Low overhead. → Time needed to find page to replace

Disadvantages:

1. Poor performance. → high no. of page faults
2. Doesn't consider the frequency of use or last used time, simply replaces the oldest page.
3. Suffers from Belady's Anomaly

2 mins Summary

Topic Virtual Memory

Topic Effective Memory Access Time

Happy Learning

THANK - YOU