

CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE



Memory Organization

Lecture No.- 01

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Recap of Previous Lecture



Topic

DMA

Topic

Cycle Stealing



Topics to be Covered



Topic

Memory Hierarchy

Topic

Memory Presentation

Topic

Memory Address Decoder

Topic

Main Memory



Topic : Memory Hierarchy



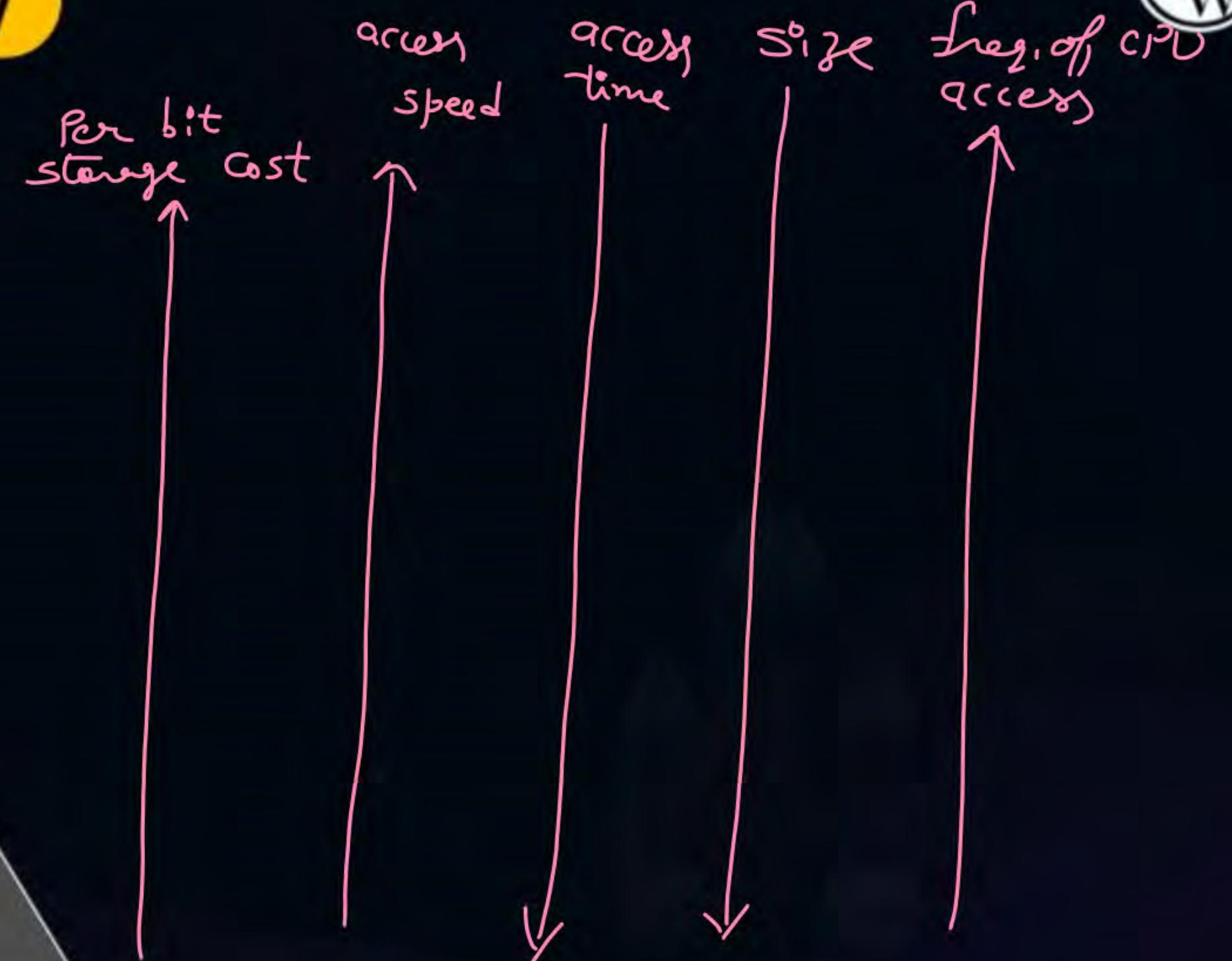
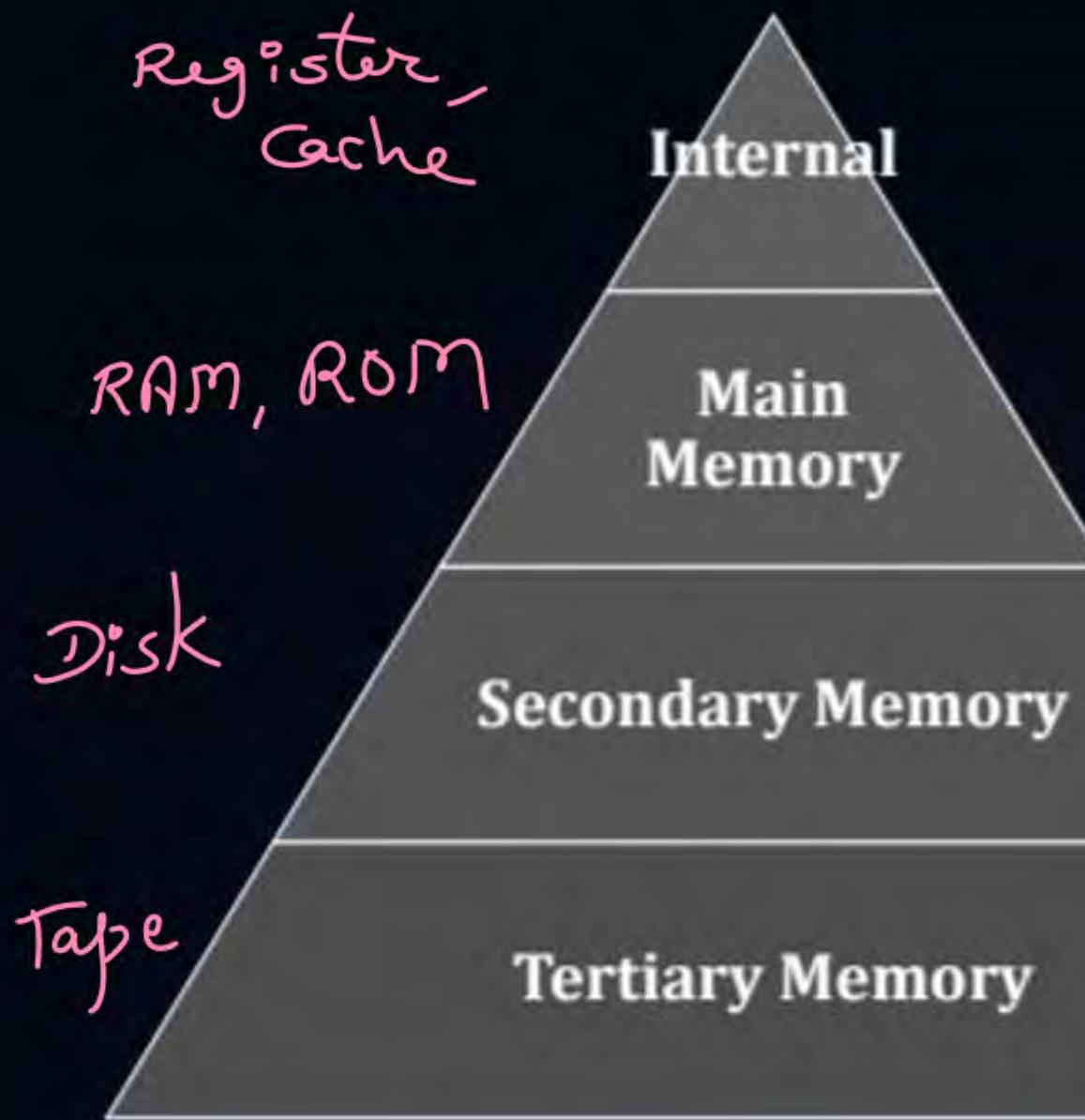
Memory hierarchy used when discussing performance issues.

Goal of Memory Hierarchy:

1. To maximize the Access Speed
2. To minimize the Per Bit Storage Cost



Topic : Memory Hierarchy



memories	size (in bits)	per bit storage cost	Total cost
m_1	s_1	c_1	$s_1 c_1$
m_2	s_2	c_2	$s_2 c_2$
m_3	s_3	c_3	$s_3 c_3$
m_4	s_4	c_4	$s_4 c_4$

mem. hierarchy cost = $s_1 c_1 + s_2 c_2 + s_3 c_3 + s_4 c_4$

Avg per bit storage cost = $\frac{s_1 c_1 + s_2 c_2 + s_3 c_3 + s_4 c_4}{s_1 + s_2 + s_3 + s_4}$

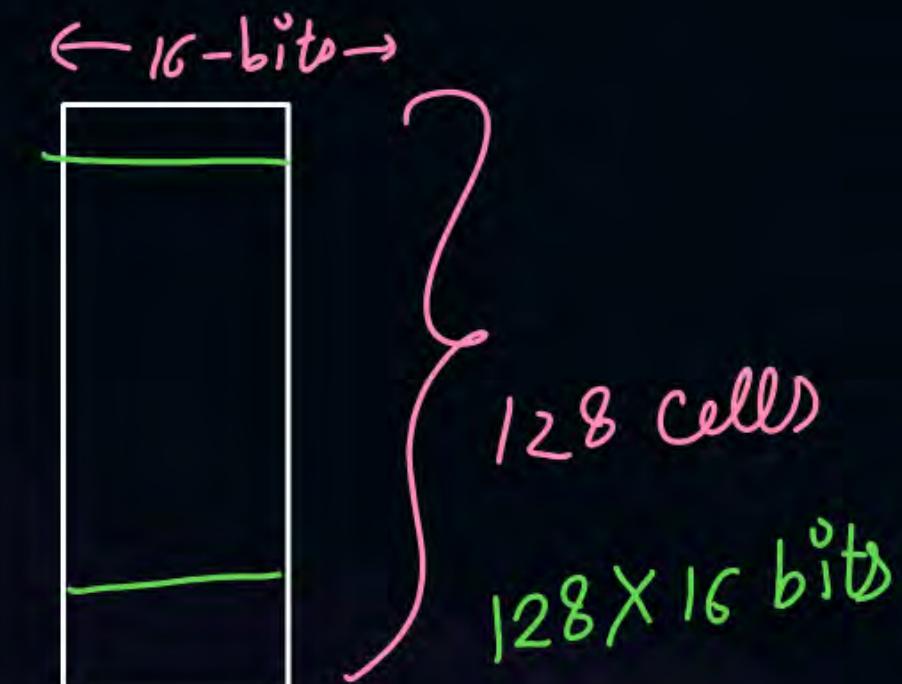
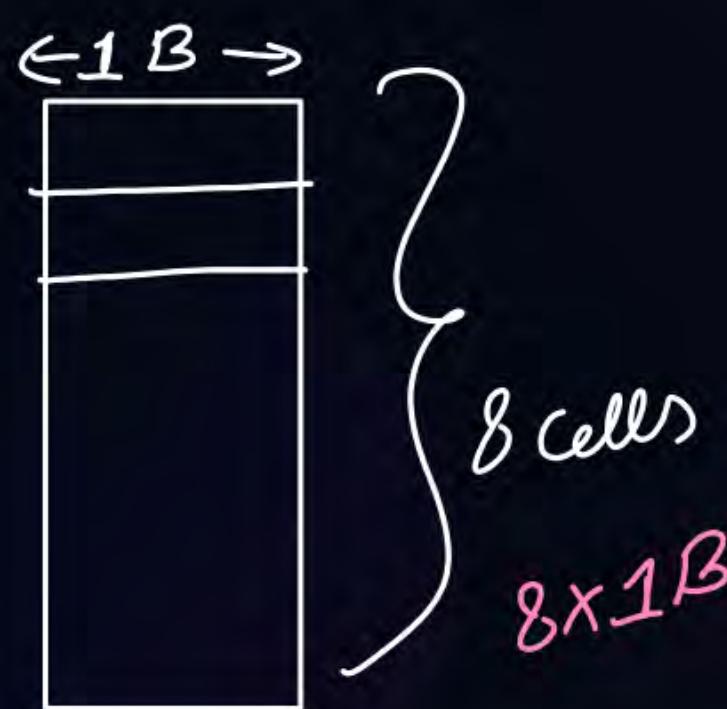


Topic : Memory Presentation

A mem. represented by

$$= \text{no. of cells} \times 1 \text{ cell capacity}$$

$$= \text{No. of mem. locations} \times \text{bits per location}$$





Topic : Memory Presentation



byte add. mem.

$256k \times 1B \Rightarrow 256KB$

Or

$256k \times 8\text{ Bits}$

#Q. Memory is represented as?

- A A \times B where A = No. of memory locations, B = No. of bits in each location
- B $2^a \times B$ where a = No. of address bits, B = No. of bits in each location
- C B \times A where, B = No. of bits in each location, A = No. of memory locations
- D (A) & (B) both

#Q. A memory has 14-bits address bus. Then how many memory locations are there?

- A 16K
- B 16384
- C 2^{14}
- D All

$$2^{14} = 16k = 16384$$

mem. cycle time \Rightarrow time needed to perform
read or write at one add. in mem.

#Q. The memory cycle time of a memory is 200nsec. The maximum rate with which the memory can be accessed?

Note: Consider memory as byte addressable.

- A 500 Bytes / Sec
- B 2000 Bytes / Sec
- C ✓ 5 Mbytes / Sec
- D 5 GBytes / Sec

$$\begin{aligned} \text{in } 200 \text{ ns, data} &= 1B \\ \text{in } 1 \text{ sec data} &= \frac{1B}{200 * 10^{-9} \text{ sec}} \\ &= 5 \text{ MB/sec} \end{aligned}$$

Ques) mem access rate = 10 MBPS

byte addressable

total time needed to read 20 bytes from mem = $\frac{2000}{10 \text{ MBPS}} \text{ ns}$

Solⁿ

for 10MB, read, time = 1sec

$$\begin{aligned} \text{for 20 byte read, time} &= \frac{1\text{sec}}{10\text{MB}} * 20\text{B} \\ &= 2 \text{usec} \\ &= 2000 \text{nsec} \end{aligned}$$

#Q. A processor can support a maximum memory of 4 GB, where the memory is word addressable (a word consists of two bytes). The size of the address bus of the processor is at least 31 bits?

$$\text{no. of cells} = \frac{2^{\text{address}}}{2^{\text{bytes}}} = 2^9 = 2^{31}$$

↓

$$\text{address} = 31 \text{ bits}$$



Topic : Memory Address Decoder



assume \Rightarrow 8 bytes mem.



$\frac{8 \times 8 \text{ bits}}{1}$

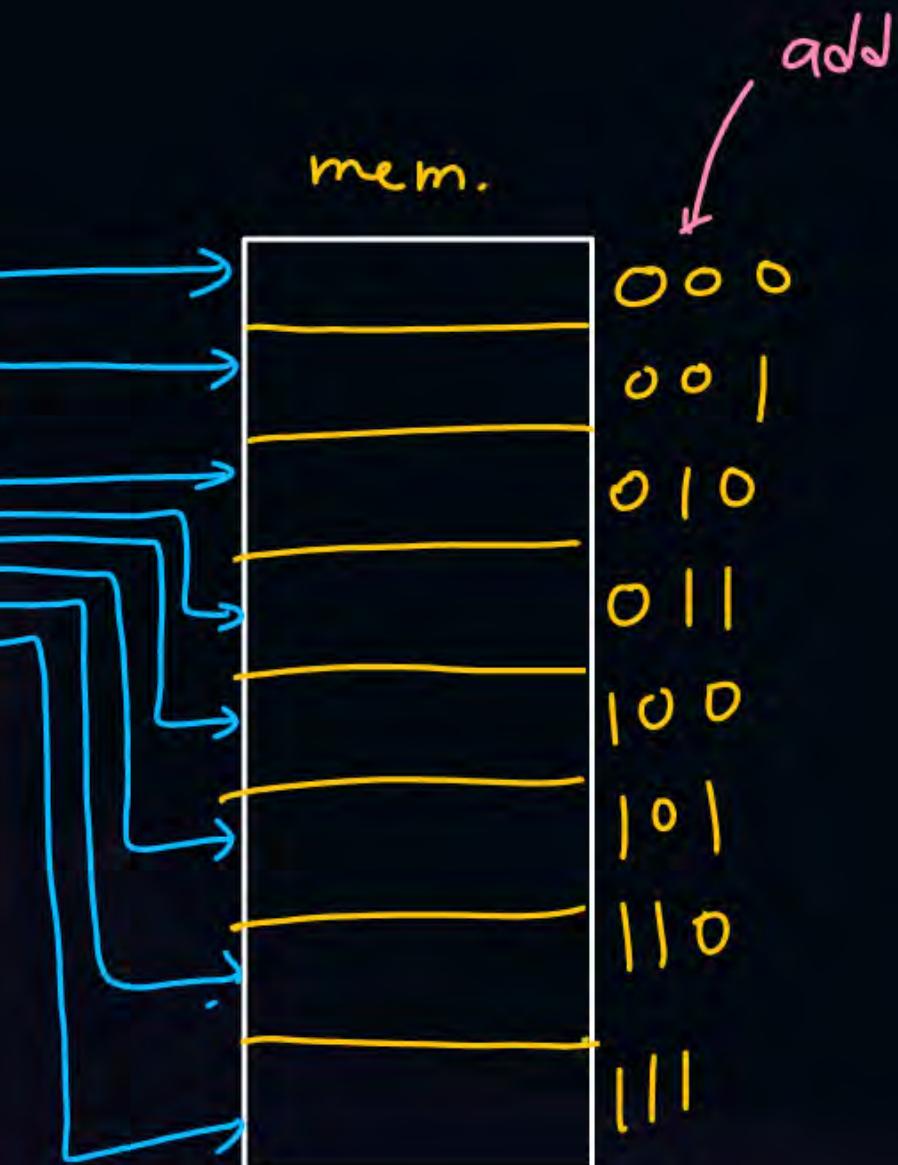
add. = 3 bits

0
0
0
0

3x8
decoder

$512 \times 8 \text{ bits}$

$\hookrightarrow 9 \times 512 \text{ decoder}$



#Q. Consider a memory of size $2K \times 8$ -bits. What is the size of decoder needed to access the cells of the memory uniquely?

$$\text{no. of cells} = 2k = 2^{11}$$

add. = 11 bits

$$\text{decoder size} = 11 \times 2048$$

Ans.

GATE-PYQ

#Q. If there are m input lines n output lines for a decoder that is used to uniquely address a byte addressable $\frac{1}{\downarrow}$ KB RAM, then the minimum value of $m + n$ is 1034?

$1K \times 1B$

$$\begin{aligned} \text{no. of cells} &= 1K = 2^{10} \\ \text{add.} &= 10 \text{ bits} \end{aligned}$$

$$\begin{aligned} \text{decoder size} &= 10 \times 1024 & m &= 10 \\ n &= 1024 \\ m+n &= 1034 \end{aligned}$$



Topic : Main Memory

Used for storing current running programs ('instns') and their data.

Types :-

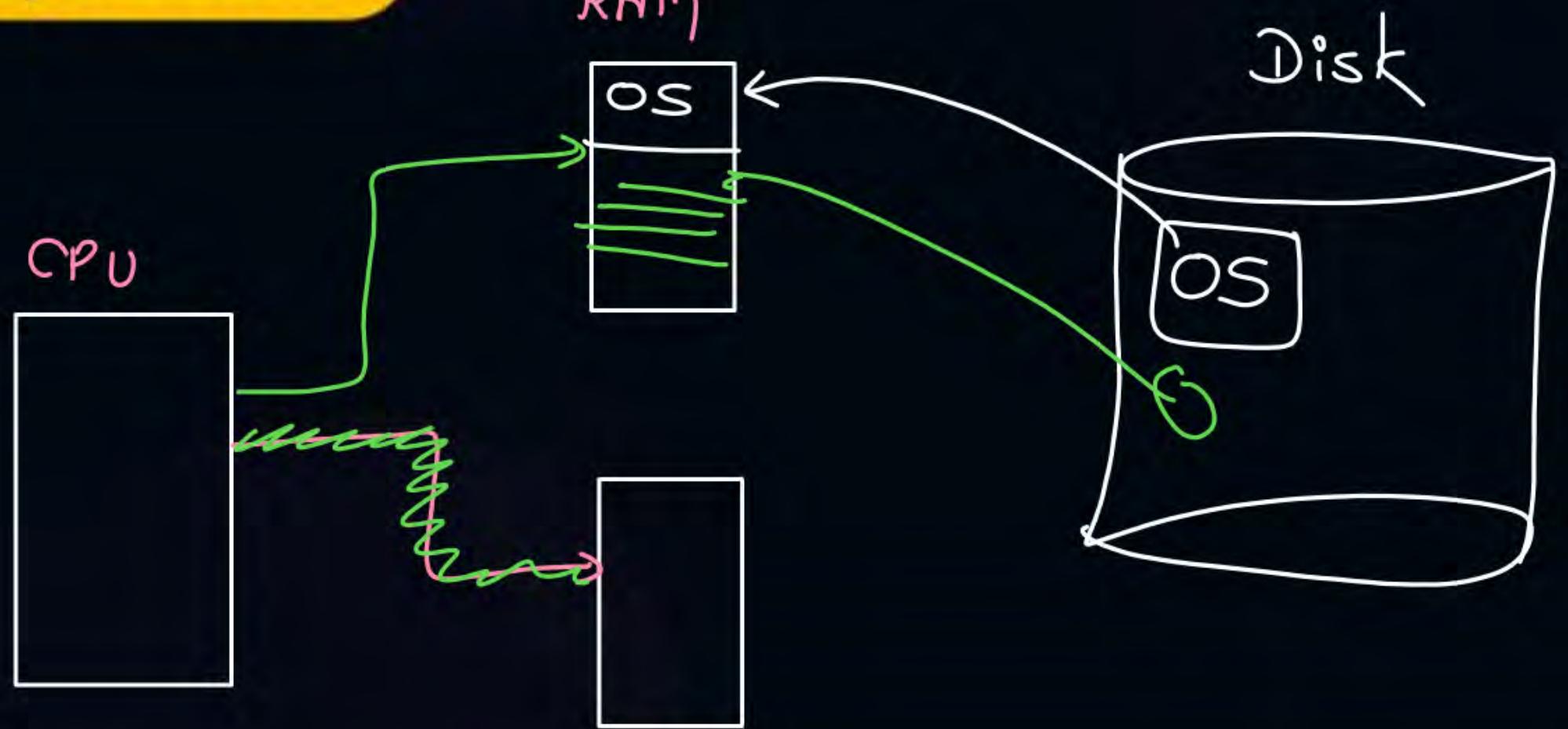
1. RAM \Rightarrow volatile
2. ROM \Rightarrow (Non-volatile)



Topic : ROM

RAM :-
RAM

P
W



1. P.O.S.T. (Power on self Test) ^{ROM}
2. Booting



Topic : Types of RAM



Static (SRAM)	Dynamic (DRAM)
1. Implemented using flip-flops	1. Implemented using capacitors
2. No refresh required	2. Periodic refresh is required
3. Faster Read/Write	3. Slow Read/Write
4. Used for Cache	4. Used for main memory
5. Expensive	5. Less Expensive
6. Low Idle power consumption	6. High Idle power consumption
7. High operational power consumption	7. Low operational power consumption

#Q. Consider 2 4-bits unsigned values A and B. What will be the maximum size of result for:

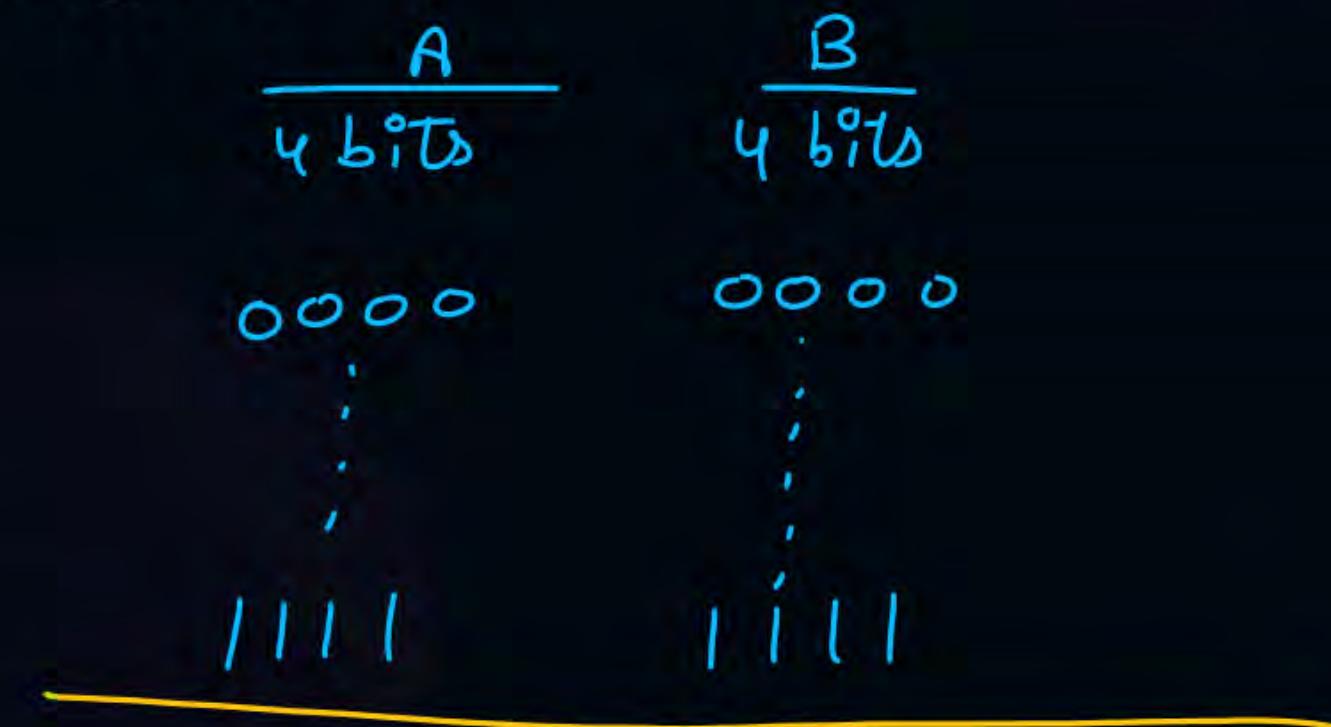
1. Addition of A and B 5 bits
2. Multiplication of A and B 8 bits

4 bits max value = $(1111)_2 = 15$

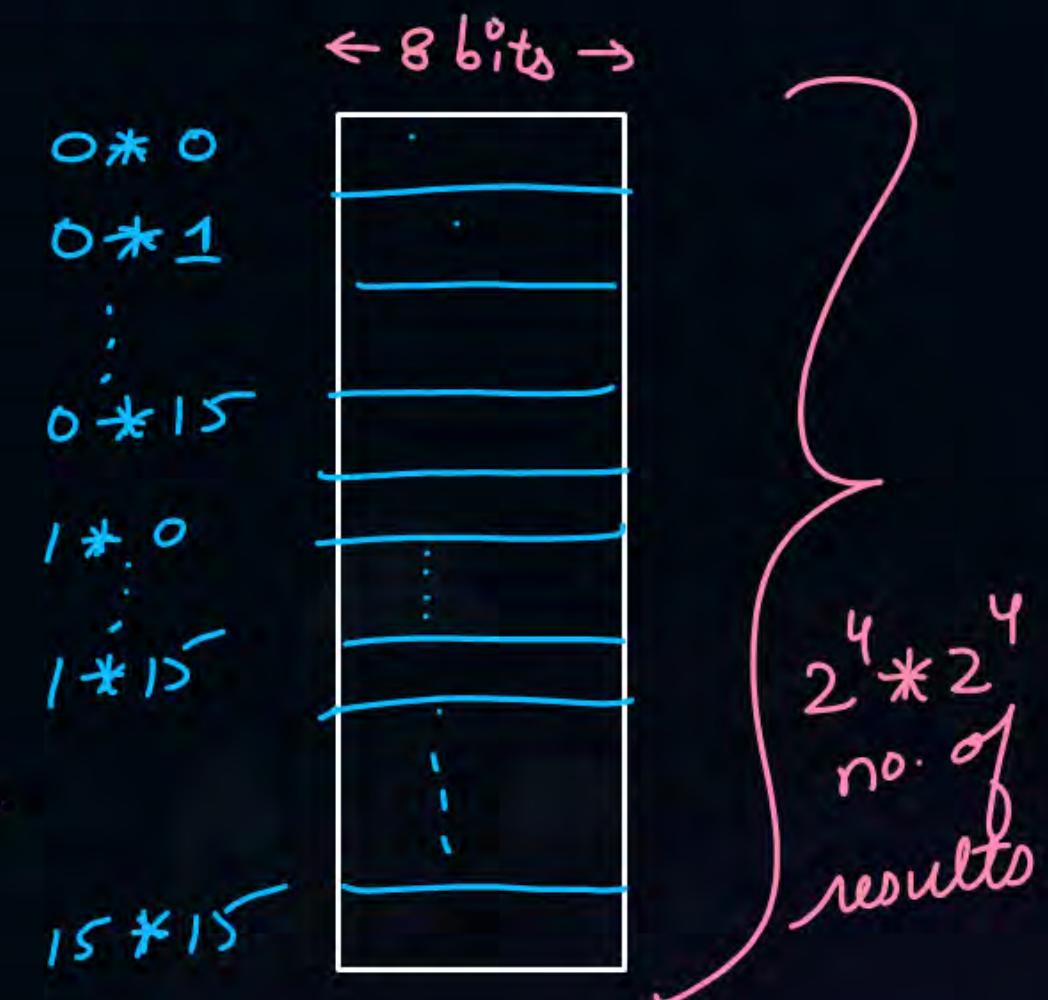
$$\begin{array}{r} 15 \\ + 15 \\ \hline 30 \Rightarrow 5 \text{ bits} \end{array} \quad \left| \quad \begin{array}{r} 15 \\ * 15 \\ \hline 225 \Rightarrow 8 \text{ bits} \end{array} \right.$$

#Q. The amount of ROM needed to store the table for multiplication of two 4-bit unsigned integer is?

- A** 64 bits
- B** 128 bits
- C** 1K bits
- D** ✓ 2K bits



$$\begin{aligned} \text{mem. size} &= 2^8 \times 8 \text{ bits} \\ &= 2^{11} \text{ bits} \\ &= 2\text{K bits} \end{aligned}$$



for n bits unsigned values

multiplication table

$(2^{2n} \times 2^n)$ bits

Addition table

$2^{2n} \times (n+1)$ bits



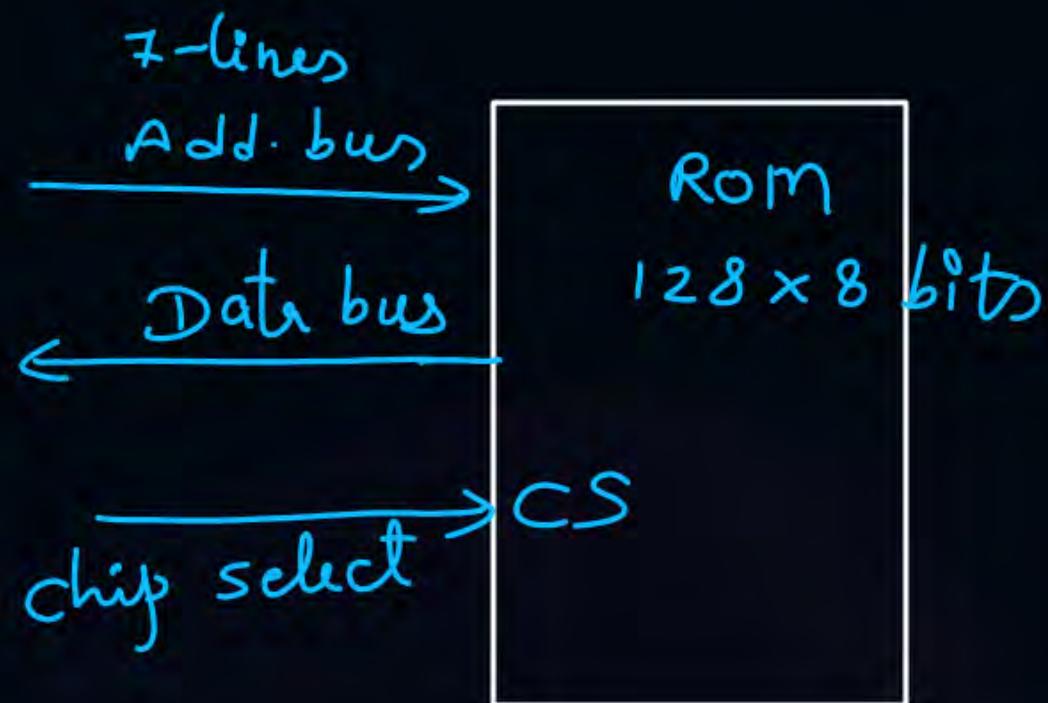
Topic : RAM Chip



CS	Read	Write	operation
0	x	x	No operation
1	0	0	No operation
1	0	1	write
1	1	x	Read



Topic : ROM Chip



CS	operation
0	No operation
1	Read



Topic : Chip Select

↓
taken from address lines



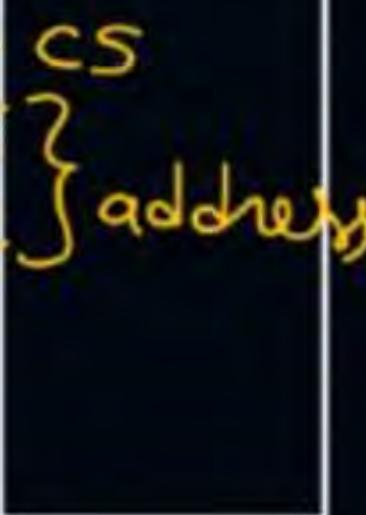
Topic : Chip Select

example:- 5 lines add. bus \Rightarrow a_4, a_3, a_2, a_1, a_0

address lines

a_4
 a_3
 a_2
 a_1
 a_0

Mem. chip



a_4 should be 1
always

address range to access
this mem.

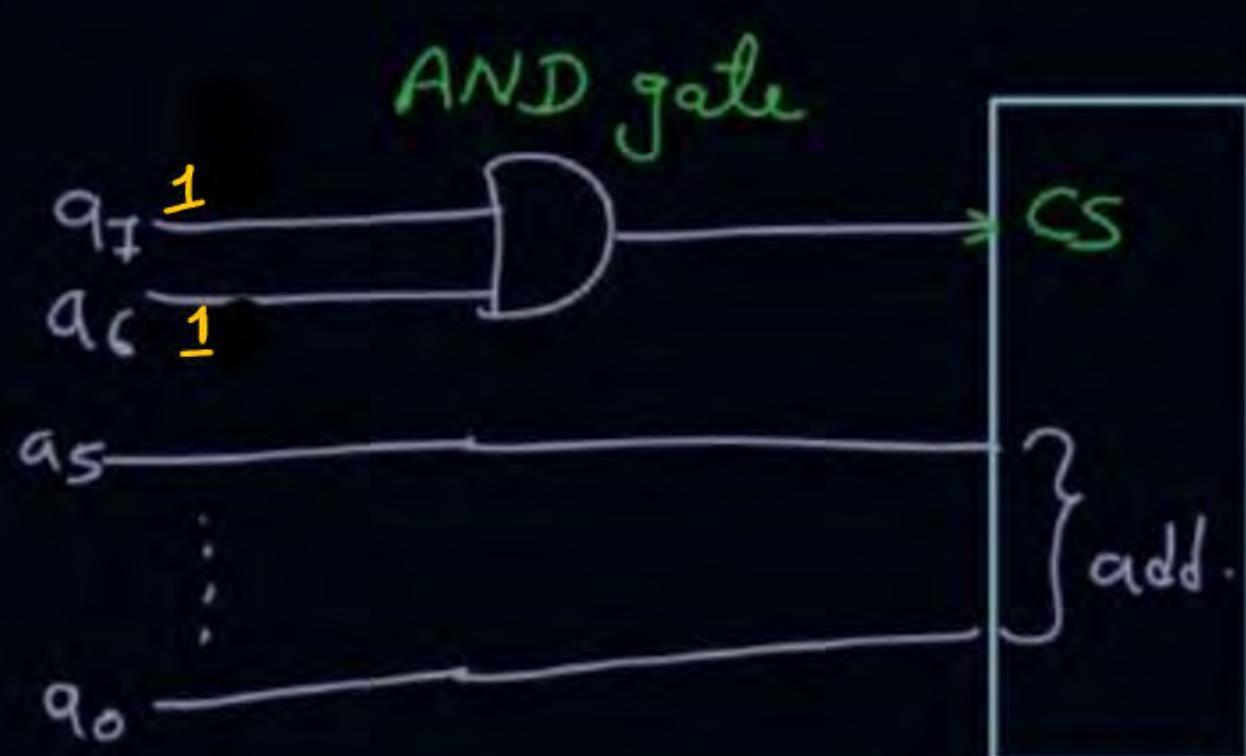
a_4	a_3	a_2	a_1	a_0
1	0	0	0	0
:				
1	1	1	1	1



Topic : Chip Select

P
W

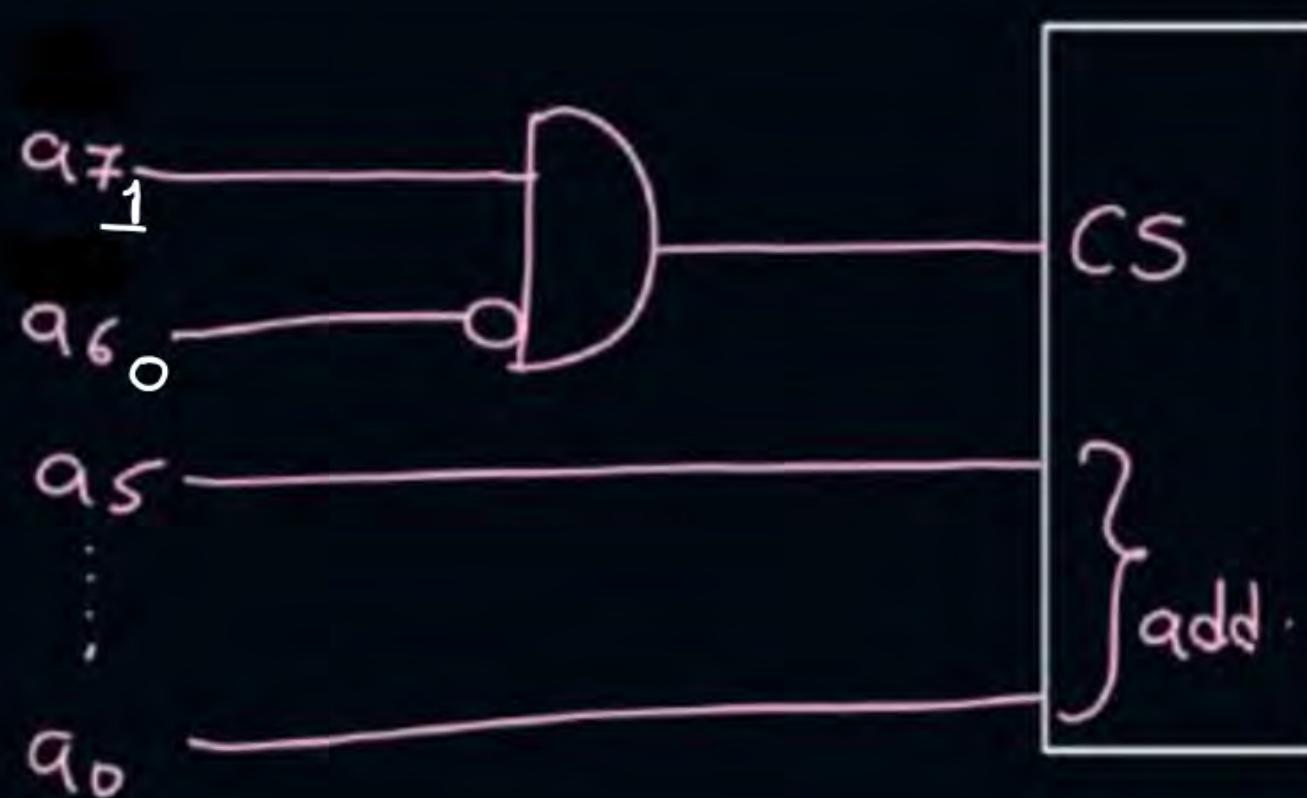
Ques:- 8 lines add. $\Rightarrow q_7 q_6 \dots q_0$





Topic : Chip Select

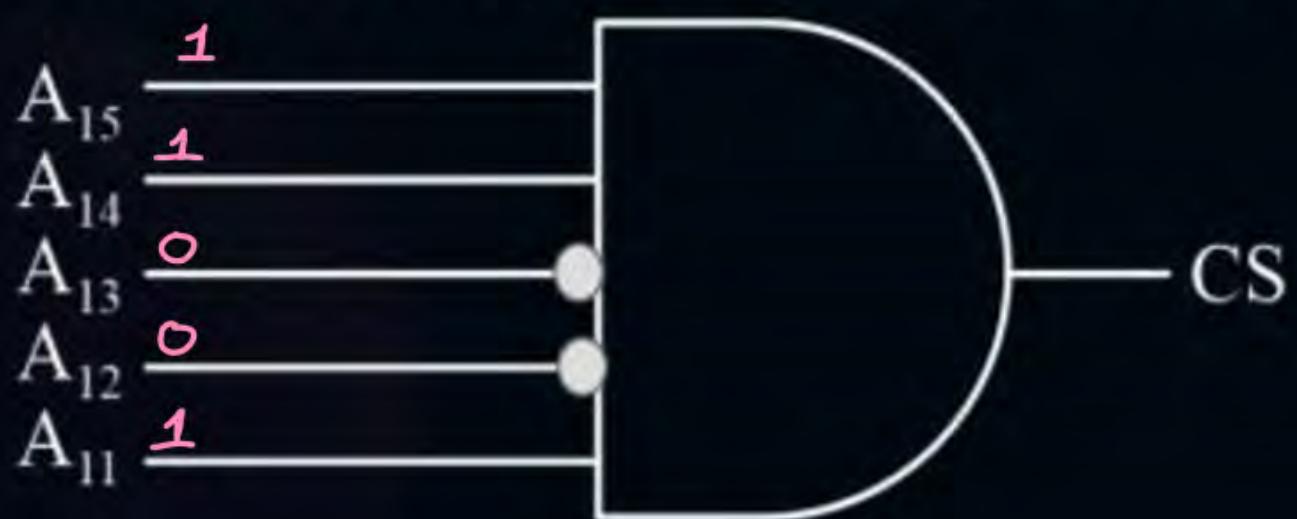
P
W



a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0
1	0	0	0	0	0	0	0
1	0	1	1	1	1	1	1

hexa
80
BF

#Q. The chip select logic for a certain DRAM chip in a memory system design is shown below. Assume that the memory system has 16 address lines denoted by A_{15} to A_0 . What is the range of address (in hexadecimal) of the memory system that can get enabled by the chip select (CS) signal?



- A** ✓ C800 to CFFF
- B** CA00 to CAFF
- C** C800 to C8FF
- D** DA00 to DFFF

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	\dots	A_0
1	1	0	0	1	0	0	0	...	0
.	.	C	8	.	8	0	0	...	0
1	1	0	0	1	1	1	1	...	1
.	.	C	F	.	F	F	F	...	F

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2 mins Summary



Topic

DMA

Topic

Cycle Stealing



Happy Learning

THANK - YOU