CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

CPU & Control Unit

Lecture No.- 02

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Recap of Previous Lecture

Topic CPU

Topic CPU Cycle

Topic CPI

Topics to be Covered

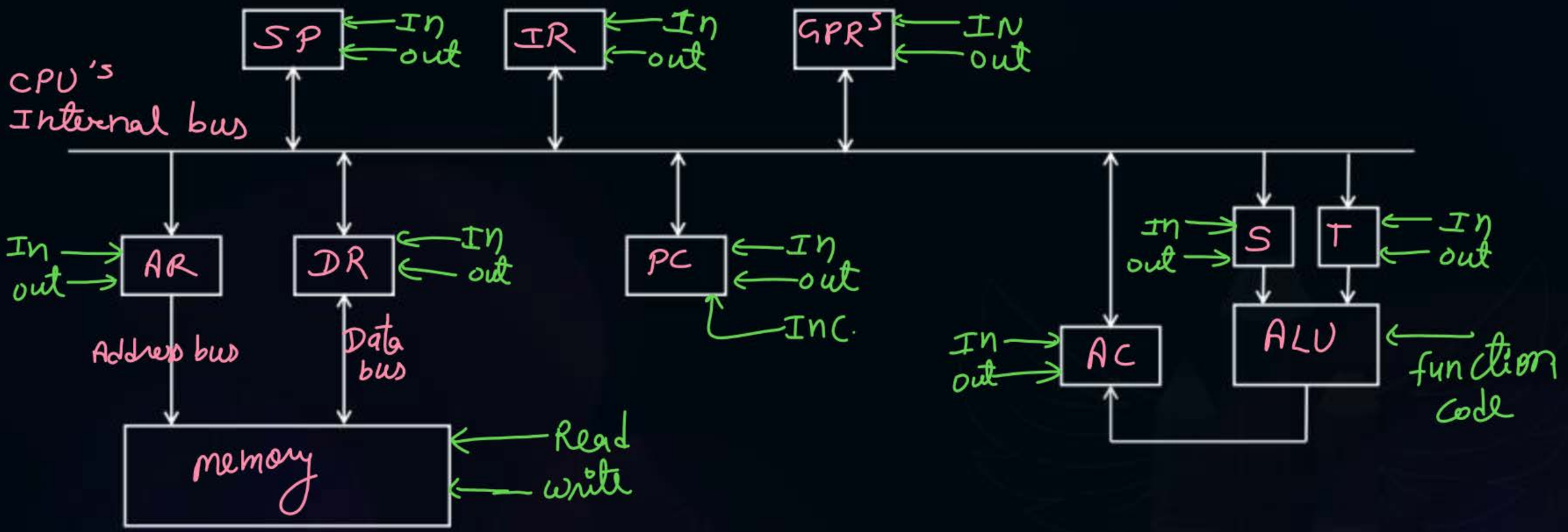
- Topic: Datapath
- Topic: Control Unit
- Topic: RISC vs CISC

Topic : Datapath

Collection of functional units such as arithmetic logic units or multipliers

Perform data processing operations

Topic : Datapath



Instruction fetch :-

$AR \leftarrow PC$ — 1

$DR \leftarrow M[AR]$ — 4

$IR \leftarrow DR,\ PC \leftarrow PC + 1$ — 1

} Total 6 cycles

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operation :-

$R1 \leftarrow R2 + R3$

$S \leftarrow R2$

$T \leftarrow R3$

$AC \leftarrow S + T$

$R1 \leftarrow AC$

} 4 cycles

Ques) each micro-operation except mem. access ⇒ 1 CPU cycle

mem. access ⇒ 4 CPU cycles

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write a micro-operation sequence for a function call instⁿ execution phase ?

$S \leftarrow SP$

$AC \leftarrow S + 1$

$SP \leftarrow AC,\ AR \leftarrow AC$

$DR \leftarrow PC$

$M[AR] \leftarrow DR$

$PC \leftarrow$ Target add.

Topic : Control Unit

It generates control signals and sends them to all components.
Components perform respective operation accordingly.

$AR \leftarrow PC$ — PC_{out}, AR_{In}

$DR \leftarrow M[AR]$ — $AR_{out}, Memory_{Read}, DR_{In}$

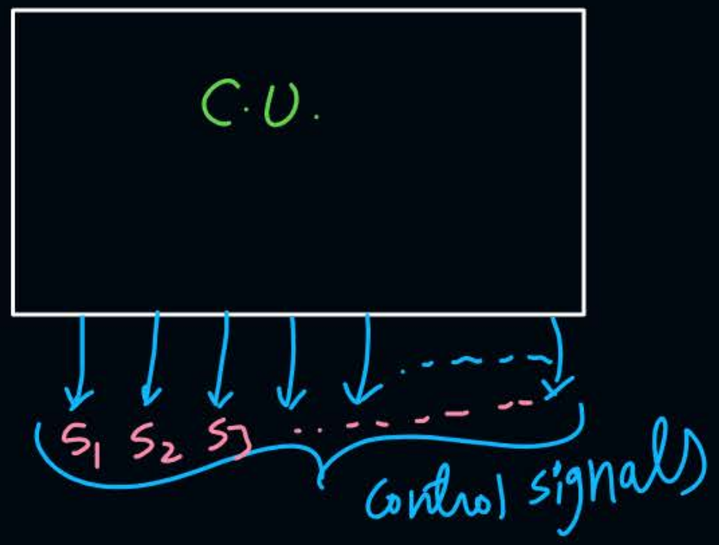
$IR \leftarrow DR, PC \leftarrow PC+1$ — $DR_{out}, IR_{In}, PC_{Inc}$

Control variable:-

Names of control signals

Control word is-

Collection of all the control signals generated at once by control unit.



Each control word is responsible for atleast one micro-operation.

S		T		Ac		ALU	GPRS	PC	AR		DR		IR		SP		Mem	
In	out	In	out	In	out	function code (4-bits)	In out ----	In out Inc	In	out	In	out	In	out	In	out	Read	write

1. AR ← PC

no operation

Control word

2. DR ← M[AR]

Topic : Control Unit Organization

How control unit is designed to generate control words.

1. Hardwired C.U.
2. Microprogrammed C.U.

Topic : Hardwired Control Unit

Control logic is implemented with Gates, flip-flops, decoders and other digital circuits.

Advantage: Can be optimized to produce a faster mode of operation.

Disadvantage:

1. Rearranging the wires among various components is difficult.
2. Difficult to change the control logic
3. Difficult to design for complex computers

Topic : Hardwired Control Unit

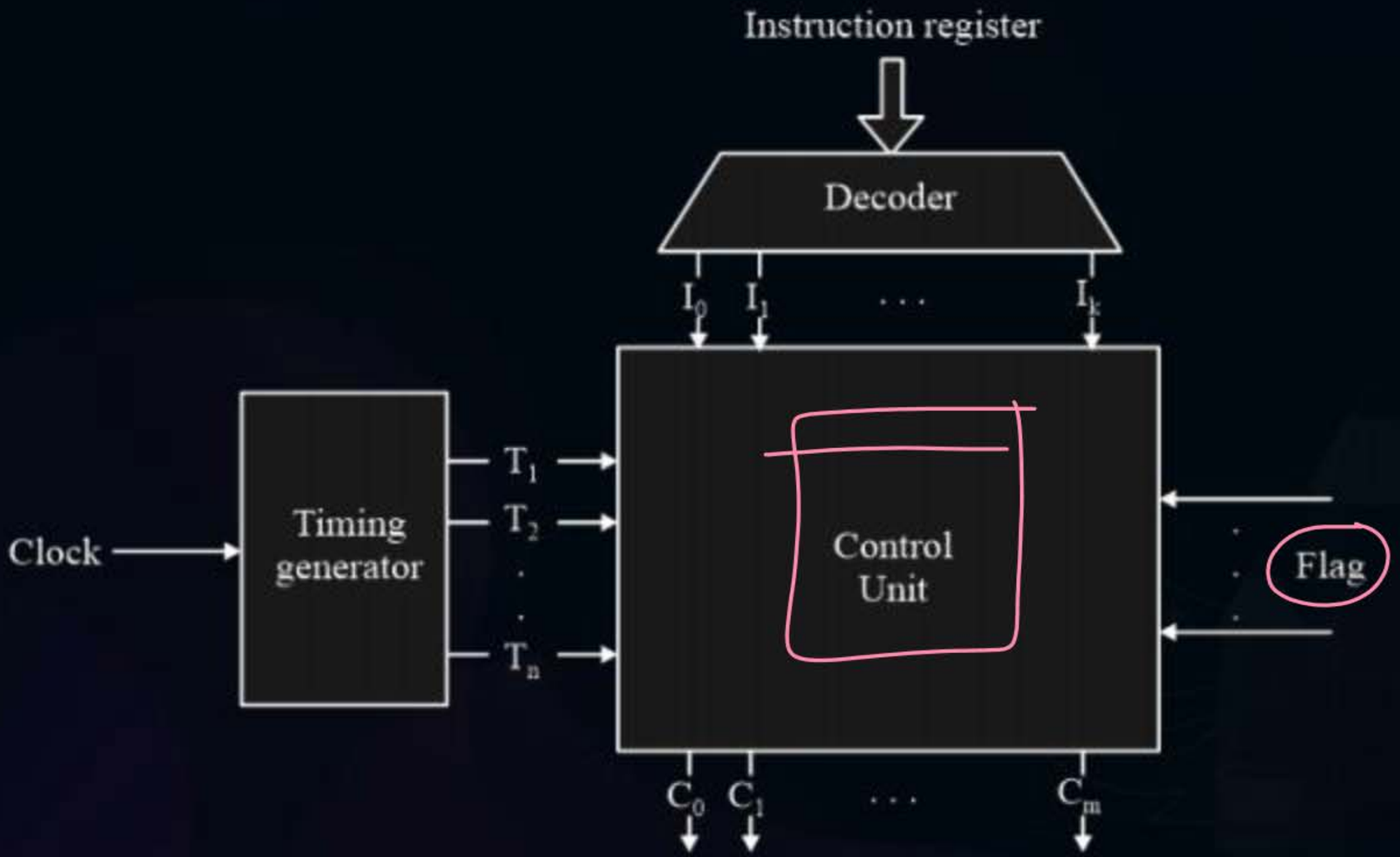
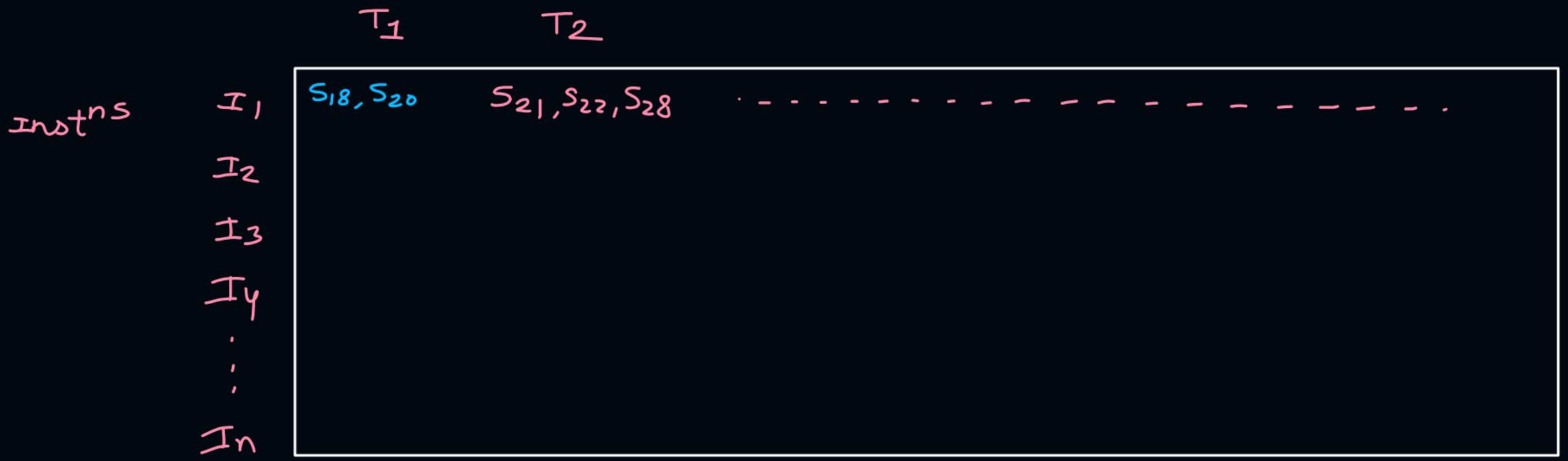


Table design



[MCQ]

GATE- PYQ

#Q. A hardwired CPU uses 10 control signals S1 to S10, in various time steps T1 to T5, to implement 4 instructions I1 to I4 as shown below:

	T1	T2	T3	T4	T5
I1	S1, S3, S5	S2, S4, S6	S1, S7	S10	S3, S8
I2	S1, S3, S5	S8, S9, S10	S5, S6, S7	S6	S10
I3	S1, S3, S5	S7, S8, S10	S2, S6, S9	S10	S1, S3
I4	S1, S3, S5	S2, S6, S7	S5, S10	S6, S9	S10

Which of the following pairs of expressions represent the circuit for generating control signals S5 and S10 respectively?

$$S_5 = I_1T_1 + I_2T_1 + I_3T_1 + I_4T_1 + I_2T_3 + I_4T_3$$
$$= (I_1 + I_2 + I_3 + I_4)T_1 + (I_2 + I_4)T_3 = T_1 + (I_2 + I_4)T_3$$

A

$S5 = T1+I2\cdot T3$ and
$S10 = (I1 + I3)\cdot T4 + (I2 + I4)\cdot T5$

B

$S5 = T1+(I2+I4)\cdot T3$ and
$S10 = (I1 + I3)\cdot T4 + (I2 + I4)\cdot T5$

C

$S5 = T1+(I2+I4)\cdot T3$ and
$S10 = (I1 + I3 + I4)\cdot T2 + (I2 + I3)\cdot T4+(I2+I4)\cdot T5$

D

$S5 = T1+(I2 + I4)\cdot T3$ and
$S10 = (I2 + I3)\cdot T2 + I4\cdot T3 + (I1 + I3)\cdot T4 + (I2+I4)\cdot T5$

Topic : Micro-Programmed Control Unit

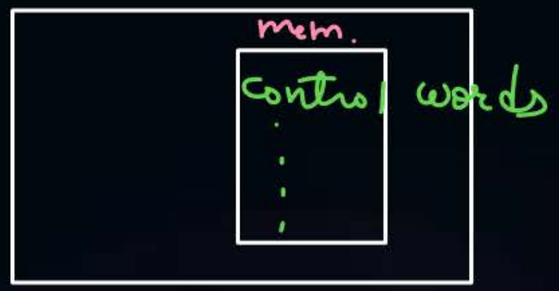
Control logic is implemented with micro-programs.

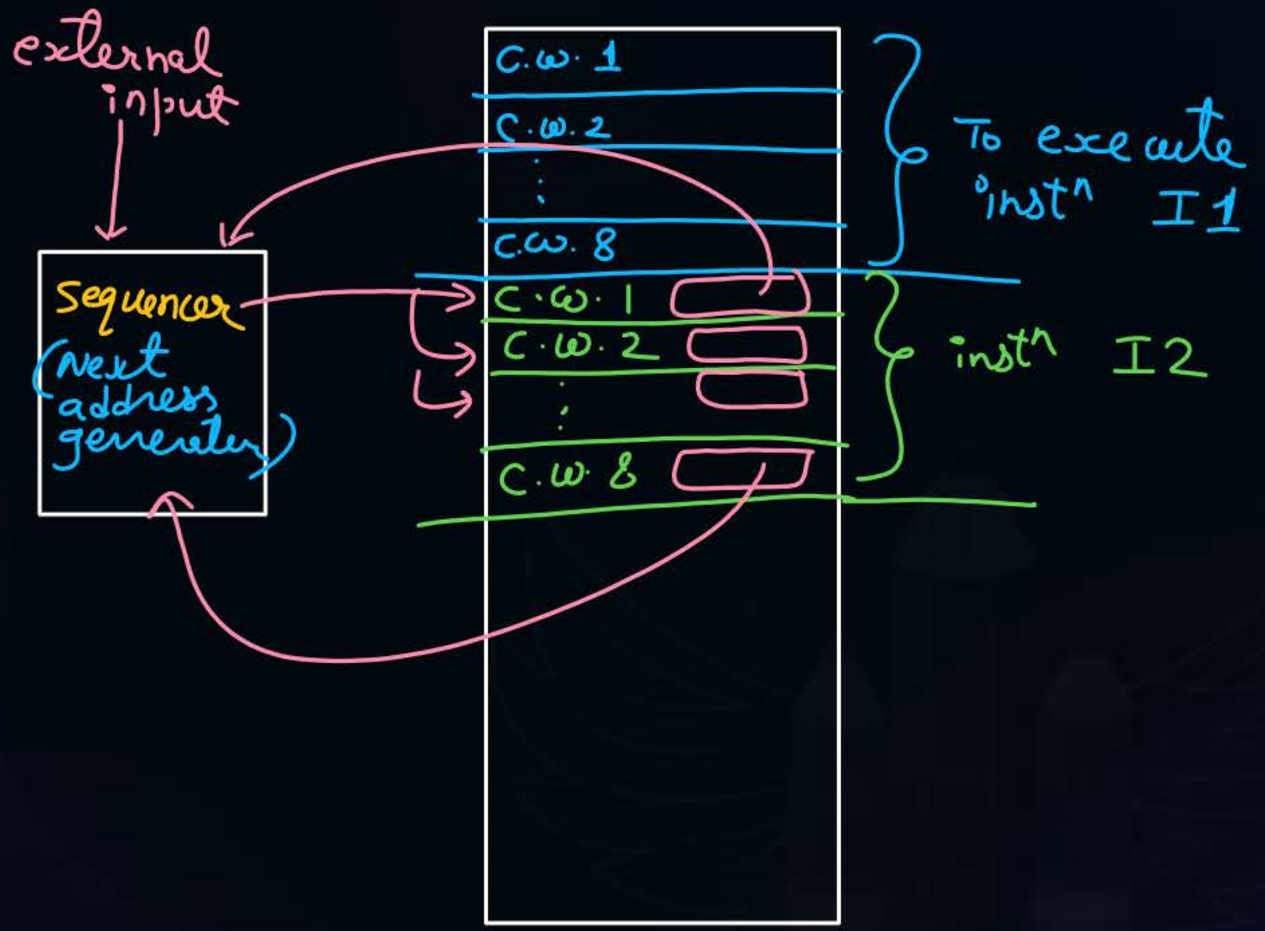
Advantage:

1. Updating the control logic is easy.
2. Designing for complexing computers is easy.

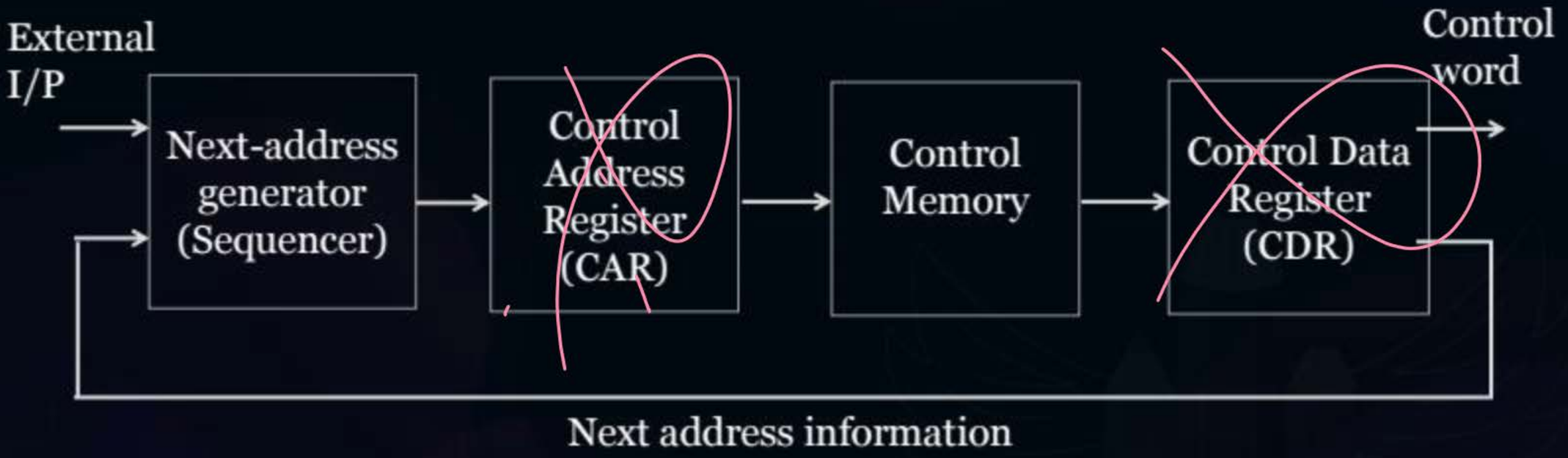
Disadvantage: Slower than hardwired control unit.

Topic : Micro-Programmed Control Unit



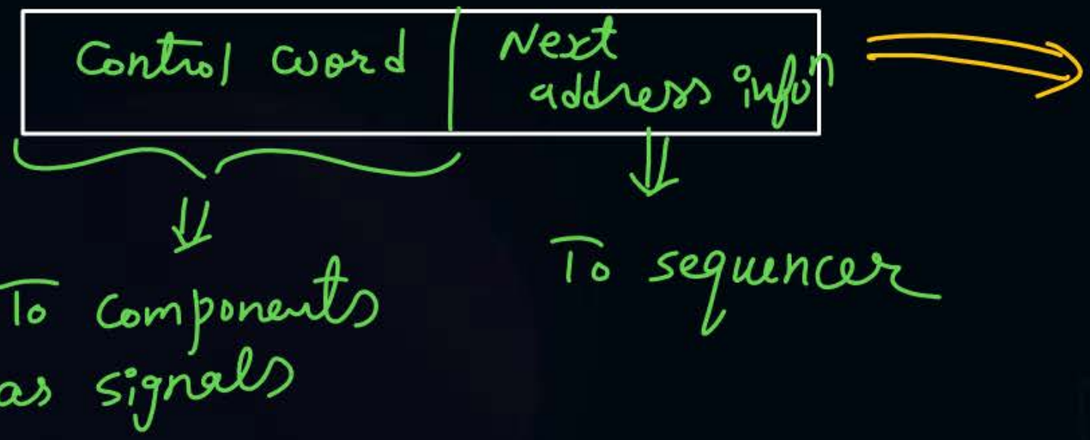


Topic : Control Word Sequencing



Topic : Control Word Sequencing

on each address in control memory a microinstruction.



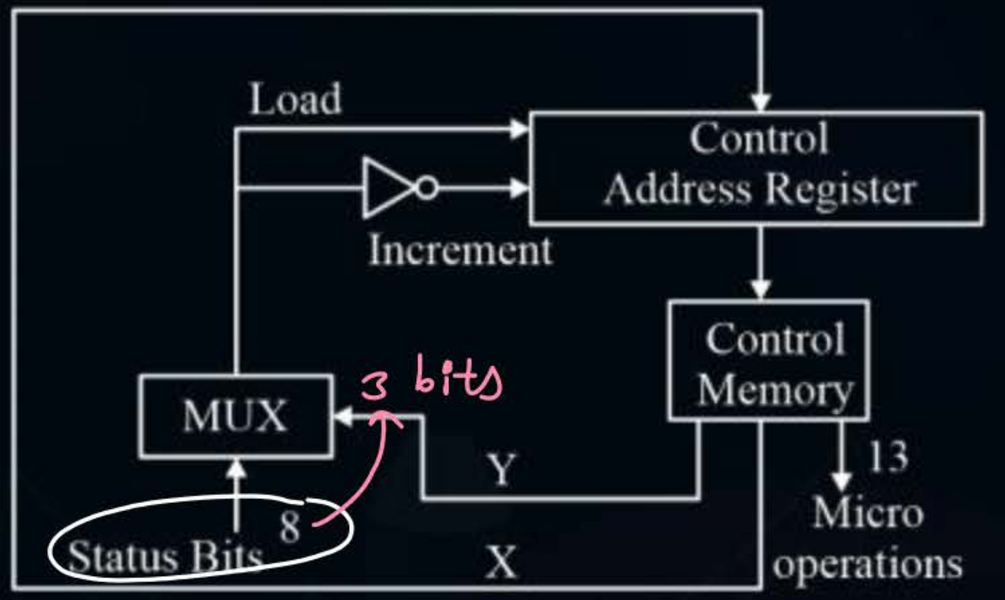
⟹ standard format of microinstr

Control word	MUX select	Address

[MCQ]

#Q. The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits in the inputs of the MUX.

How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?

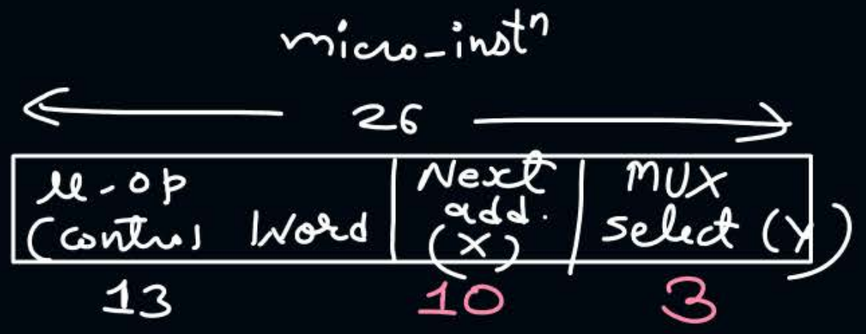


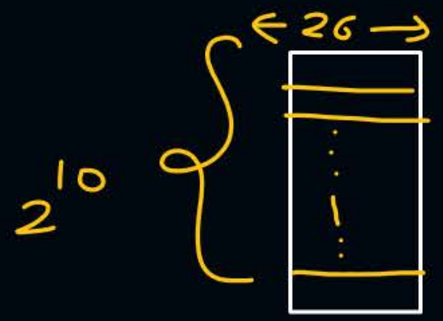
A 10, 3, 1024

B 8, 5, 256

C 5, 8, 2048

D 10, 3, 512





no. of words/microinstns in control memory = 2^{10} = 1024

Control mem. size = 2^{10} * 26 bits

= 26 k bits

Topic : Types of Microprogrammed Control Unit

Horizontal

→ for each signal, one bit stored in control word.

→ longer sized control word

if any signal can not be the part of any group then it is stored as horizontal manner.

vertical

→ signals are divided into groups in such a way that from each group one signal can be active at a time. Group infos are stored in encoded form.

→ smaller control word size

→ decoders are used

→ slower as compared to Horizontal

Horizontal

4 bits

S_0 is active

S_1 is active

0010

S_2

0100

S_3

1000

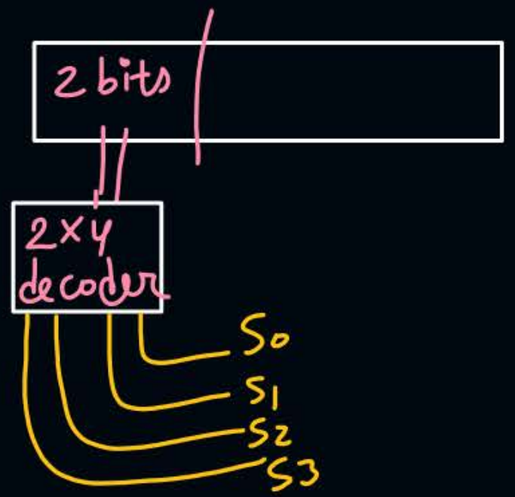
Vertical

S_0 is active

01

10

11



Topic : Speed Comparison

fastest

Hardwired > Horizontal microprogrammed > Vertical microprogrammed

slowest

[NAT]

#Q. A control unit generates 120 control signals, which are divided into 6 groups of mutually exclusive signals as below:

Group1 = 30 ⇒ 5 bits
Group2 = 13 ⇒ 4
Group3 = 12 ⇒ 4
Group4 = 3 ⇒ 2
Group5 = 27 ⇒ 5
Group6 = 35 ⇒ 6

26

Horizontal = 120 bits
vertical = 26 bits
bits saved = 94 bits

Ans.

How many bits can be saved by using vertical micro-programmed control unit as compared to horizontal one?

2 mins Summary

Topic Datapath

Topic Control Unit

Topic RISC vs CISC

Happy Learning

THANK - YOU