CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

IO Organization

Lecture No.- 02

By- Vishvadeep Gothi sir

Recap of Previous Lecture

Topic Peripheral Device

Topic IO vs Memory Buses

Topic Memory Mapped IO vs IO Mapped IO

Topic Asynchronous Data Transfer

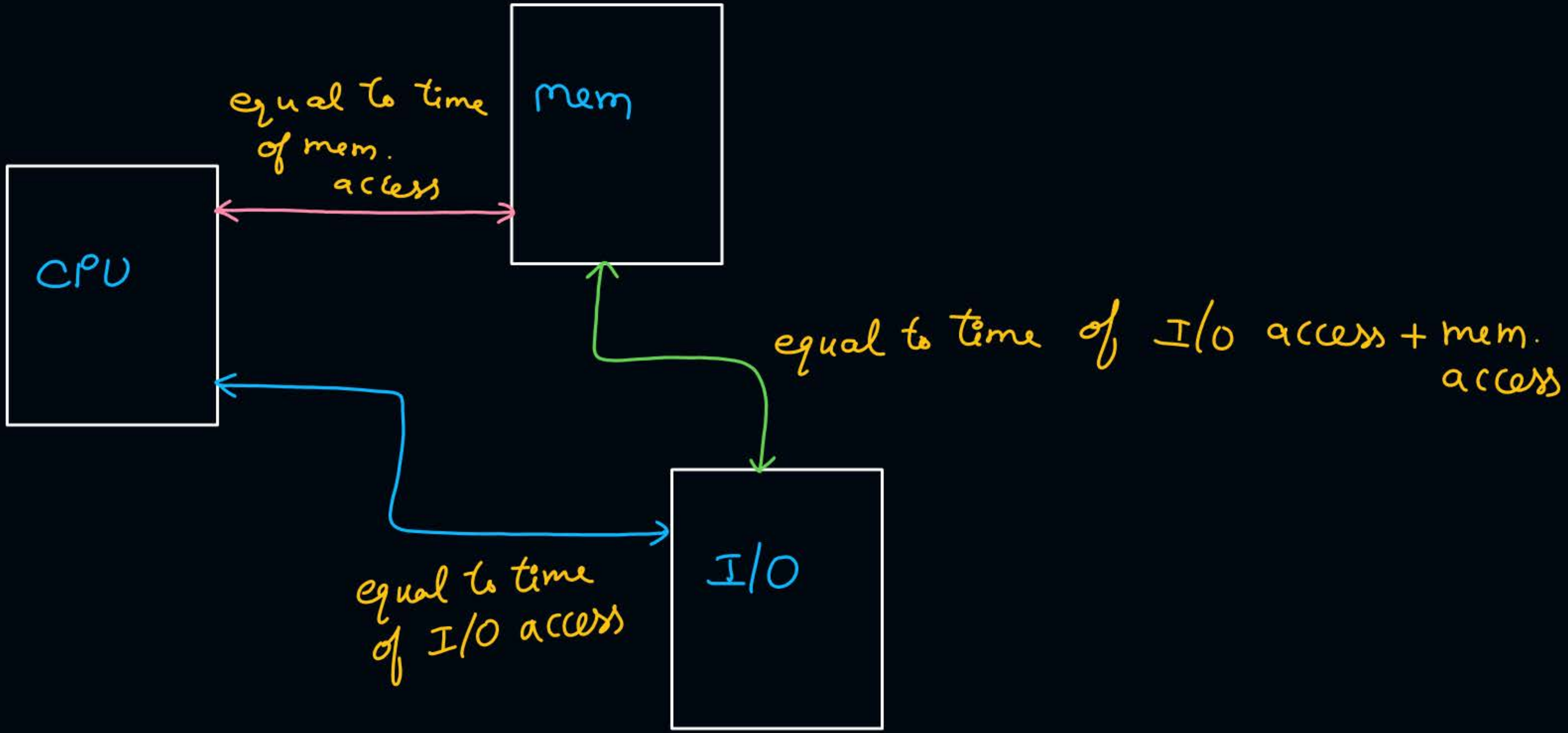
Topic Modes of Transfer

Topics to be Covered

Topic Interrupt IO

Topic DMA

Topic Cycle Stealing


mem
CPU
I/O
equal to time of mem. access
equal to time of I/O access + mem. access
equal to time of I/O access

Topic : Modes of Transfer

1. Programmed I/O or Program controlled I/O (Polling)
2. Interrupt I/O

→ b/w CPU & I/O

3. DMA (Direct mem. Access)

→ b/w I/O and mem.

Use of DMA ⇒ Booting
Page fault service
Application (Process) arrival

Topic : Programmed IO

- There is no any provision through which IO can inform to CPU about data transfer
- IO sets its own status and waits
- CPU runs program periodically and checks the status of each device one-by-one
- If any device has its status set then CPU performs data transfer for it.

Disadvantage :- wastage of CPU time due to periodic program execution and status check.

Topic : Time Required in Programmed IO

= Time needed to check status of device + data transfer time

↓

depends on I/O speed

status size = min. size of Content sent b/w I/O & CPU.

Topic : Interrupt Initiated IO

- IO device has a provision (Interrupt Signal) to inform to CPU about communication.

Topic : Interrupt Initiated IO

- IO device has a provision (Interrupt Signal) to inform to CPU about communication.
- When CPU receives interrupt:
  - It completes execution of current instruction
  - Saves the status (PC, PSW etc.) of current process onto the stack
  - Branches to service the interrupt
  - Resumes the previous process by taking out the values from stack

[MCQ] GATE- 2018

QPTRS

#Q. The following are some events that occur after a device controller issues an interrupt while process L is under execution.

P. The processor pushes the process status of L onto the control stack

Q. The processor finishes the execution of the current instruction

R. The processor executes the interrupt service routine

S. The processor pops the process status of L from the control stack

T. The processor loads the new PC value based on the interrupt

Which of the following is the correct order in which the events above occur?

A [✓ QPTRS]

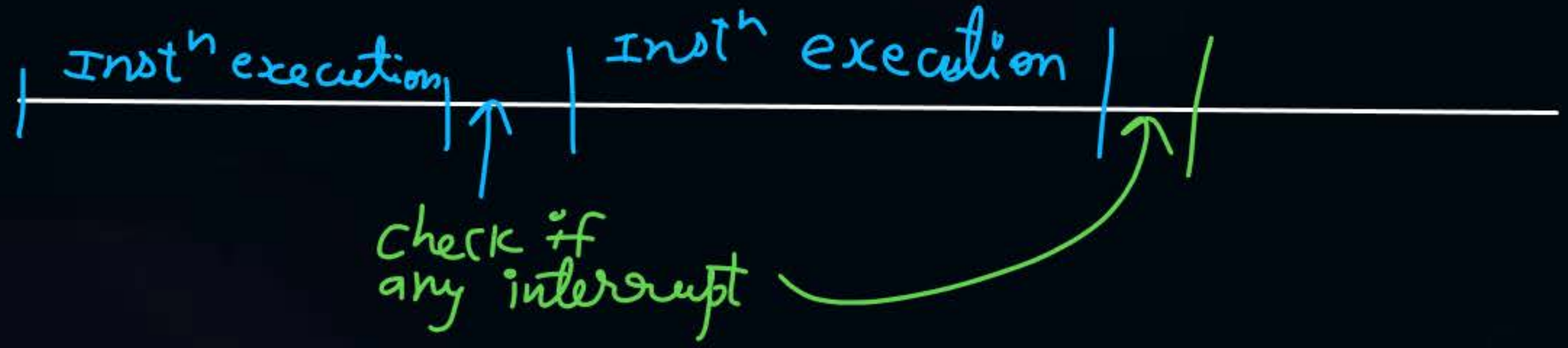
B PTRSQ

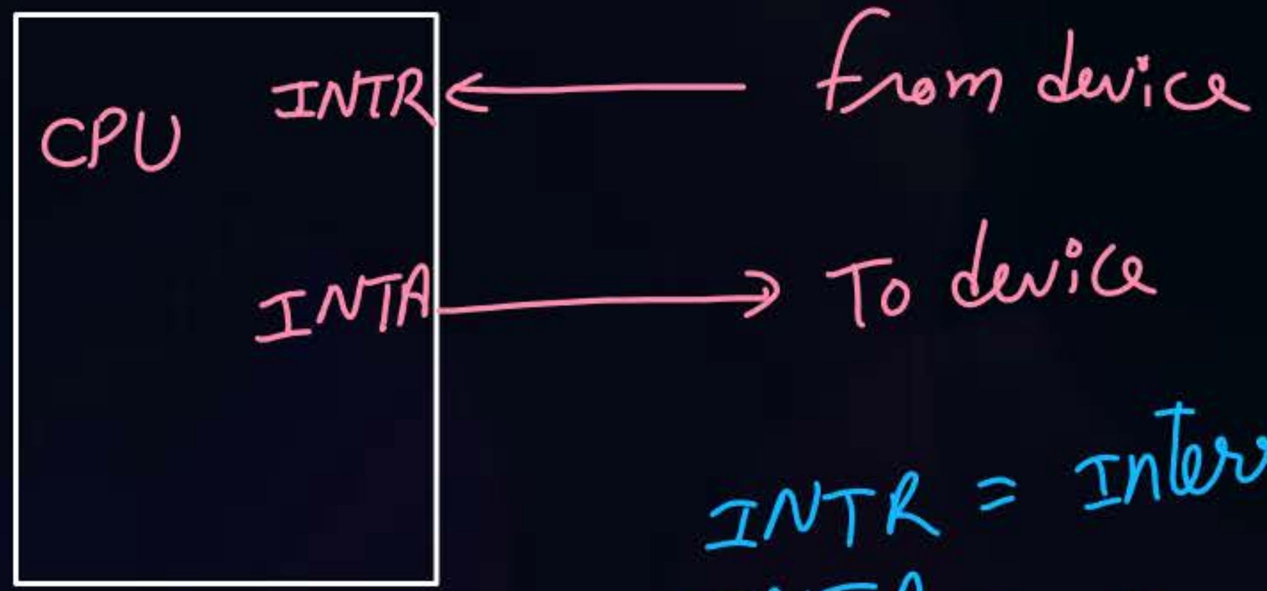
C TRPQS

D QTPRS

Topic : Interrupt Initiated IO

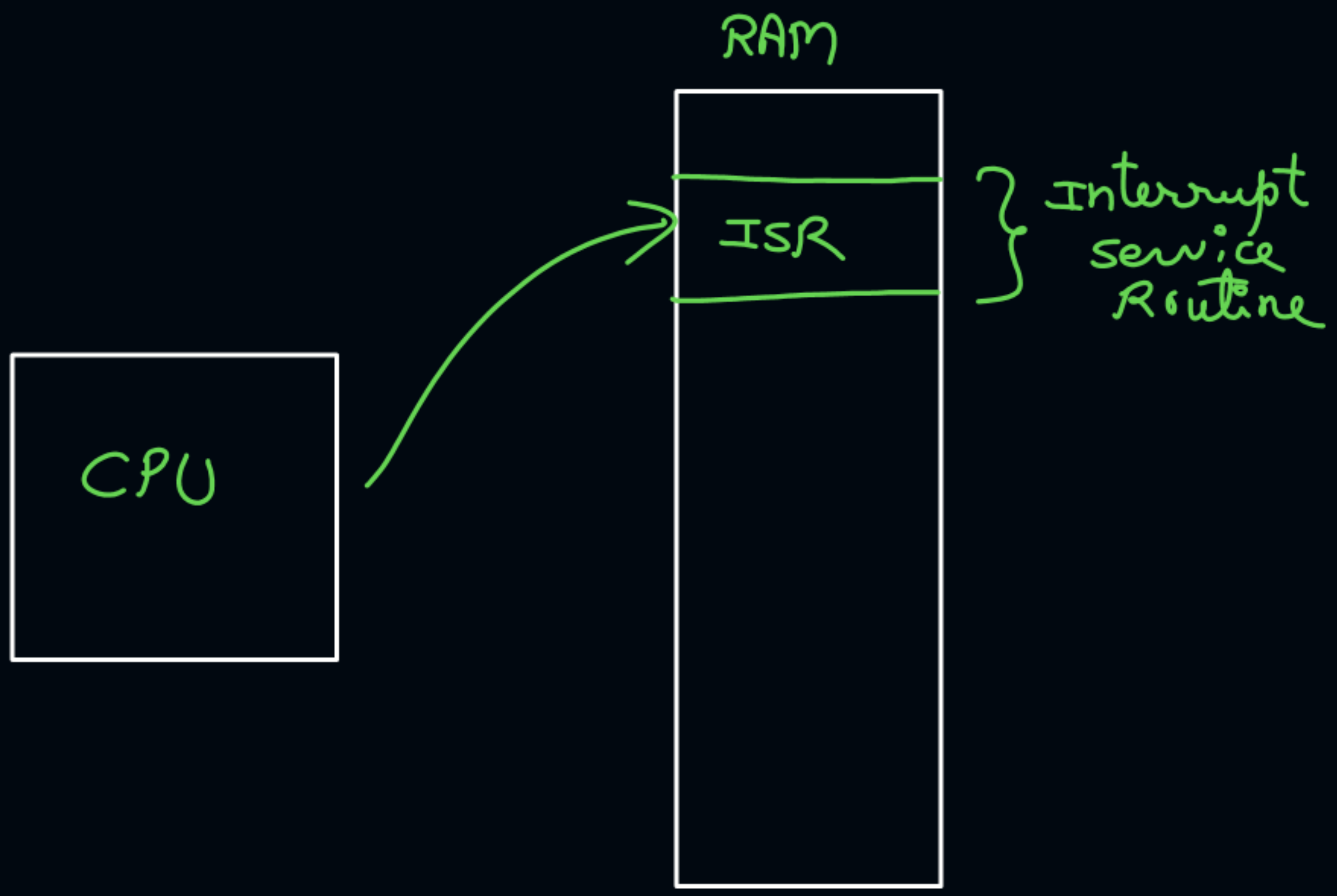
CPU checks for interrupt after every inst^n execution.





INTR = Interrupt Request

INTA = " Ack.

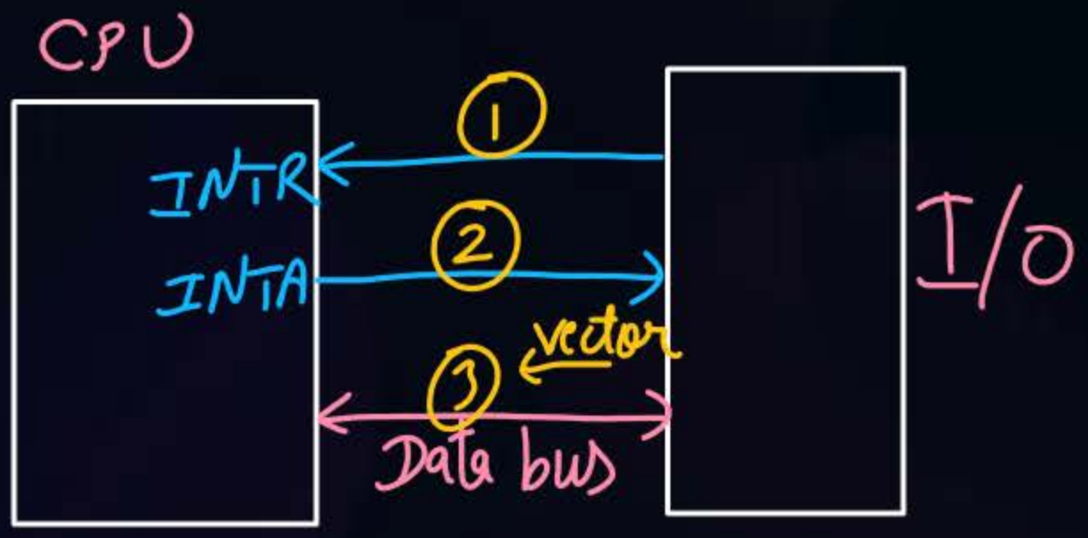

RAM
ISR
Interrupt
service
Routine
CPU

Topic : Vectored vs Non-Vectored

Vectored	Non-Vectored (scalar)
• Device sends interrupt and vector	• Device sends only interrupt

reference of ISR

CPU first executes a default ISR and obtains actual ISR.



Topic : Maskable vs Non-Maskable

Maskable	Non-Maskable
• CPU can accept or reject the interrupt	• CPU always accepts the interrupt

keep pending

or

reject

Topic : Internal Vs External

External	Internal
• Device Generates the interrupt	• Interrupt due to unexpected error during instruction execution

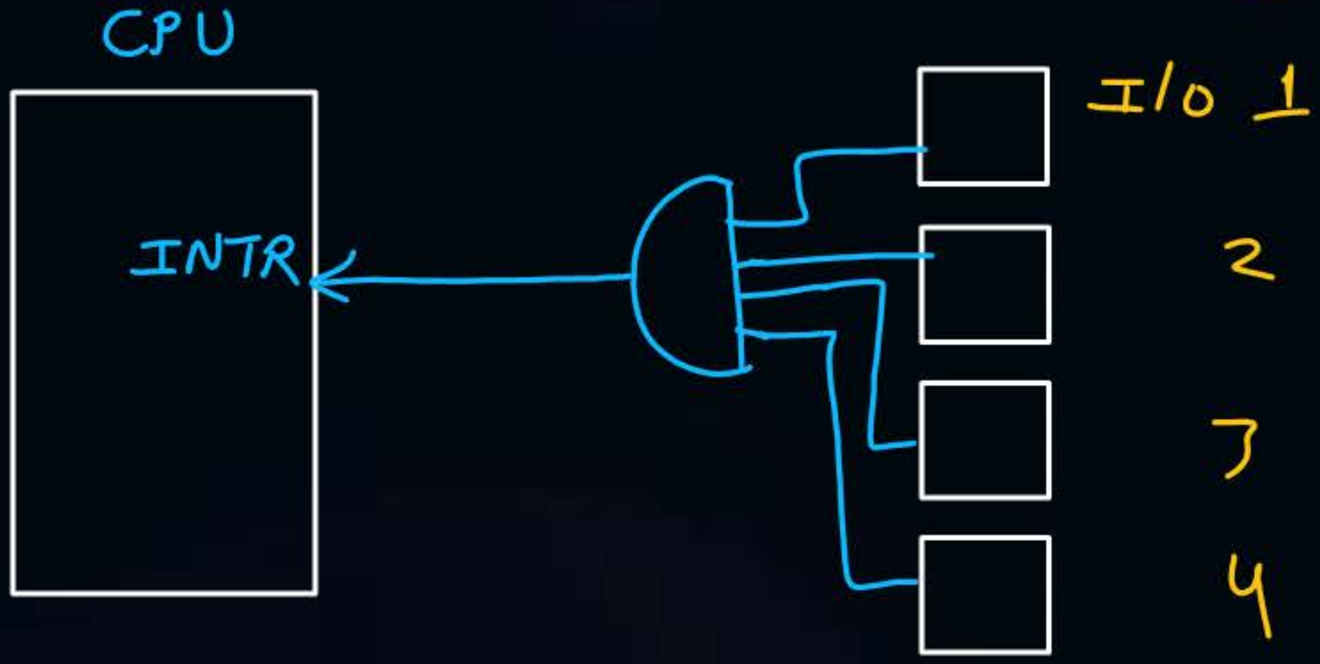
↓

1. CPU Cannot execute current inst^n.
2. CPU first services interrupt
3. CPU restarts the inst^n.

ex:- page fault.

Topic : Simultaneous Interrupts

→ CPU services interrupt of highest priority device.



Priority based interrupt handling sol^n

S/W sol^n

H/W sol^n

serial (daisy chaining)

Parallel

Topic : Time Required in Interrupt IO

$$= \text{Interrupt overhead time} + \text{Interrupt service time}$$

[NAT]

#Q. Consider a CPU which takes 0.2 microseconds as interrupt overhead time when a device generates interrupt for CPU, and CPU accepts it. After that CPU takes 5 cycles to service the interrupt. If CPU runs on 1MHz clock rate then total time CPU spends for interrupt service is 5.2 microseconds?

$$= 0.2\ \mu sec + 5 \text{ cycles}$$

$$= 0.2\ \mu sec + 5 * \frac{1}{1 MHz}$$

$$= 5.2\ \mu sec$$

[NAT]

#Q. Consider a CPU which takes 0.5 nanoseconds as interrupt overhead time when a device generates interrupt for CPU, and CPU accepts it. After that CPU takes 6 cycles to service the interrupt. The total time CPU spends for interrupt service is 1.7 nanoseconds. The clock rate of the CPU is 5000 MHz?

$$1.7\ \text{ns} = 0.5\ \text{ns} + 6\ \text{cycles} * \frac{1}{\text{clock rate}}$$

$$1.2\ \text{ns} = \frac{6}{\text{clock rate}}$$

$$\text{clock rate} = \frac{6}{1.2\ \text{ns}}$$

$$= 5\ \text{GHz}$$

$$= 5000\ \text{MHz}$$

[NAT]

#Q. A device with data transfer rate 20 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 10 microsecond.

1. Total time required in programmed IO for 10 bytes data transfer?
2. Total time required in interrupt IO for 10 bytes data transfer?
3. What is the minimum performance gain of operating the device under interrupt mode over operating it under program controlled mode?

1. Prog. I/O time = status check time + data transfer time

$$= 50\,\mu sec + (10 * 50\,\mu sec)$$

$$= 550\,\mu sec$$

for 20KB, device takes = 1 sec

for 1 B, —— " —— $= \frac{1\text{ sec}}{20\text{ K}\cancel{\text{B}}} * 1\cancel{\text{B}}$

$$= \frac{1}{20}\text{ msec}$$

$$= \frac{1000}{20}\,\mu sec$$

$$= 50\,\mu sec$$

2. Interrupt I/O $= 10\ \mu sec + (50 * 10)$

$= 510\ \mu sec$

3. Performance gain or speed up $= \dfrac{\text{slower technique time}}{\text{faster technique time}}$

$= \dfrac{550\ \mu sec}{510\ \mu sec}$

$= 1.078$

[NAT]

GATE - PYQ

Ans = 25

#Q. A device with data transfer rate 10 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 4 microsecond. The byte transfer time between the device interface register and CPU or memory is negligible. What is the minimum performance gain of operating the device under interrupt mode over operating it under program-controlled mode?

10KB, time = 1 sec

$$1B \text{ time} = \frac{1 \text{sec}}{10KB} * 1B$$

$$= 0.1 \text{msec}$$

$$= 100 \mu\text{sec}$$

$$\text{Performance gain} = \frac{\text{Prog. I/o time}}{\text{Interrupt I/o time}}$$

$$= \frac{100 \mu\text{sec} + 0}{4 \mu\text{sec} + 0}$$

$$= 25$$

2 mins Summary

Topic Interrupt IO

Topic DMA

Topic Cycle Stealing

Happy Learning

THANK - YOU