

CS & IT ENGINEERING



COMPUTER ORGANIZATION AND ARCHITECTURE

Memory Organization

Lecture No.- 02

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Recap of Previous Lecture



Topic

Memory Hierarchy

Topic

Memory Presentation

Topic

Memory Address Decoder

Topic

Main Memory

Topics to be Covered



Topic

Multiple Chips in Single Memory System

Topic

DRAM Refresh



Topic : Multiple Chips in Single Memory System

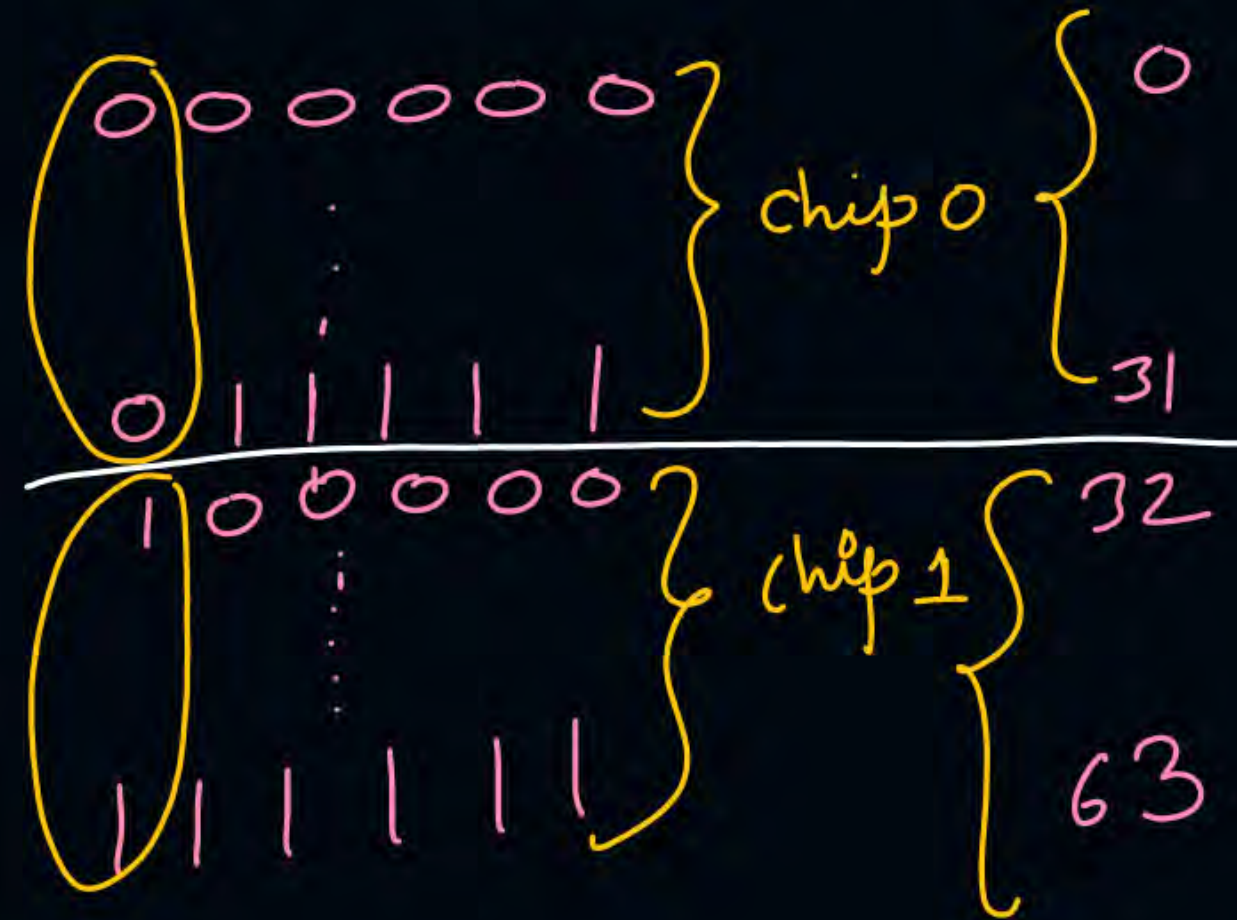


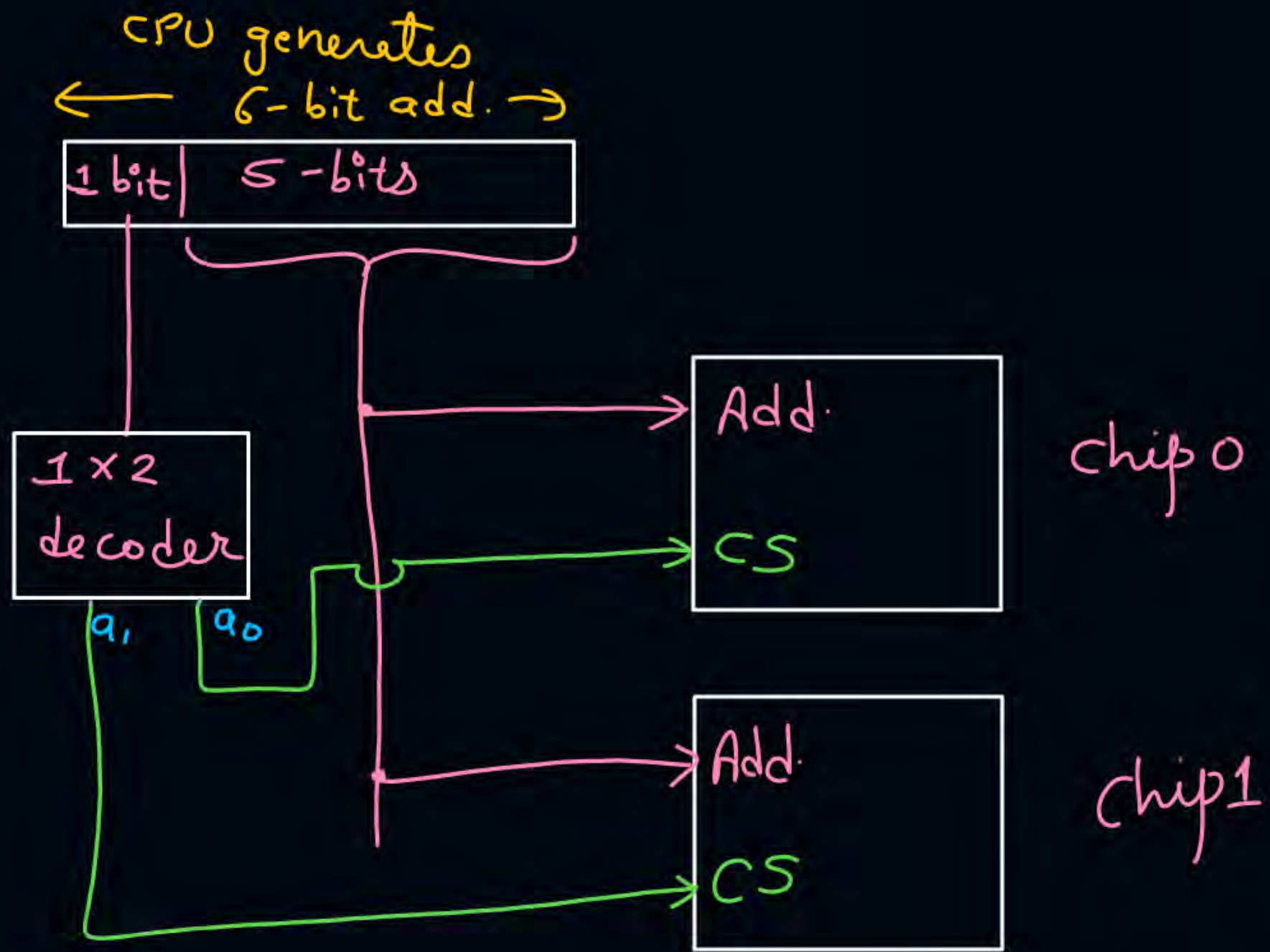
total mem capacity = no. of chips * 1 chip capacity

2 byte addressable chips of 32B used \Rightarrow Total Capacity = 64 bytes

$$\begin{array}{r} \text{Add.} \\ 32 \times 8 \text{ bits} \Rightarrow 5\text{-bits} \\ 32 \times 8 \text{ bits} \Rightarrow 5\text{-bits} \\ \hline 64 \times 8 \text{ bits} \Rightarrow 6 \text{ bits} \end{array}$$

6-bits address range



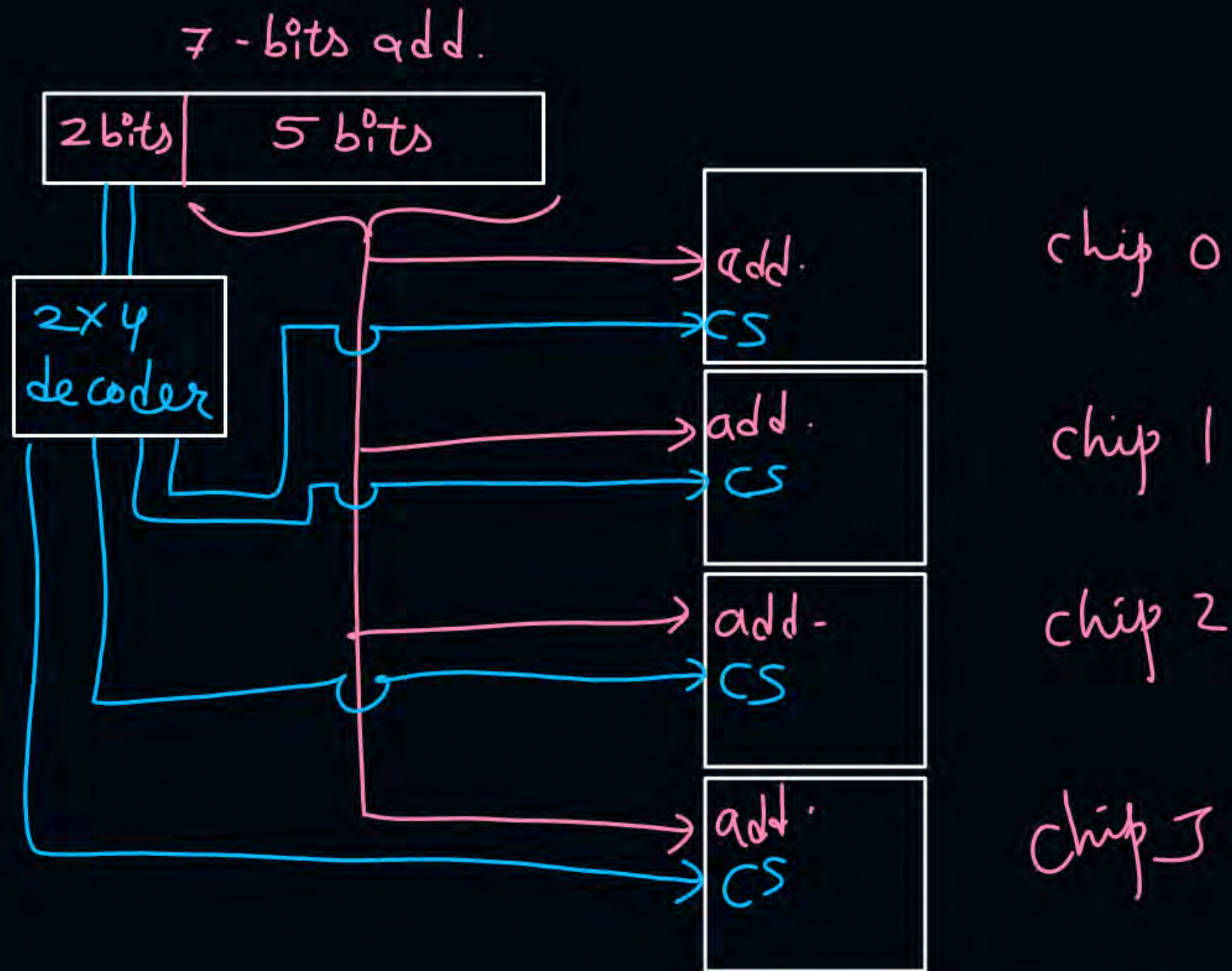


vertical arrangement
of the chips



when no. of addresses
in mem. system, needed
more than no. of address
in one chip.

4 chips 32×8 bits \Rightarrow Total capacity 128×8 bits



- #Q. (a) How many 128×8 bits RAM chips are needed to provide a memory capacity of 2048 bytes?
- (b) How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?
- (c) How many lines must be decoded for chip select? Specify the size of decoder?

$$a) \frac{2048 \times 8 \text{ bits}}{128 \times 8 \text{ bits}} = \frac{2^{11}}{2^7} = 2^4 = 16$$

b) 11 lines, 7 line common

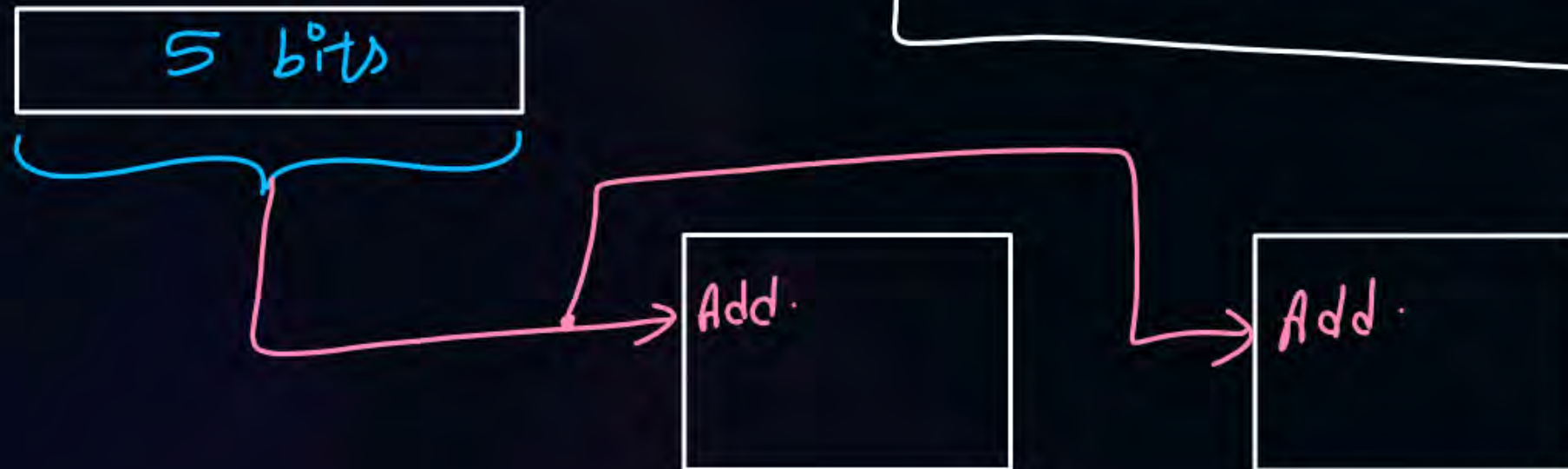
c) 4 lines, decoder = 4×16

#Q. How many 32×8 bits RAM chips are needed to provide a memory capacity of 32×16 bits?

$$= \frac{32 \times 16^2}{32 \times 8} = 2$$

→ CPU generates 5-bits add.

if data per address required more than data per address in a chip

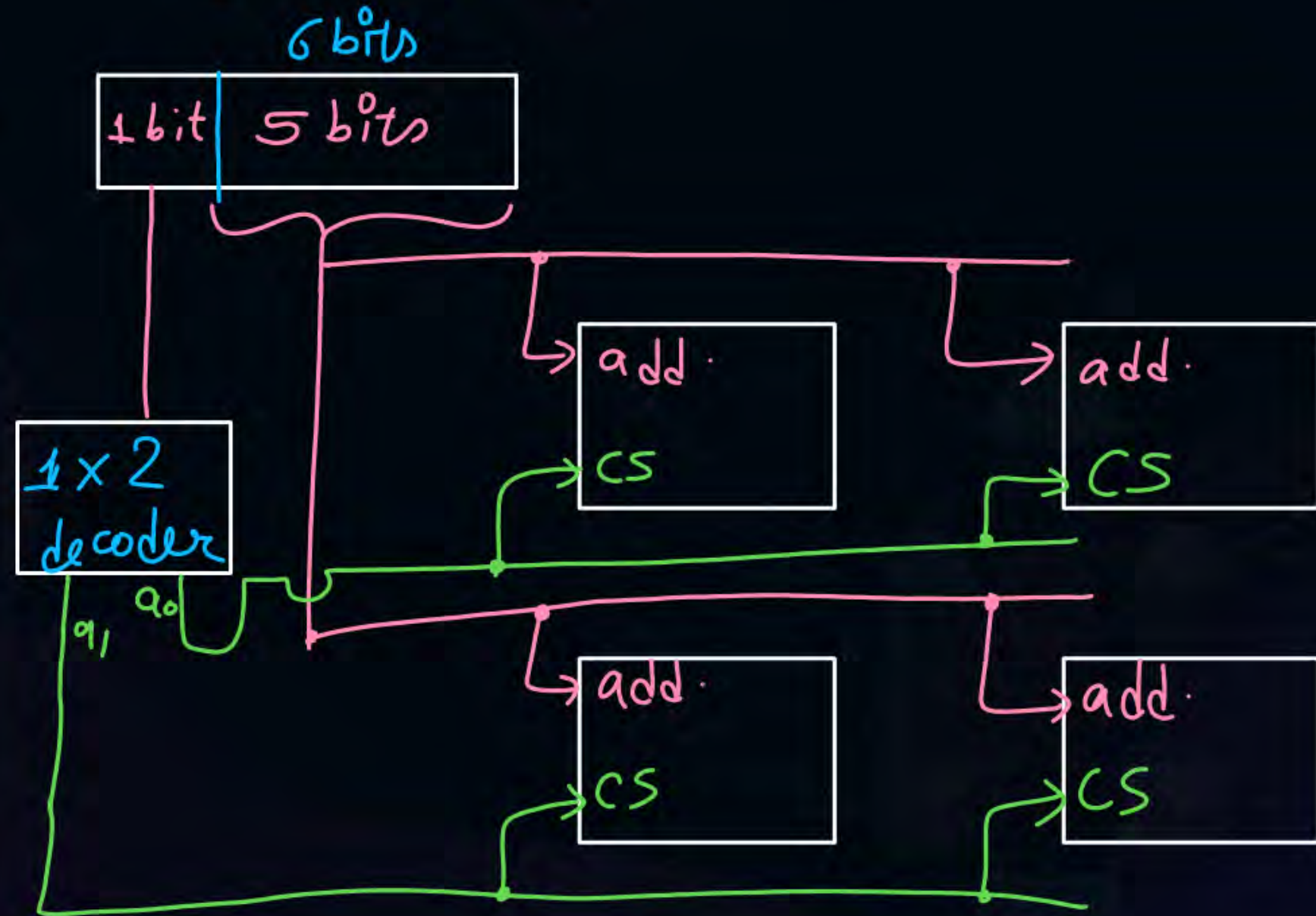


Horizontal arrangement

#Q. How many 32×8 bits RAM chips are needed to provide a memory capacity of 64×16 bits?

$$\frac{2^2 \times 2^2}{32 \times 8} = 4$$

Hybrid arrangement
 ↓
 when no. of addresses
 and data per add. both
 needed more.

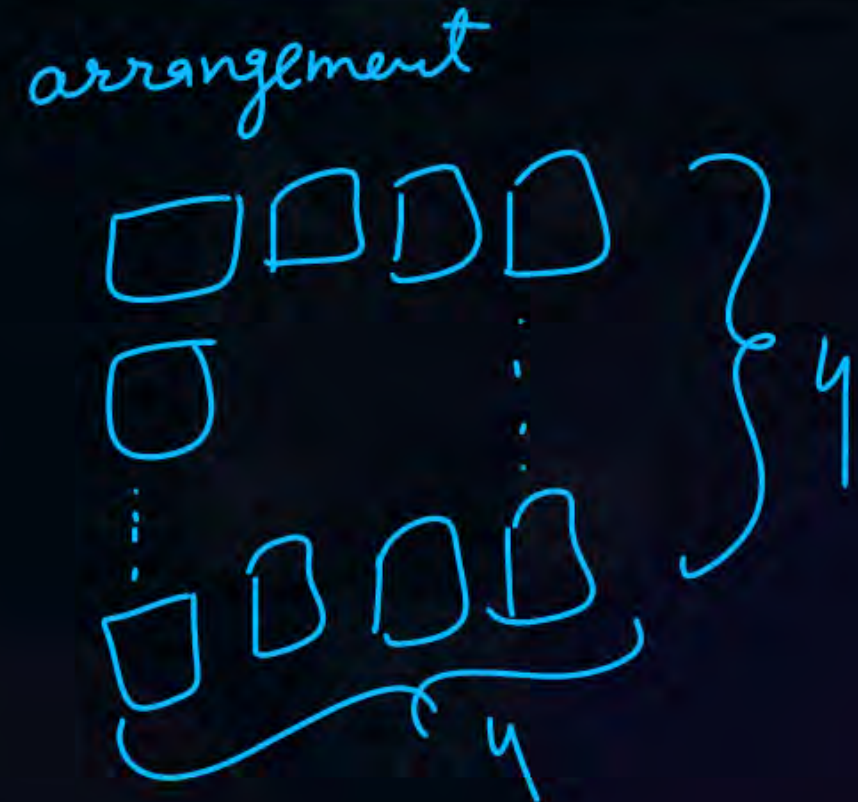


#Q. How many $32K \times 1$ RAM chips are needed to provide a memory capacity of 256K bytes?

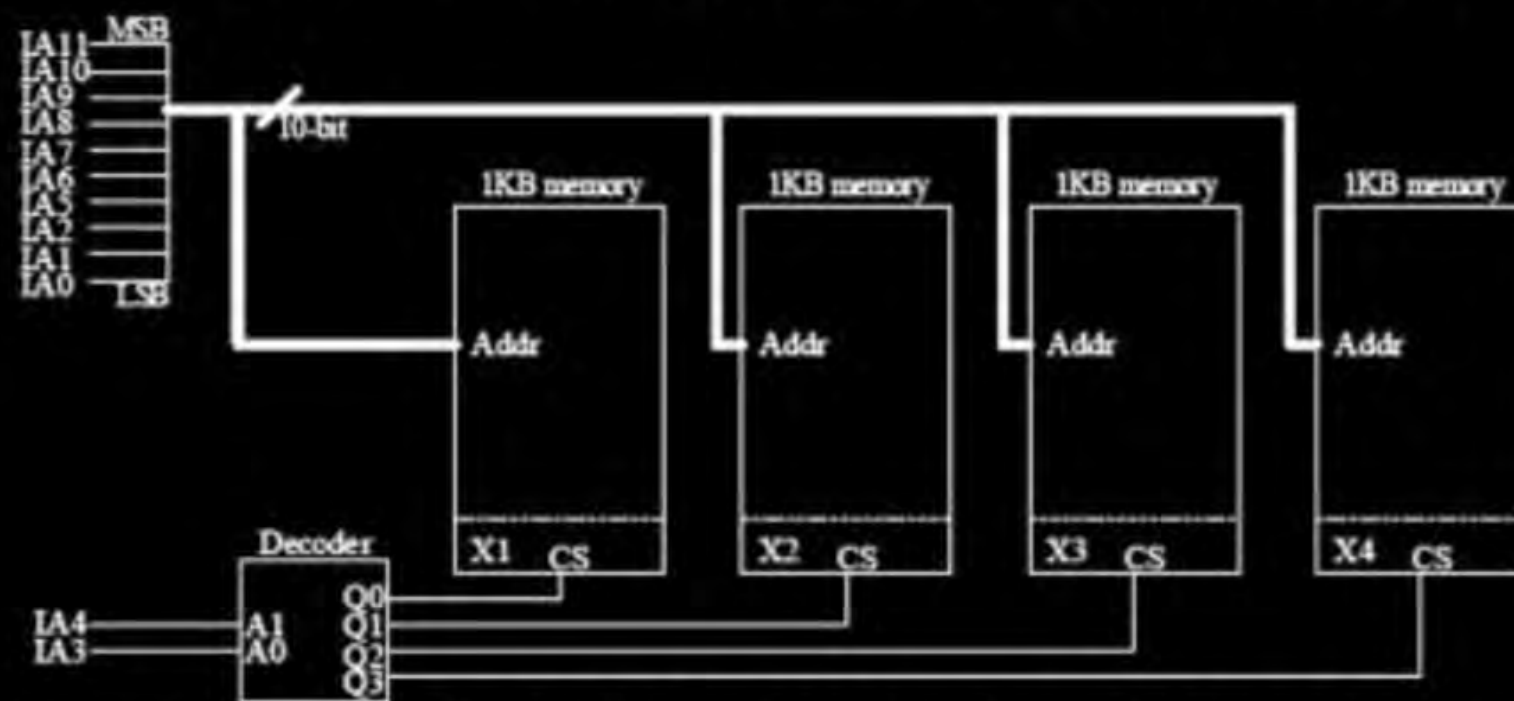
- A** 8
- B** 32
- C** ✓ 64
- D** 128

$$\frac{256K \text{ bytes}}{32K \times 1 \text{ bit}} = 64$$

Default unit of storage
↓
bits



#Q. A 4 kilobyte (KB) byte-addressable memory is realized using four 1 KB memory blocks. Two input address lines (IA4 and IA3) are connected to the chip select (CS) port of these memory blocks through a decoder as shown in the figure. The remaining ten input address lines from IA11-IA0 are connected to the address port of these blocks. The chip select (CS) is active high.

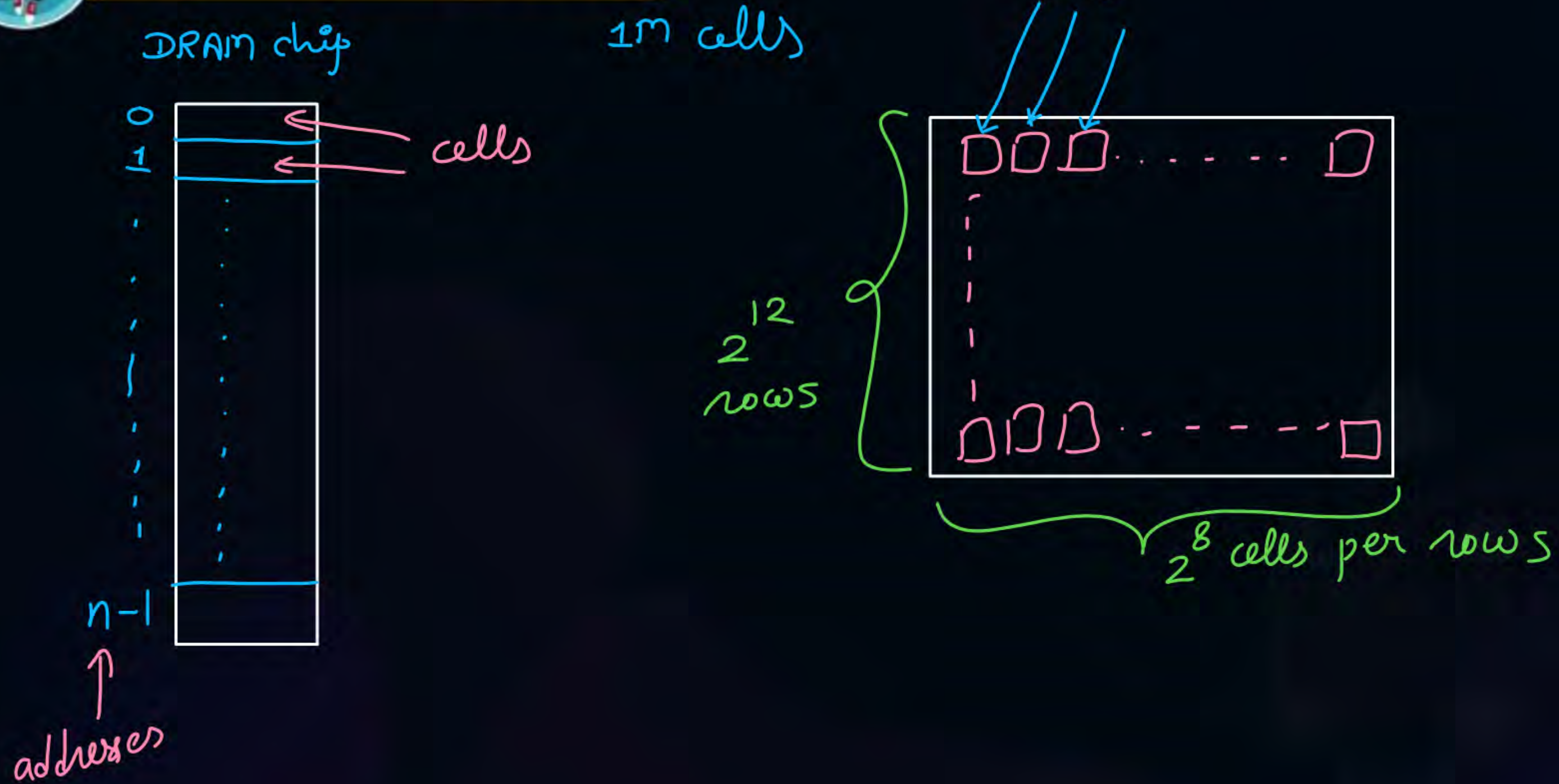


The input memory addresses (IA11-IA0), in decimal, for the starting locations (Addr=0) of each block (indicated as X1, X2, X3, X4 in the figure) are among the options given below. Which one of the following options is CORRECT?

- A** (0, 1, 2, 3)
- B** (0, 1024, 2048, 3072)
- C** (0, 8, 16, 24)
- D** (0, 0, 0, 0)



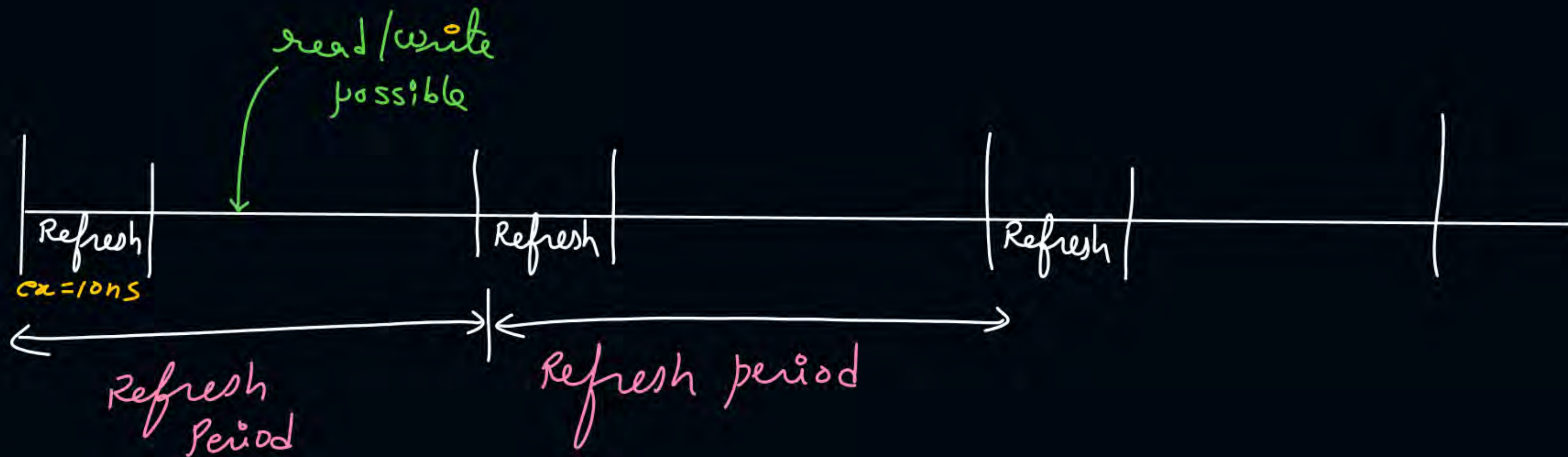
Topic : DRAM Refresh



In one refresh operation, entire row of cells can be refreshed.

1 chip refresh time = no. of rows of cells * 1 refresh operation time

n chips refresh time = _____ || _____



ex:- 100 ns

#Q. Consider a DRAM which can be refreshed in 10ns. The refresh period is 0.05 microseconds. $\Rightarrow 50 \text{ ns}$

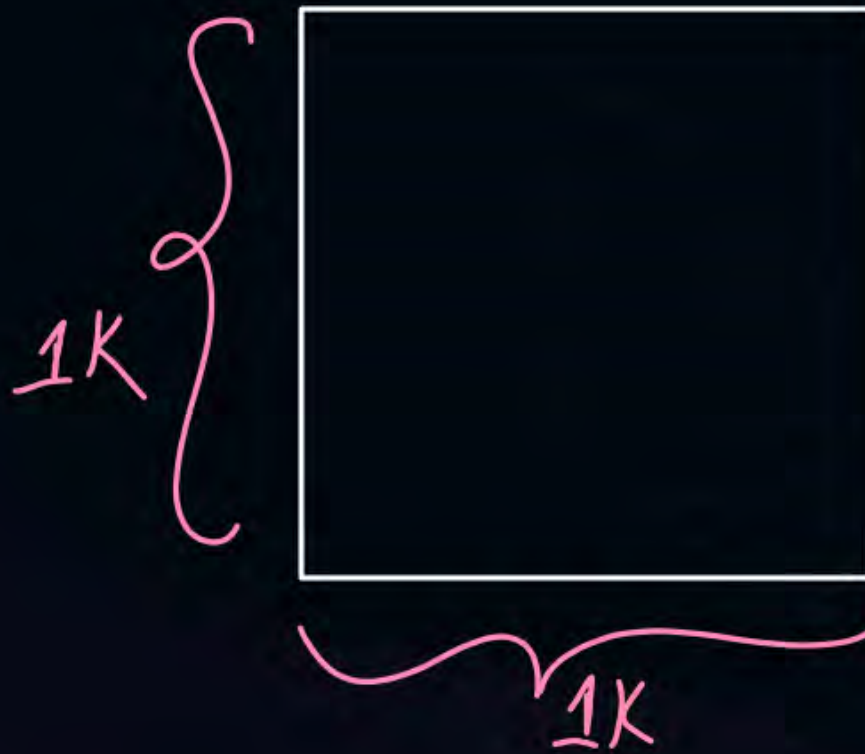
1. % of time taken in refresh? $\frac{10}{50} * 100\% = 20\%$

2. % of time remaining for read write is? $\left(\frac{50-10}{50} \right) * 100\% = 80\%$

#Q. A main memory unit with a capacity of 4 megabytes is built using $1\text{M} \times 1\text{-bit}$ DRAM chips. Each DRAM chip has 1K rows of cells with 1K cells in each row. The time taken for a single refresh operation is 100 nanoseconds. The time required to perform one refresh operation on all the cells in the memory unit is?

each chip has 1M cells

- A** 100 nanoseconds
- B** ✓ 100×2^{10} nanoseconds
- C** 100×2^{20} nanoseconds
- D** 3200×2^{20} nanoseconds

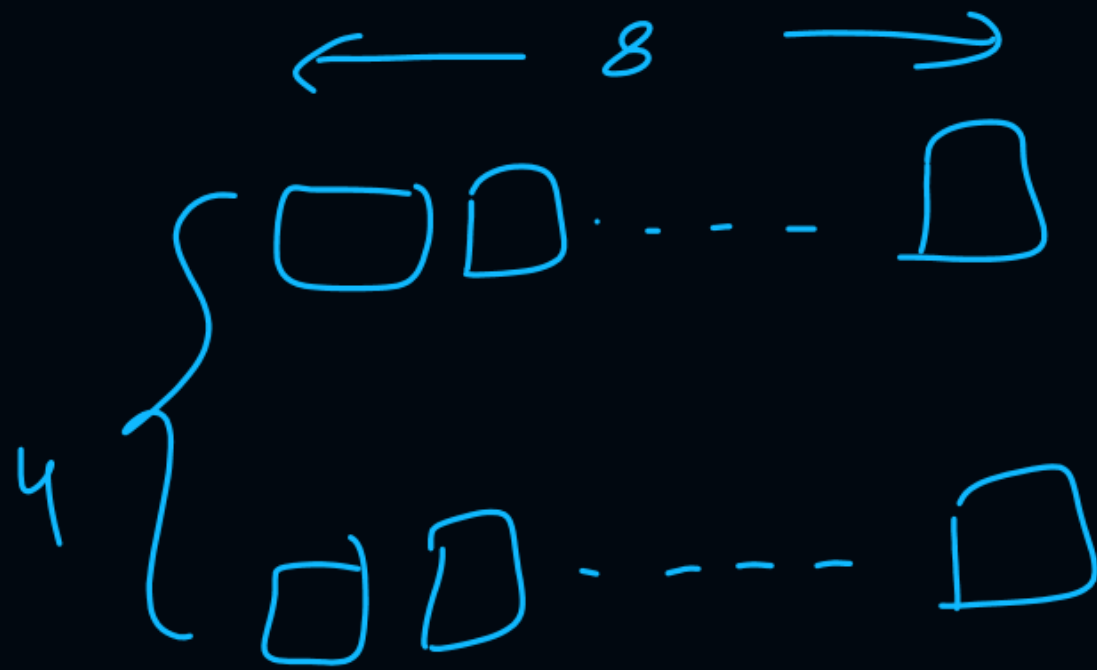


refresh time of
chip
 $= 100 * 1k$

Ques) no. of chips and arrangement of chips in prev. questⁿ?

Solⁿ

$$\frac{4M \times 8 \text{ bits}}{1M \times 1 \text{ bit}} = 32 \text{ chips}$$



#Q. A 32-bit wide main memory unit with a capacity of 1 GB is built using 256M X 4-bit DRAM chips. The number of rows of memory cells in the DRAM chip is 2^{14} . The time taken to perform one refresh operation is 50 nanoseconds. The refresh period is 2 milliseconds. The percentage (rounded to the closet integer) of the time available for performing the memory read/write operations in the main memory unit is _____?

#Q. A DRAM chip of $128K \times 8$ bits has x rows of cells with y cells in each row? If DRAM takes 20ns for 1 refresh and 10240ns for entire chip refresh then the value of $x + y$ is 768?

$$10240\text{ns} = x * 20\text{ns}$$

$$x = 512$$

$$x * y = 128k$$

$$512 * y = 128k$$

$$y = 256$$

$$x + y = 512 + 256$$

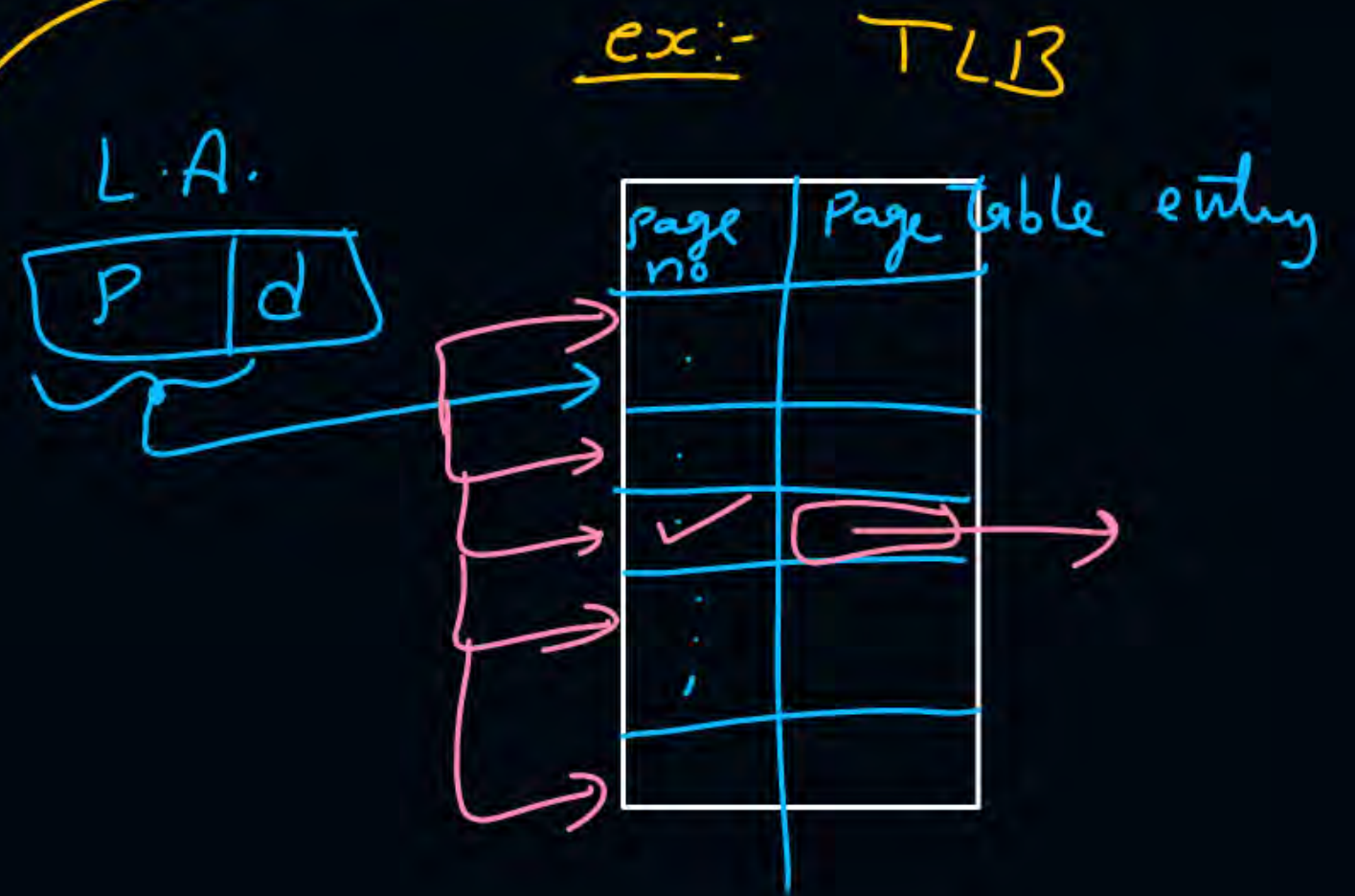
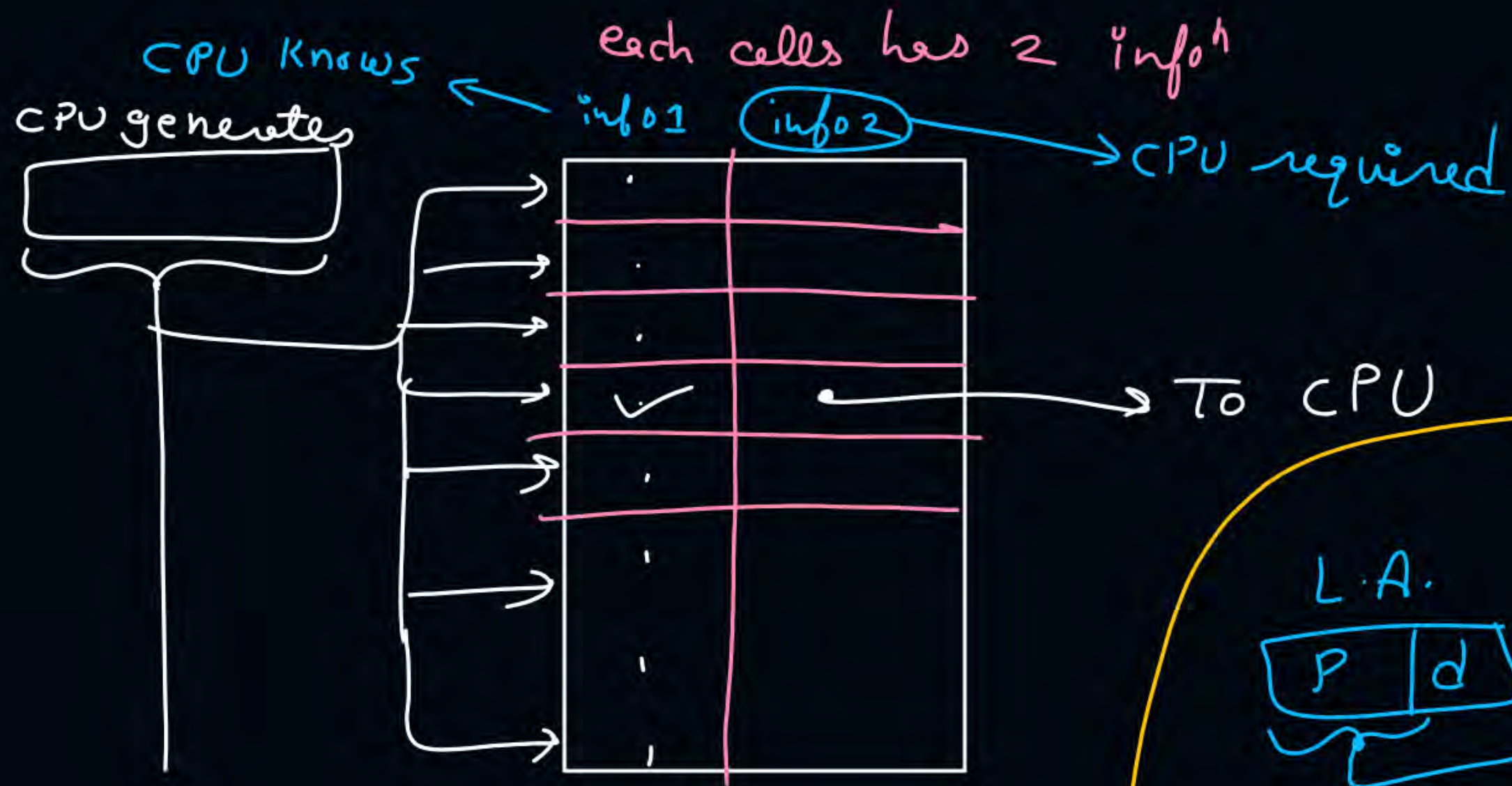
$$= \underline{\underline{768}} \text{ Ans.}$$



Topic : Associative Memory

Known as content addressable memory also

- cells do not have addresses
- searching is done based on content stored in memory.
- comparison is done in parallel
- very-very fast (faster than SRAM)
- very expensive
- used to implement fully associative cache or fully ass. TLB





2 mins Summary



Topic

Multiple Chips in Single Memory System

Topic

DRAM Refresh



Happy Learning

THANK - YOU