CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Basics of COA

Lecture No.- 02

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Recap of Previous Lecture

- **Topic** Architecure vs Organization
- **Topic** Numbers & Data in Computers
- **Topic** Components of Computer
- **Topic** System Buses
- **Topic** Types of Buses

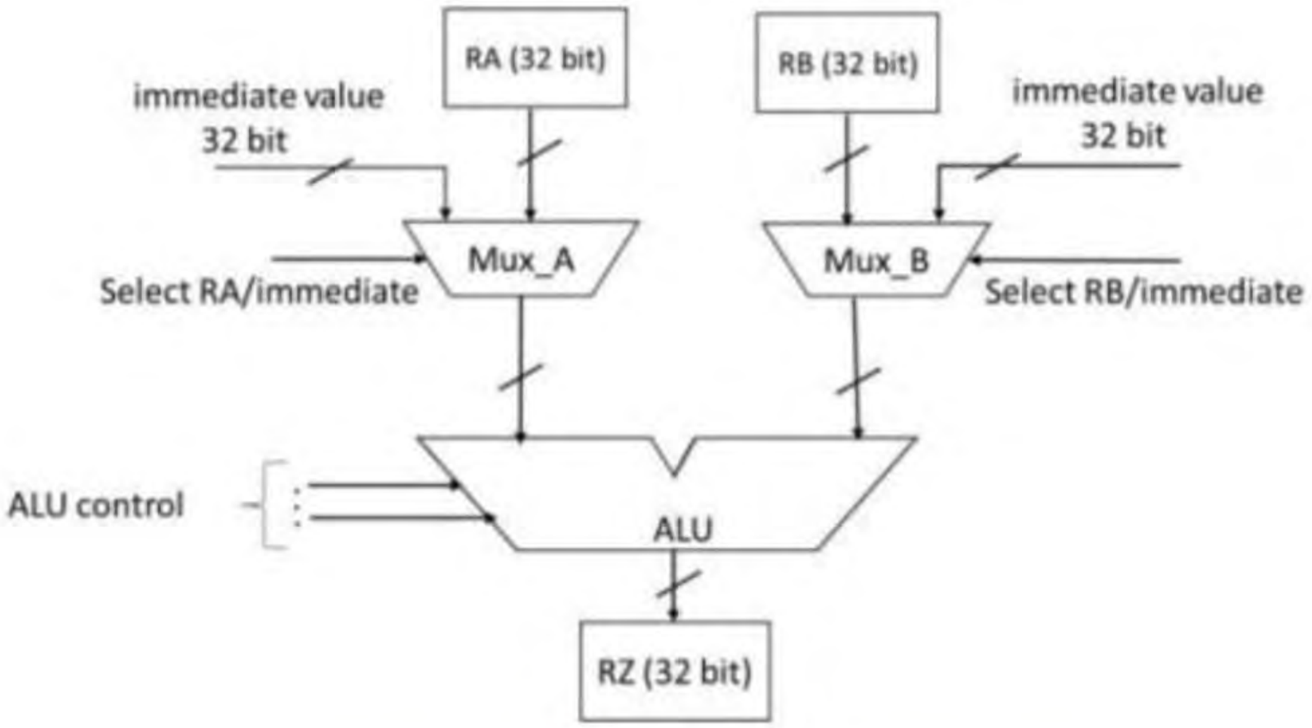
Topics to be Covered

Topic CPU Registers

Topic Memory Access

[MSQ] GATE-2025

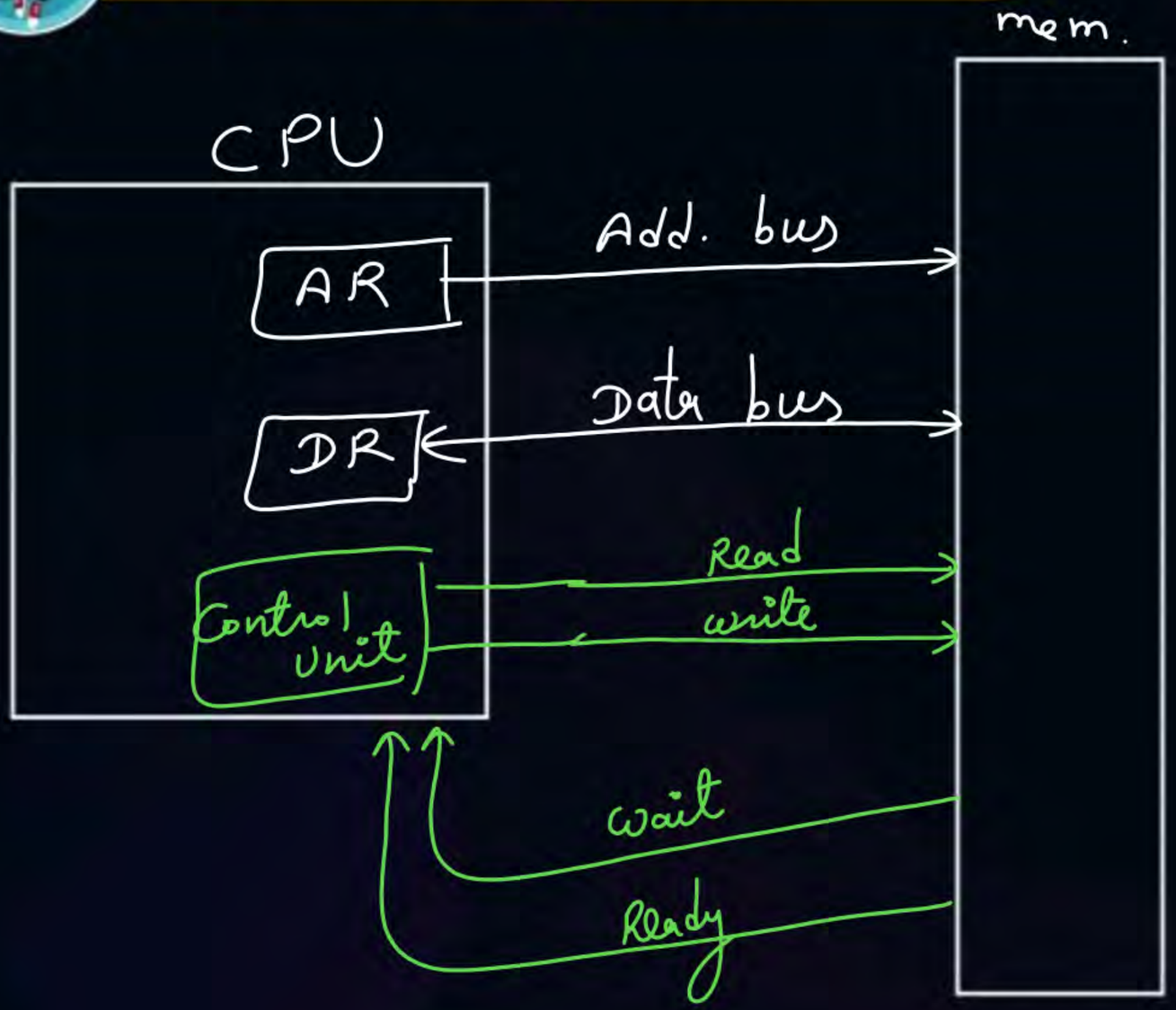
Q.27 A partial data path of a processor is given in the figure, where RA, RB, and RZ are 32-bit registers. Which option(s) is/are CORRECT related to arithmetic operations using the data path as shown?



[MSQ] GATE-2025

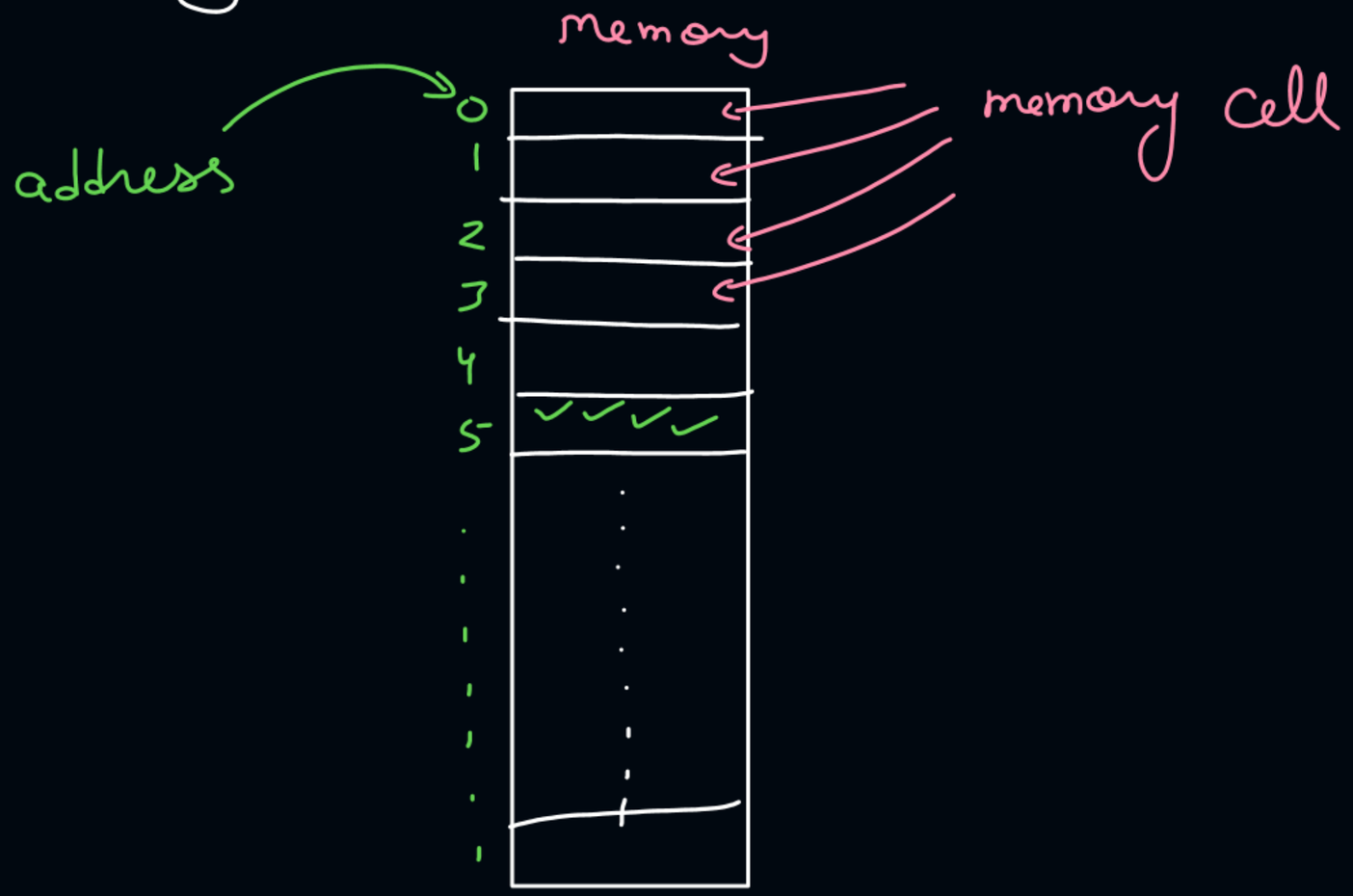
(A)	The data path can implement arithmetic operations involving two registers.
(B)	The data path can implement arithmetic operations involving one register and one immediate value.
(C)	The data path can implement arithmetic operations involving two immediate values.
(D)	The data path can only implement arithmetic operations involving one register and one immediate value.

Topic : Memory Access



when CPU receives enabled ready signal from mem., then only it can initiate read/write operation in memory.

Memory :-



Topic : Memory Operations

- **Memory Read**
  1. CPU sends add. through Add. bus to memory.
  2. CPU sends enabled Read Control signal.
  3. memory performs read on given address and send data to CPU through data bus.
- **Memory Write**
  1. CPU sends add. to mem. through address bus
  2. CPU —"— data —"— data bus
  3. CPU sends enabled write Control signal.
  4. memory performs write of given data on given address.

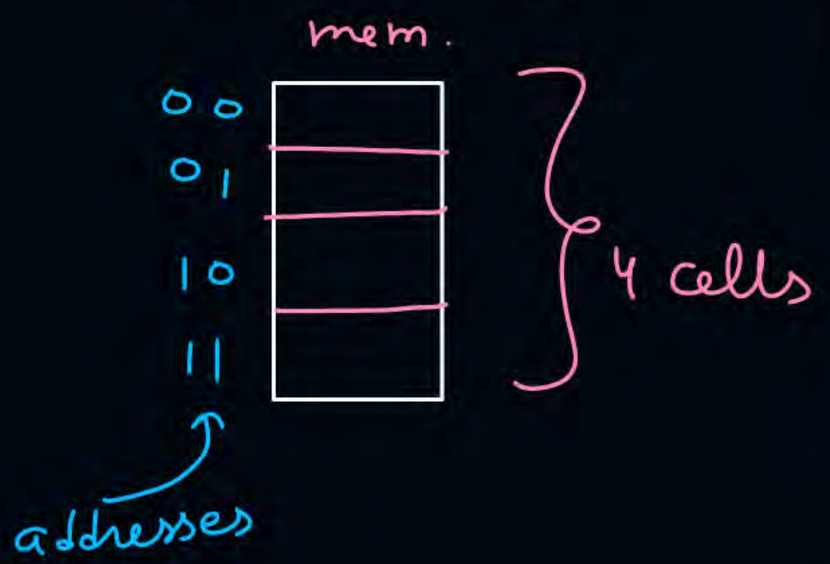
Topic : Example

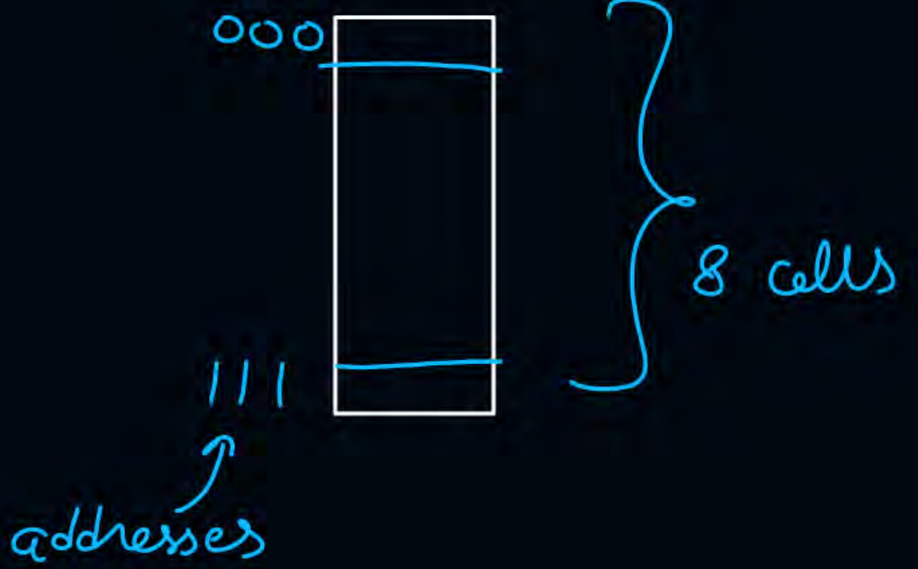
- CPU can perform 1 operation in every 10 nanoseconds
- Memory can perform 1 operation in every 100 nanoseconds

Number of memory operations CPU can perform in 500 nanoseconds?

$$\frac{500}{110ns} \cong 4$$

Memory Addressing :-





no. of cells	4	8	16	32	2^n	x
address length	2-bits	3 bits	4 bits	5 bits	n bits	$\lceil \log_2 x \rceil$ bits

no. of cells	address
$512 = 2^9$	9 bits
$16k = 2^{14}$	14 bits
$4M = 2^{22}$	22 bits
$2G = 2^{31}$	31 bits

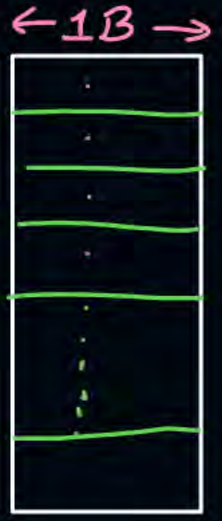
address	no. of cells
18 bits	$2^{18} = 256k$
27 bits	$2^{27} = 128M$

Types of memory :-

(default)

Byte addressable memory

In one cell, one byte stored
or
on one address, one byte stored



word addressable memory

In one cell, one word is stored
or
on one address, one word is stored

Total mem. capacity = no. of cells * 1 cell capacity

esc :-

$= 4 * 1B$

$= 4B$

address	no. of cells	mem. capacity (byte addressable)
16 bits	$2^{16} = 64k$	$64K * 1B = 64KB$
32 bits	$2^{32} = 4G$	$4G * 1B = 4GB$

ex:-

mem. capacity = 8MB

byte addressable

no. of cells = 2^{23}

address = 23 bits

no. of cells = $\frac{8MB}{1B} = 8M$

$= 2^{23}$

$\Downarrow$

add = 23 bits

ex:- mem. capacity = 16GB

mem. word addressable

1 word = 8 bytes

add. = 31 bits

soln

$$\text{no. of cells} = \frac{16\,GB}{8\,B} = 2G = 2^{31}$$

$\Downarrow$

add. = 31 bits

ex:- word addressable mem.

word length = 32 bits = 4B

mem. size = 2GB

add = 29 bits

soln

$$\text{no. of cells} = \frac{2\,GB}{4B} = \frac{2^1 \cdot 2^{30}}{2^2} = 2^{29}$$

$\Downarrow$

add = 29 bits

ex:- word addressable mem.

word size = 64 bits

address = 18 bits

mem. size = ____ Mbytes

Soln no. of cells = 2^{18}

mem. size = $2^{18} * 64$ bits

$= 2^{18} * 8$ bytes

$= 2^{18} * 2^3$ Bytes

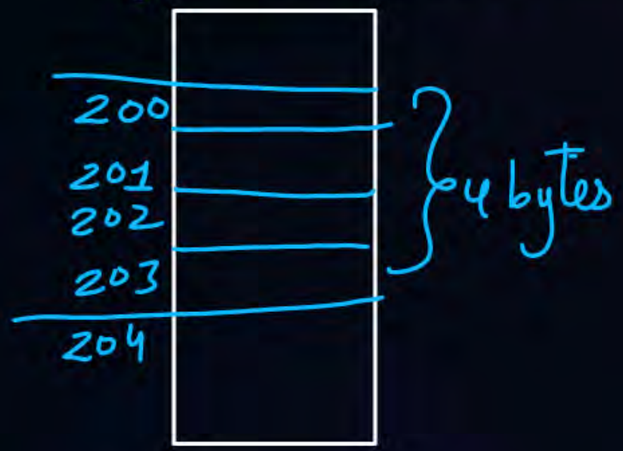
$= 2^{21}$ B = 2MB

Topic : Storing Content in Memory

A content (Instⁿ) of 4 bytes to be stored in memory starting from add = 200.

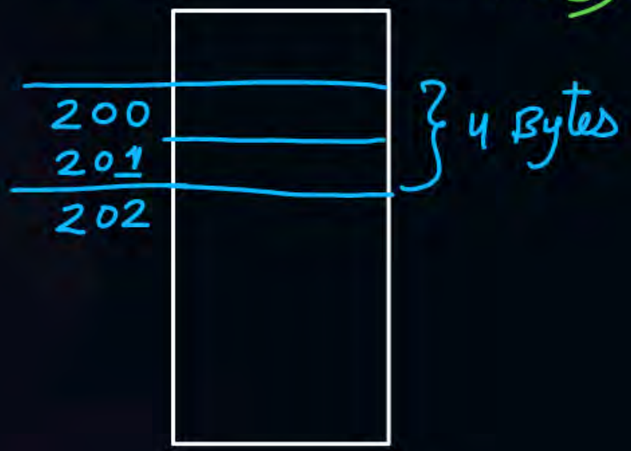
ex :- 1

Byte addressable



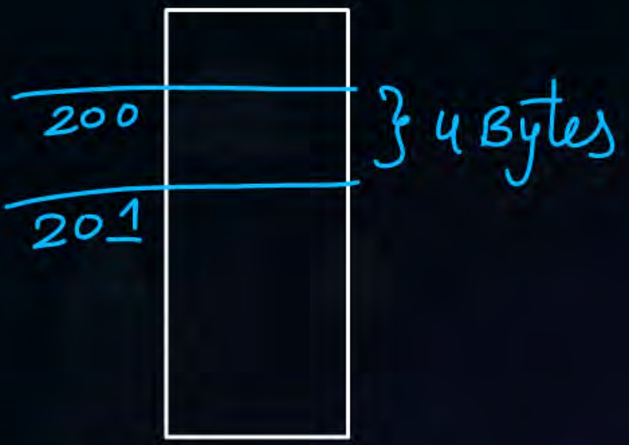
ex :- 2

word addressable (1 word = 2 B)

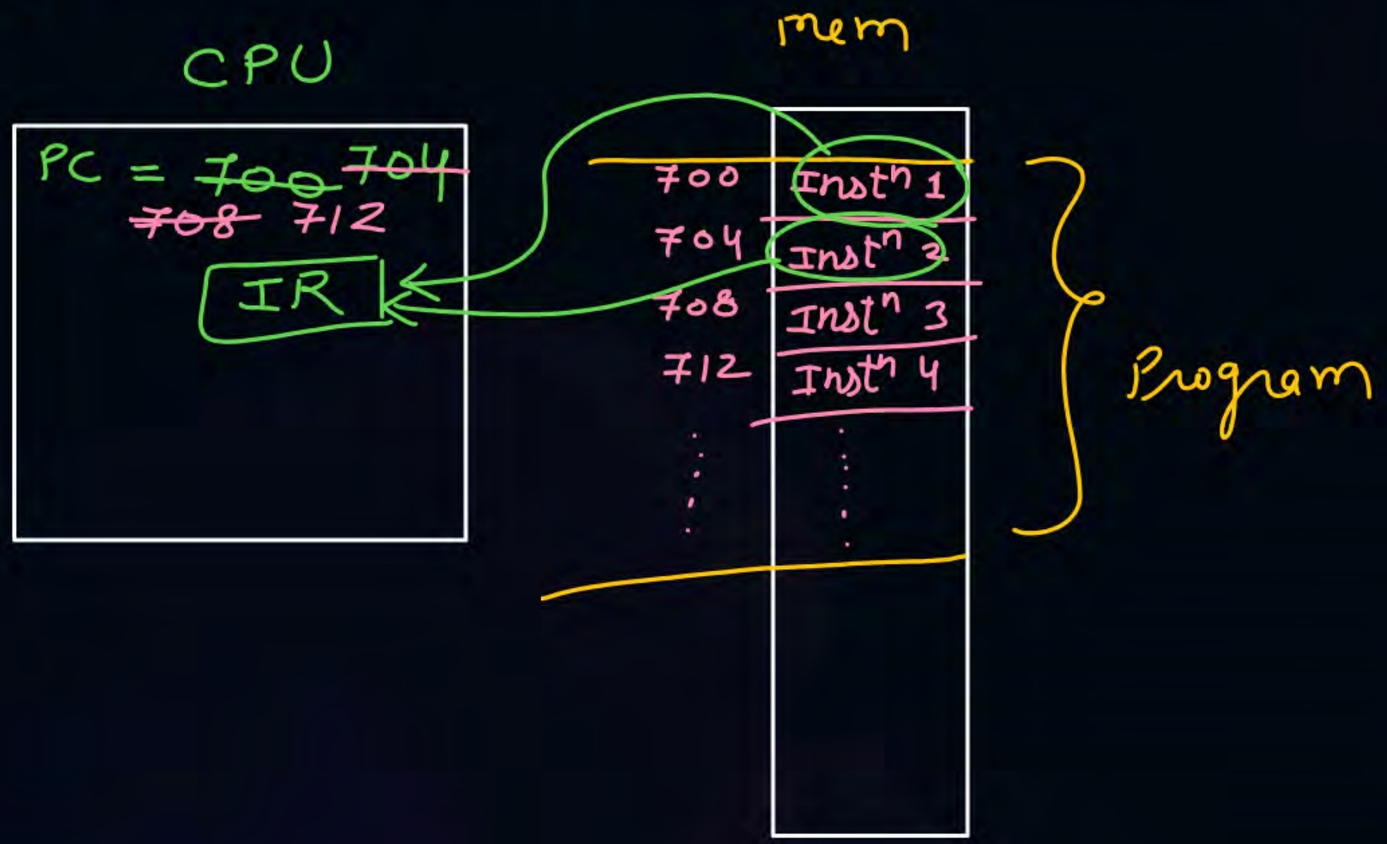


ex :- 3

word addressable (1 word = 4B)



Topic : Storing Content in Memory



[NAT]

(Byte addressable mem.)

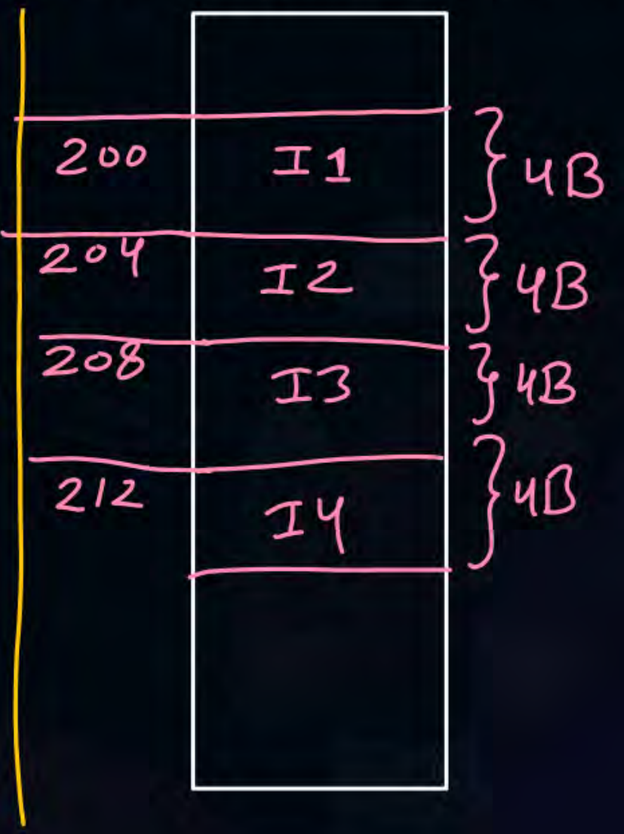
#Q. A CPU has 4 bytes instructions. A program (Instructions I_1 to I_{200}) starts at address 200 (in decimal). Find the address of following instructions:

1. I_1 = 200
2. I_7 = 224
3. I_{110} =

starting add. of $inst^n$ I_n = Base + $(i-1)$ size

= 200 + $(110-1)$ 4

= 636



[NAT]

#Q. A CPU has 4 bytes instructions. A program (Instructions I_1 to I_{200}) starts at address 800 (in decimal). What should be the PC value when instruction I_8 will be executing in CPU?

if I8 is in execution then PC will hold add. of I_9.

Add. of I_9 = 800 + (9-1)4

= 832

[NAT]

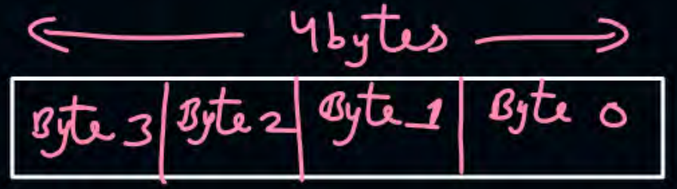
#Q. A CPU has 4 bytes instructions. A program (Instructions I_1 to I_{200}) starts at address 800 (in decimal). What should be the PC value when instruction i will be executing in CPU?

PC = add. of $inst^n$ $(i+1)$ = $800 + 4(i+1-1)$

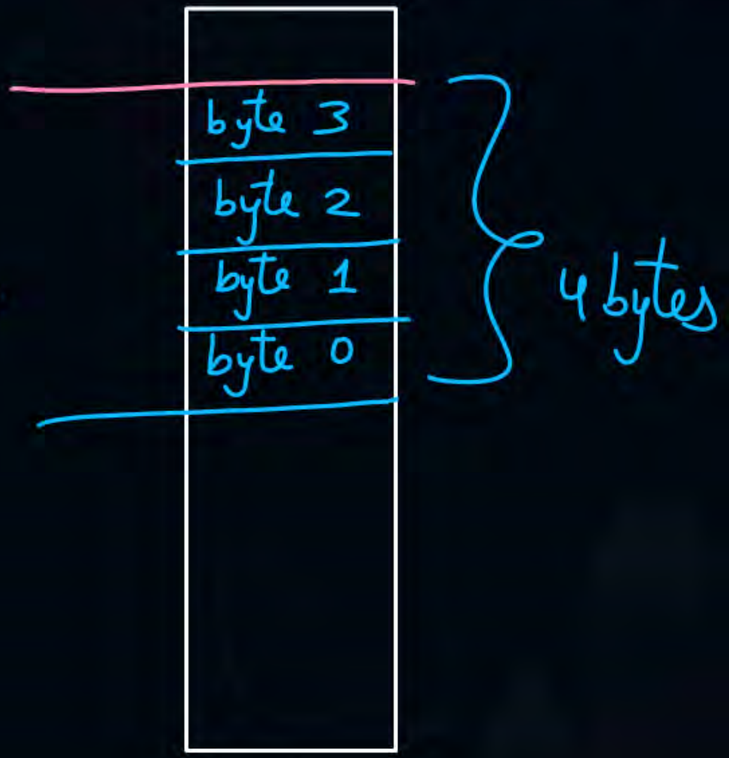
= $800 + 4i$

Topic : Byte Ordering

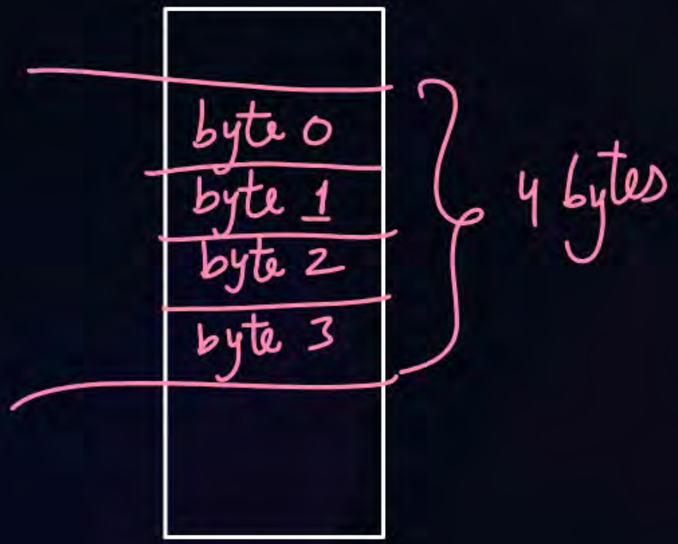
Assume 4B content



big endian →



↓ little endian



Topic : Architecture Type (Based on Size of Input)

max 32 bits

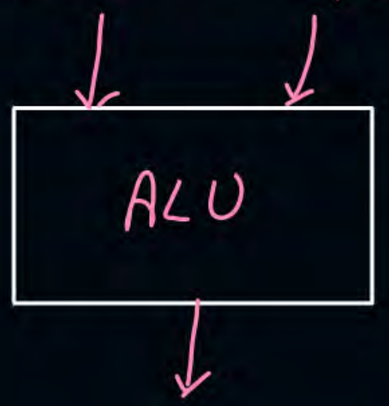
max 32-bits

32 - bits architecture

CPU word = 32 bits

= 4B

64 bits 64 bits



64-bits architecture

CPU word = 64 bits

= 8 Bytes

2 mins Summary

Topic CPU Registers

Topic Memory Access

Happy Learning

THANK - YOU