CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

CPU & Control Unit

Lecture No.- 01

By- Vishvadeep Gothi sir

Recap of Previous Lecture

Topic Addressing Modes

Topic Types of Addressing Modes

Topics to be Covered

Topic CPU

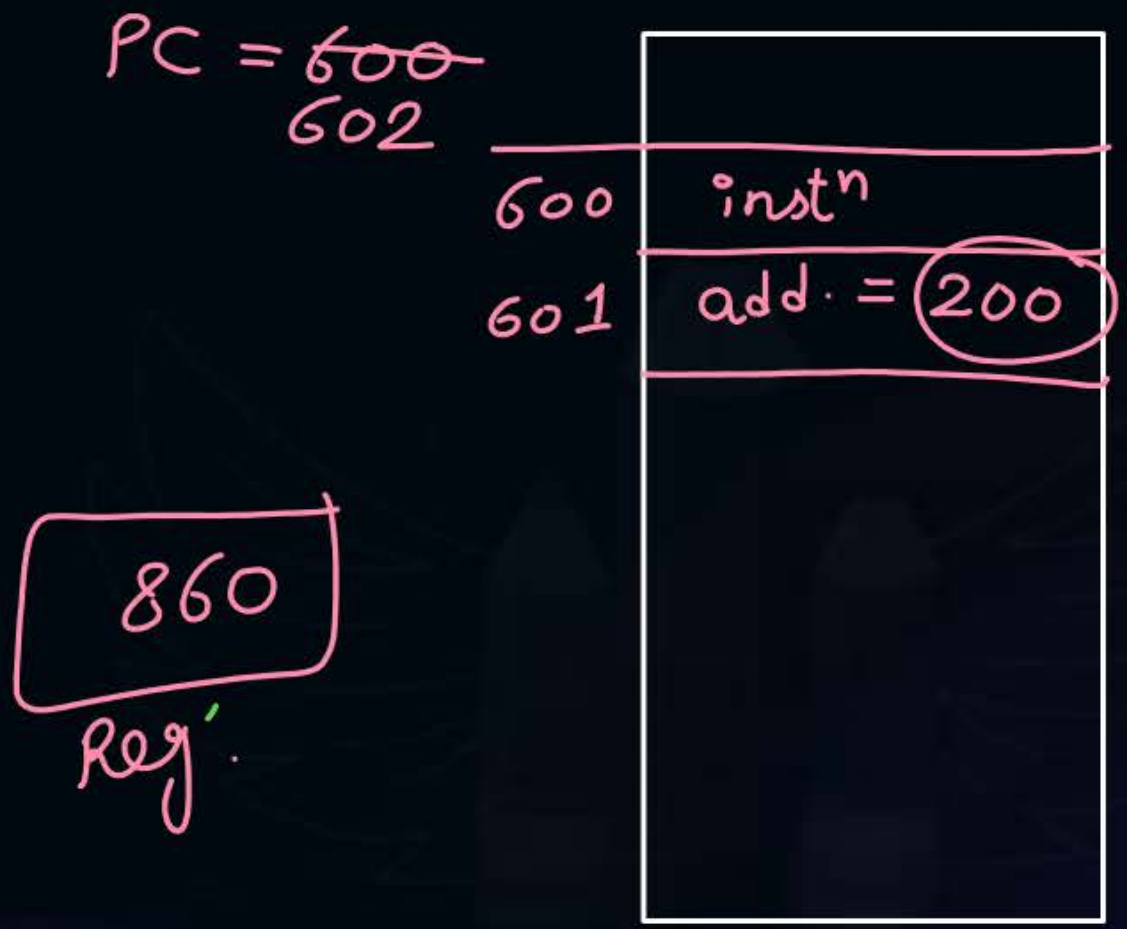
Topic CPU Cycle

Topic CPI

Question

#Q. An instruction is stored at Location 600 with its address field at location 601. The address field has the value 200. A processor register contains the number 860. Evaluate the effective address, if addressing mode is:

1. Direct ⇒ 200
2. PC-Relative ⇒ 602 + 200 = 802
3. Immediate 601
4. Register Indirect 860



[MCQ]

#Q. In case the code is position independent, the most suitable addressing mode is

A Direct mode

B Indirect mode

[✓ C Relative mode]

D Indexed mode

[MCQ]

#Q. The addressing mode that permits relocation, without any change whatsoever in the code, is

A Indirect addressing

B [✓ Base register addressing]

C Indexed addressing

D [✓ PC relative addressing]

[NAT]

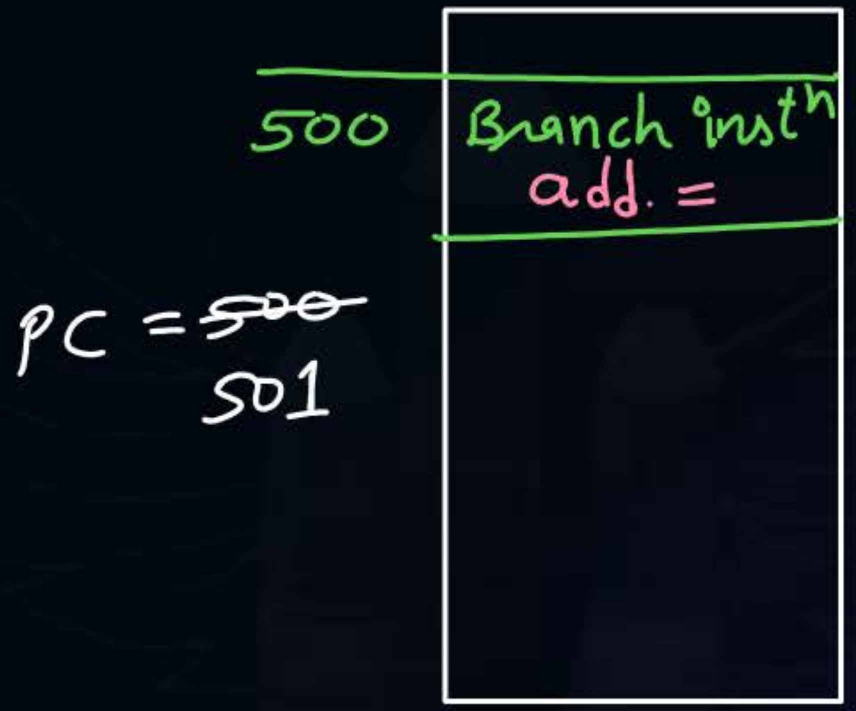
#Q. A relative branch mode type instruction is stored in memory at address 500. The branch is made to an address 700.

1. What should be the value of relative address field of the instruction? ⇒ 199
2. Determine the value of PC before instruction fetch, after the fetch and after execution phase? 500, 501, 700

$$\text{Target add.} = 700 = PC + \text{offset}$$

$$700 = 501 + \text{offset}$$

$$\text{offset} = 199$$



	PC
Before fetch	500
after fetch	501
after Execution	700

[NAT]

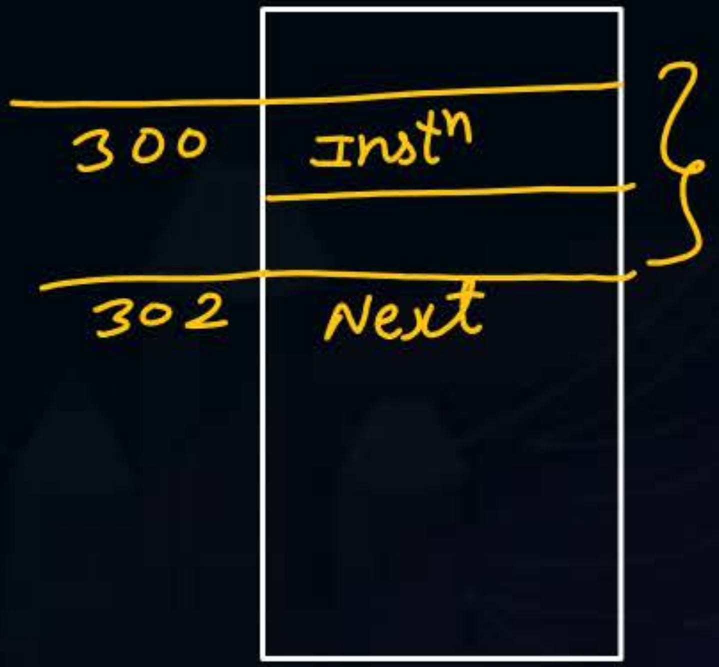
Ans = -102

#Q. A relative branch mode type instruction is stored in memory at address 300. The branch is made to an address 200. If each instruction is stored on 2 addresses in memory, then what should be the value of relative address field of the instruction?

$$200 = PC + \text{offset}$$

$$200 = 302 + \text{offset}$$

$$\text{offset} = -102$$



[NAT]

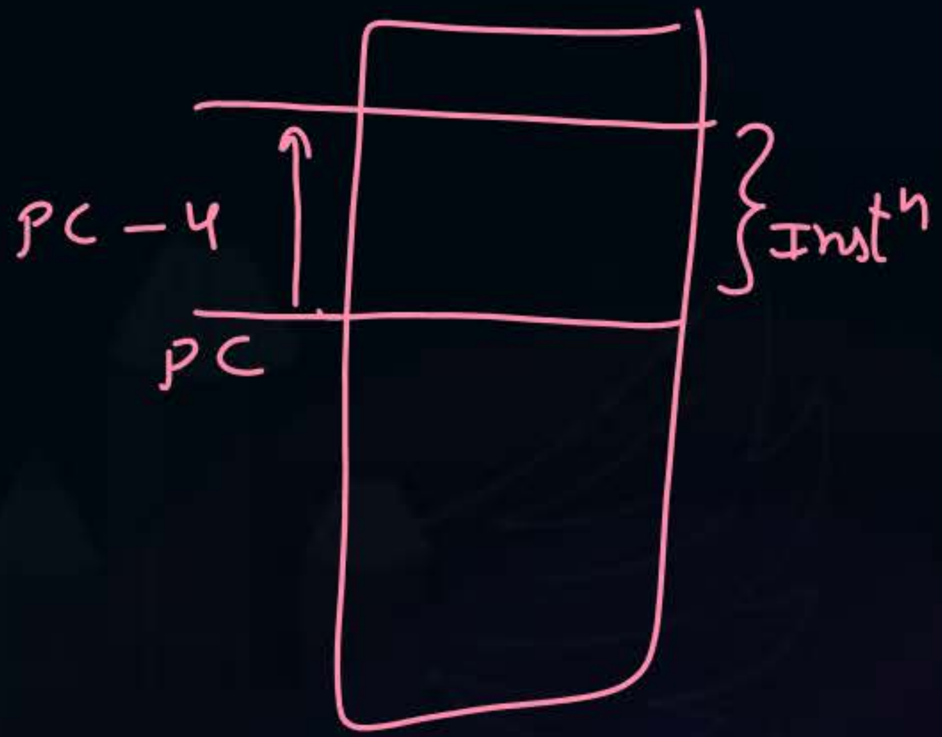
Ans = 896

#Q. A relative branch mode type instruction takes jump to an address 800. If each instruction is stored on 4 addresses in memory and offset in the instruction is -100 then the starting address of the instruction in memory is ______?

$\text{Target} = 800 = PC + \text{offset}$

$800 = PC + (-100)$

$PC = 900$



Address of instⁿ = 900 − 4
= 896

[MCQ]

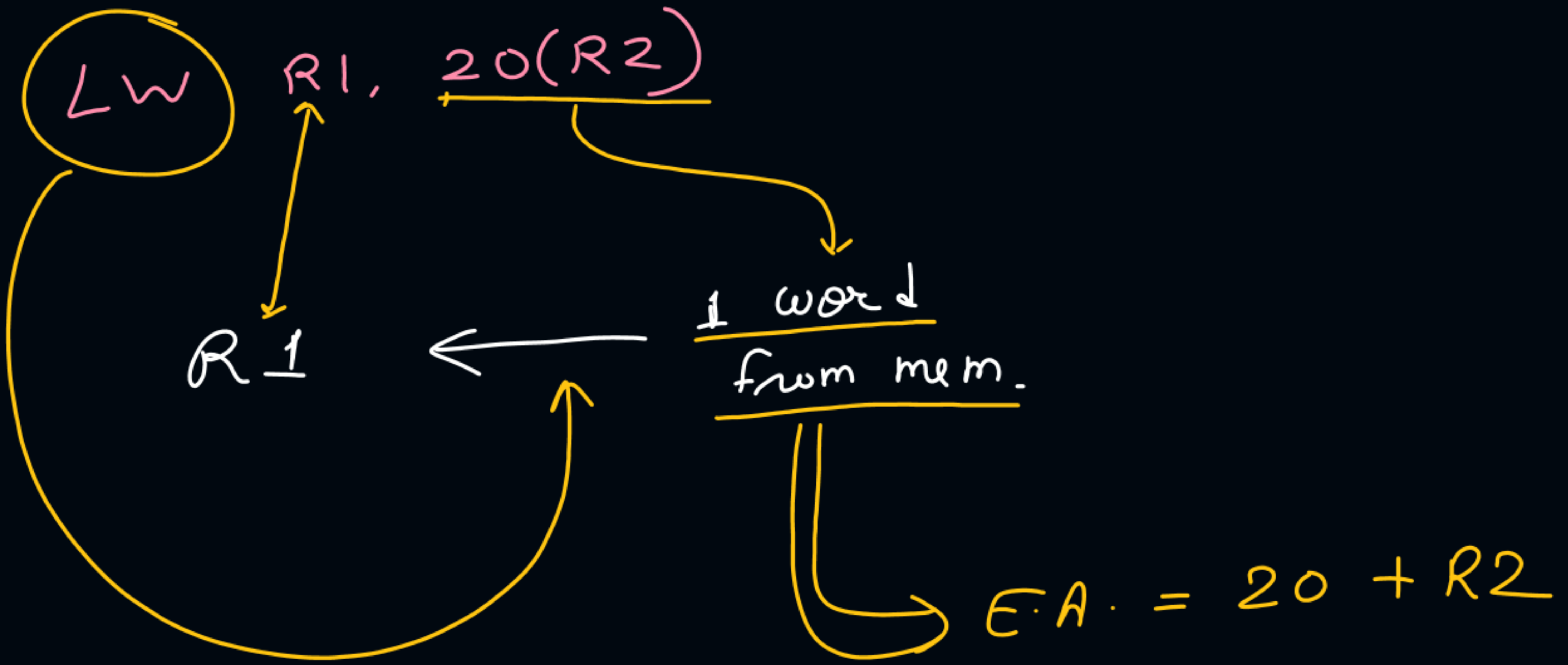
#Q. Consider a hypothetical processor with an instruction of type LW R1, 20(R2); which during execution reads a 32-bit word from memory and stores it in a 32-bit register R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Which of the following best reflects the addressing mode implemented by this instruction for operand in memory?

A Immediate Addressing

B Register Addressing

C Register indirect scaled addressing

[✓ D] Base indexed addressing



LW R1, 20(R2)

R1

1 word from mem.

E.A. = 20 + R2

[NAT]

Ans = 4

#Q. Consider a three-word machine instruction

ADD A[R0], @B

The first operand (destination) “A[R0]” uses indexed addressing mode with R0 as the index register. The second operand (Source) “@B” uses indirect addressing mode. A and B are memory addresses residing at the second and the third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).

The number of memory cycles needed during the execution cycle of the instruction is__4__.

ADD A[R0] , @B

A[R0] → Indexed mode

@B → Indirect mode

A = Base add.

R0 = Index Reg.

3 – word

opcode	Index Reg.	mode 1	mode 2	A	B

	first operand	2nd operand
decode	–	–
E.A. calculat^n &operand fetch	1	2
Execution	–	–
write back	1	–
Total	4	

[NAT]

H.W.

#Q. Consider a 6-words instruction, which is of the following type:

Opcode	Mode1	Mode2	Address1	Address2

The first operand (destination) uses register indirect mode and second operand uses indirect mode. Assume each operand is of size 2 words, each address is of 2 words and main memory takes 50ns for 1 byte access. Further assume that the opcode denotes addition operation which copies result of addition of 2 operands. One word size is 4 bytes. Total memory access time required in:

1. Fetch cycle of instruction
2. Execution cycle of instruction
3. Instruction cycle of instruction

[NAT]

H.W.

#Q. Consider a 6-words instruction, which is of the following type:

Opcode	Mode1	Mode2	Address1	Address2

The first operand (destination) uses direct mode and second operand uses indexed mode. Assume each operand is of size 4 words, each address is of 2 words and main memory takes 100ns for 1 byte access. Further assume that the opcode denotes addition operation which copies result of addition of 2 operands to destination. One word size is 4 bytes. The instruction decode takes 20 nanoseconds and each ALU operation takes 10 nanoseconds. Total time needed to execute the instruction is ______?

[NAT] GATE- 2015 set -2

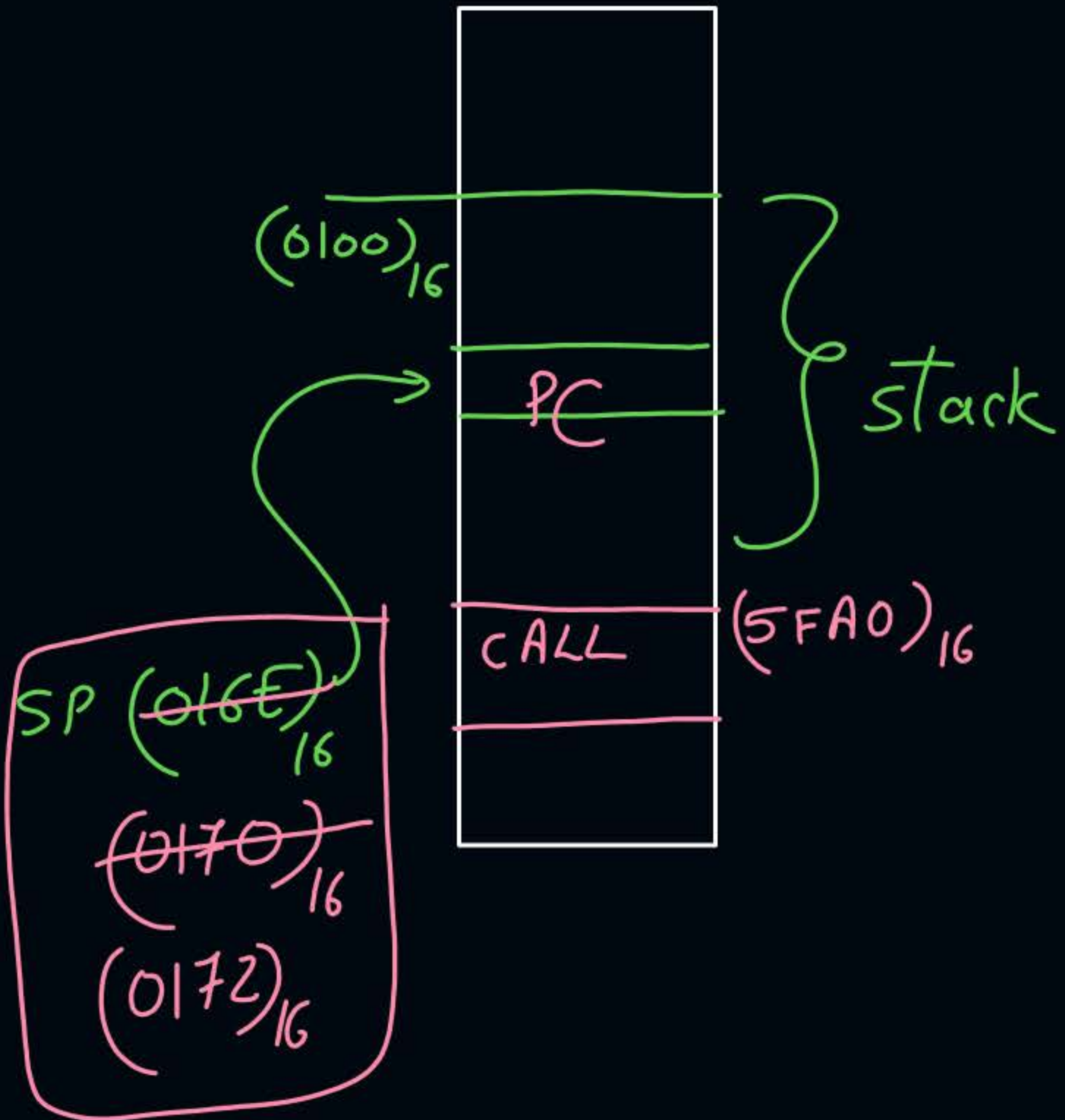
#Q. Consider a processor with byte-addressable memory. Assume that all registers, including program counter (PC) and Program Status Word (PSW), are size of two bytes. A stack in the main memory is implemented from memory location $(0100)_{16}$ and it grows upward. The stack pointer (SP) points to the top element of the stack. The current value of SP is $(016E)_{16}$. The CALL instruction is of two words, the first word is the op-code and the second word is the starting address of the subroutine (one word = 2 bytes). The CALL instruction is implemented as follows:

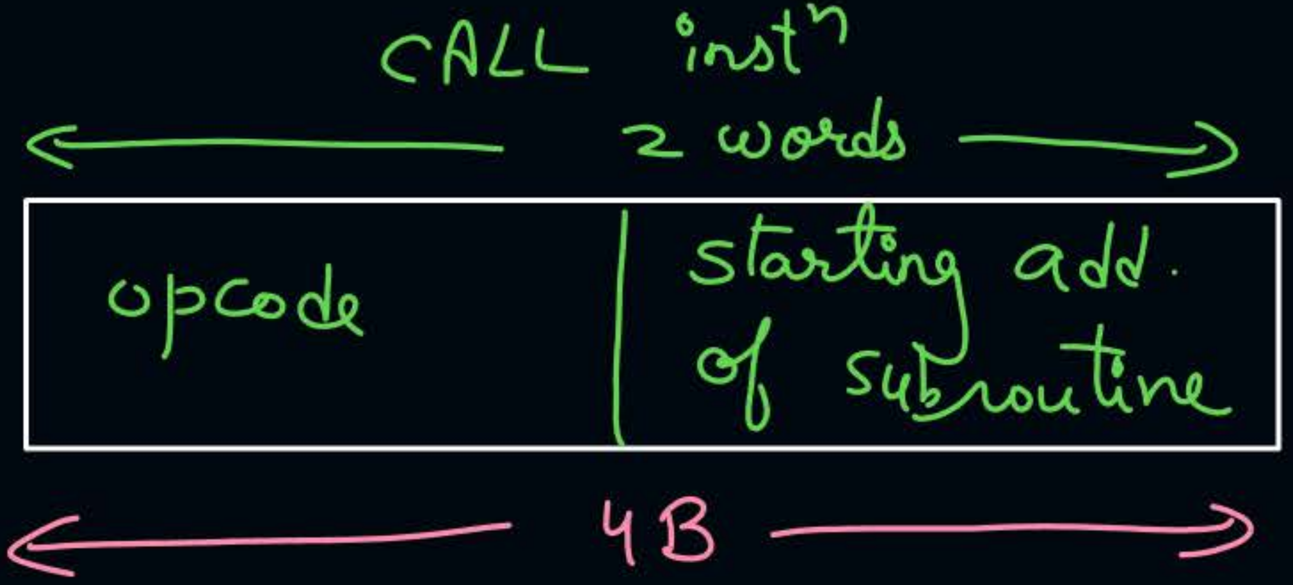
- Store the current value of PC in the stack
- Store the value of PSW register in the stack
- Load the starting address of the subroutine in PC

The content of PC just before the fetch of a CALL instruction is $(5FA0)_{16}$. After execution of the CALL instruction, the value of the stack pointer is:

(A) $(016A)_{16}$ (B) $(016C)_{16}$ (C) $(0170)_{16}$ [✓ (D) $(0172)_{16}$]

Reg ⇒ 2 Bytes


(0100)16
PC
stack
CALL
(5FA0)16
SP ~~(016E)16~~
~~(0170)16~~
(0172)16


CALL instⁿ
2 words
opcode
starting add. of subroutine
4B

Ques) from prev. quest^n,

	value of PC
before fetch	$(5FA0)_{16}$
after fetch	$(5FA4)_{16}$
after execut^n of CALL	starting add. of subroutine

Topic : CPU

1. CPU Cycle → Time in which CPU performs one smallest operation.

2. CPU Clock rate $= \frac{1}{\text{CPU cycle time}}$

3. CPI (cycles per Inst^n) :- no. of CPU cycles needed to execute an inst^n.

4. Execution Time

1 Inst^n execution time $= CPI_{avg} * \text{cycle time}$

n inst^{ns} —— 〃 —— $= n * CPI_{avg} * \text{cycle time}$

or

$$= \frac{n * CPI_{avg}}{\text{clock rate}}$$

Topic : Average CPI

Consider computing the overall CPI for a machine A for which the following performance measures were recorded when executing a set of benchmark programs. Assume that the clock rate of the CPU is 200 MHz

Instruction Category	Number of Instructions	No. of cycles per Instruction	Total
ALU	48	1	48*1 = 48
Load & Store	10	3	10*3 = 30
Branch	39	4	39*4 = 156
Other	3	5	3*15 = 15

Total = 100 instns

Total = 249

$$CPI = \frac{249}{100}$$

$$= 2.49$$

Topic : MIPS

↓
million Inst^{ns} Per second

In t time no. of inst^{ns} executed = n

In 1 —— " ———— $= \dfrac{n}{t}$

$$= \frac{\cancel{n} * \text{clock rate}}{\cancel{n} * CPI}$$

$$= \frac{\text{clock rate}}{CPI}$$

$$\boxed{MIPS = \frac{\text{clock rate}}{CPI * 10^6}}$$

MIPS for prev. example $= \dfrac{200\ \cancel{M}Hz}{2.49 * \cancel{10^6}}$

$= 80.32$ MIPS

[NAT] $Ans = 3.0$ [2025 : 2M]

#Q. An application executes 6.4×10^8 number of instructions in 6.3 seconds. There are four types of instructions, the details of which are given in the table. The duration of a clock cycle in nanoseconds is 3.0. (rounded off to one decimal place)

Instruction type	Clock cycles required per instruction (CPI)	Number of instruction of instructions executed	Total cycles
Branch	2	2.25×10^8	$4.5 * 10^8$
Load	5	1.20×10^8	$6.0 * 10^8$
Store	4	1.65×10^8	$6.60 * 10^8$
Arithmetic	3	1.30×10^8	$3.9 * 10^8$
			$21.0 * 10^8$

$$CPI = \frac{21.0 * \cancel{10^8}}{6.4 * \cancel{10^8}} = \frac{21.0}{6.4}$$

$$\text{execution time} = n * \text{CPI}_{\text{avg}} * \text{cycle time}$$

$$6.3 \text{ seconds} = \cancel{6.4} * 10^{8} * \frac{21.0}{\cancel{6.4}} * \text{cycle time}$$

$$\text{cycle time} = \frac{6.3 \text{ seconds}}{21 * 10^{8}}$$

$$= 0.3 * 10^{-8} \text{ sec.}$$

$$= 0.3 * \frac{10}{10} * 10^{-8} \text{ sec}$$

$$= 3.0 * 10^{-9} \text{ sec}$$

$$= 3.0 \text{ ns}$$

[NAT]

← Prog. + data

#Q. Consider two processors P1 and P2 executing the same instruction set. Assume that under identical conditions, for the same input, a program running on P2 takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on P1. If the clock frequency of P1 is 1GHz, then the clock frequency of P2 (in GHz) is ________?

	P1	P2
Execution time	t_1	$t_2 = 0.75t_1$
CPI	c_1	$c_2 = 1.2c_1$
freq.	$f_1 = 1\text{GHz}$	$f_2 = —$?
no. of instrs	n_1	n_2

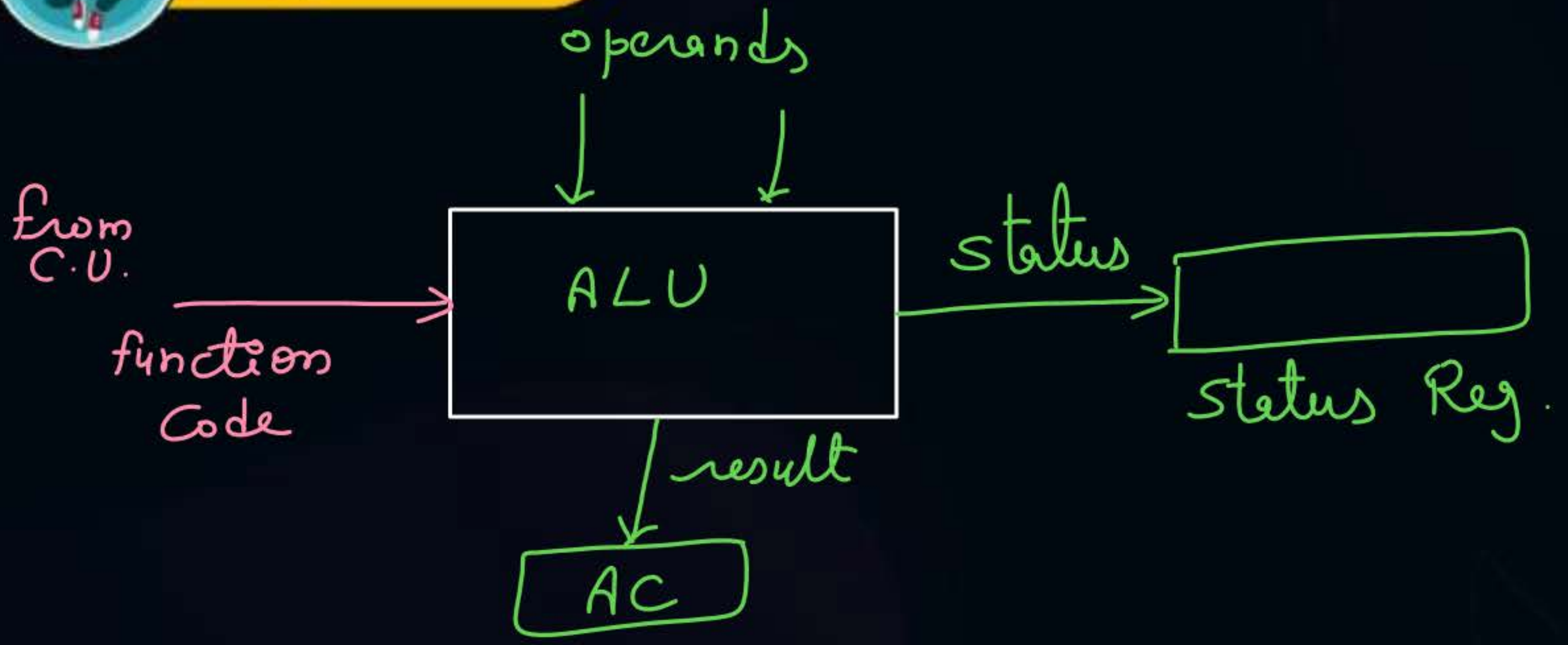
$$n_1 = n_2$$

$$\frac{t_1 * f_1}{c_1} = \frac{t_2 * f_2}{c_2}$$

$$\frac{\cancel{t_1} * 1\text{GHz}}{\cancel{c_1}} = \frac{0.75\cancel{t_1} * f_2}{1.2\cancel{c_1}}$$

$$f_2 = 1.6\text{ GHz}$$

Topic : ALU



operands
from C.U.
function Code
ALU
status
Status Reg.
result
AC

GATE WALLAH

JOIN MY TELEGRAM

VISHVADEEP SIR PW

☑ Exam notification & updates

☑ Class Notifications

☑ Weekly Live Doubt Session

☑ Important PYQS

☑ Polls & Quiz

2 mins Summary

Topic CPU

Topic CPU Cycle

Topic CPI

Happy Learning

THANK - YOU