Microprocessor

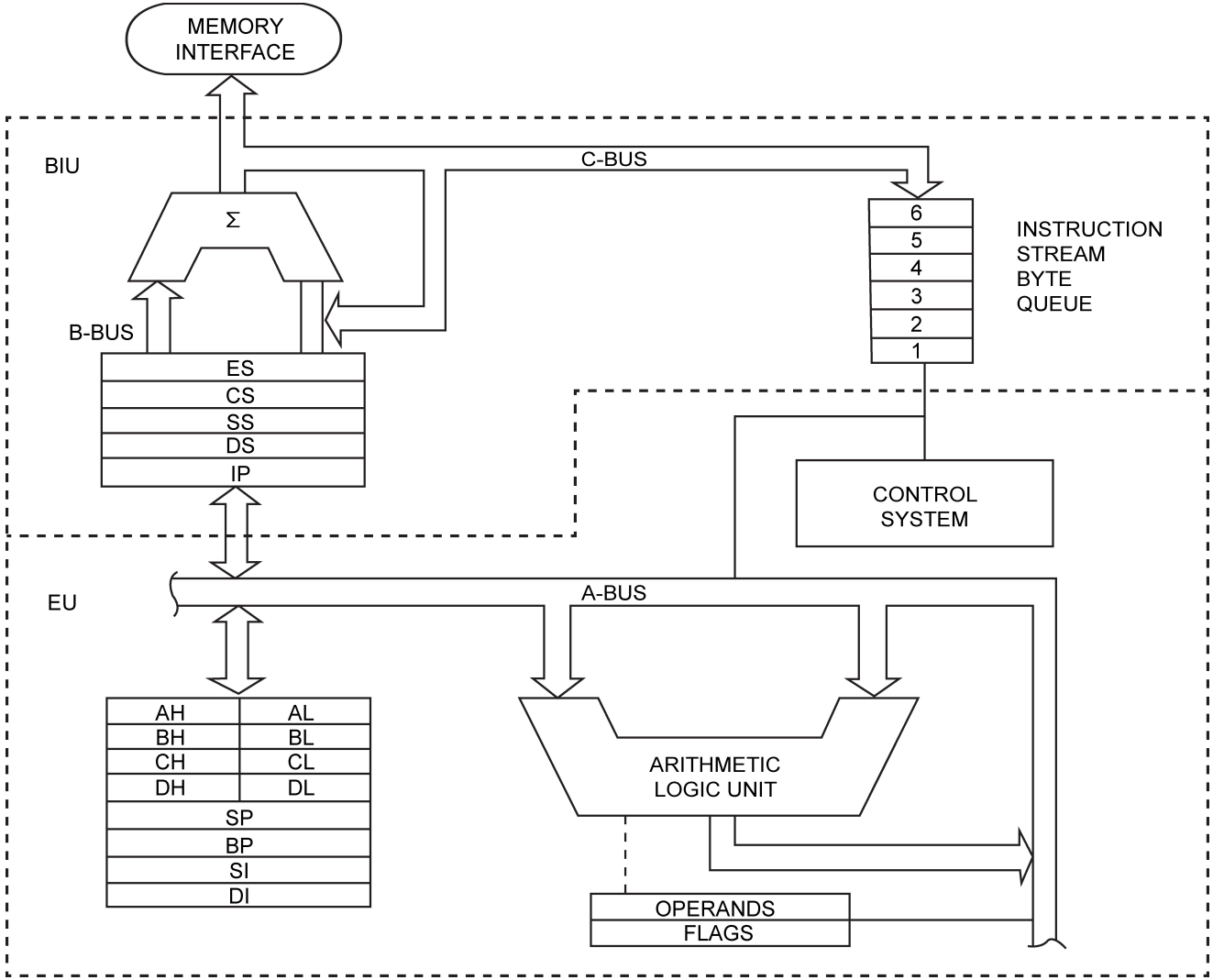
Chapter 3

Programming with 8086 Microprocessor

Internal Architecture and Features of 8086 Microprocessor

- **Features**
  - 8086 is 16-bit microprocessor which can address upto 1 MB of memory
  - It is register based microprocessor and has 16-bit data bus and 20-bit address bus
  - It has multiplexed address and data bus AD0-AD15andA16–A19
  - It can pre-fetches upto 6 instruction bytes from memory and queues them in order to speed up instruction execution.
  - Address ranges from 00000H to FFFFFH

Internal Architecture and Features of 8086 Microprocessor



Internal Architecture and Features of 8086 Microprocessor

- The internal architecture of 8086 microprocessor is divided into two independent functional unit
  - **Bus Interface Unit (BIU)**
  - **Execution Unit (EU)**
- **Bus Interface Unit (BIU)**
  - This unit is responsible for the transfer of instructions by fetching them from memory, computation of 20-bits physical address, address transfer, and the data transfer on the system bus to and from execution unit (EU)
  - BIU has four functional sub units
    - Instruction Queue
    - Segment Registers
    - Instruction Pointer
    - Summation Unit (Σ)

Internal Architecture and Features of 8086 Microprocessor

- **Bus Interface Unit (BIU)**
  - **Instruction Queue (IQ)**

➢ BIU uses a mechanism known as an instruction stream queue to implement a pipeline architecture.

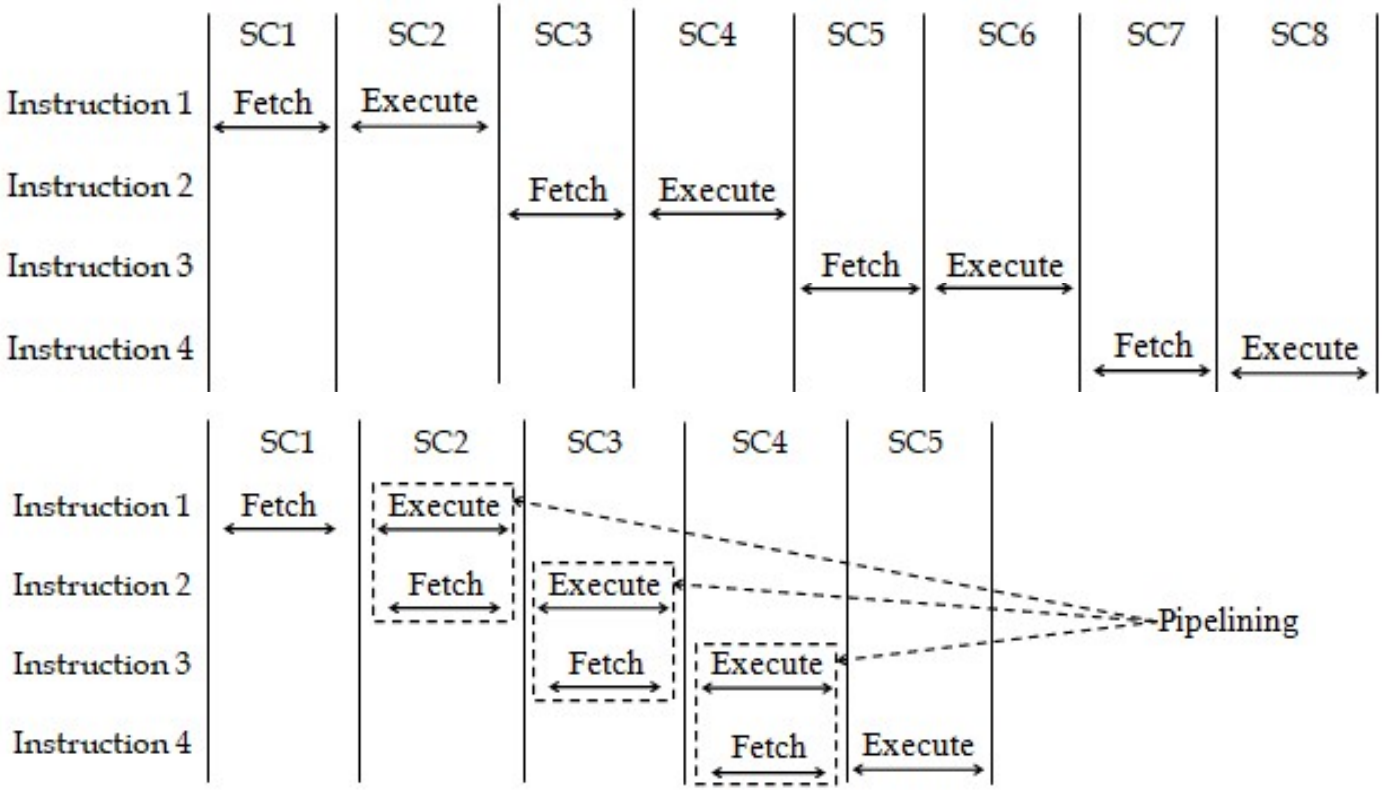
➢ BIU pre-fetches upto six instructions from the memory and places in a queue called *instruction queue (IQ)*

➢ The concept of IQ is to speed up the program execution by overlapping instructions fetch with execution. That means, while an instruction is being executing, the next instruction is fetched from memory and placed in IQ so that, EU, when completes the execution of current instruction can directly read next instruction from the queue for the execution thereby saving the fetch time.

➢ This process of fetching next instruction while executing a current instruction is called pipelining.

Internal Architecture and Features of 8086 Microprocessor

- **Bus Interface Unit (BIU)**
  - **Instruction Queue (IQ)**



Internal Architecture and Features of 8086 Microprocessor

- **Bus Interface Unit (BIU)**
  - **Segment Registers**

➢ The size of address bus is 20–bits & that of data bus is 16–bits (physically implemented using a 20–bits common bus). However, there are no registers to hold 20–bits physical address of a particular memory location.

➢ Hence, the total 1MB memory is divided into number of small segments (minimum of 8 segments each of maximum of 64KB size).

➢ However, at any given time, the 8086 works with only four segments (each of 64 KB) within this 1MB range.

➢ The four segments that the 8086 can work with at a particular time are:

code segment **:** holds the main program instructions to be executed.

stack segment **:** is a special memory (obeying LIFO principle) that holds program data during execution

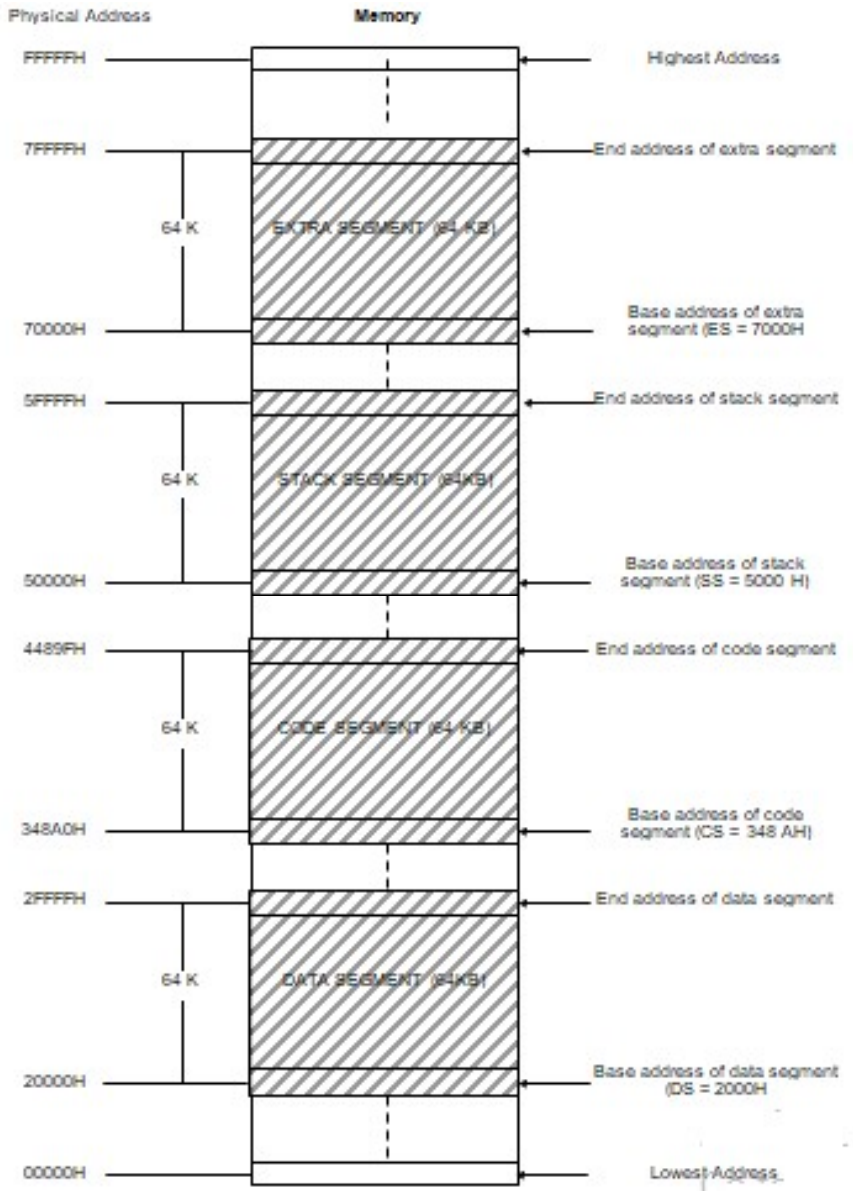
data segment **:** holds the data & variables required while writing a program

extra segment **:** is used as an extra segment to store data & variables if data segment is not enough.

Internal Architecture and Features of 8086 Microprocessor

- **Bus Interface Unit (BIU)**
  - **Segment Registers**
  - ➢ These four segments may be positioned anywhere in the 1MB address space of memory as shown in figure. But, the processor should have knowledge about their position and keep their base address – and here comes the use of segment registers.
  - ➢ Hence, the segment registers are 16–bits registers that hold the base addresses of different segments that 8086 works with at a particular time.
  - ➢ 8086 has four segment registers named code segment (CS) register, stack segment (SS) register, extra segment (ES) register, and data segment (DS) register each holding the base addresses of corresponding memory segments.

- **Bus Interface Unit (BIU)**
  - **Segment Registers**



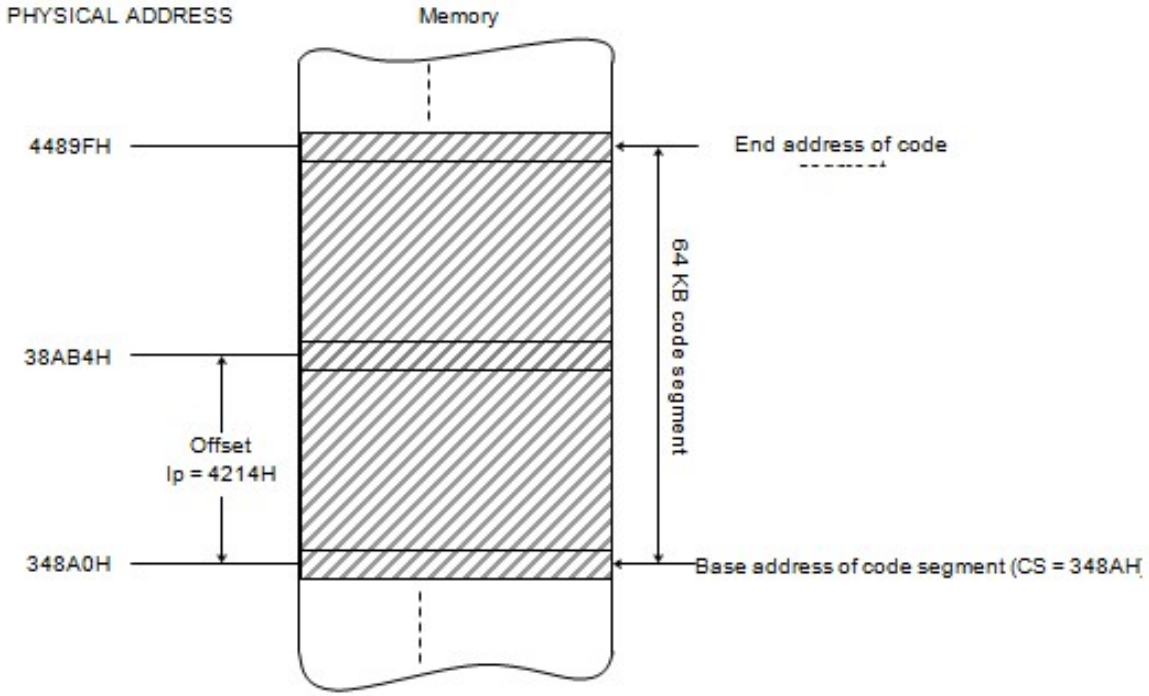
Internal Architecture and Features of 8086 Microprocessor

- **Bus Interface Unit (BIU)**
  - **Segment Registers**
  - **Code Segment (CS) Register**: It is a 16–bits register containing the base address of code segment that holds the main program written in 8086. The processor uses CS to access all the instructions referenced by instruction pointer (IP) register.
  - **Stack Segment (SS) Register**: It is a 16–bits register containing the base address of stack segment with program stack. By default, the processor assumes that all data referenced by the stack pointer (SP) and base pointer (BP) registers are located in the stack segment.
  - **Data Segment (DS) Register**: It is a 16–bits register containing the base address of 64KB data segment with program data. By default, the processor assumes that all data referenced by general purpose registers (AX, BX, CX & DX) and index registers (SI & DI) are located in the data segment
  - **Extra Segment (ES) Register**: It is a 16–bits register containing the base address of 64KB extra segment, usually with extra (additional) program data. By default, the processor assumes that the DI register references the extra segment in string manipulation instructions

Internal Architecture and Features of 8086 Microprocessor

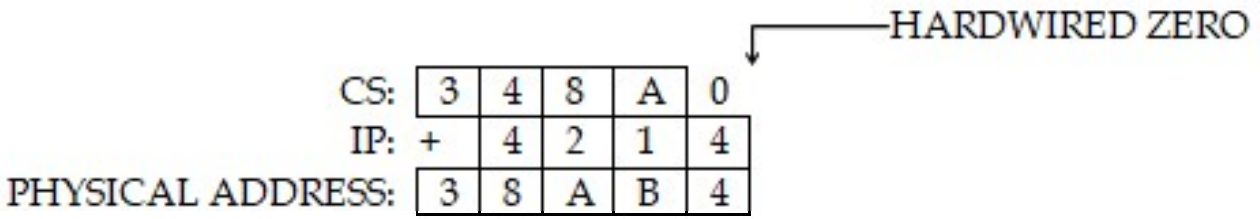
- **Bus Interface Unit (BIU)**
  - **Instruction Pointer (IP)**

➢Like program counter (PC) in 8085 microprocessor, instruction pointer holds an address or offset of the next instruction to be fetched from code segment.



Internal Architecture and Features of 8086 Microprocessor

- **Bus Interface Unit (BIU)**
  - **Computation of Physical Address in Code Segment**



PHYSICAL ADDRESS = LEFT_SHIFT_BY_4_BITS (CS) + IP
= LEFT_SHIFT_BY_4_BITS (348AH) + 4214H
= 348 A0H + 4214 H
= 38AB4H.

Internal Architecture and Features of 8086 Microprocessor

- **Bus Interface Unit (BIU)**
  - **Summation Unit (Σ)**
  - ➢ This unit is responsible for calculating the 20_bits physical address by taking base address from segment register and offset from the corresponding offset register.

Internal Architecture and Features of 8086 Microprocessor

- **Execution Unit (EU)**
  - This unit instructs BIU from where to fetch an instruction, extracts an instruction from instruction queue, decodes that, executes, and again instructs BIU to where to store the result (if any). The EU has the following functional sub-units.
    - Control System and Instruction Decoder
    - General Purpose Registers
    - Stack Pointer (SP) and Base Pointer (BP)
    - Index Registers
    - Arithmetic and Logic Unit (ALU)
    - Flag Register

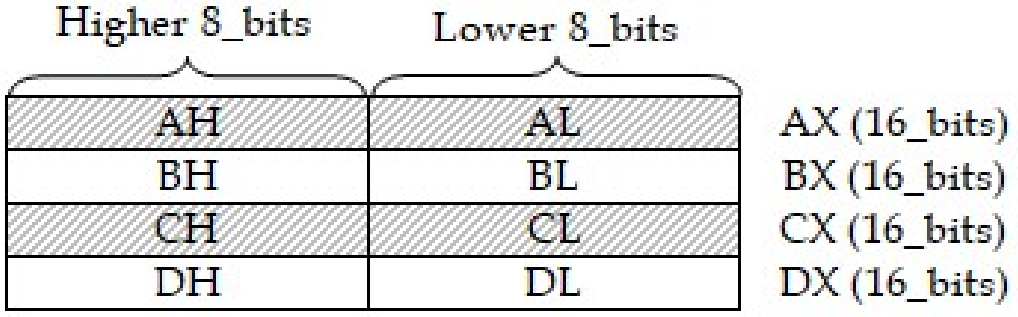
Internal Architecture and Features of 8086 Microprocessor

- **Execution Unit (EU)**
  - **Control System and Instruction Decoder**

➢ It receives the first instruction present in instruction queue, decodes that and generates different control signals for the execution. That means it is a control circuitry that directs the internal operations of microprocessor.

  - **General Purpose Registers**

➢ These are the registers that may be used in any program for general purpose problem solving. Hence, they are also called programmable registers. 8086 μp has four 16–bits general purpose registers (AX, BX, CX and DX)



Internal Architecture and Features of 8086 Microprocessor

- **Execution Unit (EU)**
  - **General Purpose Registers**
  - **Accumulator (AX):** It is a 16–bits register which can be split up into two 8–bits registers named AH and AL known as accumulator higher and accumulator lower respectively. Multiplication and division instructions use the AX or AL as default registers.
  - **Base Register (BX):** It is a 16–bits register which is generally used to store the base address of a particular variable. It is analogous to HL(M) register pair of 8085 μp. In other words, the BH and BL of 8086 are equivalent to H and L registers of 8085 respectively. BX is the only general purpose register whose content can be used to address a particular byte of 8086 memory.

Internal Architecture and Features of 8086 Microprocessor

- **Execution Unit (EU)**
  - **General Purpose Registers**

➢ **Counter Register (CX):** It is a 16–bits register which is generally used as a default counter for few of the instructions such as SHIFT, ROTATE, and LOOP

e.g.

```
        MOV CX, 0005H
again : ADD AL, BL
        ……..
        ……..
        LOOP again
        ……..
```

➢ **Data Register (DX):** It is a 16–bits register to hold a 16–bits data (or two 8–bits data in DH and DL). The DX register has its significant meaning in holding the higher 16–bits value out of 32–bits result obtained by multiplying two 16–bits numbers.