Chapter 2.2 Intel 8255A (Contd…)

- **MODE 1 INPUT CONTROL SIGNALS**
- **STB' (Strobe Input)** : This signal (active low) is generated by a peripheral device to indicate that I has transmitted a byte of data. The 8255A, in response to STB', generates IBF and INTR.
- **IBF (Input Buffer Full)** : This signal is an acknowledgement by the 8255A to indicate that the input latch has received the data byte. This is reset when the MPU reads the data.
- **INTR (Interrupt Request)** : This is an output signal that may be used to interrupt the MPU. This signal is generated if STB', IBF and INTE (Internal Flip-flop) are all at logic 1.
- **INTE (Interrupt Enable)** : This is an internal flip-flop used to enable or disable generation of INTR signal. The flip-flops $INTE_A$ and $INTE_B$ are set/reset using the BSR mode. The $INTE_A$ is enabled or disable through PC_4, and $INTE_B$ is enabled or disabled through PC_2.

Chapter 2.2 Intel 8255A (Contd…)

- **Mode 1 Input – Port A**
- Figure shows Port A as input port (when it operates in Mode 1) along with the control word and control signals (for handshaking with a peripheral). When the control word is loaded into control register, Group A is configured in Mode 1 with Port A as an input port, Port A can accept parallel data from a peripheral (like a keyboard) and this data can be read by the CPU.
- The peripheral first loads data into Port A by making the STB_A input low. This latches the data placed by the peripheral on the common data bus into Port A. Port A acknowledges reception of data by making IBF_A (Input Buffer Full) high. IBF_A is set when the STB_A input is made low.
- $INTR_A$ is an active output signal which can be used to interrupt the CPU so that the CPU can suspend its current operation and read the data written into Port A by the peripheral. $INTR_A$ can be enabled or disabled by the $INTE_A$ flip-flop which is controlled by BIT Set-Reset operation of PC_4. $INTR_A$ is set (if enabled by setting the $INTE_A$ flip-flop) after the STBA has gone high again, and if IBFA is high.
- On receipt of the interrupt, the CPU can be made to read Port A. The falling edge of the RD input resets IBF_A and it goes low. This can be used to indicate to the peripheral that the input buffer is empty and that data can again be loaded into it.

Chapter 2.2 Intel 8255A (Contd…)

- **Mode 1 Input – Port B**
- Figure shows Port B as an input port (when in Mode 1). The timing diagram and operation of Port B is similar to that of Port A except that it uses different bits of Port C for control. $INTE_B$ is controlled by Bit Set/Reset of PC_2.
- If the CPU is busy with other system operations, it can read data from the input port when it is interrupted. This is often called **Interrupt Controlled I/O**.
- If the CPU is otherwise not busy with other jobs, it can continuously poll (read) the status word to check for an IBF_B. This is often called **Program Controlled I/O**.
- The status word is accessed by reading Port C (A_1 and A_0 must be 10, $\overline{RD}$ and $\overline{CS}$ must be low). The status word format as assumed by the bits of Port C when Ports A and B are input ports in Mode 1, is shown in above figure.

Chapter 2.2 Intel 8255A (Contd…)

- **Mode 1 Input**

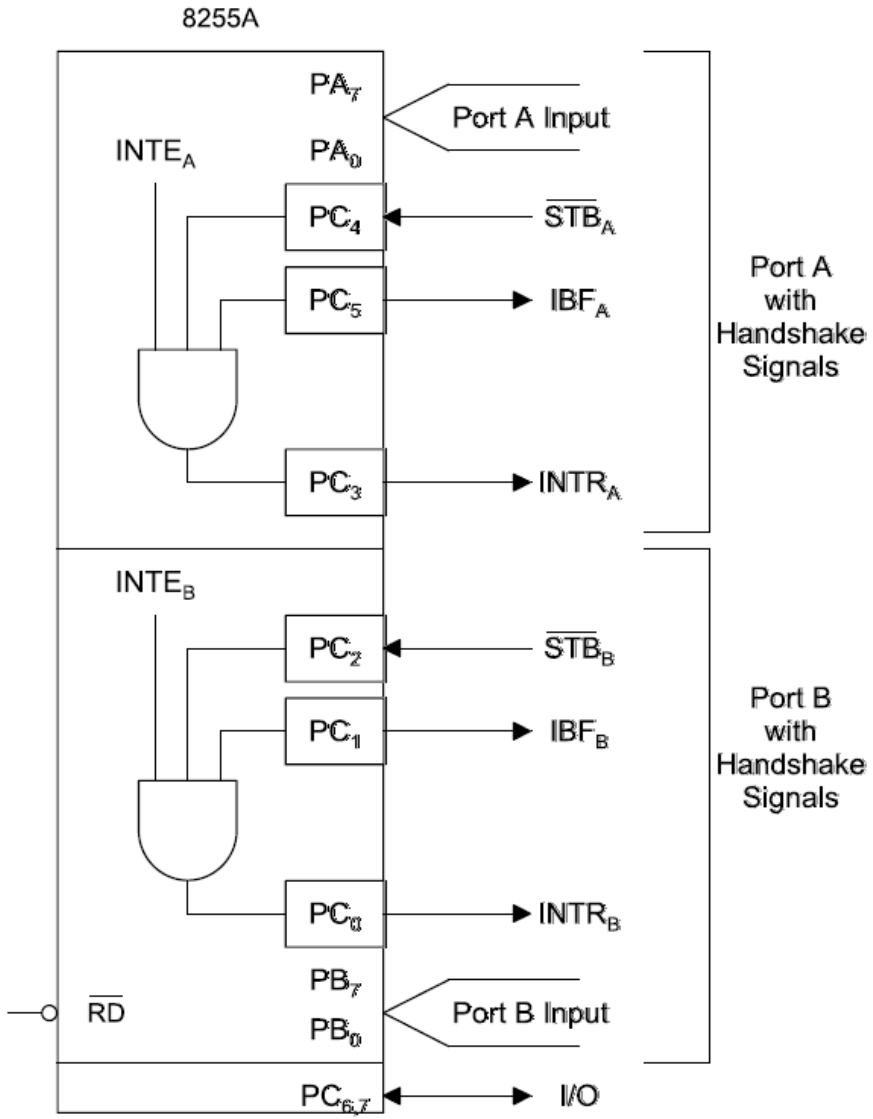

Fig: 8255A Mode 1 Input Configuration

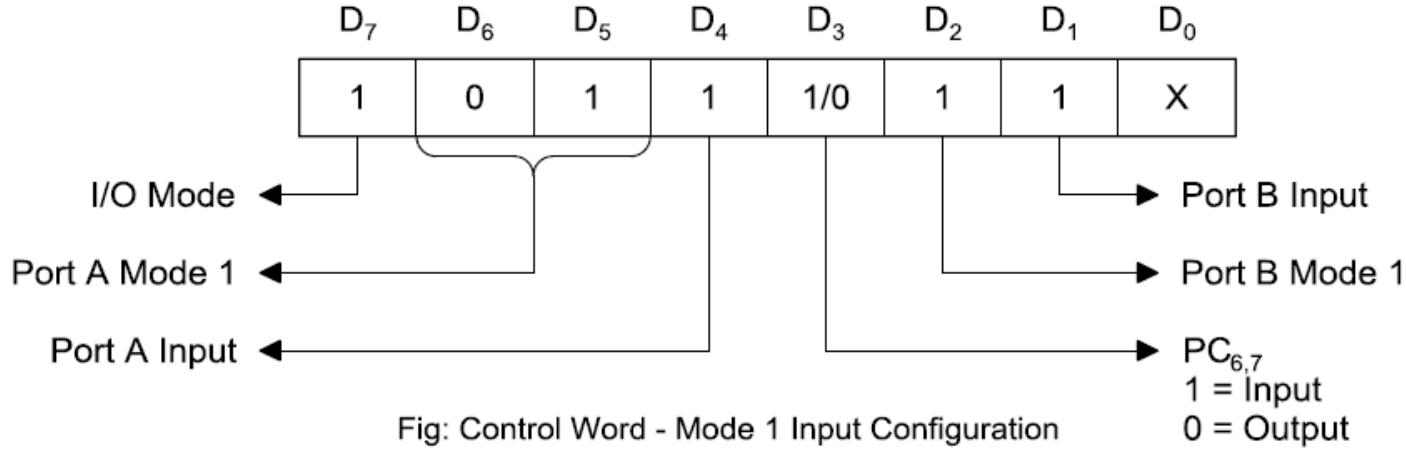

Fig: Control Word - Mode 1 Input Configuration

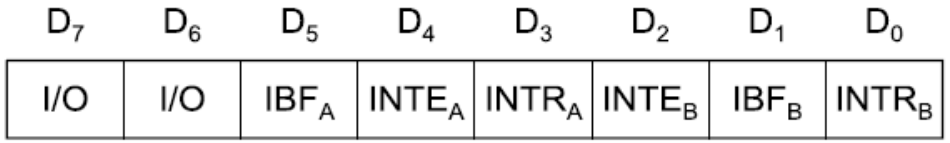

Fig: Status Word - Mode 1 Input Configuration

Chapter 2.2 Intel 8255A (Contd…)

- **Mode 1 Input**

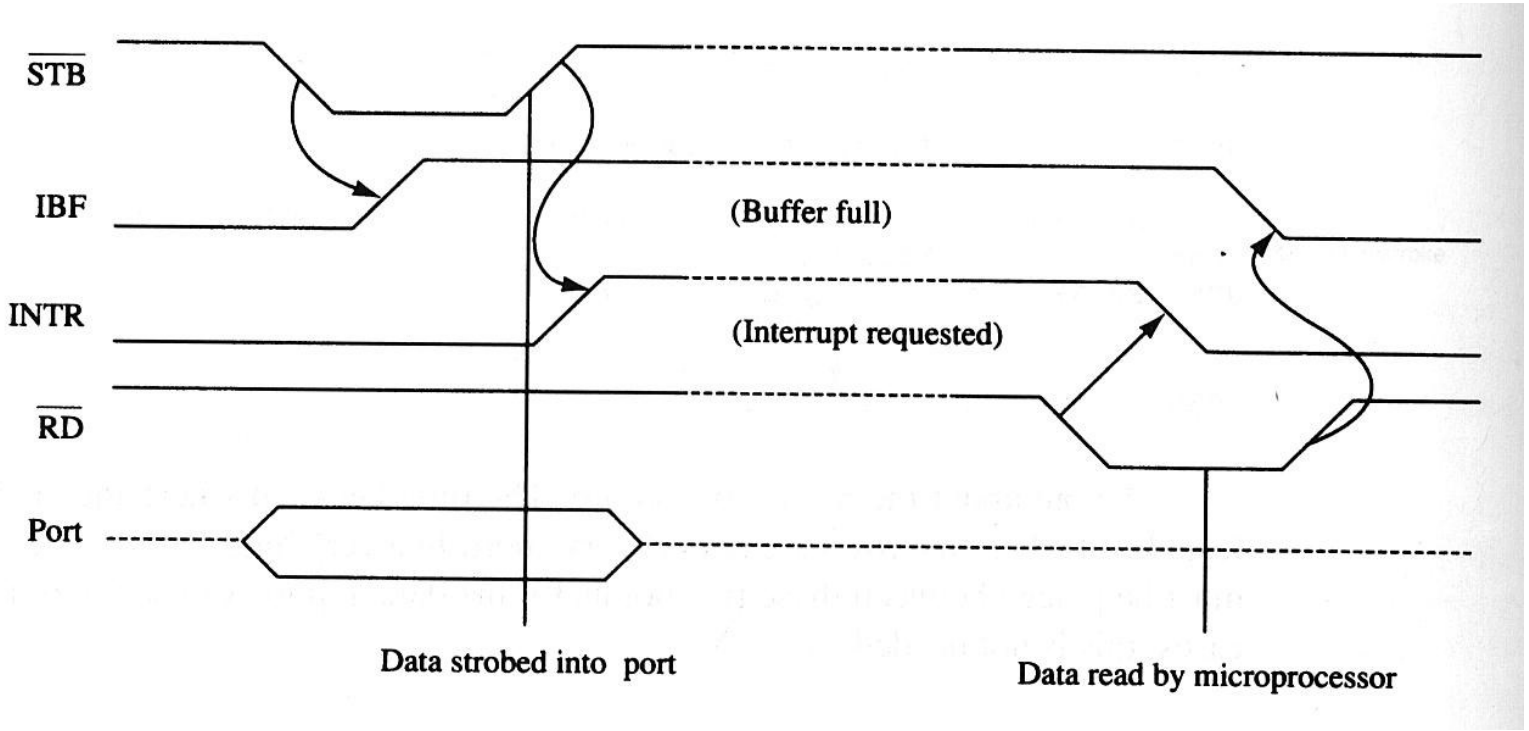

Fig: Timing Waveforms for Strobed Input (With Handshake) – 8255 Mode 1

- The peripheral first loads data into Port by making the STB' input low. Data latched into Port.
- Port A acknowledges reception of data by making IBF_A (Input Buffer Full) high. IBF is set when the STB' input is made low.
- INTR in Port A can be enabled or disabled by the INTE flip-flop - controlled by BSR operation of $\mathbf{PC_4}$. INTR is set (if enabled by setting the INTE flip-flop) after the STB has gone high again, and IBF is high.
- On receipt of the interrupt, the CPU can read data from Port.
- The falling edge of the RD' input resets IBF and it goes low - indicating to the peripheral that the input buffer is empty and can be loaded again.

Chapter 2.2 Intel 8255A (Contd…)

Mode 1 Input Control Signals

STB' (Strobe Input): A low on this input loads data into the input latch. The 8255A, in response to STB', generates IBF and INTR.

IBF (Input Buffer Full): A high on this output indicates that the data bus has been loaded into the input latch; in essence, an acknowledgement, IBF is set by STB input being low and is reset by the rising edge of the RD' input.

INTR (Interrupt Request): This is an output signal that may be used to interrupt the CPU. This signal is generated if STB', IBF and INTE (Internal Flip Flop) are all at logic 1. This is reset by the falling edge of the RD' (Read) signal.

INTE: This is an internal flip-flop used to enable or disable the generation of the INTR signal. The two flip-flops $INTE_A$ and $INTE_B$ are set/reset using the BSR mode through PC_4 and PC_2.

Chapter 2.2 Intel 8255A (Contd…)

Mode 1 Output – Port A

Figure below shows Port A configured as an output port (when in Mode 1) along with the control word and control signals (for handshaking with a peripheral). When the control word is loaded into the control register, Group A is configured in Mode 1 with Port A as an output port. The CPU can send out data to a peripheral (like a display device) through Port A of the 8255.

The $\overline{OBF_A}$ output (Output Buffer Full) goes low on the rising edge of the $\overline{WR}$ signal (when the CPU writes data into the 8255). The $\overline{OBF_A}$ output from 8255 can be used as a strobe input to the peripheral to latch the contents of Port A. The peripheral responds to the receipt of data by making the $\overline{ACK_A}$ input of the 8255 low, thus acknowledging that it has received the data sent out by the CPU through Port A. The $\overline{ACK_A}$ low resets the $\overline{OBF_A}$ signal, which can be polled by the CPU through $\overline{OBF_A}$ of the status word to load the next data when it is high again.

$INTR_A$ is an active high output of the 8255 which is made high (if the associated INTE flip-flop is set) when $\overline{ACK_A}$ is made high again by the peripheral, and when $\overline{OBF_A}$ goes high again (see timing diagram in Figure below). It can be used to interrupt the CPU whenever the output buffer is empty. It is reset by the falling edge of $\overline{WR}$ when the CPU writes data onto Port A. It can be enabled or disabled by writing a '1' or a '0' respectively to PC_6 in the BSR mode.

Figure below shows Port B as an output port when in Mode 1. The operation of Port B is similar to that of Port A. $INTE_B$ is controlled by writing a '1' or '0' to PC_2 in the BSR mode.

The status word is accessed by issuing a Read to Port C. The format of the status word as assumed by the bits of Port C when Ports A and B are Output ports in Mode 1 is shown in Figure below.

Chapter 2.2 Intel 8255A (Contd…)

Mode 1 C

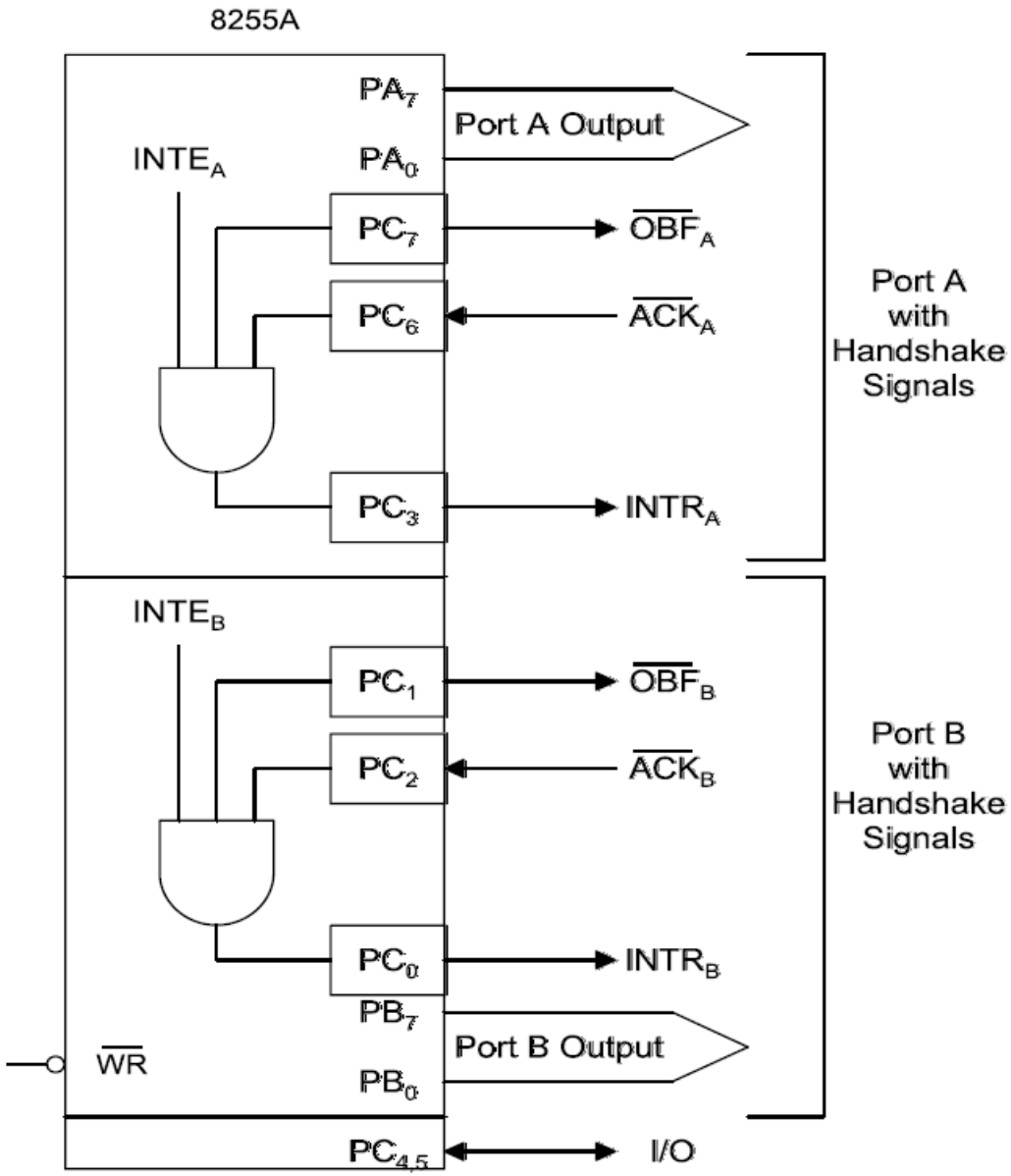

Fig: 8255A Mode 1 Output Configuration

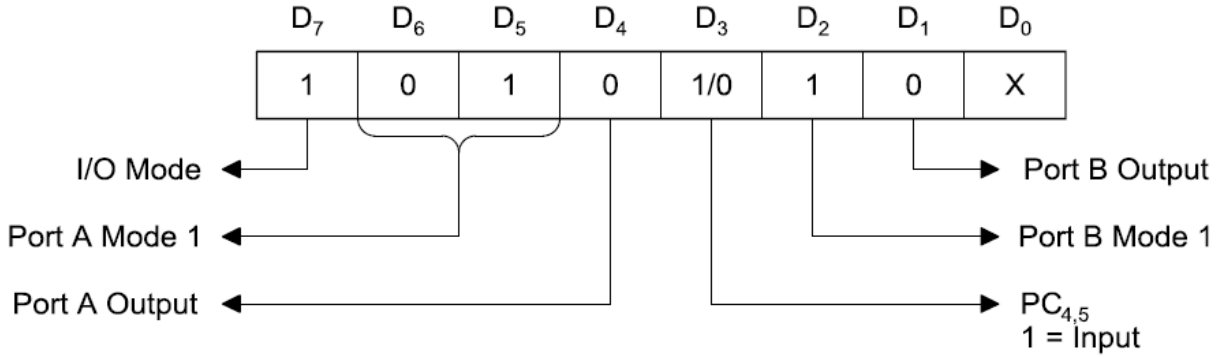

Fig: Control Word - Mode 1 Output Configuration

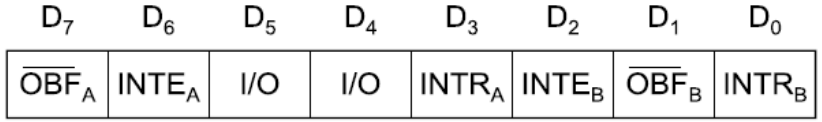

Fig: Status Word - Mode 1 Output Configuration

Chapter 2.2 Intel 8255A (Contd…)

Mode 1 Output Control Signals

OBF' (Output Buffer Full): The OBF' will go low to indicate that the CPU has written data out to the specified port. The OBF' will be set with the rising edge of the WR' input and reset by ACK' input being low.

ACK' (Acknowledgement Input): A low on this input informs the 8255A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request): A high on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when OBF', ACK' and INTE are all 1 and reset by falling edge of WR'.

INTE: This is an internal flip-flop to a port and needs to be set to generate the INTR signal. The two flip-flops $INTE_A$ and $INTE_B$ are set/reset using the BSR mode through PC_6 and PC_2.

Chapter 2.2 Intel 8255A (Contd…)

- **Mode 1 Output**

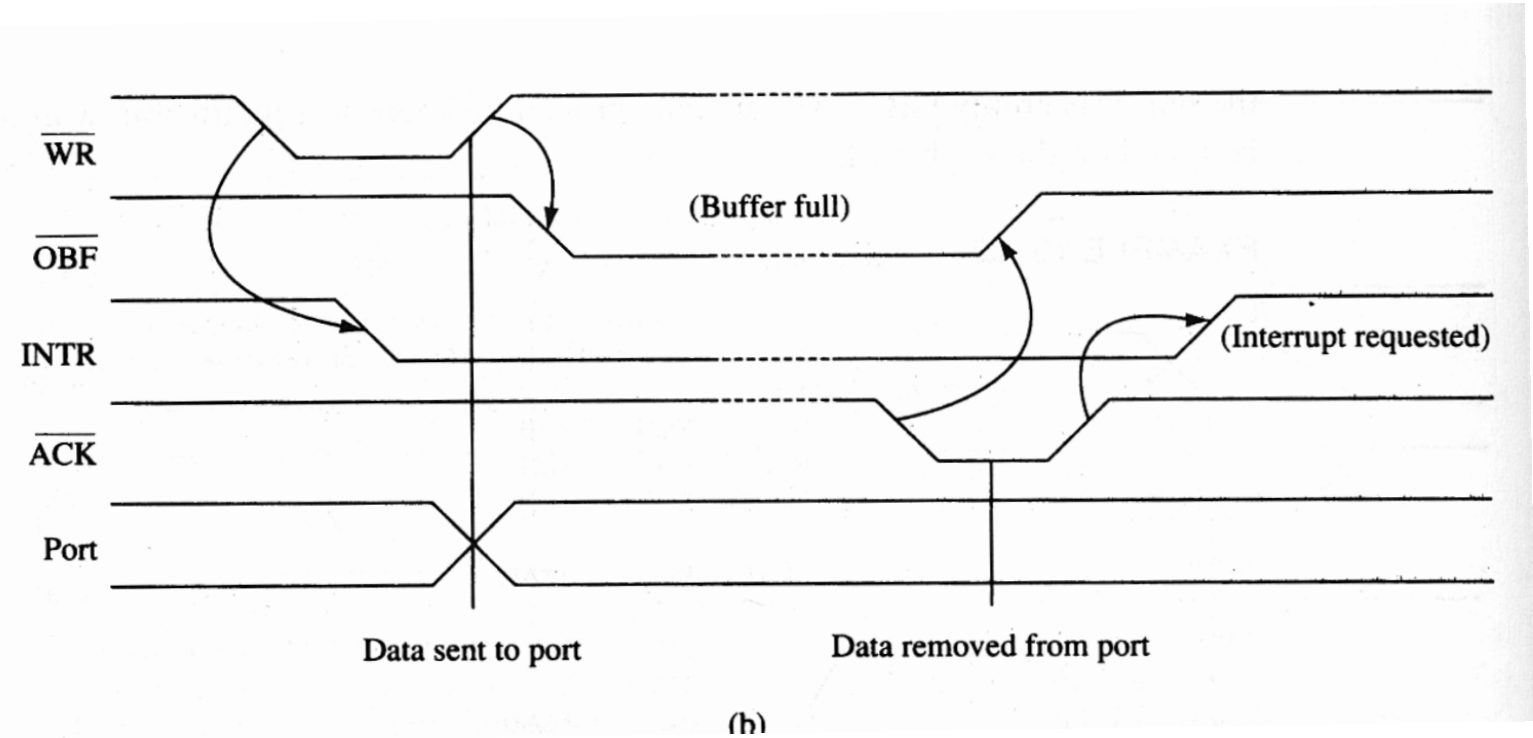

Fig: Timing Waveform for Strobed (With Handshake) Output - 8255 Mode 1

- OBF' goes low on the rising edge of the WR signal (when the CPU writes data into the 8255). The OBF output as a strobe input to the peripheral to latch the contents of Port.
- ACK input of the 8255 set low, - acknowledging peripheral has received the data. ACK low resets the OBF signal, which can be polled by the CPU through OBF of the status word to load the next data when it is high again. ACK' rising edge sets INTR to CPU indicating empty buffer.
- $INTR_A$ can be enabled by using Port C bits - PC6 and $INTR_A$ can be enabled by using Port C bits - PC_2.

Chapter 2.2 Intel 8255A (Contd…)

Example 3

Figure (on the right) shows an interfacing circuit using the 8255A in Mode 1. Port A is designated as the input port for a keyboard with interrupt I/O and port B is designated as the output port for a printer with status check I/O.

a) Find port addresses by analyzing the decode logic.

b) Determine the control word to set up port A as input and port B as output in Mode 1.

c) Determine the BSR word to enable $INTE_A$.

d) Determine the masking byte to verify the OBF' line in status check I/O.

e) Write subroutine to accept character from keyboard and send character to printer.

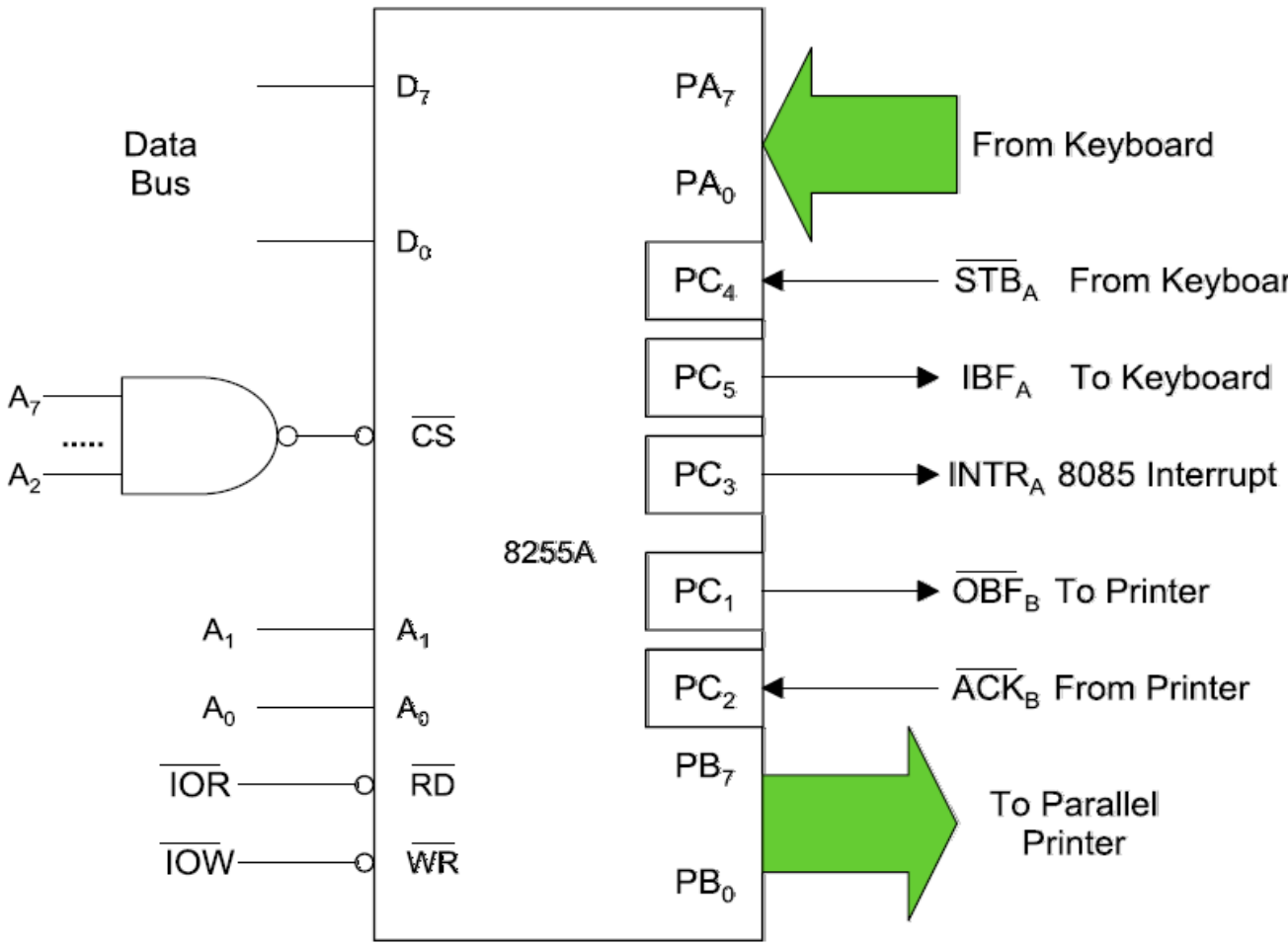

Fig: 8255A Mode 1 Example