1. Design an address decoding circuit of an input and output ports where output interface port is B0H and input interface port is B5H.

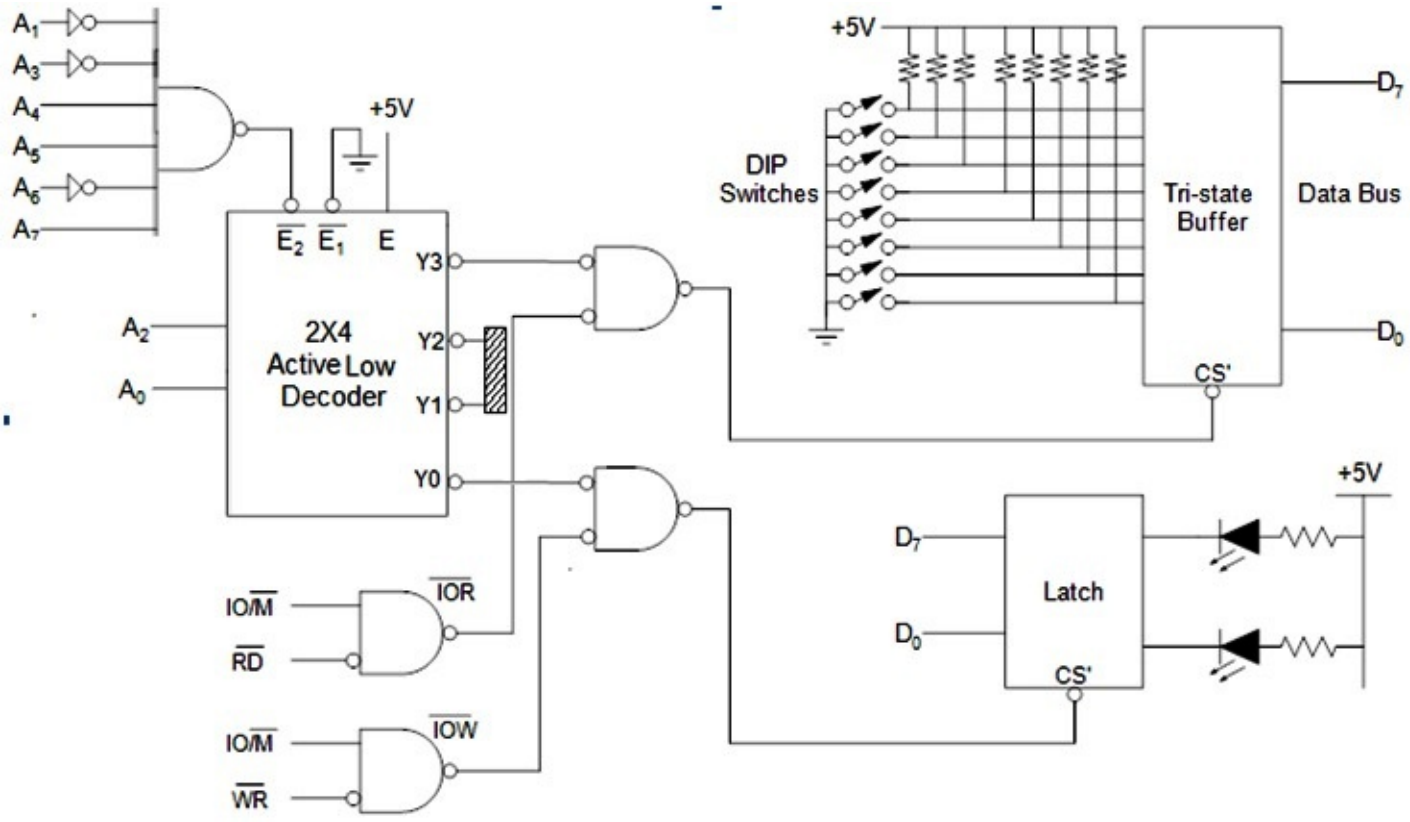
Step 1: Memory Mapping

Device Address	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Output: B0H	1	0	1	1	0	0	0	0
Input: B5H	1	0	1	1	0	1	0	1

Step 2: Decide decoder pins

Here, bit A2 and A0 in address lines for input and output are different, so we require a 2X4 decoder. Rest of the address lines will be decoded to generate chip enable signals for 2X4 decoder.

Step 3: Draw a decoding circuit



Step 4: Explanation

Here A_0 and A_2 are used as inputs of decoder. Output port (latch) is connected at output Y0 and will be selected when A_2A_0=00. Input port (tri-state buffer) is connected at input Y3 and will be selected when A_2A_0=11. Rest of the address bits are used to enable decoder and it will be enabled when $A_7A_6A_5A_4A_3A_1$=101100.

2. Design an address decoding circuit of a memory device interfacing with one 2 KB RAM chip and one 4KB ROM chip at address 5000H.

Step 1: Address Mapping

Memory Block	Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
RAM	Start:5000H	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	End:57FFH	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1
ROM	Start:5800H	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	End:67FFH	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1

Here the starting address for RAM is 5000H. We can calculate the end address by adding the size of RAM in bytes in hexadecimal value minus one to the starting address.

i.e. end address = starting address+(size of RAM in hex-1)

= 5000H + (800H-1) ; 2048 in hex is 800H

= 5000H + 7FFH

= 57FFH

Similarly, starting address for ROM is end address of RAM plus one (i.e. 5400H). We can calculate the end address same as RAM.

i.e. end address = 5800H + (1000H-1) ; 4096 in hex is 1000H

= 5800H + FFFH

= 67FFH

Step 2: Decide decoder pins

We check all address bits one by one starting from MSB until we get different bit. After getting different bit, we check whether that bit gives unique address to differentiate RAM and ROM. If yes, we take that bit as input decoder. If no, we pair that bit with next bit. If those combine bits give unique address to differentiate RAM and ROM, , we take that bit as input decoder. If no, we combine those two bits with another next bit and we repeat this process until we get unique address to differentiate RAM and ROM. In this case $A_{13}A_{12}A_{11}$ will give unique address and hence 3X8 decoder will be used and $A_{13}A_{12}A_{11}$ bits will be used as input of decoder.

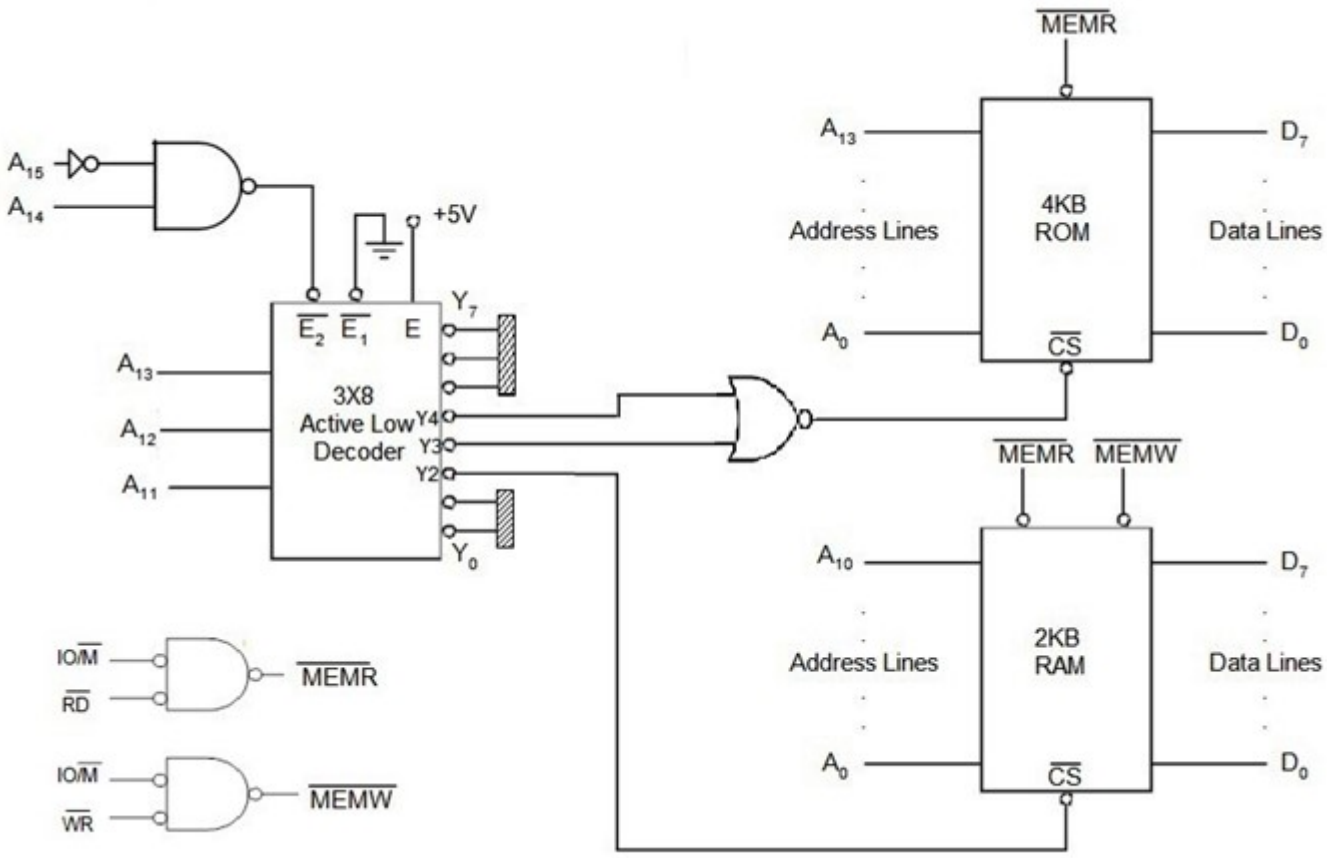
Memory Block	Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
RAM	Start:5000H	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	End:57FFH	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1
ROM	Start:5800H	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	End:67FFH	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1

Step 3: Decide address bits for RAM and ROM

We check start and end bits one by one of RAM starting from MSB until we get different bits. After getting different bits, we can say the address bits required for RAM is from different bit to A_0. We repeat same process for ROM.

Memory Block	Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
RAM	Start:5000H	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	End:57FFH	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1
ROM	Start:5800H	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
	End:67FFH	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1

Step 4: Draw decoding circuit



Step 5: Explanation

Here A15A14 bits are used to enable 3X8 decoder and will be enabled when A15A14=01. $A_{13}A_{12}A_{11}$ are used as input of 3X8 decoder. When $A_{13}A_{12}A_{11}$=010, RAM will be selected and when $A_{13}A_{12}A_{11}$=011 or 100, ROM will be selected.

3. Design an address decoding circuit of an input and output ports where input interface port is 82H and output interface port is 84H.

Device Address	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Input: 82H	1	0	0	0	0	0	1	0
Output: 84H	1	0	0	0	0	1	0	0

4. Design an address decoding circuit of a memory device interfacing with two 4KB RAM chip and one 8KB ROM chip at address 9000H.

Memory Block	**Address**	**A_{15}**	**A_{14}**	**A_{13}**	**A_{12}**	**A_{11}**	**A_{10}**	**A_9**	**A_8**	**A_7**	**A_6**	**A_5**	**A_4**	**A_3**	**A_2**	**A_1**	**A_0**
RAM1	Start:9000H																
	End:																
RAM2	Start:																
	End:																
ROM	Start:																
	End:																