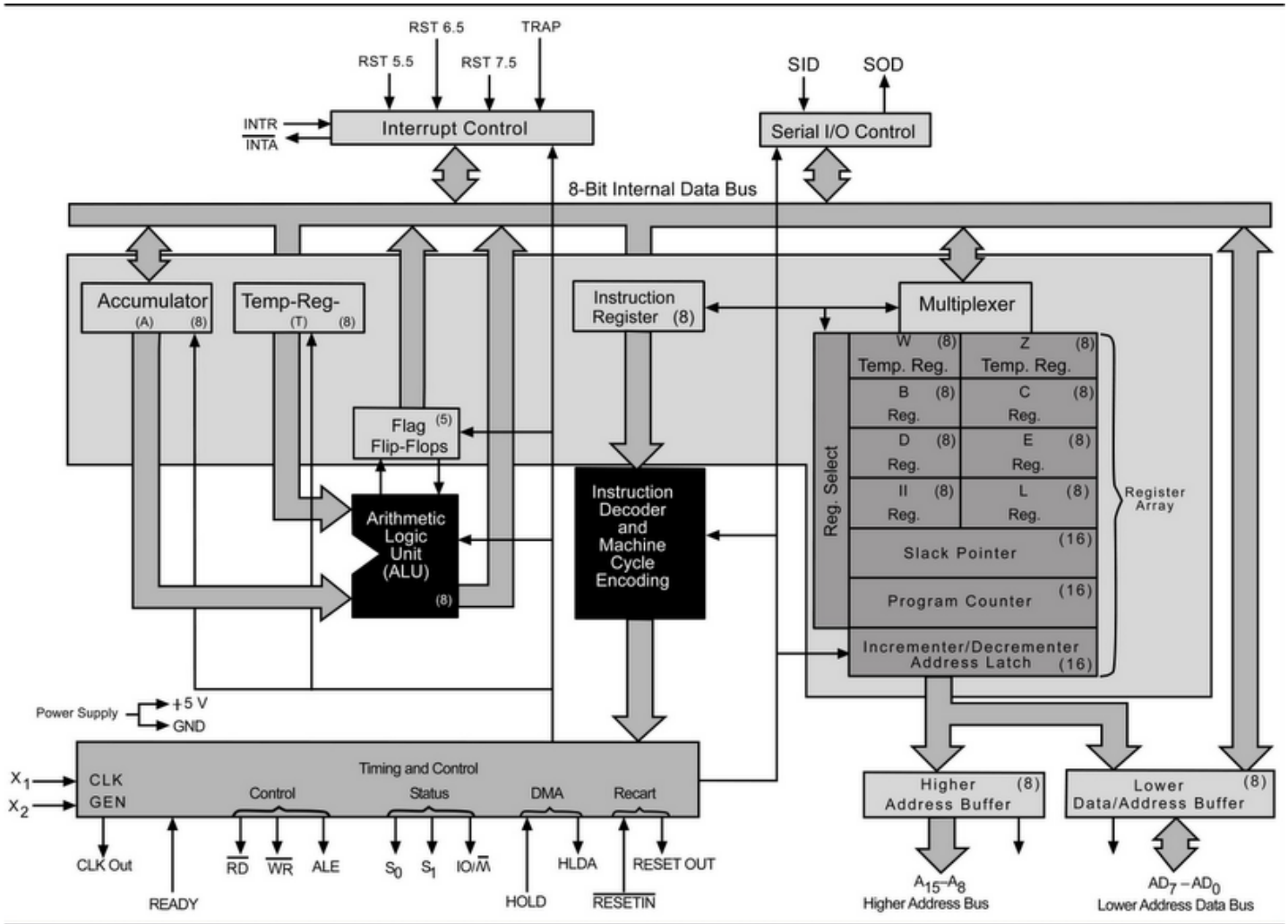
Chapter 2

Programming with 8085 Microprocessor

2.1 Internal Architecture and Features of 8085 Microprocessor

It is an 8-bits microprocessor. That means it can access 8-bits of data from/to memory/IO devices at a time. It is an accumulator-based microprocessor because almost all arithmetic and logical operations are based on accumulator as one of the operands. It has 16-bits memory address bus and can address up to maximum of 64KB memory space.



Internal Architecture of 8085 Microprocessor

1. Arithmetic and Logic Unit: It performs 8-bits arithmetic and logical operations.

- *Arithmetic operations*: addition, subtraction, comparison, and increment/decrement
- *Logical operations*: ANDing, ORing, XORing, and Complement

2. Register Array: It is a collection of different registers as a fastest memory of a computer system – sometimes are also called processor memory. A register is set of flip-flops used as a temporary memory during the internal operation of µP.

a. Accumulator (A – 8 bits)

- It is one of the default source operands and resultant operand for almost all ALU, I/O and load/store operations of µP

- Hence 8085 µP is also called an accumulator based µP.

b. Temporary Registers (T, W, & Z – 8 bits each):

- These are the registers used temporarily by µP during the internal operation of an instruction.
- Not accessible to the programmer

c. General Purpose Registers (B, C, D, E, H, & L – 8 bits each):

- These are the registers used in programming for general purposes. They are also called *programmable registers*.

- They can be used individually as 8-bit registers or in pairs as 16-bits registers BC, DE, and HL.
- H& L can be utilized in indirect addressing mode. The pair HL represents a 16-bit memory address.

d. Flag Register (F – 8 bits): It is a register consisting of 5 flags. A flag is a particular status of ALU operation.

D7	D6	D5	D4	D3	D2	D1	D0
S	**Z**	X	**AC**	X	**P**	X	**CY**

Carry Flag (CY) – is set if the last ALU operation generates a carry.
Parity Flag (P) – is set if the result of last ALU operation has even number of 1s (even parity checker).
Auxiliary Carry Flag (AC) – is set if the lower nibble (lower 4-bit) of last ALU operation generates a 1 carry.
Zero Flag (Z) – is set if the result of last ALU operation is zero.
Sign Flag (S) – is set if the MSB of result of last ALU operation is 1.

Examine the status of different flags after the addition of 4CH and 59H.

```
                1
FCH:    1 1 1 1   1 1 0 0
59H:    0 1 0 1   1 0 0 1
        ---------------------
155H: 1 0 1 0 1   0 1 0 1   <-- 8-bits
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- *S* – As an MSB of the above 8-bits result is 0, S = 0.
- *Z* – Because the above addition yields a non-zero result, Z = 0.
- *AC* – As there is a carry from lower nibble to higher nibble (i.e., from D3 bit to D4 bit), AC = 1.
- *P* – As there are even (4) number of ones in the 8-bits result, P = 1.
- *CY* – As there is a carry from higher nibble (i.e., from bit D7), CY = 1

Hence the status in the flag register after above addition will be as shown below.

S	Z		AC		P		CY
0	0	X	1	X	1	X	1

= 15H if all don't cares are made zero

e. Instruction Register (IR – 8 bits):
- holds an opcode (binary code corresponding to an instruction) after reading from the memory.
- The opcode is further given to the instruction decoder to decode and identify the corresponding instruction.

f. Program Counter (PC – 16 bits):
- holds an address of next instruction to be executed.
- acts as a counter to sequence the execution of a program.

g. Stack Pointer (SP – 16 bits):
- holds an address of top of the stack till where data is present.
- A stack is special memory segment that obeys last-in-first-out (LIFO) principle.

3. MUX and Register Select:
- MUX is a multiplexer used to select a desired register from multiple registers (of register array) during the execution of an instruction.
- Register select acts as selection line for the MUX

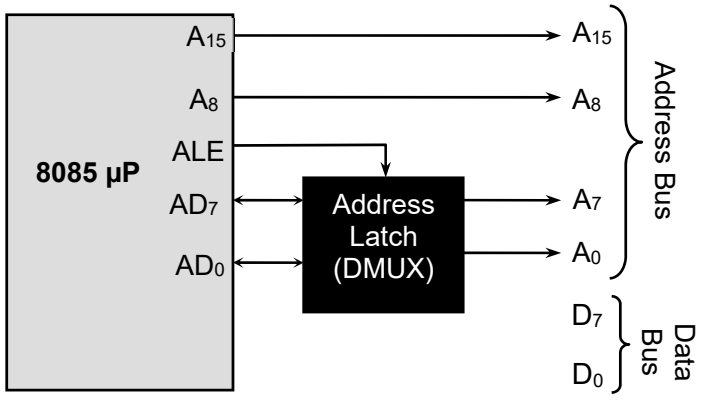
4. Instruction Decoder and Machine Cycle Encoding:
- Instruction decoder is used to decode the opcode present in IR to recognize an instruction corresponding to that opcode by selecting a particular output line.
- Machine cycle encoding generates the different T-states of a particular machine cycle during the execution of an instruction.

5. Timing and Control Unit:
- generates the different control signals (to other functional units of microprocessor) at different time cycles to control the internal operation of microprocessor.
- Beside that, it also accepts the different signal issued to microprocessor by other peripheral devices and handles them accordingly.

6. Internal Data Bus:
- 8-bits fastest data bus that interconnects the three functional units of microprocessor: ALU, register array and control unit.
- The data transfer through this bus does not take even a single time cycle.

7. Higher Address Bus, Lower Address-Data Bus, and Address Latch:
- They are collectively known as system bus that interconnects microprocessor with other functional units: memory and I/O devices.
- System bus is a pathway used to send address and data to and from microprocessor.
- ***higher address bus ($A_{15} – A_8$)*** is always used to transfer higher byte of memory address.
- ***lower address/data bus ($AD_7 – AD_0$)*** is formed by multiplexing lower address bus ($A_7 – A_0$) and data bus ($D_7 – D_0$) that can transfer lower byte memory address or I/O address or data at a time. While using this bus, it is demultiplexed to either $A_7 – A_0$ or $D_7 – D_0$ using *address latch*.
- ***Address latch*** is a demultiplexer that allows microprocessor to use system bus as either data bus or address bus. A signal named ALE (address latch enable) is used as a selection line as shown in figure 5.11.

If ALE =1, then system bus acts as address bus
If ALE =0, then system bus acts as data bus



8. Higher Address Buffer, and Lower Address-Data Buffer:
- Temporary memory that collectively buffers the content before sending from µP to the system bus or from system bus to µP.

9. Serial I/O Control Block:
- Responsible for the serial communication of microprocessor with peripheral devices.
- Two Pins: SID (Serial Input Data) and SOD (Serial Output Data)

10. Interrupt Control Block:
- Responsible for handling one or more interrupts coming to microprocessor from peripheral devices.
- *An interrupt is a kind of disturbance to the* microprocessor *created by its peripherals or external devices. A disturbance is created by a peripheral device to get it served by µP.*
- Different Interrupt pins: INTR, $\overline{\text{INTA}}$, RST5.5, RST6.5, RST7.5 and TRAP