GOOD MORNING
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★ Chapter 1 : Introduction -4 marks

- Define Embedded System
- Example : "Digital Camera" with explanation
- Types of Embedded System
- Characteristics + Explanation
- Design metrics
- Application of Embedded System.
- ~~Numerical~~ : Simplified Revenue Model. Derivation.

Week 1 : Qno. 1, 2, 3, 5, 6.

★ Chapter 2 : Hardware Designs. - 8 marks.

- Steps for designing Single Purpose Processor.
- Design questions : - Fibonacci series : VImp.
  - x^n VImp. - Largest of 4 integers.
  - LCM. (6§ Bhadra)
  - HCF
- Dual purpose processor design.
  - Median & Variance of 5 numbers -- 70 Mark
- Optimization. (Explanation + Example) - VVImp

Week #3 : 2, 4, 5 + Example, 8, 9.

★ Chapter 3 : Software design Issue. - 8 marks.

- Datapath & Control Unit.
- General purpose processor
- Datapath operation with example. - Imp.
- Instruction Cycle.
- Addressing modes - Imp
- Development Environment, Software development process - VVImp ; Embedded System Dev. Proces
- Pipelining, 6 stage - Imp
- General purpose processor v/s application specific.
- DSP + Characteristic & Advantages

- Programmer's view
- Selecting a microprocessor
- General purpose processor design.

Chapter-4 Memory - 8 marks.

Imp - Write Ability & Storage Performance ~~Permanance~~
Imp - Types of mapping - VImp
- Types of ROM - Imp
  - Storing + Erasing data
V. Imp - Cache Write Technique
- Internal design of a ROM
V. Imp - Compose: (i) 1K×8 ROMs into 1K×32 ROM
  (ii) 1K×8 ROMs into 4K×8 ROMs
  (iii) 1K×8 ROMs into 4K×16 ROM
- Implementing combinational function using ROM
- Cache
- SRAM and DRAM
- Memory Hierarchy

Ch-5 Interface 8 marks

- Strobe, Handshake, Strobe + Handshake Compromise
- Arbitration, Priority + Daisy chain - VVImp.
- Interrupt processor
- Multilevel Bus Architecture - Two level - Imp.
- Design an interface circuit
- DMA + Operation - - Imp
- Serial & Parallel Communication
- USB Protocol, Serial Protocol; I^2C
- Wireless Protocols
- Port base I/O, Bus based I/O, Memory mapped I/O, Interrupt driven I/O

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Ch 6 RTOS - 12 marks

- Operating System Architecture
- GPOS v/s RTOS ✓Imp
- Kernel, Types of Kernel - VImp.
- Thread, Process, Differences - VImp. - At least 6 dys
- Concept of multithreading, Importance
- User-level Thread v/s Kernel-level threads.
- Multi tasking v/s multi processing
- Scheduling Algorithm, Numerical
- Deadlock & Coffman's condition
- Context switching - Imp.
- Task synchronization, "Busy / Wait"

Ch. 7 Control System - 8 marks

- Open loop System v/s Closed loop System
- Challenge of modeling a real physical system.
- PID Control -- VVImp.
- Metrics to used to measure control objective.
- Design an open loop automobile cruise controller and derive condition for no oscillation and reduction of road disturbance and determine performance parameters

Imp

- Design an closed loop control system for automo

- - -

- PID controller in software ⇒ Algorithm.

Ch-8 : IC Technology - 8 marks

- IC manufacturing process
- Photolithography -- VVImp
- Full Custom IC, Semi-Custom IC, PLD.
  - ↳ Implementation, Adv. Disadv.
- F = xz + y on IC.

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Ch-9 Microcontrollers - 8 marks

- 8051 Microcontroller
- Microcontroller v/s microprocessor
- Internal structure of 8051 / Architecture
- Addressing modes
- Optimal features
- Assembly program - Old questions + C program.
- Pin diagram of 8051.

Ch-10: VHDL - ~~10 marks~~ 8 marks.

- VHDL Code
- Component
- Dataflow, Behavioral, Structural modeling
- Explain process in VHDL
- Structure of VHDL code.
- Explain component.
- Algorithm + FSM VHDL code.