

# Interfacing Digital to Analog Converter (DAC).

## Objective :-

- To convert binary to analog voltage or to the digital value.

## THEORY:-

Interfacing a digital to analog converter (DAC) involves converting straight binary to analog voltage or current proportional to the digital value. DAC can be broadly classified in three categories: Current output, voltage output, and multiplying Type.

voltage output DAC is comparatively slower than current output DAC because of the delay in converting the current signal into voltage signal.

## Characteristics of DAC.

- Resolution
- Accuracy
- Linearity
- Settling time
- Monotonicity
- Temperature coefficient.

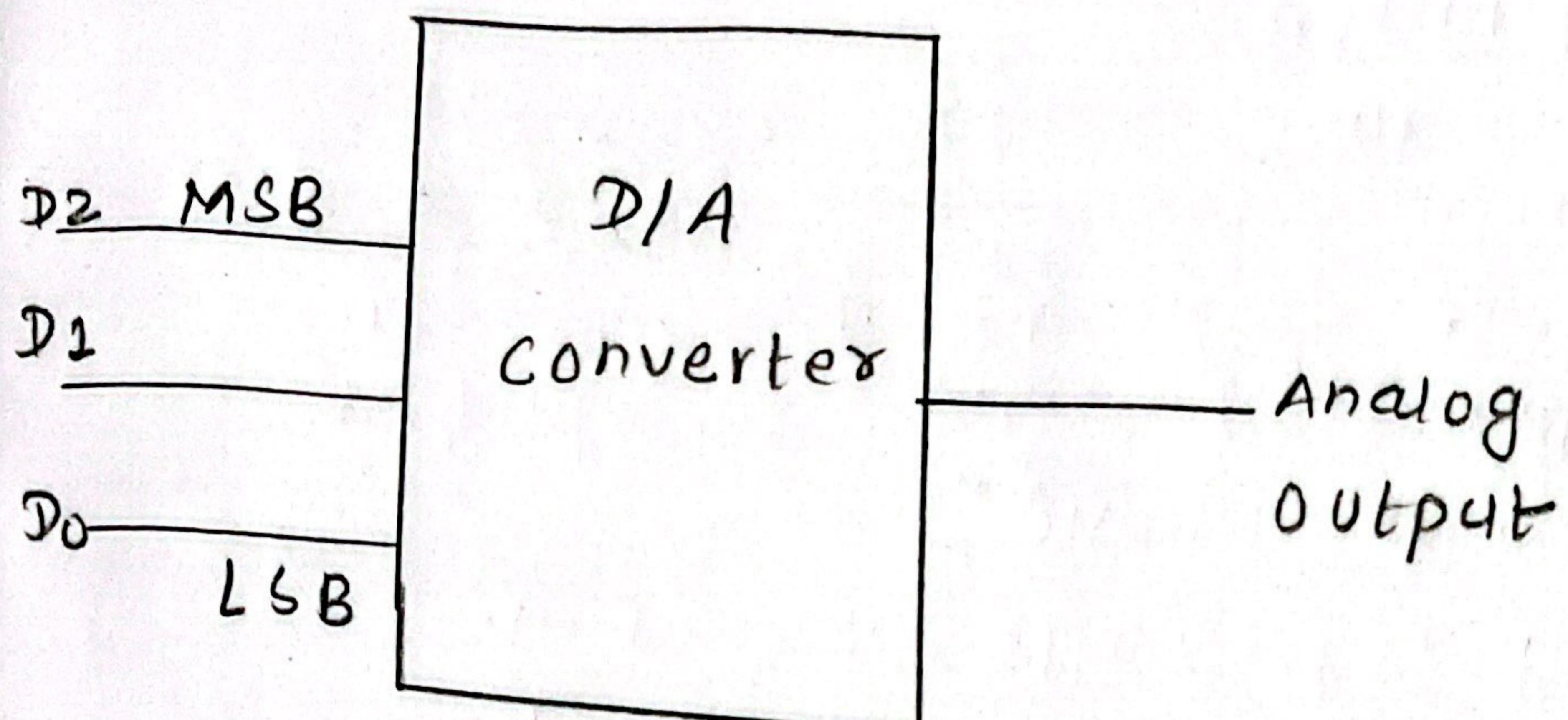


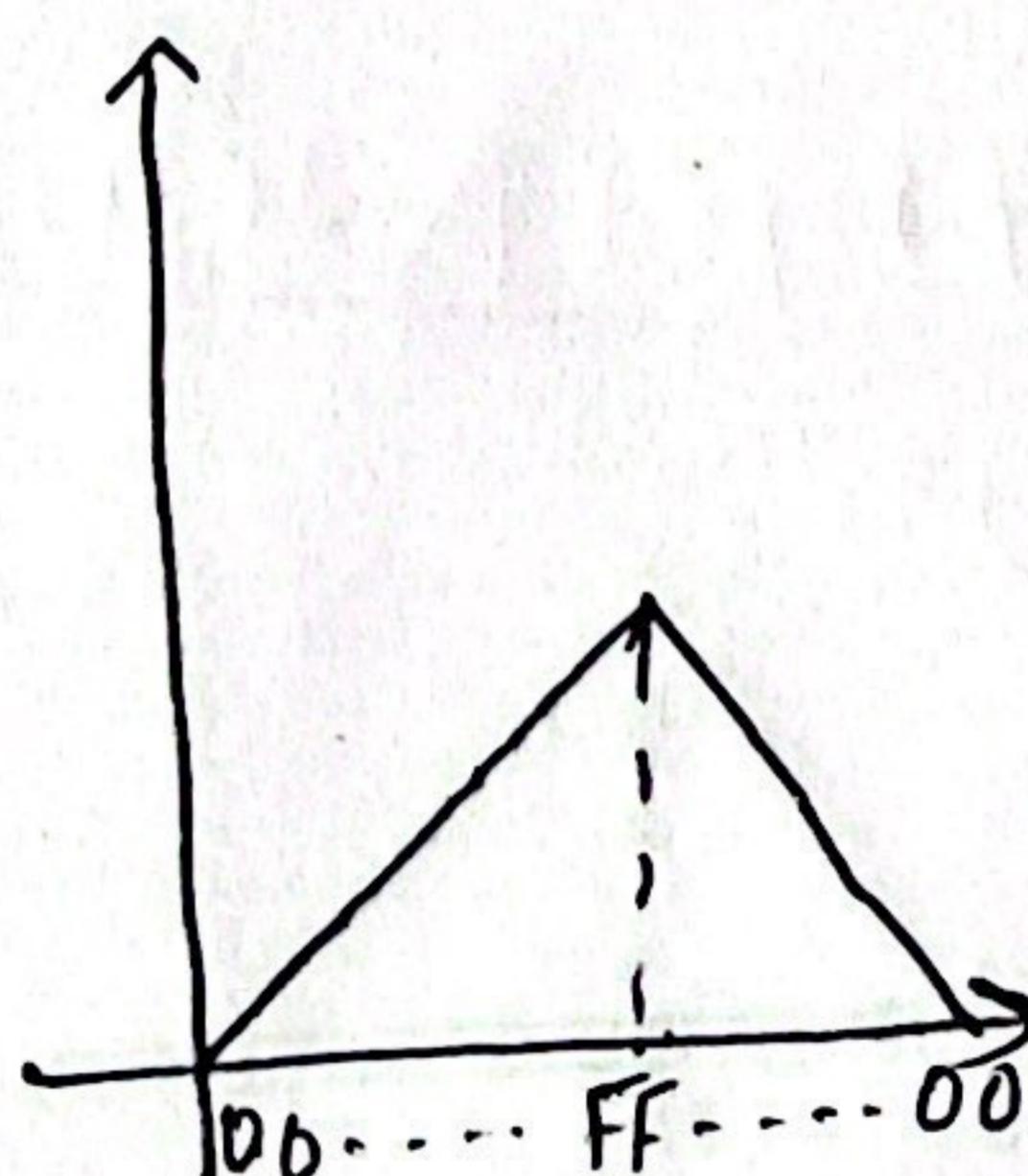
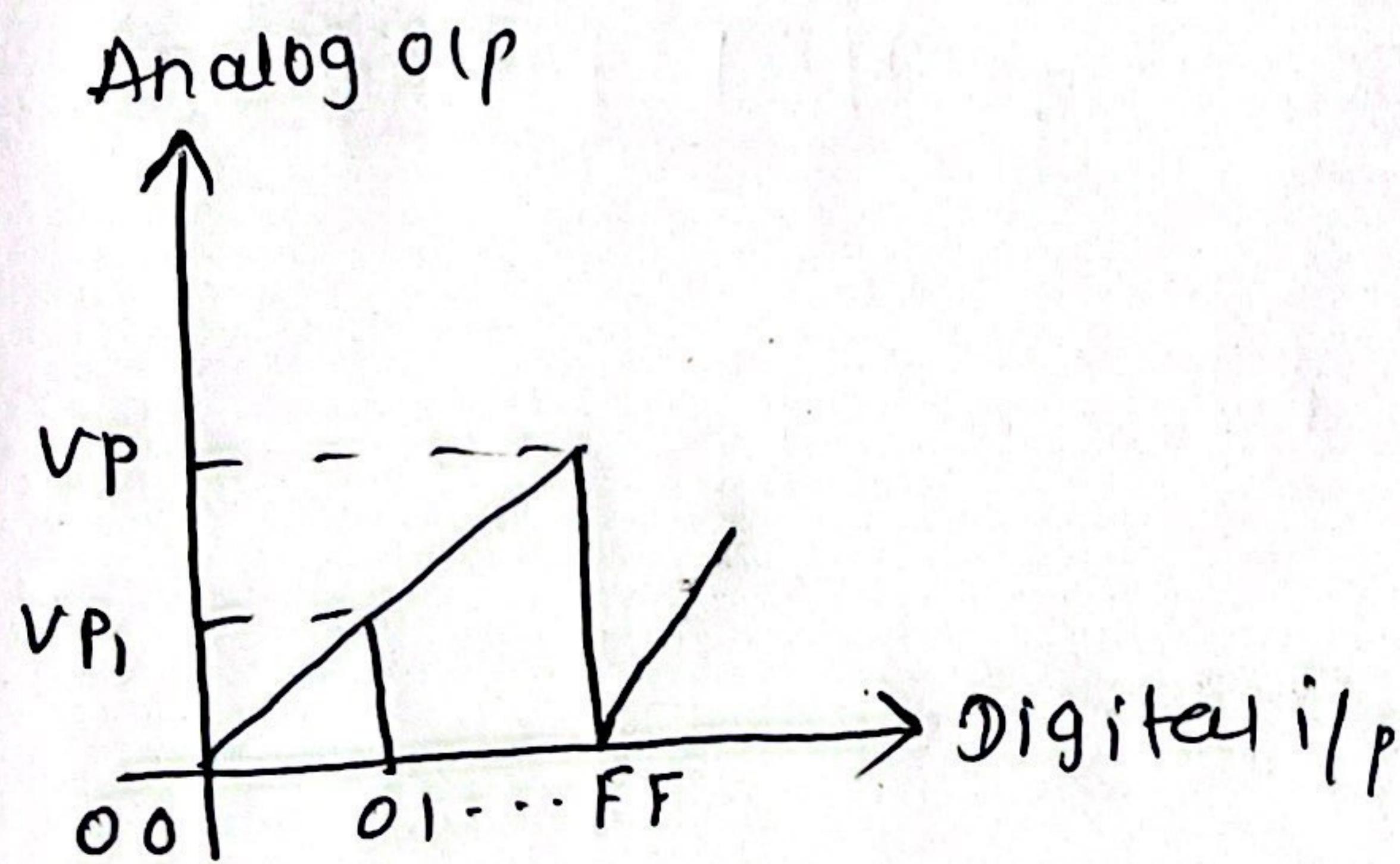
Fig: A 3-bit D/A converter.

port A → data O/p to DAC

port B → data Latch (O/p)

port C → read status of DAC

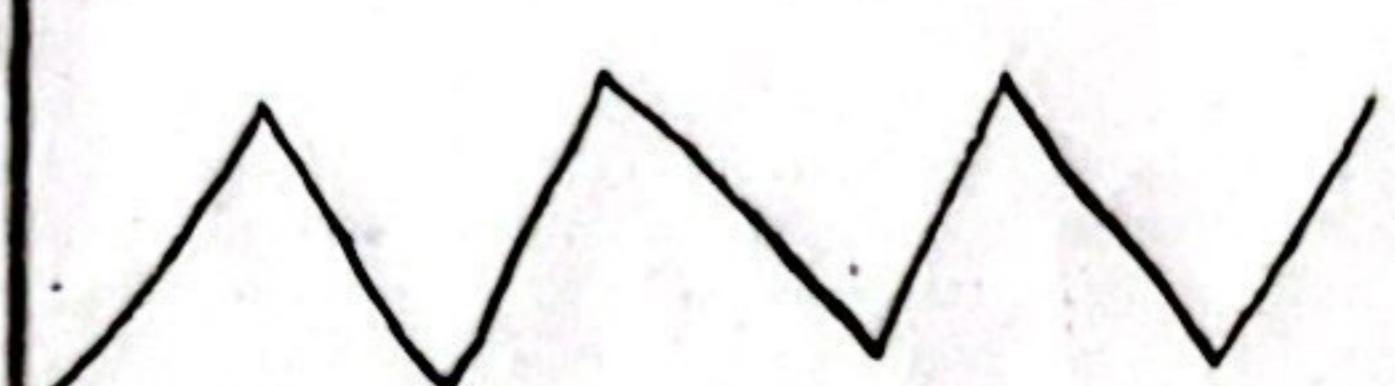
I/O control word: 1 0 0 0 1 0 0 1  
= 89H



Q:N1 WAP to generate a ramp waveform.

	Instruction	Opcode	After execution
9000	MVI A, 89H	3E 89	
9001			
9002	OUT 43	D3	
9003		43	
9004	MVI A, 01H	3E 01	
9005		D3	
9006	OUT 41H	41	
9007		3E	
9008	MVI A, 00H	00	
9009		D3	$f = 387.9\text{Hz}$
900A	OUT 40	40	$V_{PP} = 52.8\text{V}$
900B		3C	
900C	INRA	FE	
900D	CPI FFH	FF	
900E	JNZ 900A	C2	
900F		0A	
9010		90	
9011	JMP 9008	C3	
9012		08	
9013	RST 5	90 EF	

Q2 WAP to generate a triangular waveform-

Memory Address	Instruction	Opcode	After execution
9000	MVI A, 89H	3E	
9001		89	
9002	OUT 43H	D3	
9003		43	
9004	MVI A, 01H	3E	
9005		01	
9006	OUT 41H	D3	
9007		41	
9008	MVI A, 00H	3E	
9009		00	$f = 194.4 \text{ Hz}$
900A	OUT 40H	D3	
900B		40	$V_{PP} = 52.8 \text{ V}$
900C		3C	
900D	INR A	FE	
900E	CPI FFH	FF	
900F		C2	
9010	JNZ 9004	0A	
9011		90	
9012		3D	
9013	CLR A	D3	
9014	OUT 40H	4B	
9015		FE	
9016	CPI 00H	00	
9017		C2	
9018	JNZ 9012	12	
9019		90	
901A	JMP 9008	C3	
901B		08	
901C	RSTS	90	
		FF	

Q.WAP to generate a square wave form.

Memory address	Instruction	opcode	After execution
9000	MVI A, 89H	3E	
9001		89	
9002	OUT 43H	D3	
9003		43	
9004	MVI A, 01H	3E	
9005		01	
9006	OUT 41H	D3	
9007		41	
9008	MVI C, 0FH	OE	
9009		OF	
900A	MVI A, FFH	3E	
900B		FF	
900C	OUT 40H	D3	
900D		40	
900E	DCRC	0A	
900F	JNZ 900A	90	
9010		OE	
9011		OF	
9012	MVI C, OFH	3E	
9013		00	
9014	MVI A, 00H	D3	
9015		40	
9016	OUT 40H	0D	
9017		C2	
9018	DCRC	14	
9019	JNZ 9014	90	
901A		C3	
901B		08	
901C	JMP 9008	90	
901D			
901E			
901F	RST 5	EF	

## DISCUSSION AND CONCLUSION:-

with the reference to the theoretical knowledge regarding the concept of converting digital signal into the Analog signal.

Concluding the lab work, we were able to meet the objective. The code and corresponding output is also mentioned in this report.

# Interfacing x Analog to digital converter (ADC):

## Objective:

- To convert analog signal into the digital signal.

## THEORY:

The A/D converter is a quantizing process where by an analog signal is represented by equivalent binary states.

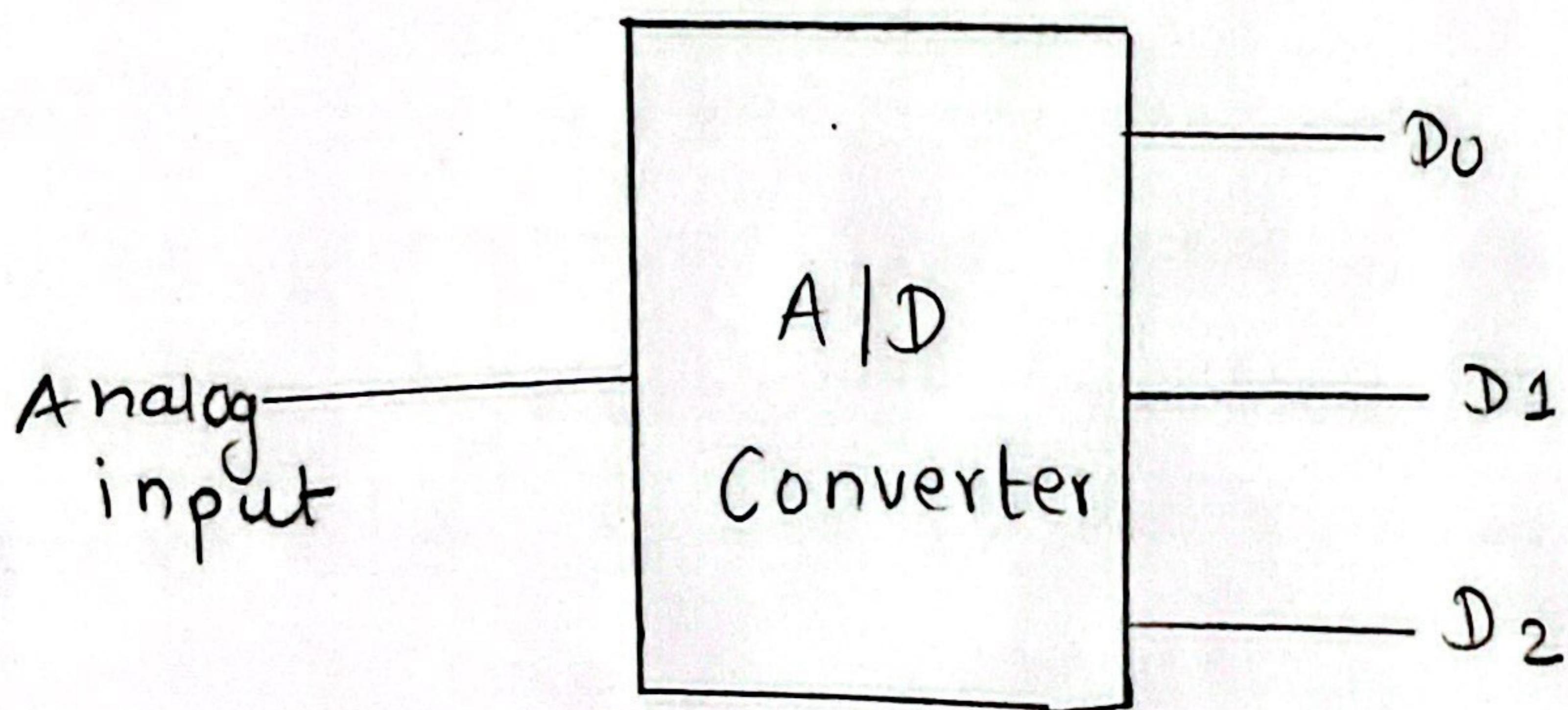


Fig: A 3-bit ADC block diagram.

## Types of ADC

Analog to digital converters are the following types:

1. Successive approximation (SA) ADC
2. Ramp ADC
3. dual slope ADC
4. parallel ADC

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Successive approximation principle can be easily understood using a simple example; the determination of the weight of an object. By using a balance and placing the object on one side and an approximate weight on the other side, the weight of the object is determined.

Successive approximation ADC works on the three major elements: the A/D converter, the SAR and the comparator. The conversion technique involves comparing the output of the D/A converter  $V_o$  with the analog input signal  $V_{in}$ .

When the DAC output matches the analog input to the DAC is equivalent digital signal. In the case of a 4-bit A/D converter, bit  $D_3$  is turned on first and the output of the DAC is compared with an analog signal.

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Memory Address	Instructions	OPCODE
8C00	MVIA, 81H	3E
8C01		81
8C02	OUT 43H	D3
8C03		43
8C04	START: MVIA,00H	06
8C05		00
8C06	LOOP1: IN 42H	DB
8C07		42
8C08	ANI 02H	E6
8C09		02
8C0A	JZ 8C06H	06
8C0B		8C
8C0C		CD
8C0D	CALL 8C4EH	4E
8C0E		8C
8C0F		DB
8C10	LOOP2: IN 42H	42
8C11		E6
8C12	ANI 02H	02
8C13		C2
8C14	JNZ 8C10H	10
8C15		8C
8C16		78
8C17	LOOP3: MOVA,B	D3
8C18		40
8C19		CD
8C1A	6UT UOH	UE
8C1B		8C
8C1C		42
8C1D	CALL 8CUEH	E6
8C1E	IN 42 H	01
8C1F		ANI 01H
8C20		

8C21	JZ 8C28H	CA
8C22		28
8C23		8C
8C24	INR B	04
8C25	JMP 8C17H	(B)
8C26		17
8C27		8C
8C28	FINISH: MOVA1B	F5
8C29	PUSH PSW	JB
8C2A	IN 50H	50
8C2B		E6
8C2C		08
8C2D	ANI 08H	C2
8C2E		U4
8C2F	JNZ 8C44H	8C
8C30		21
8C31	LXI H, 8C5AH	5A
8C32		8C
8C33		CD
8C34	CALL 0B5BH	5B
8C35		0B
8C36		F1
8C37	POP PSW	CD
8C38	CALL 0C41H	U1
8C39		0C
8C3A		CD
8C3B	CALL 0C5CH	5C
8C3C		0C
8C3D		CD
8C3E	CALL 0C5CH	5C
8C3F		0C
8C40		C3
8C41	JMP 8C04H	04
8C42		8C
8C43		
8C44	DISPKBD: POPPSW	F1

8C45	STA 8FF1H	32
8C46		F2
8C47		F1
8C48	CALL 0UUCH	8F
8C49		CD
8C4A		UC
8C4B	TMP 8C04H	04
8C4C		C3
8C4D		04
8C4E	DELAY: LXI H, 2000H	8C
8C4F		21
8C50		00
8C51	DCX D	20
8C52	MOV A, D	1B
8C53	ORA E	7A
8C54	JNZ 8C51H	B3
8C55		C2
8C56		51
8C57	RET	8C
		C9

8C5A	ORL 8C5AH	44
8C5B	DIGITAL: DB'DIGITAL VALUE':	49
8C5C		47
8C5D		49
8C5E		54
8C5F		41
8C60		UC
8C61		20
8C62		56
8C63		41
8C65		4C
8C67		3A
8C68		20
8C69		20

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