

Week 2:

- 1.) Write short note on concepts behind register transfer level (RTL).

Ans:

Register-transfer level (RTL) is a design abstraction which models a synchronous digital circuit in terms of the flow of digital signals (data) between hardware registers, and the logical operations performed on those signals.

Register-transfer level abstraction is used in hardware description languages (HDLs) like Verilog and VHDL to create high-level representation of a circuit, from which lower-level representation and ultimately actual wiring can be derived.

Designs using the Register-Transfer Level specify the characteristics of a circuit using operations and the transfer of data between the registers. Modern definition of an RTL code is "Any code that is synthesizable is called RTL code."

RTL is used in the logic design phase of the integrated circuit design cycle. An RTL description is usually converted to a gate-level description of the circuit by a logic synthesis tool. The synthesis results are then used by placement and routing tools to create a physical layout. Logic simulation tools may use a design's RTL description to verify its correctness.

- Differentiate combinational logic and sequential logic with some components.



### Combinational Logic

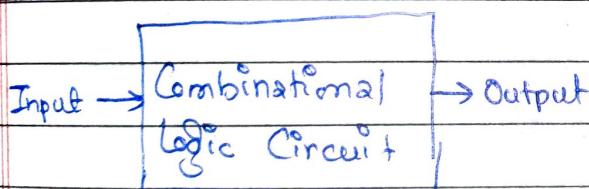
It is the logic circuit in which the output is a function of the present inputs (Time Independent Logic).

2. It does not have the ability to store data.

3. It does not require any feedback.

4. It is independent of clock and does not require triggering to operate.

Example: Adder, Subtractor.



Combinational logic

### Sequential logic

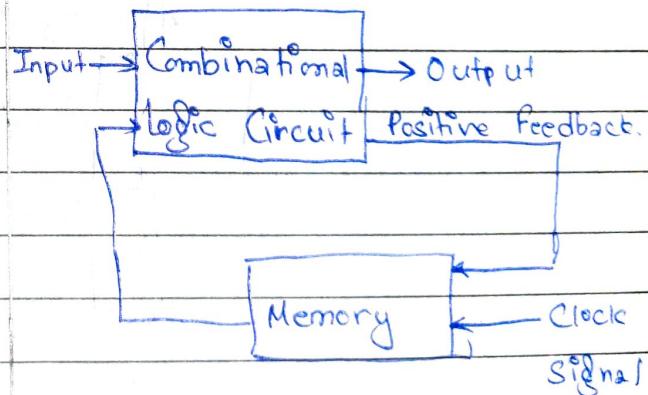
It is the logic circuit in which the output is a function of clock, present inputs and the previous states of the system.

It has memory to store the present states.

It involves feedback from output to input that is stored in the memory for the next operation.

It is clocked and is triggered for operation with electronic pulses.

Example: Counter, Register.



Sequential logic

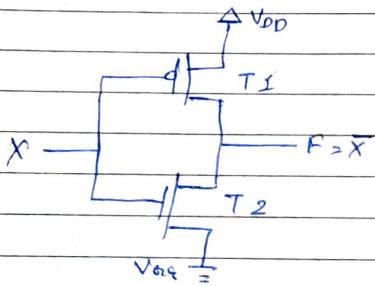


- 2) Write short notes on CMOS transistor & with material composition and describe the operation of the transistor as a switch with gate voltage.

Ans:

CMOS transistor is a semiconductor technology used in the transistors that are manufactured into most of today's computer microchips. Semiconductors are most of silicon and germanium materials which "sort of" conduct electricity, but not enthusiastically. Areas of these materials that are "doped" by added impurities become full-scale conductors of either extra electrons with a negative charge or of positive charge carriers. In CMOS technology, both kinds of transistor are used in a complementary way to form a current gate that forms an effective means of electrical control.

CMOS as a switch:



Truth table

X	F = \bar{X}
0	1
1	0

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c) Design problem:

Y is '1' if a is '1' or b and c are '1'.

Z is '1' if b or 'c' is '1', but not both, or if all are '1'.

Here,

Truth table:

a	b	c	Y	Z
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

b) K-map:

For Y

a \ bc	00	01	11	10
0	0	0	1	0
1	1	1	1	1

For Z

a \ bc	00	01	11	10
0	0	0	1	1
1	0	1	0	1

$$Y = a + bc$$

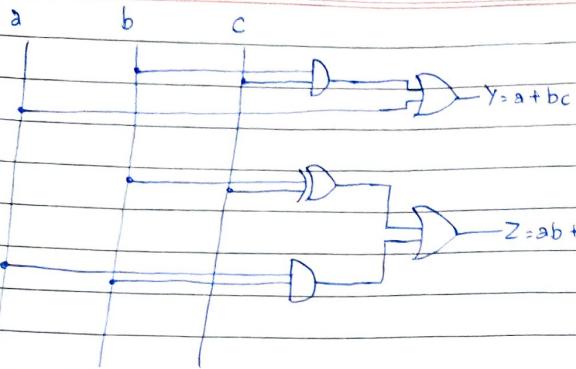
$$\begin{aligned} Z &= \bar{b}c + \bar{b}\bar{c} + ab \\ &= ab + b \oplus c \end{aligned}$$

$$\therefore Y = a + bc$$

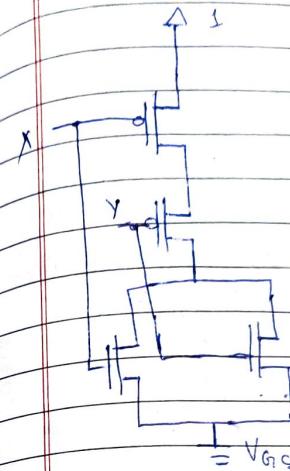
$$Z = ab + b \oplus c$$

c) Circuit diagram.





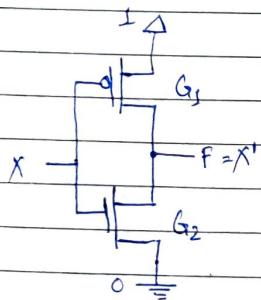
NOR gate with nMOS and pMOS transistor.



- 3.) Present how Inverter, NOR gate and NAND gate with nMOS and pMOS transistors.

Ans:-

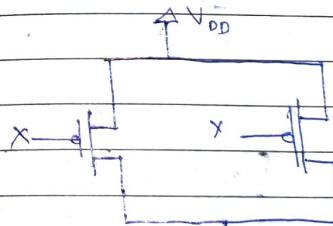
Inverter with nMOS and pMOS transistor.



When  $X = 0$ , Gate transistor  $G_1$  conducts and  $G_2$  does not. So, output  $F$  is 1. Similarly at  $X = 1$ , Gate  $G_2$  conducts but  $G_1$  does not. So, output is 0.

X	$F = \bar{X}$
0	1
1	0

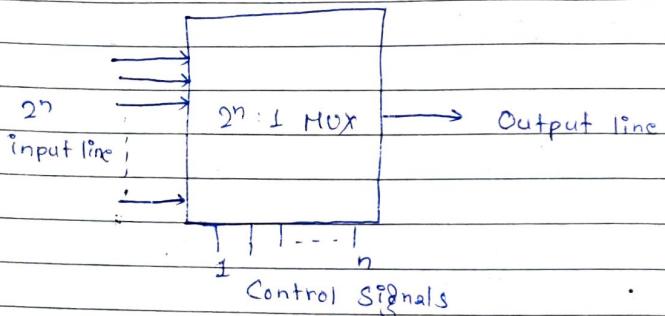
NAND gate with nMOS and pMOS transistor



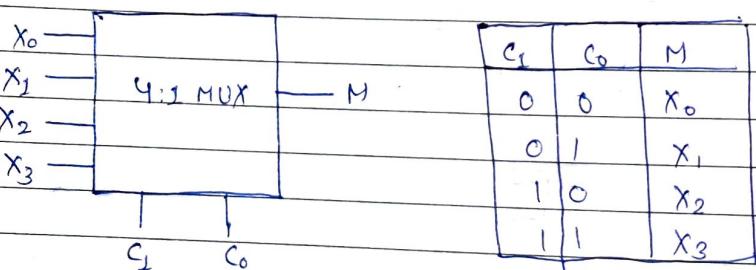
- 5.) Write short notes on combinational components with block diagram:  
Multiplexer, decoder, adder, arithmetic-logic unit (ALU).

### Multiplexer:

A multiplexer (or MUX) is a device that selects between several analog or digital input signals and forwards it to a single output line. A multiplexer of  $2^n$  inputs has  $n$  select lines and 1 output line. It is also known as data selector.



For 4:1 MUX:



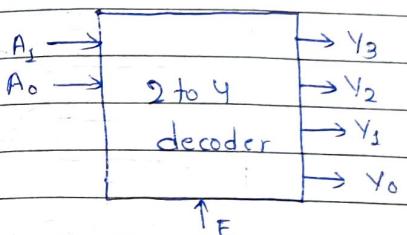
### Applications:

- (i) Communication system
- (ii) Computer memory
- (iii) Telephone Network

### Decoder:

Decoder is a combinational circuit that has ' $n$ ' input lines and maximum of  $2^n$  output lines. One of these outputs will be active High based on the combination of inputs present, when the decoder is enabled.

### 2:4 Decoder



### Truth table:

Enable E	Inputs		Outputs			
	A <sub>1</sub>	A <sub>0</sub>	Y <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

### Boolean functions:

$$Y_3 = E \cdot A_1 \cdot A_0$$

$$Y_2 = E \cdot A_1 \cdot A_0'$$

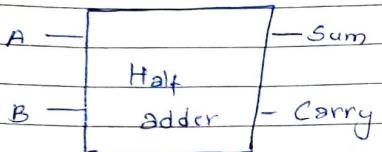
$$Y_1 = E \cdot A_1' \cdot A_0$$

$$Y_0 = E \cdot A_1' \cdot A_0'$$

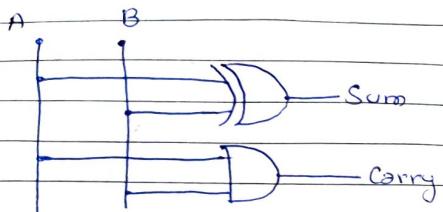
### Adder:

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors adders are added in ALU. It is of two main types: Half adder, Full adder.

### Half adder:



Block Diagram



Logic Diagram

### Boolean expression:

$$\text{Sum} = A \oplus B$$

$$\text{Carry} = A \cdot B$$

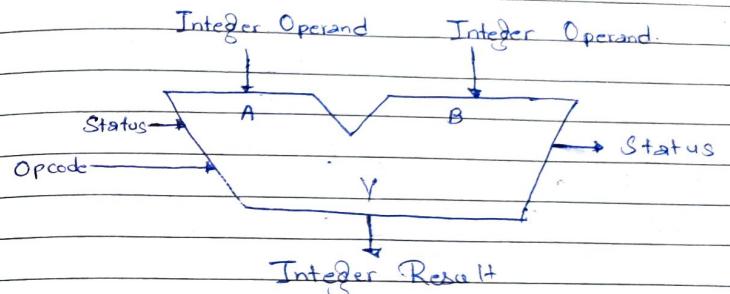
### Truth table:

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half adder adds two single binary digits A and B. It has two outputs, sum and carry (C).

### Arithmetic - Logic Unit

An arithmetic logic unit (ALU) is a combinational digital electronic circuit that performs arithmetic and bitwise operations on integer binary numbers. An ALU is a fundamental building block of many types of computing circuits, including the CPU of computers, FPGAs and GPUs. A single CPU, FPU or GPU may contain multiple ALUs.

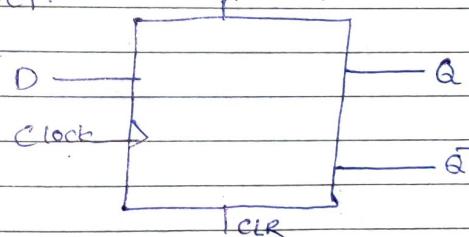


Symbolic Representation of ALU.

- Q) Write short notes on D-flip-flop, SR flip-flop, JK flip flop with block diagram & truth table

Ans:

D-type flip-flop is a modified Set-Reset flip-flop with the addition of an inverter to prevent the S and R inputs from being at the same logic level.

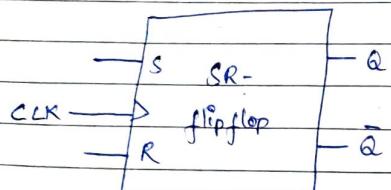


Block Diagram

CLK	D	Q	$\bar{Q}$	Description
↓	X	Q	$\bar{Q}$	No change
↑	0	0	1	Reset
↑	1	1	0	Set.

### SR-flip-flop:

SR flip-flop is one of the most basic sequential logic circuit possible. The SR description stands for Set-Reset.



### Block Diagram:

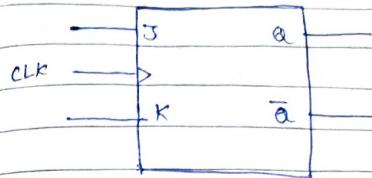
### Truth table:

CLK	S	R	Q	$\bar{Q}$	Decision
↑	0	0	$Q_0$	$\bar{Q}_0$	Previous output
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	X	X	Invalid

### JK Flip-flop:

JK flip flop is basically a gated SR flip-flop with the addition of clock input circuitry.

### Block Diagram:



### Truth table:

CLK	J	K	Q	$\bar{Q}$	
↑	0	0	$Q_0$	$\bar{Q}_0$	Previous Output
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	$\bar{Q}_0$	$Q_0$	Toggle

### Short notes:

#### i) Register:

Registers are groups of flip-flops, where each flip-flop is capable of storing one bit of information. A n-bit register is a group of n flip-flops.

The basic function of a register is to hold information in a digital system and make it available to the logic element for computing process.

There are 4 types of registers:

1. Serial-in-serial-out (SISO)
2. Serial-in-parallel-out (SIPO)
3. Parallel-in-serial-out (PISO)
4. Parallel-in-parallel-out (PIPO).

### ii) Shift Register

A shift register is a cascade of flip-flops, sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position in the bit array stored in it, "shifting in" the data present at its input and "shifting out" the last bit in the array, at each transition of clock input.

Shift registers can have both parallel and serial inputs and output. There are also "bidirectional" shift registers.

### iii) Counter.

A counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal.

A counter circuit is usually constructed of a numbers of flip-flops connected in cascade. Counters are very widely used component in digital circuits, and manufactured as separate integrated circuits.

There are two types of counters:

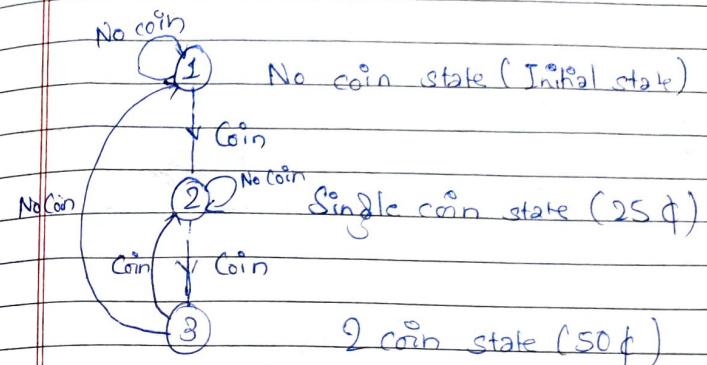
i) Asynchronous counter: Changing state bits are used as clock to subsequent state flip-flops.

ii) Synchronous counter: All state bits change under control of a single clock.

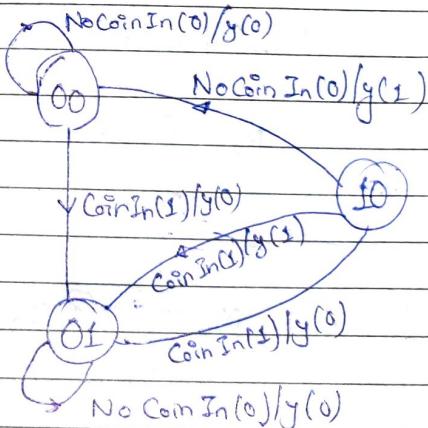
Q) A vending machine which accepts 25 p and needs 50 p. Design a combinational logic and implementation block model.

Ans:

State Diagram:



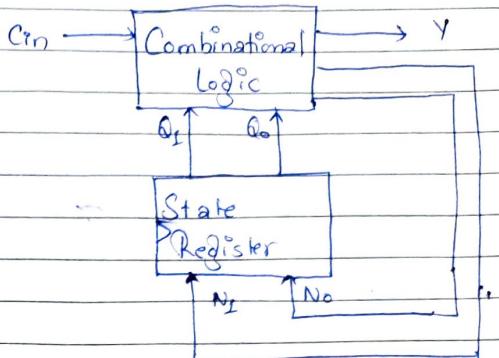
Finite State Diagram :



Truth table:

Inputs		Input $Cin$	Next State		Output $y$
State $Q_1$	$Q_0$		$N_1$	$N_0$	
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	0	1	1

Implementation Model



K-maps:

For  $y$ :

$Q_1$	Q <sub>0</sub>			
	00	01	11	10
0	0	0	0	0
-1	(1)	1	X	X

For  $N_1$ :

$Q_1$	Q <sub>0</sub>				$Cin$
	00	01	11	10	
0	0	0	0	0	
1	0	1	X	X	

$$y = Q_1$$

$$N_1 = Q_0 \oplus Cin$$

For  $N_0$ :

$Q_1$	Q <sub>0</sub>				$Cin$
	00	01	11	10	
0	0	1	0	1	
1	0	1	X	X	

$$N_0 = Q_0 \oplus Cin$$

Circuit Diagram:

