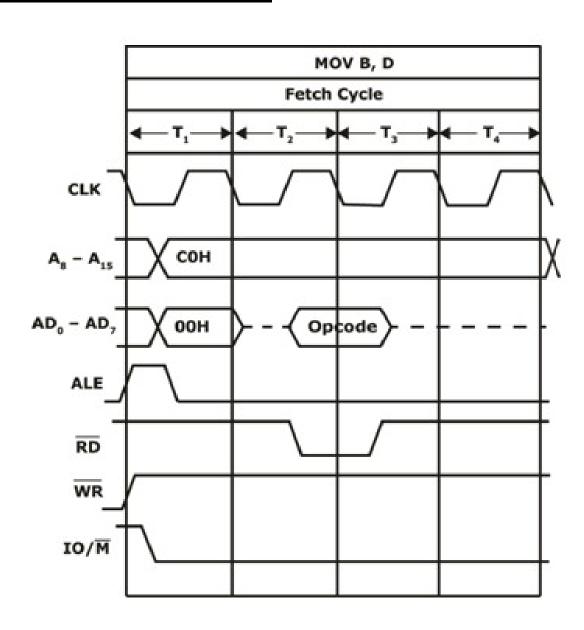
Example (MOV B, D)

C000	OPCODE
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Instruction cycle of MOV B, D Fetch cycle	$T_1:$ $T_2:$ $T_3:$ $T_4:$	MAR MBR IR B	← PC ← [MAR] ← MBR, PC← PC + 1 ← D
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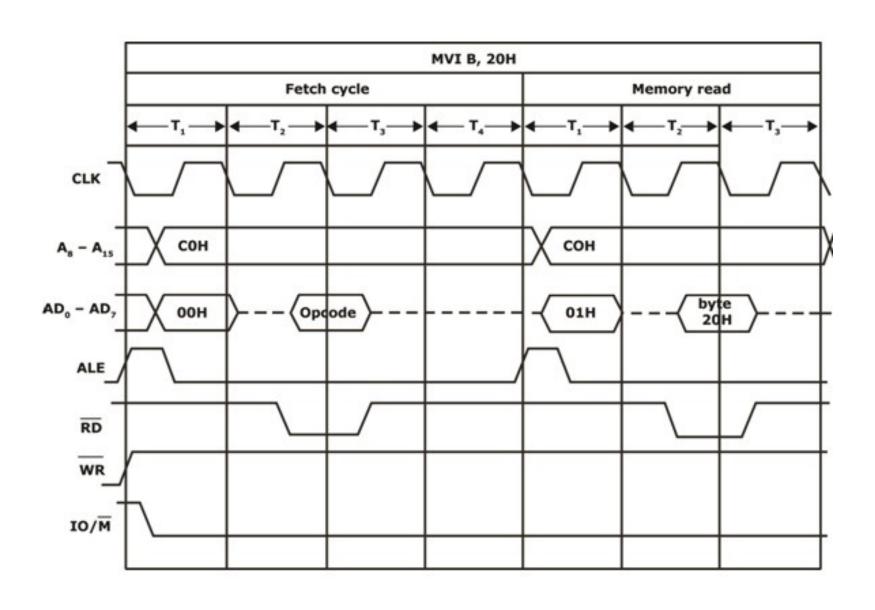


Example (MVI B, 20H)

C000	OPCODE
C001	20

on cycle B, 20H	Fetch cycle	$T_1:$ $T_2:$ $T_3:$ $T_4:$	MAR ← PC MBR ← [MAR] IR ← MBR, PC← PC + 1 Unspecified
Instruction of MVI B, 2	Memory Read cycle	T ₅ : T ₆ : T ₇ :	$\begin{array}{ll} MAR \leftarrow PC \\ MBR \leftarrow [MAR] \\ B & \leftarrow MBR, PC \leftarrow PC + 1 \end{array}$

Example (MVI B, 20H)

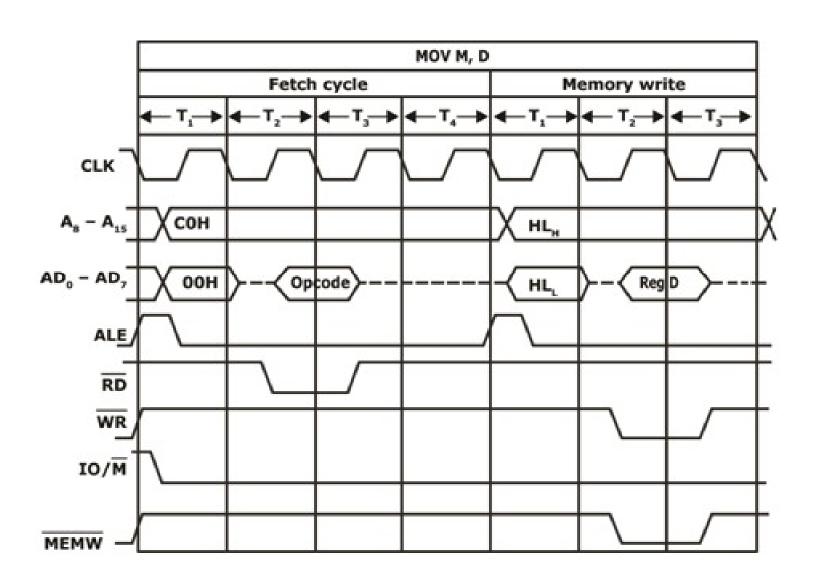


Example (MOV M, D)

C000	OPCODE

on cycle V M, D	Fetch cycle	$T_1:$ $T_2:$ $T_3:$ $T_4:$	MAR ← PC MBR ← [MAR] IR ← MBR, PC← PC+1 Unspecified
Instruction cycle of MOV M, D	Memory Write cycle	T ₅ : T ₆ : T ₇ :	$\begin{array}{l} MAR \leftarrow HL \\ MBR \leftarrow D \\ [MAR] \leftarrow MBR \end{array}$

Example (MOV M, D)

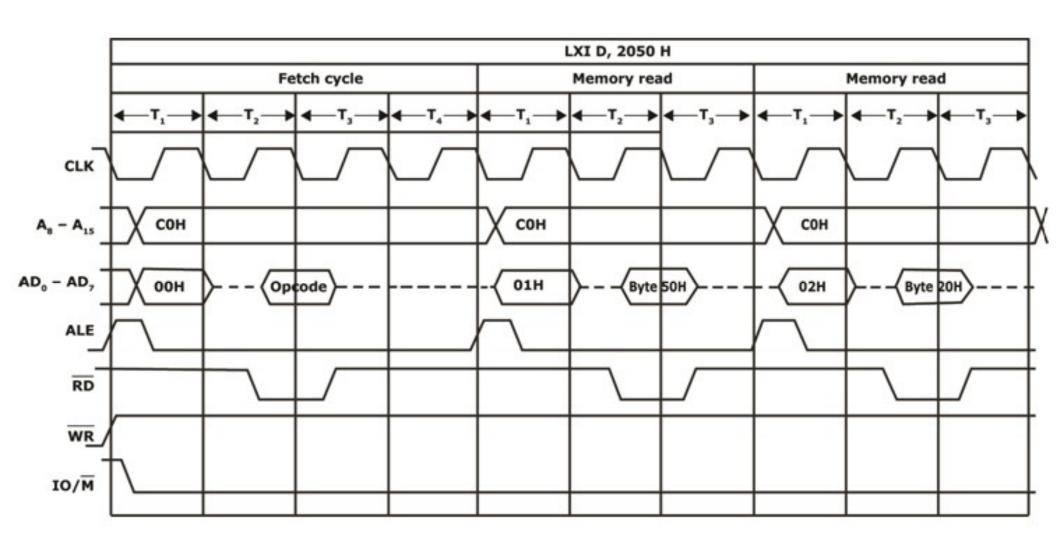


Example (LXI D, 2050H)

C000	OPCODE
C001	50
C002	20

I D, 2050H	Fetch cycle	T_1 : T_2 : T_3 : T_4 :	MAR ← PC MBR ← [MAR] IR ← MBR, PC← PC + 1 Unspecified
Instruction cycle of LXI D, 2050H	Memory Read cycle	T ₅ : T ₆ : T ₇ :	$MAR \leftarrow PC$ $MBR \leftarrow [MAR]$ $E \leftarrow MBR, PC \leftarrow PC + 1$
Instruction	Memory Read cycle	T ₈ : T ₉ : T ₁₀ :	$MAR \leftarrow PC$ $MBR \leftarrow [MAR]$ $D \leftarrow MBR, PC \leftarrow PC + 1$

Example (LXI D, 2050H)

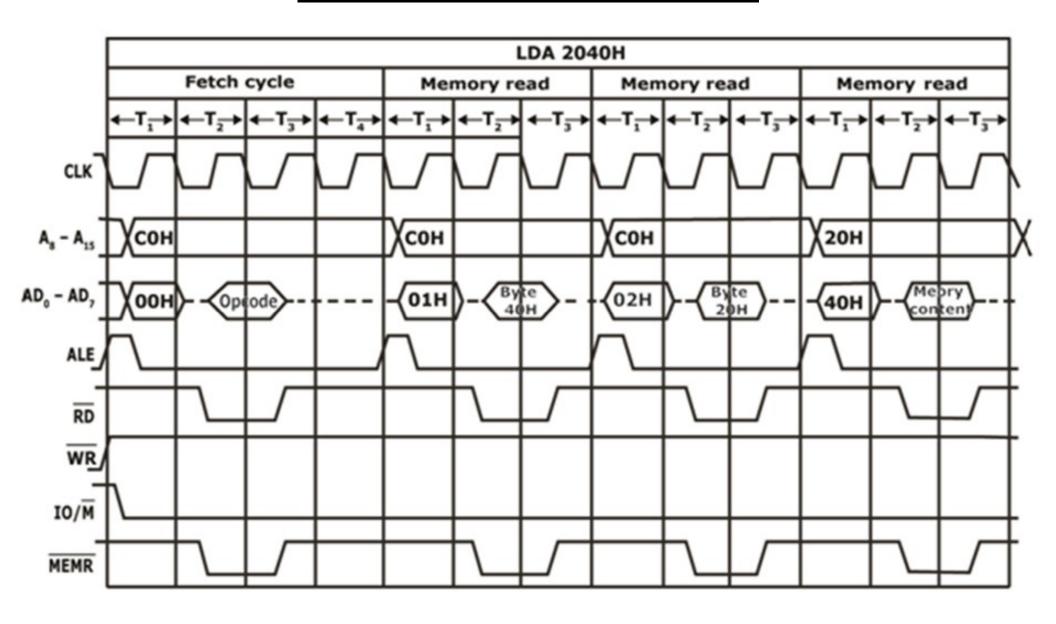


Example (LDA 2040H)

C000	OPCODE
C001	40
C002	20

	le	T ₁ :	MAR ← PC
	cyc	T ₂ :	$MBR \leftarrow [MAR]$
	Fetch cycle	T ₃ :	IR \leftarrow MBR, PC \leftarrow PC + 1
	Fe	T4:	Unspecified
040H	Read	T ₅ :	MAR ← PC
)A 2	ory I	T ₆ :	$MBR \leftarrow [MAR]$
Instruction cycle of LDA 2040H	Memory Read cycle	T ₇ :	$Z \leftarrow MBR, PC \leftarrow PC + 1$
" cycl	Read	Ts:	MAR ← PC
ctio	rry 1	T ₉ :	$MBR \leftarrow [MAR]$
Instru	Memory Read cycle	T ₁₀ :	$W \leftarrow MBR, PC \leftarrow PC + 1$
		T ₁₁ :	MAR ← WZ
	ycle	T ₁₂ :	$MBR \leftarrow [MAR]$
6	Memory Read cycle	T ₁₃ :	A ← MBR

Example (LDA 2040H)



Example (OUT FOH)

C000	OPCODE
C001	FO

Fetch cycle T_1 : $MAR \leftarrow PC$ T_2 : $MBR \leftarrow [MAR]$ Instruction cycle of OUT FOH T_3 : IR \leftarrow MBR, PC \leftarrow PC + 1 T_4 : Unspecified Memory Read cycle T_5 : $MAR \leftarrow PC$ T_6 : $MBR \leftarrow [MAR]$ $Z \leftarrow MBR, PC \leftarrow PC + 1$ T_7 : VO Write cycle T_8 : IOAR ←Z To: IOBR \leftarrow A T_{10} : [IOAR] ← IOBR

Example (OUT FOH)

