Multicycle Processor

EE309: Microprocessor

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1 The States

S_1

$PC \rightarrow ALU - A, iMeM_A$
$+1 \rightarrow ALU - B$
$ALU - C \rightarrow PC$
$iMeM_D \rightarrow IR, T_0$

S_2

'111' $\rightarrow A_3$
$PC \rightarrow D_3$

S_3

$IR_{9 \rightarrow 11} \rightarrow A_1$
$IR_{6 \rightarrow 8} \rightarrow A_2$
$D_1 \rightarrow T_1$
$D_2 \rightarrow T_2$

S_{31}

$IR_{9 \rightarrow 11} \rightarrow A_1$
$D_1 \rightarrow T_1$
$IR_{0 \rightarrow 5} \rightarrow SE \rightarrow T_2$

S_{32}

$IR_{9 \rightarrow 11} \rightarrow A_3$
$IR_{0 \rightarrow 8} \rightarrow SE \rightarrow shift_7 \rightarrow D_3$

S_4

$T_1 \rightarrow ALU - A$
$T_2 \rightarrow Shifter(IR_0 AND IR_1)$
$ALU - C \rightarrow T_0$

S_5

if(IR_{12} OR $IR_{13} = 1$):
$IR_{3-5} \rightarrow A_3$
else:
$IR_{6-8} \rightarrow A_3$
$T_0 \rightarrow D_3$

S_6

$IR_{6 \rightarrow 8} \rightarrow A_2$
$D_2 \rightarrow T_2$
$IR_{0 \rightarrow 5} \rightarrow SE \rightarrow T_1$

S_7

$T_1 \rightarrow ALU - A$
$T_2 \rightarrow ALU - B$
$ALU - C \rightarrow T_0$

S_8

$T_0 \rightarrow dMeM_A$
$dMeM_D \rightarrow T_0$

S_9

$IR_{9 \rightarrow 11} \rightarrow A_3$
$T_0 \rightarrow D_3$

S_{10}

$T_1 \rightarrow ALU - A$
$T_2 \rightarrow ALU - B$
$ALU - C \rightarrow T_0$
$IR_{9 \rightarrow 11} \rightarrow A_1$
$D_1 \rightarrow T_1$

$$\frac{S_{11}}{\begin{array}{c}T_0 \rightarrow dMeM_A \\ T_1 \rightarrow dMeM_D\end{array}}$$

$$\frac{S_{17}}{\begin{array}{c}T_1 \rightarrow shift(1) \rightarrow T_1 \\ count++\end{array}}$$

$$\frac{S_{12}}{\begin{array}{c}IR_{0\rightarrow 8} \rightarrow SE(7) \rightarrow shift(7) \rightarrow T_1 \\ counter_{reset}\end{array}}$$

$$\frac{S_{18}}{\begin{array}{c}IR_{9\rightarrow 11} \rightarrow A_3 \\ D_3 \rightarrow T_0\end{array}}$$

$$\frac{S_{13}}{\begin{array}{c}T_1 \rightarrow ALU - A \\ \text{'1000000000000000'} \rightarrow ALU - B \\ ALU - C \rightarrow T_0\end{array}}$$

$$\frac{S_{19}}{\begin{array}{c}dMem_D \rightarrow T_2 \\ T_0 \rightarrow ALU - A, dMeM_A \\ +1 \rightarrow ALU - B \\ ALU - C \rightarrow T_0\end{array}}$$

$$\frac{S_{14}}{\begin{array}{c}count_{out} \rightarrow A_2 \\ D_2 \rightarrow T_2 \\ IR_{9\rightarrow 11} \rightarrow A_3 \\ D_3 \rightarrow T_0\end{array}}$$

$$\frac{S_{20}}{\begin{array}{c}count_{out} \rightarrow A_3 \\ T_2 \rightarrow D_3\end{array}}$$

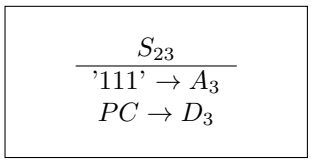
$$\frac{S_{15}}{\begin{array}{c}T_0 \rightarrow ALU - C, dMeM_A \\ T_2 \rightarrow dMeM_D \\ +1 \rightarrow ALU - B \\ ALU - C \rightarrow T_0\end{array}}$$

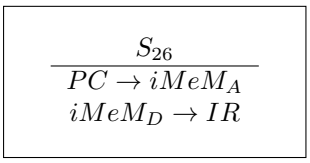
$$\frac{S_{21}}{\begin{array}{c}T_0 \rightarrow ALU - A \\ -1 \rightarrow ALU - B \\ ALU - C \rightarrow T_0 \\ IR_{0\rightarrow 5} \rightarrow SE(10) \rightarrow T_2\end{array}}$$

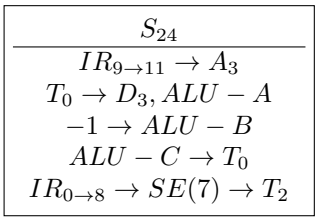
$$\frac{S_{16}}{\begin{array}{c}T_1 \rightarrow shift(1) \rightarrow T_1 \\ IR_{9\rightarrow 11} \rightarrow A_3 \\ T_0 \rightarrow D_3 \\ count++\end{array}}$$

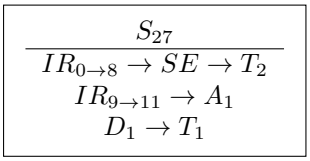
$$\frac{S_{22}}{\begin{array}{c}T_0 \rightarrow ALU - A \\ T_1 \rightarrow ALU - B \\ ALU - C \rightarrow PC\end{array}}$$

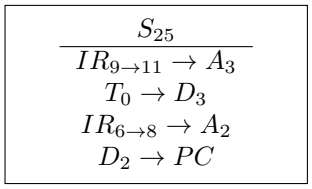
$$\frac{S_{23}}{\begin{array}{c}\text{'111'} \rightarrow A_3 \\ PC \rightarrow D_3\end{array}}$$









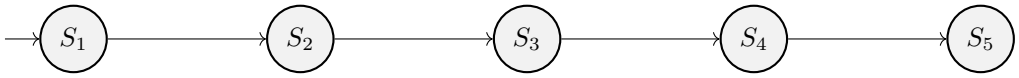


Salient points:

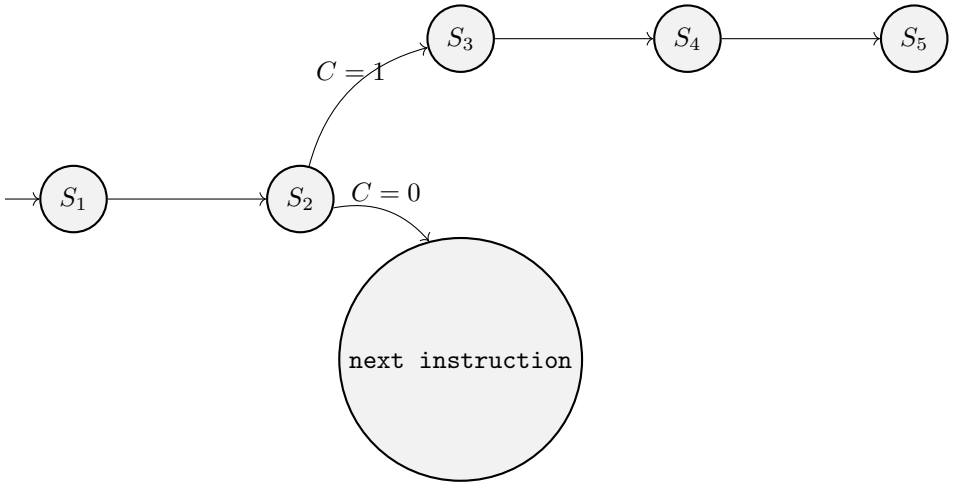
- To minimise the number of states, some conditions based on the instructions are introduced as can be seen in S_4 or S_5
- An additional counter is added to keep track of the register bit to check in instruction LM or SM
- Masking is employed in state S_{13} to check whether the corresponding register bit is set or not

2 Instruction Flow

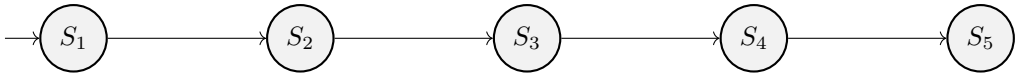
2.1 ADD



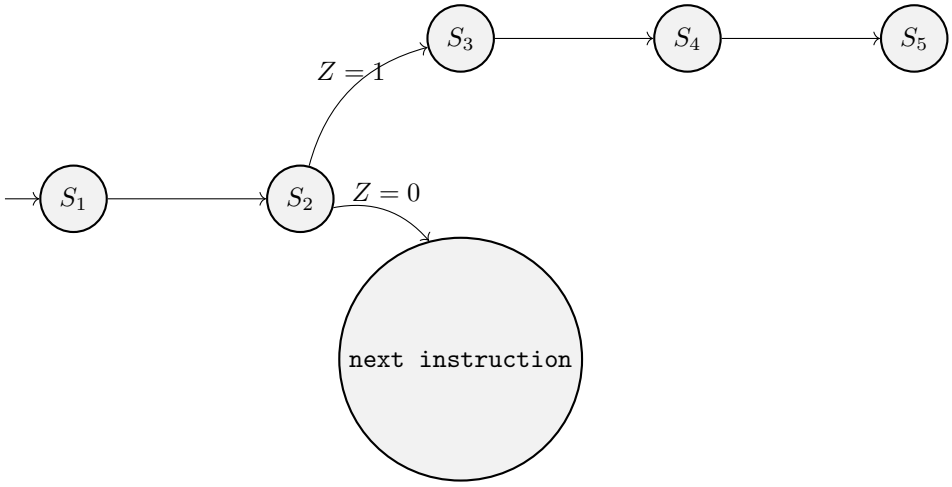
2.2 ADC



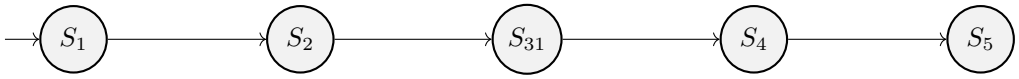
2.3 ADL



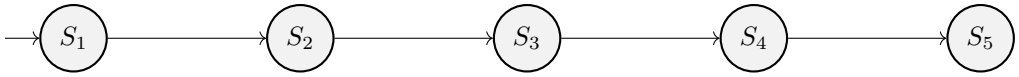
2.4 ADZ



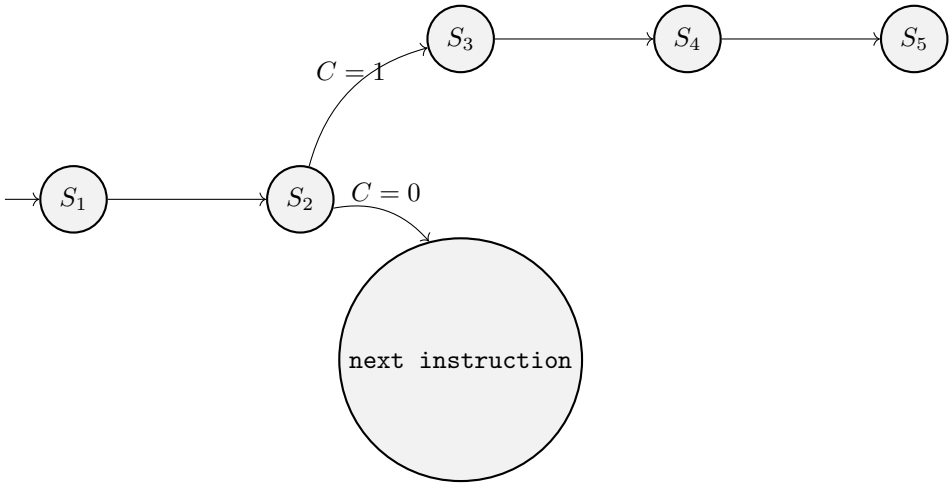
2.5 ADI



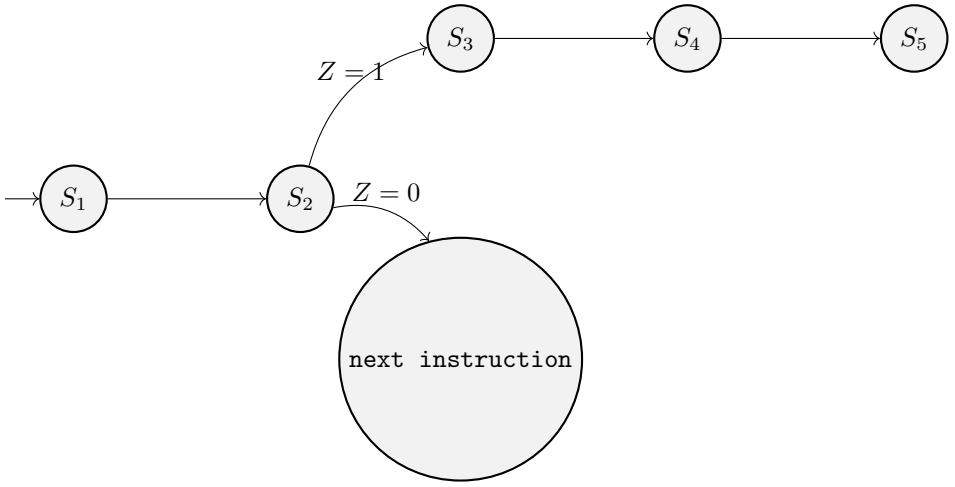
2.6 NDU



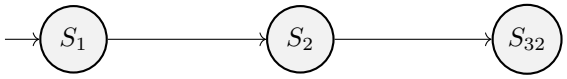
2.7 NDC



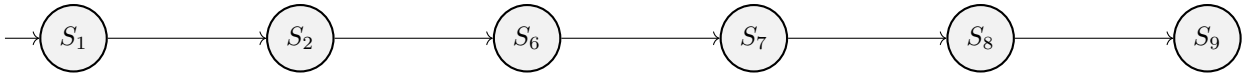
2.8 ADZ



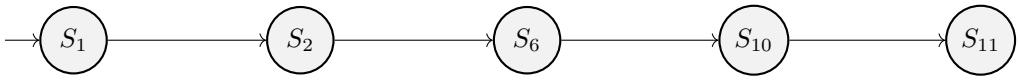
2.9 LHI



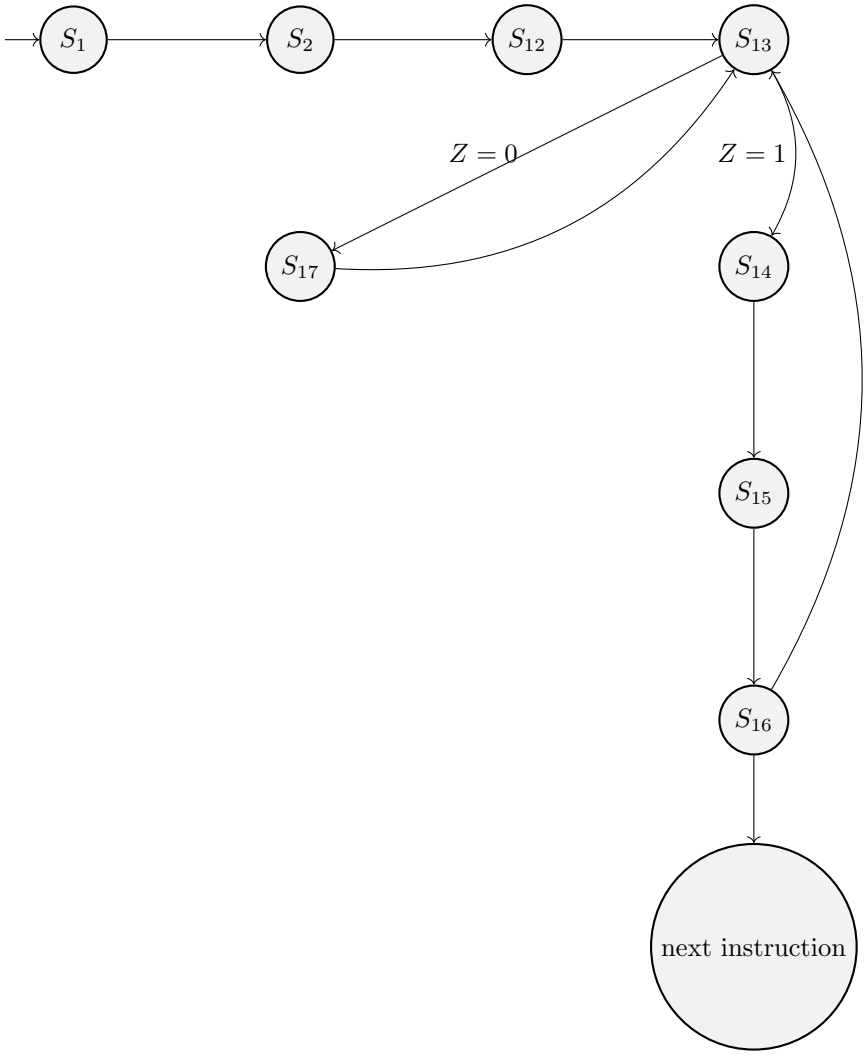
2.10 LW



2.11 SW

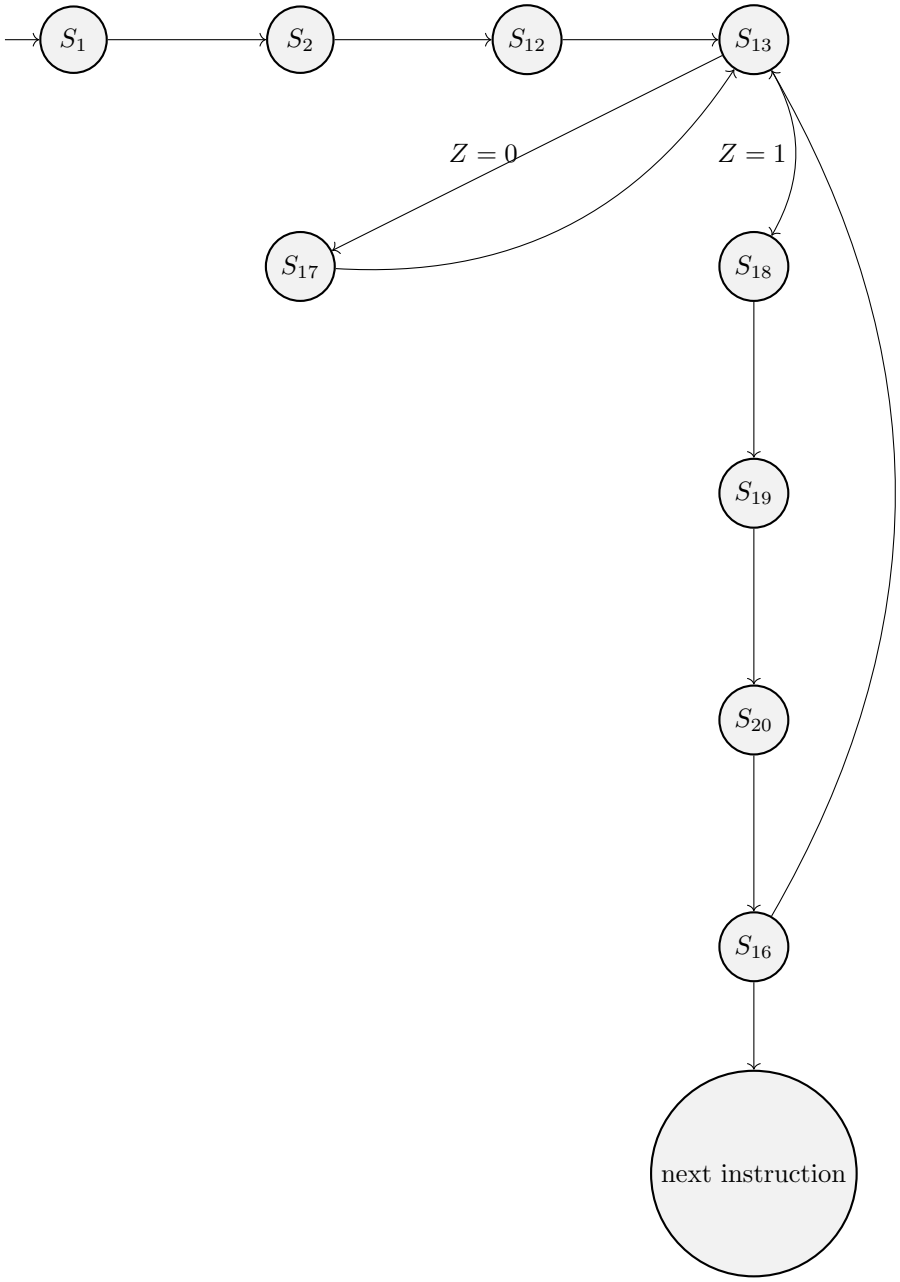


2.12 SM



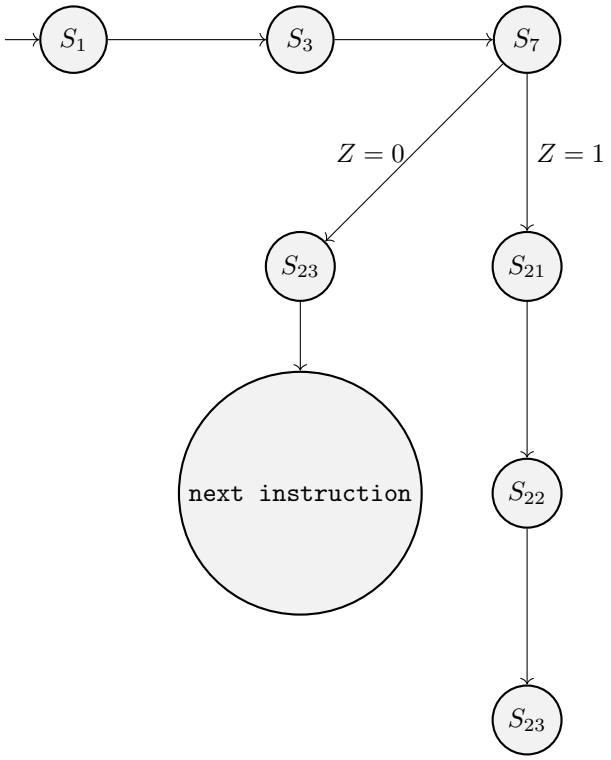
The loops are executed until all the registers bits aren't checked

2.13 LM



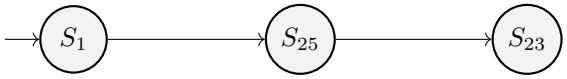
The loops are executed until all the registers bits aren't checked

2.14 BEQ

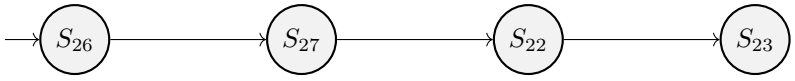


2.15 JAL

2.16 JLR



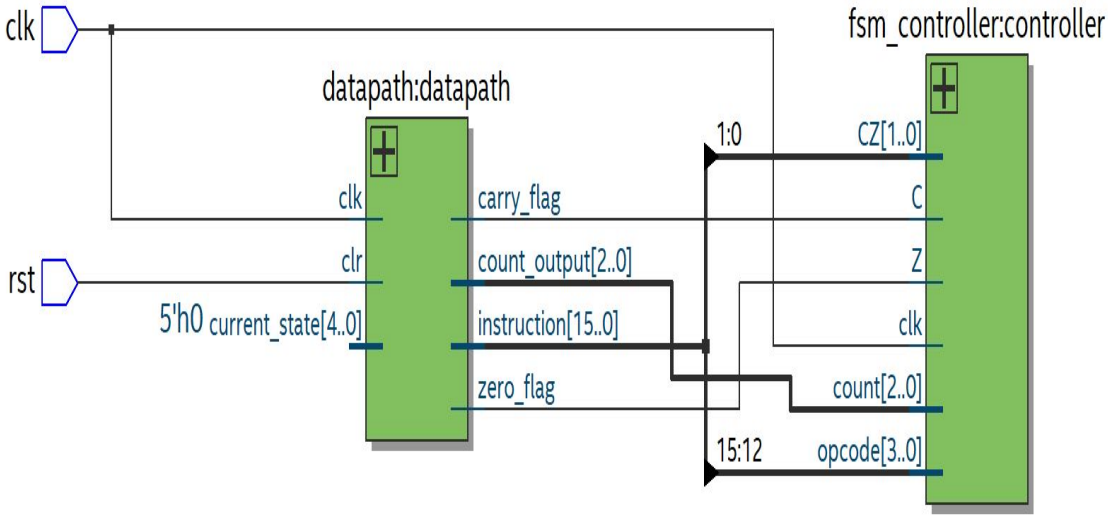
2.17 JRI



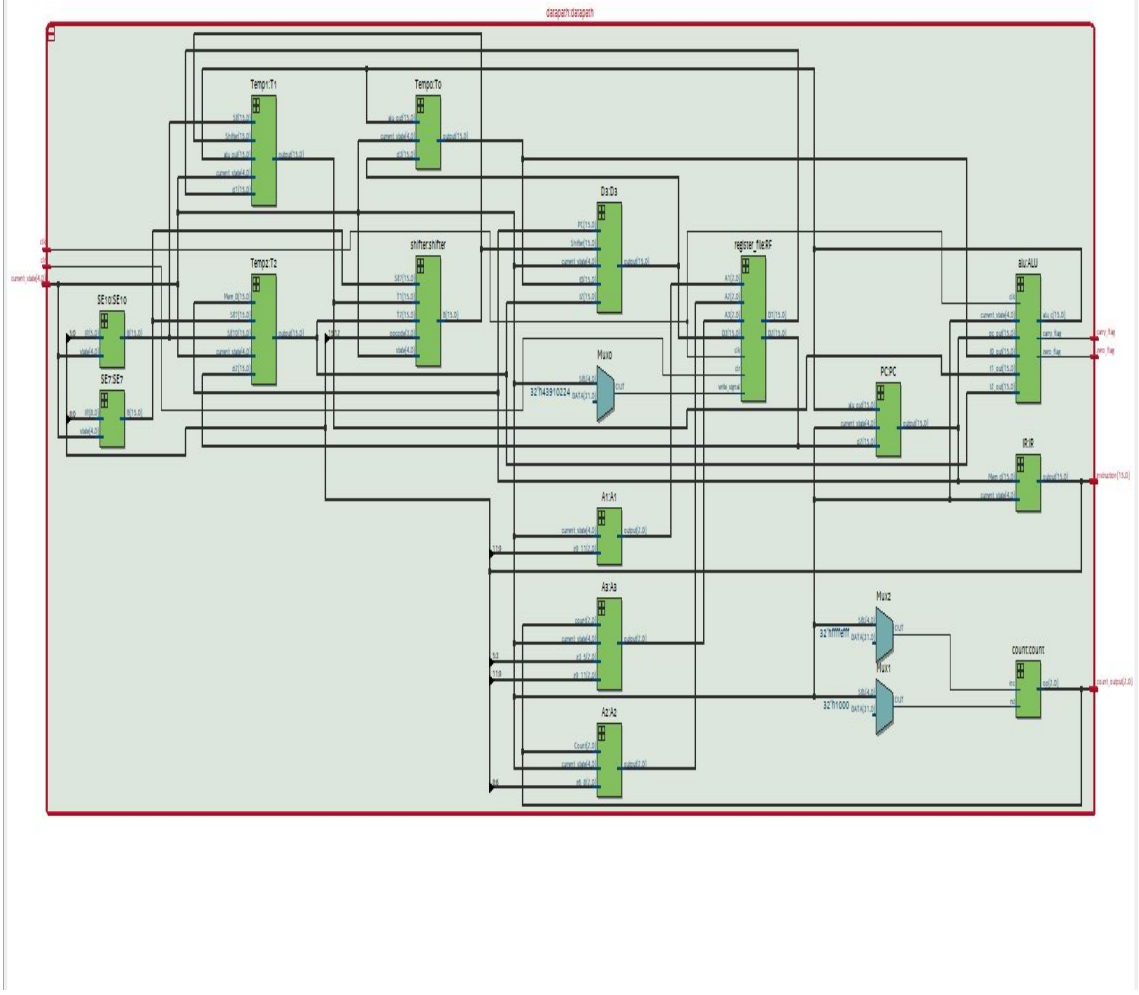
∗Condition C = 1/0 or Z = 1/0 refers to carry or zero flag being set or not respectively

3 Pictures

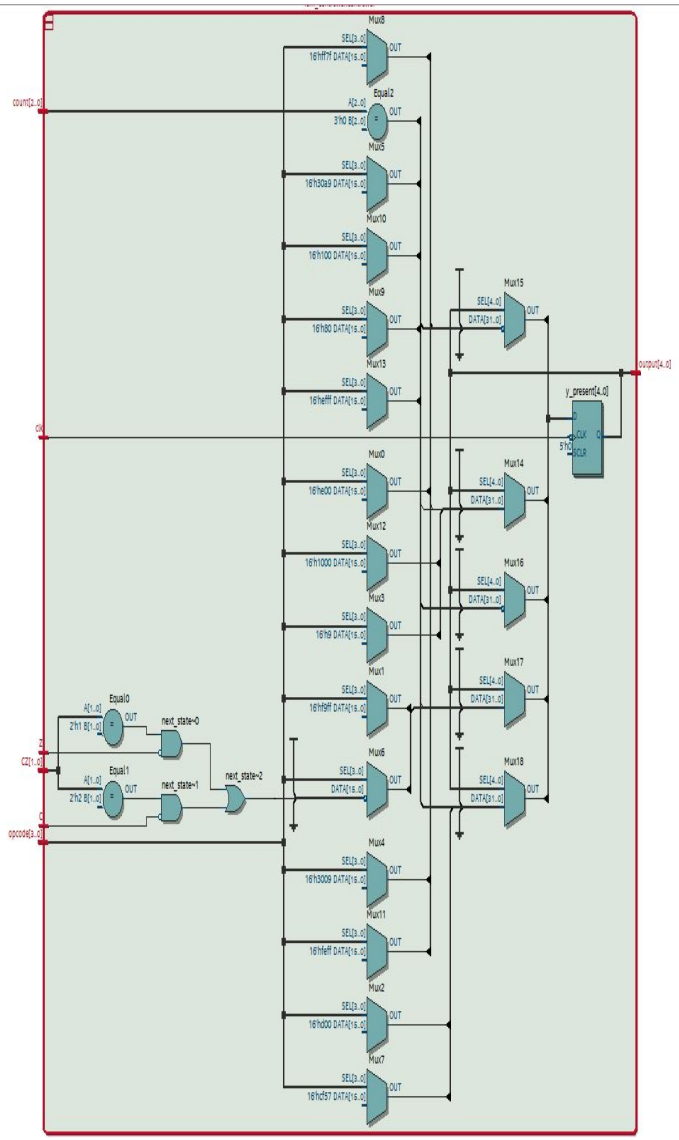
3.1 Overall Design



3.2 Datapath


datapath:datapath
Tempr:Tr
Tempo:To
Tempo:Tz
shifter:shifter
Da:Da
register_file:RF
alu:ALU
SE16:SE16
SE7:SE7
Mux0
PC:PC
IR:IR
At:At
Az:Az
Ao:Ao
Mux2
Mux1
count:count

3.3 Controller



4 State diagram of FSM