Instruction	Operand	Bytes / MachineCycle / T-States	Machine Cycle	Flags					Description	Machine Code
				S	Z	AC	P	CY		
ACI	DATA	2/2/7	F R	✔	✔	✔	✔	✔	Add 8-bit & CY to A	CE data
ADC	R	1/1/4	F	✔	✔	✔	✔	✔	Add R & CY to A	1000 1SSS
ADC	M	1/2/7	F R	✔	✔	✔	✔	✔	Add M & CY to A	8E
ADD	R	1/1/4	F	✔	✔	✔	✔	✔	Add R to A	1000 0SSS
ADD	M	1/2/7	F R	✔	✔	✔	✔	✔	Add M to A	86
ADI	DATA	2/2/7	F R	✔	✔	✔	✔	✔	Add 8-Bit to A	C6 data
ANA	R	1/1/4	F	✔	✔	1	✔	0	AND R with A	1010 0SSS
ANA	M	1/2/7	F R	✔	✔	1	✔	0	AND M with A	A6
ANI	DATA	2/2/7	F R	✔	✔	1	✔	0	AND 8-bit data with A	E6 data
CALL	ADDR	3/5/18	S R R W W						Call Unconditional	CD addr
CC	ADDR	3/5/9-18	S R R W W						Call on CY	DC addr
CM	ADDR	3/5/9-15	S R R W W						Call on Minus	FC addr
CMA		1/1/4	F						Complement A	2F
CMC		1/1/4	F					✔	Complement CY	3F
CMP	REG	1/1/4	F	✔	✔	✔	✔	✔	Compare R with A	1011 1SSS
CMP	M	1/2/7	F R	✔	✔	✔	✔	✔	Compare M with A	BE
CNC	ADDR	3/5/9-18	S R R W W						Call on No CY	D4 addr
CNZ	ADDR	3/5/9-18	S R R W W						Call on No Zero	C4 addr
CP	ADDR	3/5/9-18	S R R W W						Call on +ve	F4 addr
CPE	ADDR	3/5/9-18	S R R W W						Call on Even parity	EC addr
CPI	DATA	2/2/7	F R	✔	✔	✔	✔	✔	Compare 8-bit with A	FE addr
CPO	ADDR	3/5/9-18	S R R W W						Call on Odd Parity	E4 addr
CZ	ADDR	3/5/9-18	S R R W W						Call on Zero	CC addr
DAA		1/1/4	F	✔	✔	✔	✔	✔	Decimal Adjust accumulator	27

DAD	Rp	1/3/10	F B B						Add Rp to HL	00Rp 1001
DCR	R	1/1/4	F	✔	✔	✔	✔		Decrement R	00SS S101
DCR	M	1/3/10	F R W	✔	✔	✔	✔		Decrement M	35
DCX	Rp	1/1/6	S						Decrement Rp	00Rp 1011
DI		1/1/4	F						Disable Interrupt	F3
EI		1/1/4	F						Enable Interrupt	FB
HLT		1/2/5	F B						Halt	76
IN	PORT	2/3/10	F R I						Input from 8-bit port	DB data
INR	R	1/1/4	F	✔	✔	✔	✔		Increment R	00SS S100
INR	M	1/2/7	F R	✔	✔	✔	✔		Increment M	34
INX	Rp	1/1/6	S						Increment Rp	00Rp 0011
JC	ADDR	3/3/7-10	F R R						Jump on Carry	DA addr
JM	ADDR	3/3/7-10	F R R						Jump on Minus	FA addr
JMP	ADDR	3/3/10	F R R						Jump Unconditional	C3 addr
JNC	ADDR	3/3/7-10	F R R						Jump on No Carry	D2 addr
JNZ	ADDR	3/3/7-10	F R R						Jump on No Zero	C2 addr
JP	ADDR	3/3/7-10	F R R						Jump on Positive	F2 addr
JPE	ADDR	3/3/7-10	F R R						Jump on Even parity	EA addr
JPO	ADDR	3/3/7-10	F R R						Jump on Odd parity	E2 addr
JZ	ADDR	3/3/7-10	F R R						Jump on Zero	CA addr
LDA	ADDR	3/3/13	F R R R						Load A direct	3A addr
LDAX	Rp	1/2/7	F R						Load A from Memory Address in BC / DE	000X 1010
LHLD	ADDR	3/5/16	F R R R R						Load HL direct	2A addr
LXI	Rp, 16-bit	3/3/10	F R R						Load 16-bit in Rp	00Rp 0001
MOV	Rd, Rs	1/1/4	F						Move Rs to Rd	01DD DSSS
MOV	M, R	1/2/7	F W						Move R to M	0111 0SSS

MOV	R, M	1/2/7	F R						Move M to R	01DD D110
MVI	R, DATA	2/2/7	F R						Load 8-bit in R	00DD D1100
MVI	M, DATA	2/3/10	F R W						Load 8-bit in M	36 data
NOP		1/1/4	F						No Operation	00
ORA	R	1/1/4	F	✔	✔	0	✔	0	OR A with R	1011 0SSS
ORA	M	1/2/7	F R	✔	✔	0	✔	0	OR A with M	B6
ORI	DATA	2/2/7	F R	✔	✔	0	✔	0	OR A with 8-bit	F6 data
OUT	PORT	2/3/10	F R O						Output to 8-bit Port	D3 data
PCHL		1/1/6	S						Move HL to PC	E9
POP	Rp	1/3/10	F R R						Pop Rp	11Rp 0001
PUSH	Rp	1/3/12	S W W						Push Rp	11Rp 0101
RAL		1/1/4	F						Rotate A Left through Carry (D7 -> CY ->D0)	17
RAR		1/1/4	F						Rotate A Right through Carry (D0 -> CY -> D7)	1F
RC		1/3/6-12	S R R						Return on Carry	D8
RET		1/3/12	F R R						Return	C9
RIM		1/1/4	F						Read Interrupt Mask	20
RLC		1/1/4	F						Rotate Accumulator Left (D7 -> CY, D7 -> D0)	07
RM		1/3/6-12	S R R						Return on Minus	F8
RNC		1/3/6-12	S R R						Return on No Carry	D0
RNZ		1/3/6-12	S R R						Return on No Zero	C0
RP		1/3/6-12	S R R						Return on Positive	F0
RPE		1/3/6-12	S R R						Return on Even Parity	E8
RPO		1/3/6-12	S R R						Return on Odd Parity	E0
RRC		1/1/4	F						Rotate Accumulator Right (D0 -> CY. D0 -> D7)	0F
RST	N	1/3/12	S W W						Restart	11XX X111
RZ		1/3/6-12	S R R						Return on Zero	C8

SBB	R	1/1/4	F	✔	✔	✔	✔	✔	Subtract R from A WITH borrow	1001 1SSS
SBB	M	1/2/7	F R	✔	✔	✔	✔	✔	Subtract M from A WITH borrow	9E
SBI	DATA	2/2/7	F R	✔	✔	✔	✔	✔	Subtract 8-bit from A	DE data
SHLD	ADDR	3/5/16	F R R W W						Store HL directly	22 addr
SIM		1/1/4	F						Set interrupt Mask	30
SPHL		1/1/6	F						Move HL to SP	F9
STA	ADDR	3/4/13	F R R W						Store A directly	32 addr
STAX	Rp	1/2/7	F W						Store A in memory location in BC / DE	000X 0010
STC		1/1/4	F					1	Set CY	37
SUB	R	1/1/4	F	✔	✔	✔	✔	✔	Subtract R from A	1001 0SSS
SUB	M	1/2/7	F R	✔	✔	✔	✔	✔	Subtract M from A	96
SUI	DATA	2/2/7	F R	✔	✔	✔	✔	✔	Subtract 8-bit from A	D6 data
XCHG		1/1/4	F						Exchnage HL with DE	EB
XRA	R	1/1/4	F	✔	✔	0	✔	0	XOR A with R	1010 1SSS
XRA	M	1/2/7	F R	✔	✔	0	✔	0	XOR A with M	AE
XRI	DATA	2/2/7	F R	✔	✔	0	✔	0	XOR A with 8-bits	EE data
XTHL		1/5/16	F R R W W						Exchange top of stack with HL	E3

Machine Cycles:
F – Opcode Fetch
R – Memory Read
W – Memory Write
S – Stretch OpCode Fetch
I – I/O Read (Input)
O – I/O Write (Output)
B – Bus Idle