Exercise on Reducing Switching Activity

In this exercise you will learn how to estimate the power dissipation of a synthesized network of gates based on the results of a simulation. At the same time, you will learn how to reduce the switching activity (an consequently the power dissipation) by using:

- Flip-flops with enable.
- Clock gating.

Description of the Exercise

As seen during the lecture you have to estimate the power dissipation of the three different schemes that can be used to implement a serial to parallel converter. The converter accepts 1 byte (8 bits) of data every clock cycle and has to provide at its output 4 bytes (32 bits) of data every 4 clock cycles. The three different schemes to implement the converter are shown in Figure 1.

Tasks to be performed:

1. Write the VHDL behavioral description of the three schemes. You might want to break the schemes into sub-blocks and use a hierarchical approach.
2. Simulate the schemes using the testbench and vectors provided: `/home/dt40/lab2/`. Copy the following files:
   - `tb_shiftreg.vhd` testbench for scheme a)
   - `tb_shiftreg-enable.vhd` testbench for scheme b)
   - `tb_shiftreg-gated2.vhd` testbench for scheme c)
   - `testvecs.in` test vectors

   The simulation has to be run for 41000 ns.
3. Load the design into Synopsys Design Vision, generate the SAIF annotation file, and synthesize the converter.
4. Run the simulation to generate the SAIF file containing the switching activity.
5. Evaluate the power dissipated in Synopsys Design Vision.

Report for Lab 2

You must write a short report indicating the power dissipation value you obtained for the three schemes. Moreover, you have to write a short comment of those results.

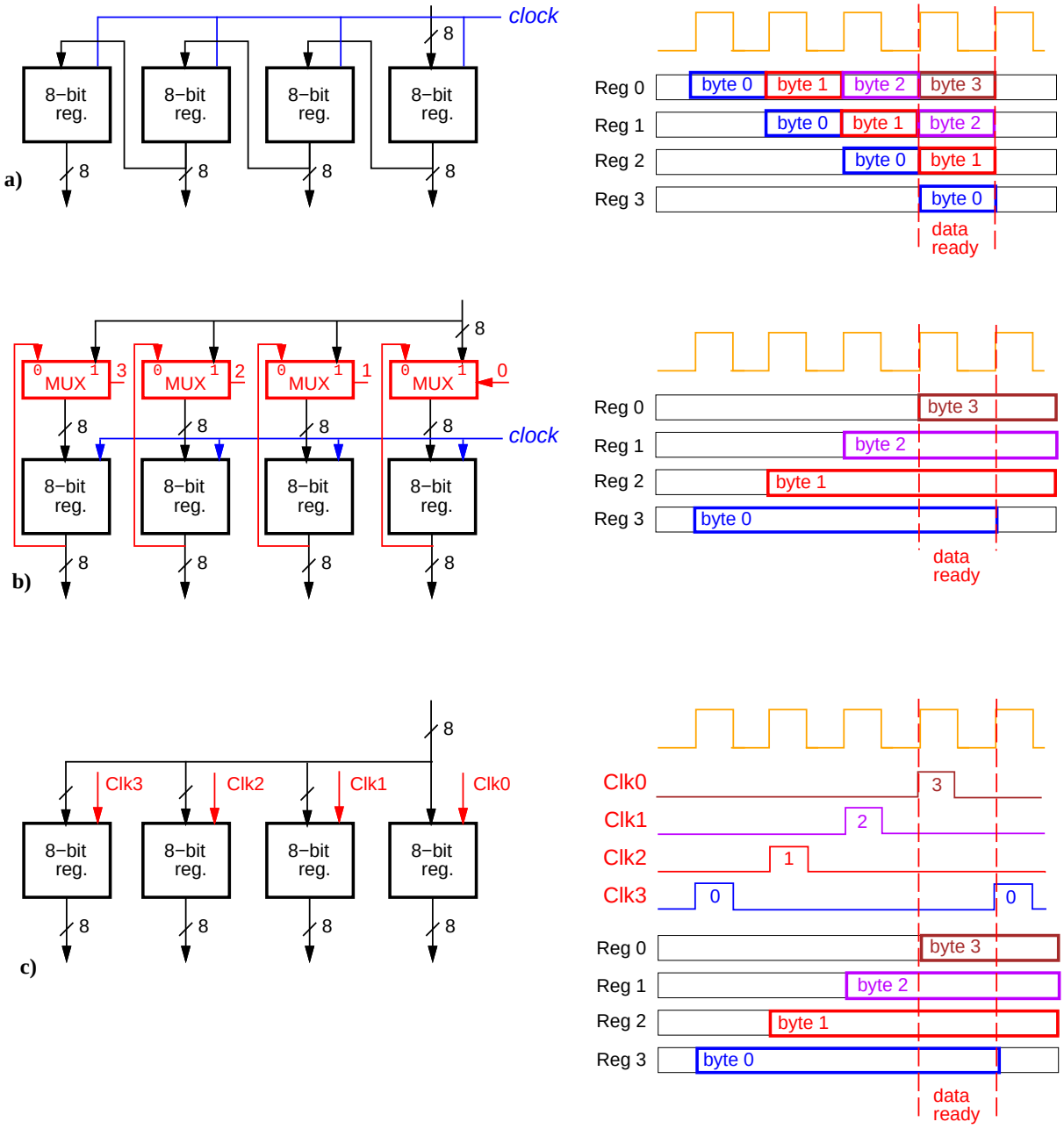

Figure 1: Schemes for serial to parallel converter. a) 32-bit shift register, b) registers with enable, c) clock gating.