Chapter 3

Synthesis

In synthesis the design is compiled and optimized with the specific technology libraries wanted, given some constraints like clock frequency and maximum area.

First the design needs to be analyzed and then elaborated in Design Vision, to check the design for errors/problems. Then the design needs to be uniquified, so that instances that appear more than once in the design, are generated uniquely. The only constraint in this example is the clock period, which needs to be set before synthesis. Finally the synthesis is performed, where the design is optimized for the technology libraries.

3.1 Enviroment setup for Design Vision

To setup the working environment for Design Vision

```
$ source $SCRIPTBOX/setup_syn2005.09.csh
```

The technology libraries used in your design are specified in the configuration file *.synopsys_dc.setup*, which is usually placed into the working directory.
Design Vision is started with the command:

```
$ design_vision -db &
```

The *-db* option starts Design Vision in db mode, which enables the possibility of saving design constraints in a seperate file, and save the synthesized design in a db file.

The command will open the window shown in Figure 3.1. Notice the *"Command Window"* at bottom which is used to enter plain text commands.

3.2 Synthesis of design

After starting Design Vision we first need to analyze the design. Choose from the menu line *File* → *Analyze*. In the new window (Figure 3.2) choose Add, and select all of your VHDL files, except the testbench, and click ok. The files needs to be analyzed in hierarchical order from the leave blocks to the top-level (i.e. bottom-up). Use the arrows in the right side of the window, to move the files up or down the list.

After the files have been analyzed, we need to create the RTL structure of the design with *Elaborate*. This is done by choosing from the menu line *File* → *Elaborate*. In the new window (Figure 3.3) select *WORK* as library, and *FPMUL1(CFG_FPMUL1_SCHEMATIC) – Configuration* as the design and click ok.

To view the RTL block diagram of the design click on *Schematic* → *New Design Schematic View*, resize the newly opened window and zoom (if needed). You should see something similar to Figure 3.4.

Now the clock should be set. In the Schematic window left-click on the port *CLOCK* and then choose from the menu line *Attributes* → *Specify Clock*. In the new window (Figure 3.5) fill out the wanted period

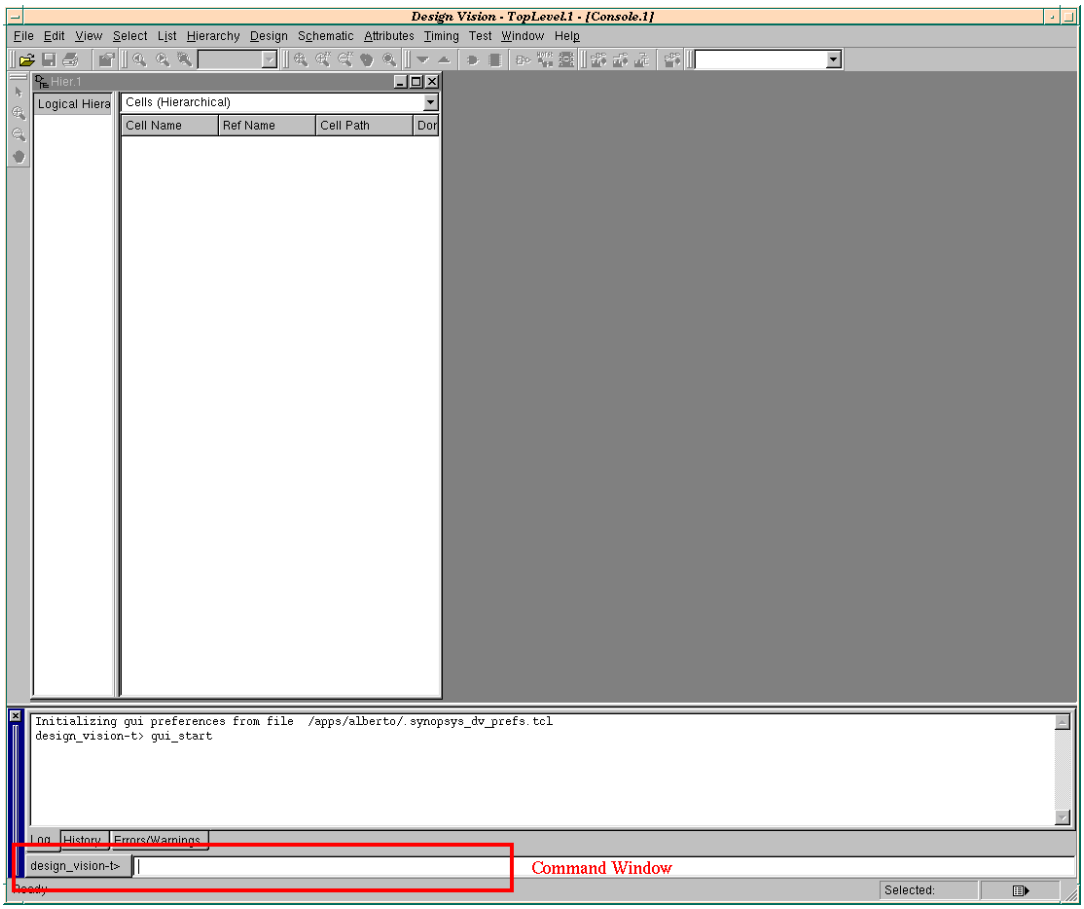

Figure 3.1: Design Vision window at start.

(in nanoseconds) and also specify the rising and falling edge (e.g. if you want a 50% duty cycle, you set the rising edge equal to 0, and the falling edge equal to half the period). Click on *Apply* when done.

To start the synthesis of the design, from the menu choose *Design* → *Compile Design*. In the new window you can specify a number of options. Just leave the options unchanged, and click OK. Now the synthesis starts and optimizes the design so that the clock constraint is met. The time it takes for Synopsys to perform the synthesis, depends on the constraints (the chosen clock period in this case). When the synthesis is done, a message will appear stating that the Datebase has changed. Just click OK and continue.

Repeat the steps to open a new schematic view (*Schematic* → *New Design Schematic View*) to see the syntesized unit. At this point, you can do a number of operations to evaluate the performance of your design.

Display critical path click on *View* → *Highlight* → *Critical Path*. The schematic window will display the critical path (Figure 3.6).

Navigate the design Double-click of any of the blocks in the Schematic window to see the cells composing every block in the design.

Reports You can generate a number of reports on your design:

Timing → *Report Timing*

Design → *Report Area*

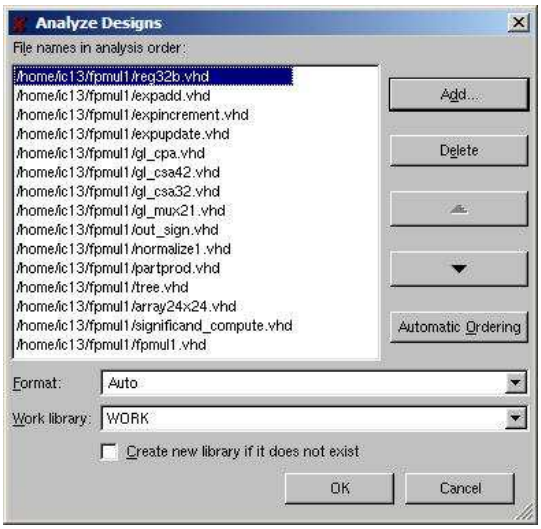

Figure 3.2: Analyze Design window in Design Vision

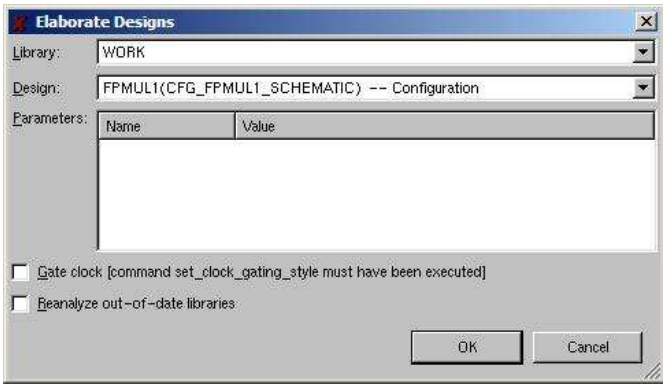

Figure 3.3: Elaborate Design window in Design Vision

Design → Report Power

After synthesis, you can save the design in a number of formats by selecting as a **db** file and as a Verilog file, by selecting from the menu line *File → Save As*. Some relevant formats are:

db Synopsys' internal database format.

vhd VHDL for gate-level simulation.

v Verilog for exporting the netlist to the layout tool.

Also the design constraints need to be saved for later use in the layout tool. This is done by selecting *File → Save Info → Constraints*.

Once the design is saved, select *File → Exit* to exit the tool.

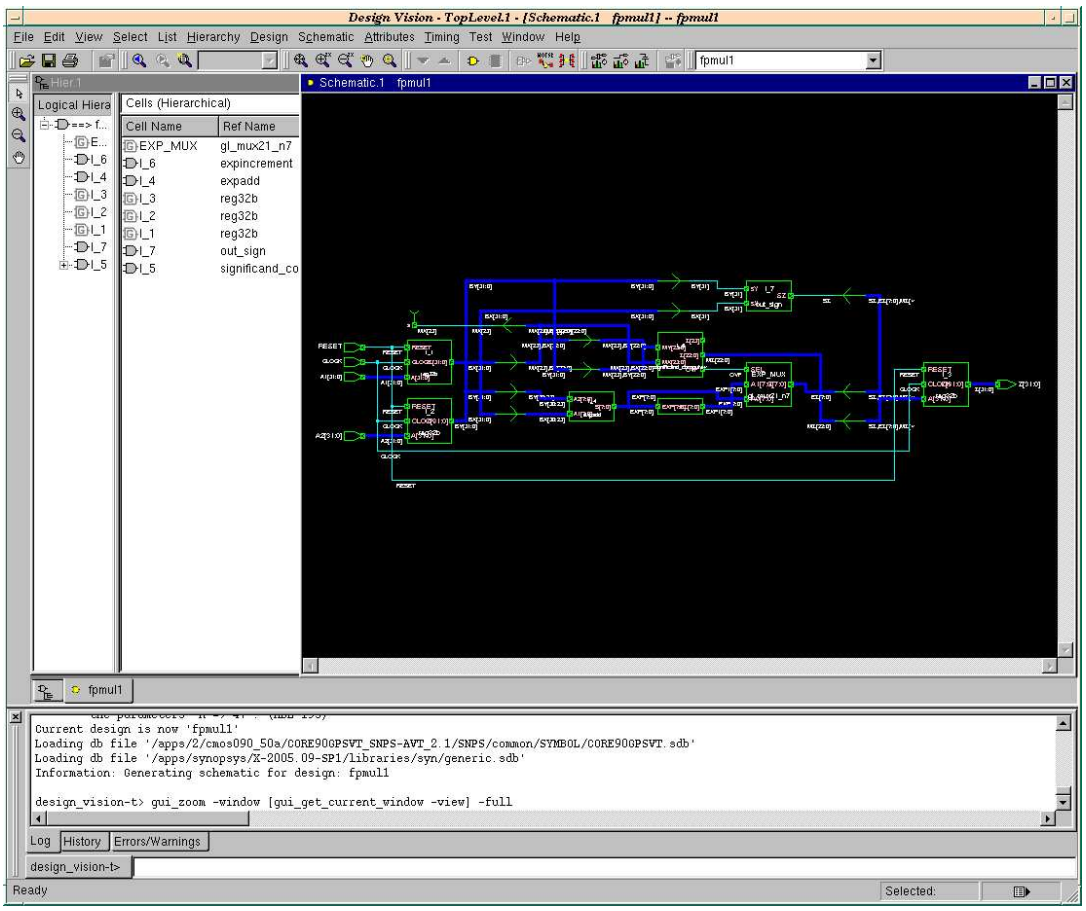

Figure 3.4: Design Vision window after *Elaborate*.

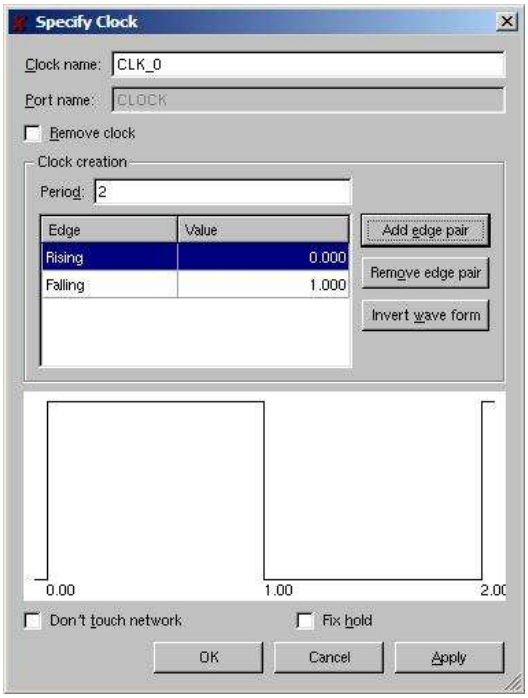

Figure 3.5: Specify clock window in Design Vision

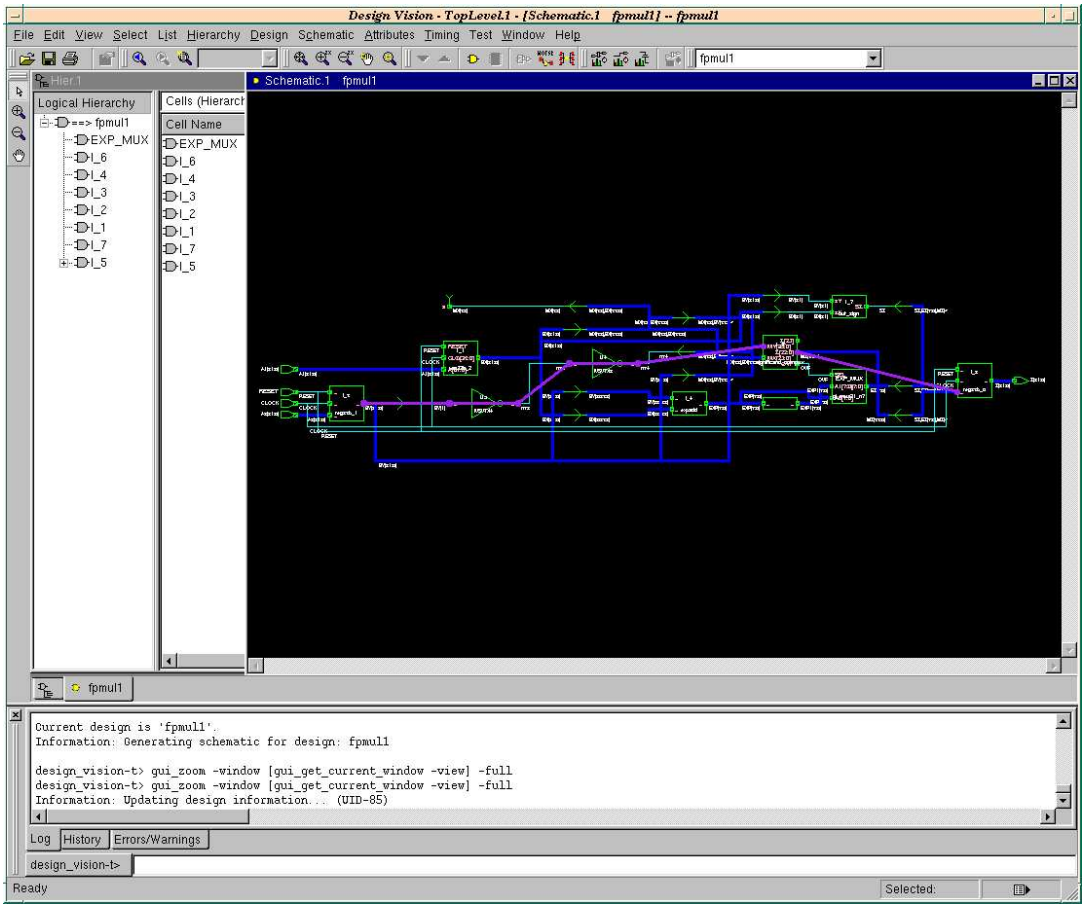

Figure 3.6: Design Vision: critical path.