Informatics and Mathematical Modelling
Technical University of Denmark

02207 : Advanced Digital Design Techniques

Preliminary Report

Low Pass Filter Design for Image Smoothening

Group dt07

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Problem Description

We have an image of 256x256 pixels with pixel size of eight bits. Our task is to design a processor that filters the image using a low-pass filter in two passes. During the first pass the filter window passes through the image horizontally and convolution is done vertically. During the second pass the filter window passes through the image vertically and convolution is done horizontally. The processor has to be able to do the filtering using 3x3, 5x5, 7x7 and 9x9 pixel filter windows and this has to be taken into account in the implementation.

Design

In this section we describe our design: The image to be filtered and the resulting image are stored in memory, the memory is connected to the processor with a bus that has to have a transfer ratio of $8*n^2$, where n is the size of nxn pixel filter window and eight the number of bits per pixel. Since in our case the largest filter window is 9x9 the bus has to have transfer ratio of 648 bits. On each processing cycle $8*n^2$ bits are transferred from the memory to the processor, the processor does the convolutions (vertical for the horizontal pass and horizontal for the vertical pass), results are stored in to memory and the cycle starts anew with new $8*n^2$ bits from the memory.

The processor is divided in three parts (Figure 1).

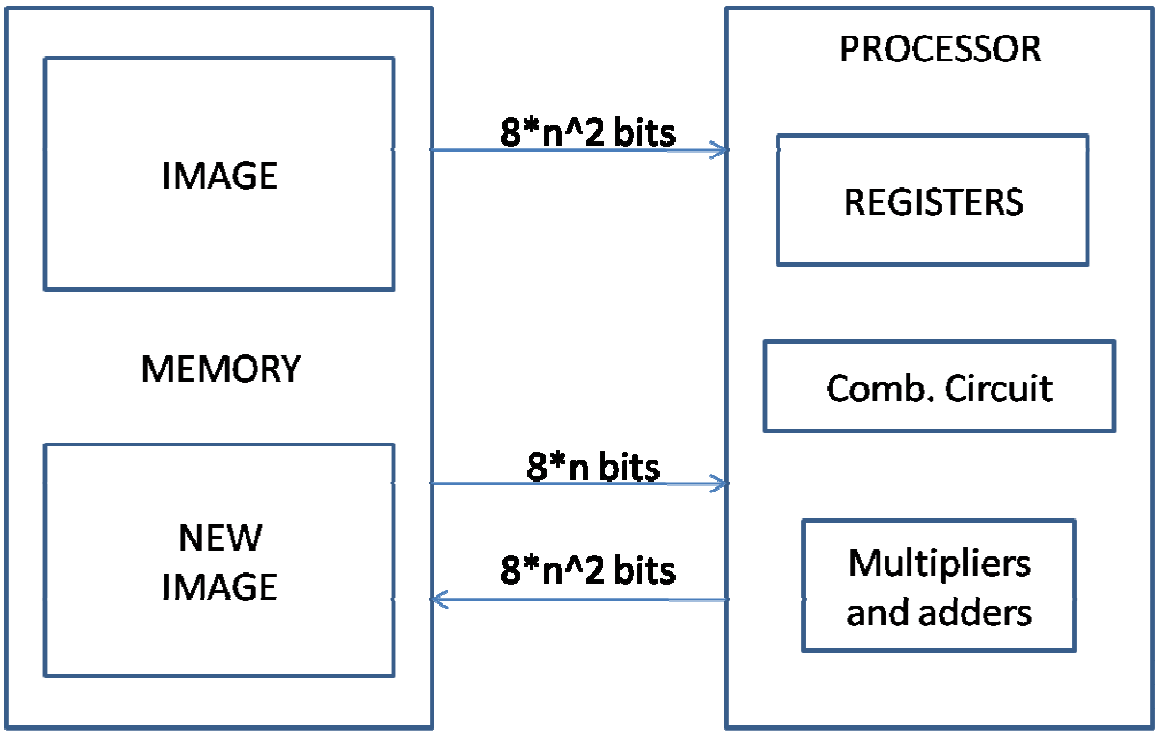

Figure 1: Architecture

The first part contains the registers where the values that are to be processed are stored. The registers contain the filter matrix and the matrix of the pixels that are going to be filtered. Thus we need registers to store $2*8*n^2$ bits (and since the largest n is nine we need to store 1296 bits – this means 1296 registers).

The second part is a combinational circuit that is used to control which bits are transferred from the memory to the registers and vice versa. The circuit also controls how the values in the registers are used depending on the filtering pass (horizontal or vertical).

The third part is where the actual computation is done using multipliers and adders (Figure 2). We use n eight bit multipliers (two eight bit inputs, one eight bit output) to obtain the result of the convolution and an adder to compute the final result. Another adder is used to add together the final result and previously calculated value which is fetched from the memory.

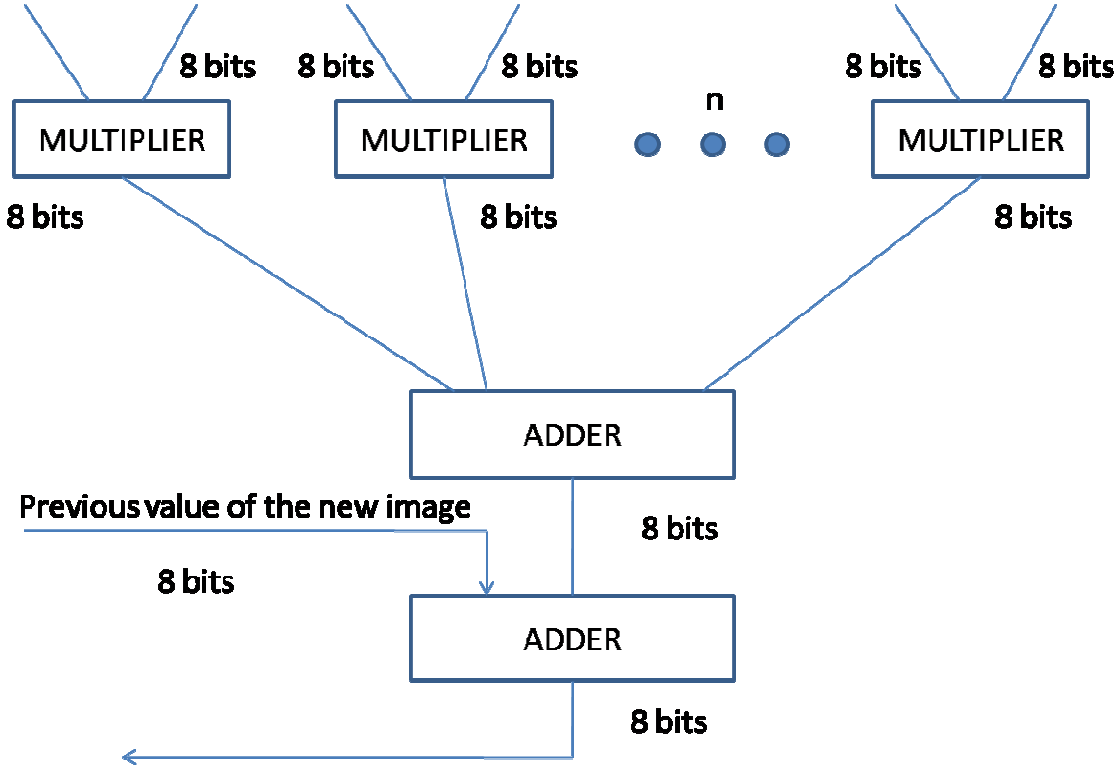

Figure 2: Multipliers and adders

Processing cycle

Each processing cycle requires six clock cycles:

1. The processor gets a matrix from the memory and stores it in the registers.
2. The data arrives at the combinational circuit and the parts of the matrix to convolute are chosen.
3. The pixels are convoluted with the multipliers and adders (the processor does the computation).
4. The processor looks up the value that was already calculated for the pixel (if no value has yet been calculated this is 0).
5. The values from 3rd and 4th steps are added together.
6. The data is stored on memory.