

Exercise on Synthesis

In this exercise you have to synthesize a 24-bit adder with different timing constraints and comment on the results. You must be *somewhat* familiar with the tool to perform quickly the required tasks. You can use the tutorial to get familiar with the tool.

Copy the Synopsys configuration file (it specifies the libraries to be used):
 /apps/misc/02207/labs/lab1/.synopsys_dc.setup to the working directory.

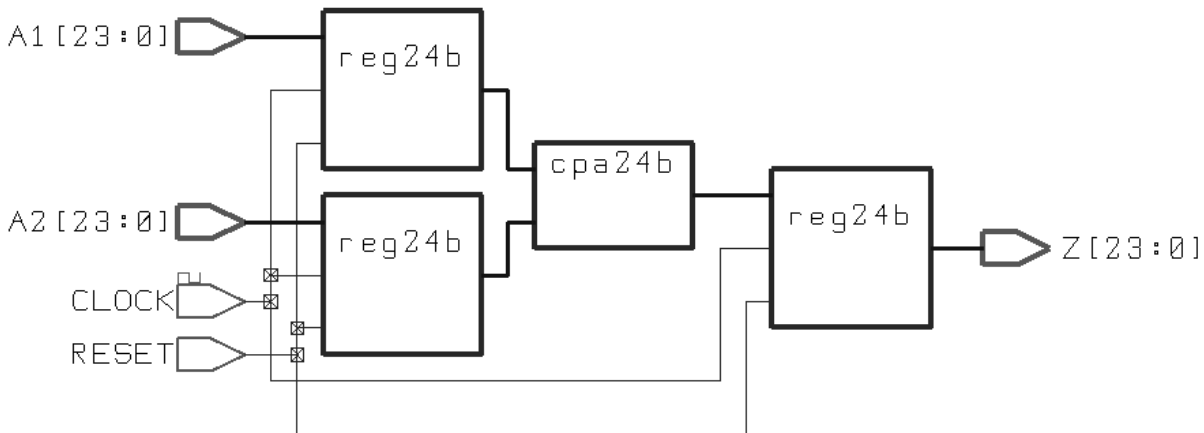


Figure 1: Example of scheme for synthesis.

Tasks to be performed:

1. Write a one-file behavioral description of a 24-bit adder (for example a carry-ripple adder).
2. Verify that the adder is working properly (use Modelsim)
3. Write a behavioral description of a 24-bit register.
4. Create a top-level netlist that looks like the one in Figure 1.
5. Import the design into Synopsys and synthesize it specifying different clock periods (T_C).
6. Estimate the area and power dissipation for the different designs.

Hints

- To exercise the tool capabilities of optimization for low power, you might give the following commands in the "Command Window"

```
set_max_dynamic_power 1
set_max_leakage_power 1
```

- To compute the number of cells of the different types (SVT/HVT), you can use the following procedure.
 1. Once the unit has been synthesized, save the top-level as a VHDL file.
IMPORTANT: remember to change the name of the new file to not overwrite the original VHDL file containing the top-level before synthesis.
 2. Suppose that you created `adder24b-syn.vhd` in the previous step, you can use the following sequence of UNIX commands to count the cells:
SVT cells:

```
grep SVT adder24b-syn.vhd | grep port | wc -l
```


HVT cells:

```
grep HVT adder24b-syn.vhd | grep port | wc -l
```

Report for Lab 1

The report for this lab should contain:

How the critical path, the area and the power dissipation change as the timing constraint (T_C) is increased/decreased.

How the cells mix (SVT/HVT) changes with the different T_C s.

Comments on the results obtained.