Report for the JPEG unit design - requirements -

02207 Advanced Digital Design Techniques

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Deadline

The reports will be collected from the mailbox at the main entrance of Building 322, ground floor

Monday, December 11 at 12:00 (noon)

Report Requirements

The report must consist of three parts:

- Main body - About 10 pages of text describing the work performed and the results obtained.
- Appendix - The appendix must contain the VHDL code of your unit and the Synopsys reports for delay, area and power dissipation.
- Archive file - Archive containing ALL VHDL files, test vectors and Synopsys .db file (top-level entity).

The Main body must be printed and handed in (mailbox)

The Appendix and the Archive file must be uploaded to Campusnet

Report Preparation

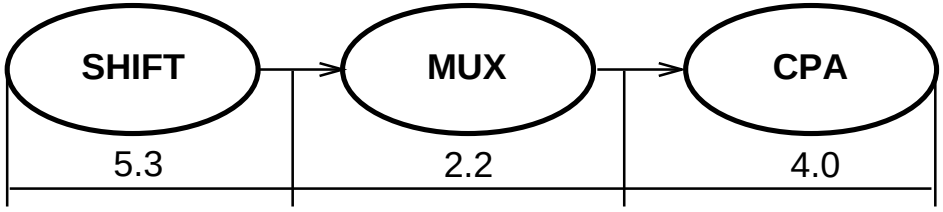
The Main body should contain:

- The description of the architecture and literature sources.
  The references must be detailed.
- Clear drawings of the architecture and sequencing of operations.
  IMPORTANT: Synopsys plots are NOT acceptable
- Detailed description of the datapath (n. of FUs, bit-width, etc.)
- Description of the controller (state diagram, or . . .)
- A section indicating the design choices (e.g. pipelining, clock-gating, . . .)

Report Preparation (cont.)

- The results obtained for the final implementation.

  Critical path delay and through which blocks:



SHIFT	MUX	CPA	critical path
5.3	2.2	4.0	$11.5\ ns$

  Number of cycles required to process a 8×8 block and the sample image (64×64)

  Power dissipation for the provided sample image and the power breakdown

  Area

Report Preparation (cont.)

- A conclusion describing the work performed and the results obtained.
- MANDATORY summary table organized EXACTLY as:

Critical Path $[ns]$	N. cycles (8×8)	N. cycles (64×64)	E_{pc} $[mW/MHz]$	AREA $[\mu m^2]$
X.XX	YYY	ZZZZ	XX.XX	YYYYYY

Note - $E_{pc} = \frac{P_{ave}}{f} = P_{ave} T_{clk}$ (energy per cycle)

For example, $P_{ave} = 357.3\ mW$ and $T_{clk} = 10\ ns \quad \Rightarrow$

$$E_{pc} = \frac{357.3\ mW}{100\ MHz} = 3.57\ mW/MHz$$

Appendix

The appendices must be included in the electronic (Campusnet) version of the report ONLY.

Appendices include:

1. The VHDL code of the design.
2. The reports generated by Synopsys for delay, power and area.

Archive file

The following files must be included in the archive:

- All VHDL files *.vhd
- the test vector files;
- the .db file where you saved the synthesized design.

Acceptable formats are: zip and tar

Other formats (e.g. rar) are not acceptable

Example of archive preparation

We can use tar on Databar's machines as follows:

1. Group 19 creates archive of jpeg01 directory:
   `tar cvf dt19.tar jpeg01/*.vhd jpeg01/*.db`
   To test what is contained in the .tar file:
   `tar tvf dt19.tar`
   or
   you can compress it at the same time:
   `tar cvfz dt19.tgz jpeg01/*.vhd jpeg01/*.db`
2. uploade the file dt19.tar (or dt19.tgz) to Campusnet.

Checklist

1. Print out the main body of the report
   (no more than 10 pages).
2. Turn in the printed and signed report in the mailbox.
3. Upload the electronic report (main body + appendicies)
   to Campusnet.
4. Prepare the archive files of your VHDL code.
5. Upload the archive file to Campusnet.
6. Good luck for the exam!