Chapter 2

Simulation of design

Modeltechs Modelsim is a powerful tool, for simulating digital designs. By either programming your design in Verilog or VHDL[1] and opening it in Modelsim, it is possible to either manually provide inputs to your design, or use a testbench, to provide inputs to Modelsim via test vectors, and control the computed results, with what you would expect from the design.

2.1 Enviroment setup for Modelsim

To start Modelsim, you first need to source the configuration file

```
$ source $SCRIPTBOX/setup_modelsim.csh
```

Then it is possible to start Modelsim with the command:

```
$ vsim &
```

Remember to be in the directory containing your VHDL files when starting Modelsim. When Modelsim is started, it is necessary to create a new project and import the VHDL files into it. To create the new project select *File* → *New* → *Project* and choose an appropriate name. On the pop-up window select *Add Existing File* and select all the VHDL files in the directory.

2.2 Compiling VHDL files

You should now be set for compiling the VHDL files describing the FP multiplier. This can either be done from Modelsim or via the command **vcom** in the terminal. To avoid compiling errors, the files needs to be compiled according to the hierarchy in the following order:

1. reg32b.vhd
2. expadd.vhd
3. expupdate.vhd
4. expincrement.vhd
5. gl_cpa.vhd
6. gl_csa42.vhd
7. gl_csa32.vhd

[1] In this course VHDL is used

8. gl_mux21.vhd
9. out_sign.vhd
10. normalize1.vhd
11. partprod.vhd
12. tree.vhd
13. array24x24.vhd
14. significand_compute.vhd
15. fpmul1.vhd
16. tb_fpmul1.vhd

To compile from the terminal, enter the following command:

```
$ vcom filename1.vhd filename2.vhd ...
```

where the filenames are the name of the VHDL files in the design. To compile from **vsim** choose from the menu line *Compile* → *Compile All*. Then choose the files by left-clicking with the mouse on the individual files. Hold down the Ctrl-key to choose more files at the same time.

2.3 Simulating with testbench

To simulate with a testbench you can either start **vsim**, specifiying the testbench file, or choose it from the Modelsim GUI. From the GUI, double click on the *work* directory, right-click on *cfg_tb_fpmul1_behavioral* and choose *Simulate*. To start the testbench directly from the terminal, enter the command:

```
$ vsim cfg_tb_fpmul1_behavioral &
```

If you want to see the waveforms of the inputs and outputs you can select *View* → *Debug Windows* → *Waves* from the menus or you can type commands in the modelsim command line, such as:

```
$ add wave A1
$ add wave A2
$ add wave Z
```

where A1 and A2 are inputs and Z is output of the multiplier.

When the simulation is started, it is easier to issue commands to Modelsim from the commandline, instead of clicking with the mouse. From the commandline, in the bottom of the GUI, left-click and enter the command:

```
$ run 1000ns
```

This simulates the design, using the testbench, for 1000 ns.

Depending on the clock period of the design, this will simulate the unit for a certain amount of clock periods. Now it should be possible to see from the log window, that all the tests run passes.