Informatics and Mathematical Modelling
Technical University of Denmark

02207 : Advanced Digital Design Techniques

Lab 1: Exercise on Synthesis

Group *dt07*

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1 Purpose of the Exercise

The goal of the exercise was to get familiar with the process of synthesis of digital circuits, using special tools for synthesis such as Design Vision. A register-level netlist containing a 24-bit adder is synthesized in the exercise, for different values of the clock time period. The reports concerning the timing constraints, area, power consumption etc. are documented in the report.

2 Behavioral Description for 24-bit Adder

The VHDL code for a simple 24-bit adder is provided below.

The behavior of this adder is verified in Modelsim.

3 Behavioral Description for 24-bit Register

4 Top-Level Netlist from 24-bit Adder and 24-bit Register

5 Synthesis Results