Project

DTU 02207

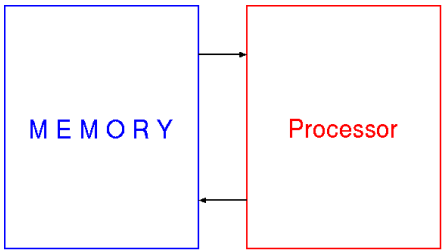
Adv. Digital Design Tech.

Projects

For images of $N \times N$ pixels design a processor implementing:

1. Low-pass filter (2×1-D LPF)
2. Low-pass filter (2-D LPF)
3. Median Filtering
4. Gradient (edge-detection)
5. Variance

Architecture of processor



Memory contains the images: 256 × 256 pixels 8 bit/pixel

Processor processes the image and store the modified image back in memory

Low-pass filter (2×1-D)

Implement low-pass filter with masks of size

$$3 \times 3, \quad 5 \times 5, \quad 7 \times 7, \quad 9 \times 9$$

The coefficients of the mask are *n*-bit integers

A 2D filter is constructed by two passes of a 1D filter:

1. First the filter is applied horizontally and
2. the result of this filtering is then filtered vertically

Low-pass filter (2-D)

Implement low-pass filter with masks of size

$$3 \times 3, \quad 5 \times 5, \quad 7 \times 7, \quad 9 \times 9$$

The coefficients of the mask are *n*-bit integers

The 2D filter is realized with one pass

Median Filtering

The median filter is typically used as a noise filter in signals.

The aim of this task is to implement a unit that reads an image from memory and performs this median filtering.

A 3×3 portion of the image is considered by the filter.

In order to determine the median of these nine values, it is necessary to sort the values.

You decide yourself on a sorting algorithm and the amount of parallellism implemented.

Gradient (edge-detection)

To detect edges in images it is necessary to compute the gradient

Use the 3×3 mask described in the DIP book

Variance

The variance of the pixel values in an image is a statistical measure that may be used in determining certain features of the image.

The formula is the following

$$\sigma^2 = \frac{\sum_i^{N^2} (p_i - \mu)^2}{N^2}$$

where μ is the mean value of the pixel intensity function

The assignment is to construct a processor computing this variance

You are encouraged to handle the special case of $\mu = 0$ and may assume an input flag indicating this case.

Documentation

1. Digital Image Processing book(s)
2. Project specifications (these slides)
3. Research papers describing how the problem has been previosly solved

Questions

Design Tasks

1. Determine the architecture of your processor.
   - How many multipliers, adder, etc.
   - How much memory.
   - How many clock cycles.
   - Sequence of operations.
2. Determine the bit-width of the datapath.
3. Write the specifications of your processor.

Write the first report.

Design Tasks (cont.)

4. Write the VHDL RTL description of your processor.
5. Verify the functionality of the processor.
6. Synthesize the processor using the library of standard cells
   - Determine the fastest possible implementation
   - Report: latency, critical path, area and power dissipation
7. Modify the design to reduce the power dissipation minimizing the performance degradation.

—— ALTERNATIVELY ——

6. Implement the processor on FPGA
7. Display the filtered image on the monitor using the VGA output of the FPGA board.

—— END ALTERNATIVELY ——

8. Write the final report.

Reports

The first report (2/3 pages) must include:

- The description of the processor architecture.
- The details of the datapath: n. of FUs, bit-width, ...
- The sequencing of ops, and n. of cycles required.

The final report should be 10 pages max

- A detailed description of architecture implemented and operations performed.
- A detailed timing and power estimation report of the gate-level netlist synthesized.
- A conclusion.

Deadlines and Support

- Monday, November 12, 2007
  Deadline for the first report.
  In electronic format (PDF file uploaded on CampusNet).
- ⋆TENTATIVE⋆ Monday, December 10, 2007
  Deadline for the final report
  Hardcopy + electronic (PDF) +
  ALL the VHDL files you used (zip file)

Support

- Conference feature on CampusNet
- 1 hour of *Project Hints*
  TIME: TBA (after deadline first report).

Cheating

- Copying from other group's work
- Internet
- Work-load should be equal inside a group
- other . . .