Lab 3: Exercise on Retiming

An alternative implementation of digit recurrence division (for example, radix 4 with carry-save adder) is to retime the recurrence so that the quotient-digit selection is performed at the end of one cycle and the digit used in the next (see Figure 1). This retiming creates two slices in the implementation: a most-significant slice , which includes the quotient-digit selection, and the rest. This might reduce the critical path by eliminating the need of a buffer to distribute the quotient digit to the most-significant slice. It also allows this slice to be optimized for delay, and the other part optimized for energy dissipation.

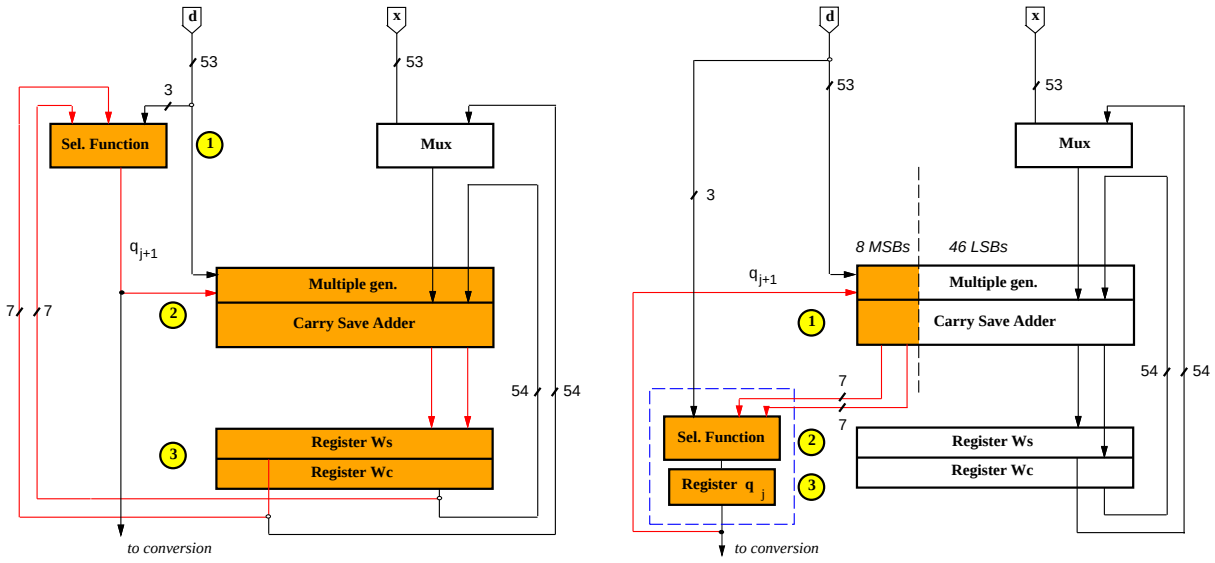

Figure 1: Retiming of the radix-4 division recurrence.

The VHDL description of the scheme to the left of Figure 1 and the test vectors can be found in `/home/dt40/lab3`

Tasks to be performed:

1. Synthesize the non-retimed unit and find the minumum clock period.
2. By using the test vectors, estimate the power dissipated by the synthesized unit and report:
   - the breakdown of the energy dissipation (dynamic and static) for the composing blocks in Figure 1 (left);
   - the number of cells of type SVT and HVT for all the composing blocks.
3. Retime the unit as indicated in Figure 1 (right) by changing the connection and applying other moodifications in the top-level VHDL file `divr4_rec.vhd`.
4. Synthesize the retimed unit and find the minumum clock period.
5. Repeat step 2 for the retimed unit.
6. Write a report with the data requested above.