

EXPERIMENT 1

V-I CHARACTERISTICS OF RECTIFIER AND ZENER DIODE

i) DIODE CHARACTERISTICS

Aim:

- (a) To study and plot the forward characteristics of a silicon diode.
- (b) To calculate the forward static and dynamic resistance of the diode at a particular operating point

Components required:

SL No:	Component	Specification	Quantity
1	Diode	IN4001	1
2	Resistor	1kΩ	1

Equipments required:

SL No:	Equipment	Range	Quantity
1	Ammeter	0-200mA	1
2	Voltmeter	0-1 V	1

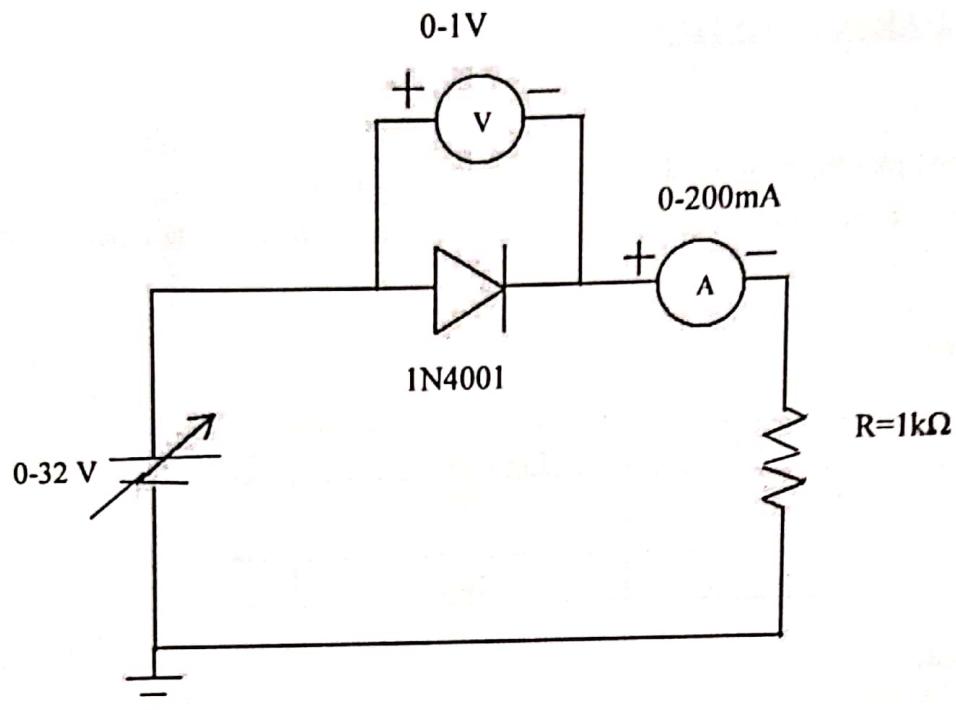
Theory:

Static and Dynamic Resistance:

At a given operating point, the static and dynamic resistance of a diode can be determined from its characteristics as shown in Fig.1. The *static or dc resistance*, R_D , of the diode at the operating point (the point where the load line intersects the diode characteristics), Q, is simply the quotient of the corresponding levels of V_D and I_D . The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics. Fig. 1

$$\text{Static Resistance, } R_D = V_D/I_D$$

Circuit diagram:



Component description:



Type number of diode:

- (a) Maximum forward current rating:mA
- (b) Maximum reverse current rating:mA
- (c) Maximum peak inverse voltage rating:V

Design:

Let maximum current flowing through circuit be 35mA.

$$\text{Then, } R > \frac{V_{\max} - V_{cut-off}}{I_{\max}} \Rightarrow R > \frac{32 - 0.7}{35 * 10^{-3}}$$

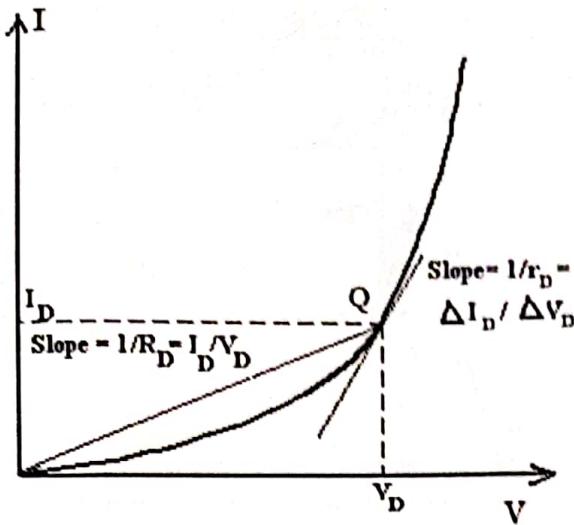


Figure 1. Diode Characteristics

Dynamic or ac Resistance, r_d , is defined as the quotient of this change in voltage and change in current around the dc operating point.

$$r_d = \Delta V_D / \Delta I_D$$

Procedure:

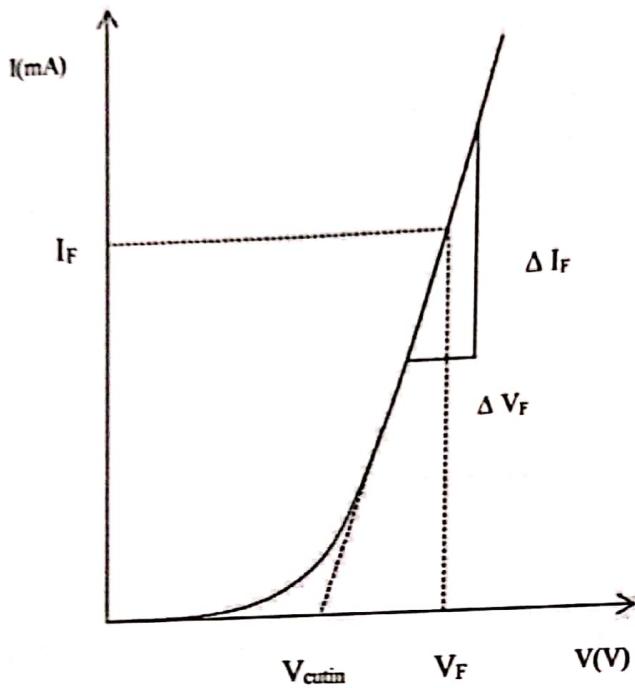
1. Identify the anode and cathode of the diode and set up the circuit on the breadboard as shown in the circuit diagram.
2. Switch on the power supply and slowly increase the voltage from 0V. Note down the readings of voltmeter and ammeter for each value of voltage.
3. Tabulate the readings and plot the graph for the forward bias condition.
4. Calculate the static and dynamic resistance of the forward biased diode.

Calculations :

$$\text{Static Resistance, } R_D = V_F/I_F$$

$$\text{Dynamic Resistance, } r_d = \Delta V_F / \Delta I_F$$

Expected graph:



Observations:

SL.No.	Voltage (V)	Current (mA)

Result:

The forward characteristics of the given diode has been studied and plotted.

Cut-in voltage, $V_{\text{cut-in}}$ =
Static resistance, R_D =
Dynamic resistance, r_d =

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ii) ZENER DIODE CHARACTERISTICS

Aim:

- (a) To study and plot the reverse characteristics of a zener diode.
- (b) To calculate the dynamic resistance of the zener diode under reverse-biased condition

Components required:

Sl. No:	Component	Specification	Quantity
1	Zener diode	SZ6V2	1
2	Resistor	1.5kΩ	1

Equipments required:

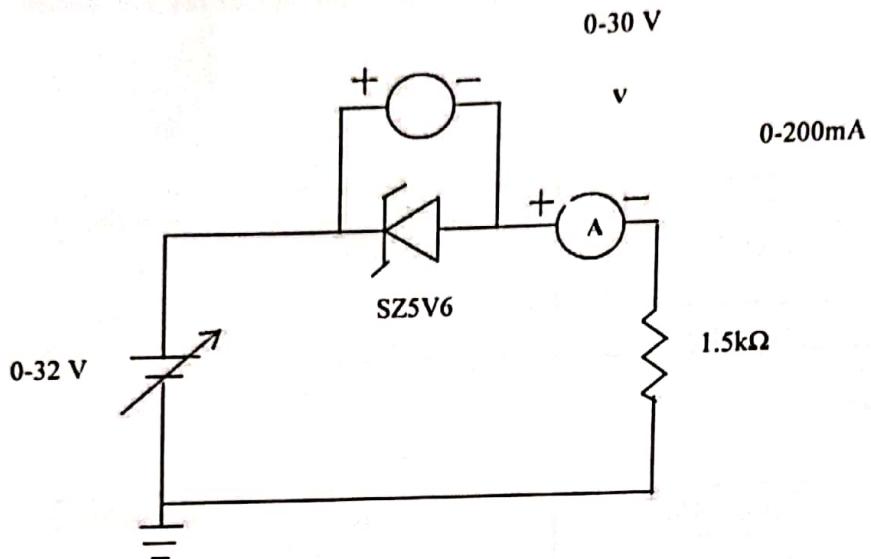
Sl. No:	Equipment	Range	Quantity
1	Ammeter	0-200mA	1
2	Voltmeter	0-30 V	1

Theory:

A zener diode is a diode which allows current to flow in the forward direction in the same manner as an ideal diode, but also permits it to flow in the reverse direction when the voltage is above a certain value known as the breakdown voltage, "Zener knee voltage", "Zener voltage", "avalanche point",.

A conventional solid-state diode allows significant current if it is reverse-biased above its reverse breakdown voltage. When the reverse bias breakdown voltage is exceeded, a conventional diode is subject to high current due to avalanche breakdown.

Circuit diagram:



Component description:



Type number of zener diode:

- (a) Breakdown voltage : V
- (b) Maximum current rating: mA
- (c) Maximum wattage rating: W

Design:

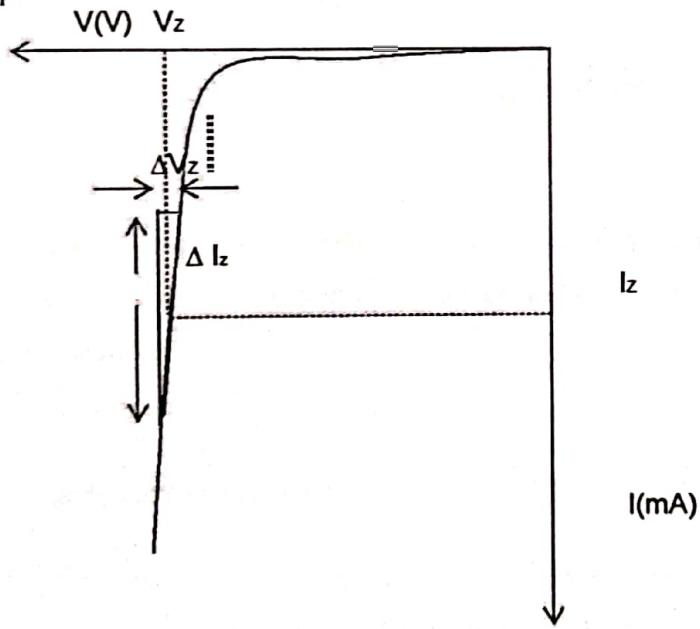
$$V_{max} = 32V, I_{max} = 20mA$$

$$\text{Then, } R > \frac{V_{max} - V_{zener}}{I_{max}} \Rightarrow R > \text{_____}$$

Select R =

Procedure:

1. Identify the anode and cathode of the diode and set up the circuit on the breadboard as shown in the circuit diagram.
2. Switch on the power supply and slowly increase the voltage from 0V. Note down the readings of voltmeter and ammeter for each value of voltage.
3. Tabulate the readings and plot the graph for the reverse bias condition.
4. Calculate the dynamic resistance of the reverse biased diode.

Expected graph:**Observations:**

SI No.	Voltage(V)	Current(mA)

Calculations:

$$\text{Dynamic Resistance, } r_z = \Delta V_z / \Delta I_z$$

Result:

The reverse characteristics of the zener diode has been studied and plotted.

Zener breakdown voltage	=
Dynamic resistance	=

EXPERIMENT 2

FULLWAVE RECTIFIER

Aim:

- (a) To study the characteristics of centre tapped full wave and bridge rectifiers.
- (b) To study the performance of shunt capacitor filter

Components required:

Sl. No:	Component	Specification	Quantity
1	Diode	1N4001	4
2	Resistor	1kΩ	1
3	Capacitor	100μF,25V	1
4	Transformer	230/9 , 230/9-0-9	1

Theory:

A rectifier is an electrical device that converts alternating current (AC), which periodically reverses direction, to direct current (DC), which flows in only one direction. The process is known as rectification.

Full Wave Center-tapped Rectifier

This type of rectifier uses two diodes and a transformer with center tapped secondary winding. During the positive half cycle of the input AC diode D1 is forward biased and the current starts flowing to the load through it. During the negative half of the input diode D2 forward biased and D1 becomes reverse biased. Load current start flowing through D2 during this negative peak. Note that the current flow through load has not changed even when the voltage polarity changed.

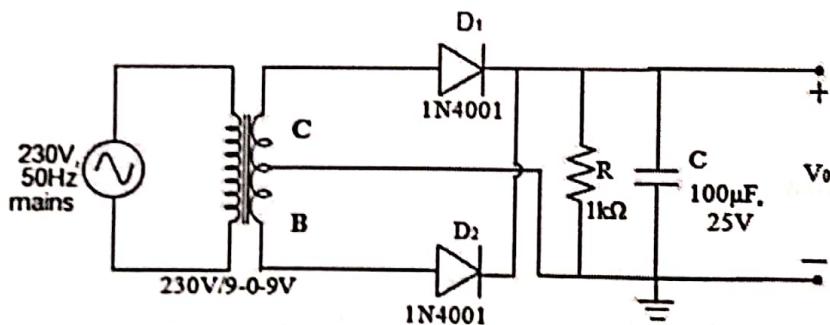
Full Wave Bridge Rectifier

Using the same secondary voltage, this bridge rectifier can produce almost double the output voltage as compared with full wave center-tapped transformer rectifier. During the positive half of the input AC diodes D₂ and D₃ are forward biased and D₁ and D₄ are reverse biased. Thus load current flows through D₂ and D₃ diodes. During the negative half cycle of the input diodes D₁&D₄ are forward biased and D₂&D₃ are reverse biased. Therefore load current flows through D₁&D₄ diodes.

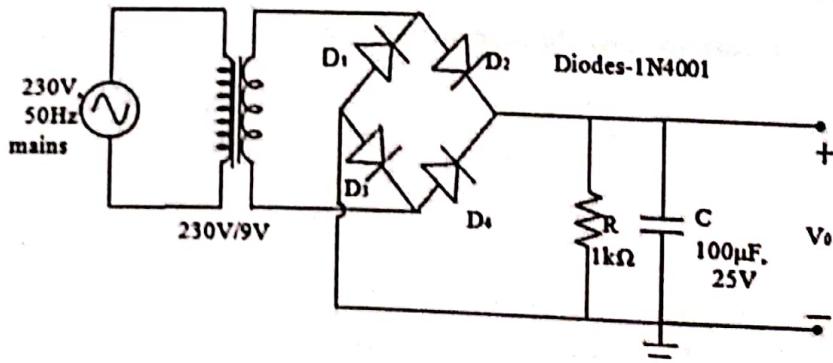
Procedure:

1. Set up the circuit as shown in the circuit diagram without the C-filter.
2. Switch on the main supply. Observe the transformer secondary voltage and the output waveform.
3. Measure the peak values and calculate the ripple factor.
4. Now, connect the C-filter and observe the waveforms and measure V_{r(pp)} of the ripple waveform.
5. Calculate ripple factor and rectification efficiency using the given formula.

1. Central tapped full wave rectifier



2. Bridge full wave rectifier



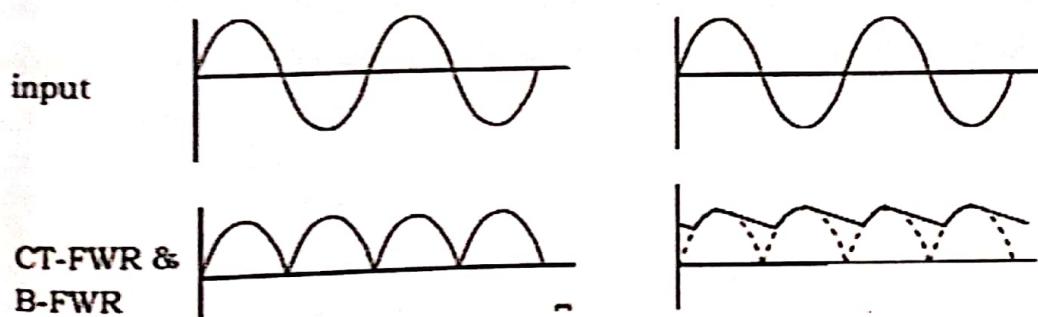
Observations:

	CT-FWR	B-FWR
Without filter	$V_m = \dots V$	$V_m = \dots V$
With filter	$V_{(pp)} = \dots V$	$V_{(pp)} = \dots V$

Calculations:

	CT-FWR	B-FWR
Without filter	$V_{dc} = \frac{2V_m}{\pi} =$ $V_{rms} = \frac{V_m}{\sqrt{2}} =$ $r = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} =$ $\eta = \left(\frac{V_{dc}}{V_{rms}}\right)^2 =$	$V_{dc} = \frac{2V_m}{\pi} =$ $V_{rms} = \frac{V_m}{\sqrt{2}} =$ $r = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} =$ $\eta = \left(\frac{V_{dc}}{V_{rms}}\right)^2 =$
With filter	$V_{dc} = V_m - \frac{V_{(pp)}}{2} =$ $V_{ac,rms} = \frac{V_{(pp)}}{2\sqrt{3}} =$ $r = \frac{V_{ac,rms}}{V_{dc}} =$	$V_{dc} = V_m - \frac{V_{(pp)}}{2} =$ $V_{ac,rms} = \frac{V_{(pp)}}{2\sqrt{3}} =$ $r = \frac{V_{ac,rms}}{V_{dc}} =$

Expected waveforms



Result:

The characteristics of centre-tapped full wave and bridge rectifiers with and without C filter were studied and output waveforms were plotted.

For center tapped full wave rectifier

Ripple factor without C filter =

Ripple factor with C filter =

Efficiency

For bridge full wave rectifier

Vipple factor without C filter

Vipple factor with C filter

Efficiency

Efficiency without C filter

Efficiency with C filter

Efficiency with C filter

EXPERIMENT 3

SIMPLE ZENER VOLTAGE REGULATOR

Aim

To set up and study a zener diode shunt regulator and to plot its line and load regulation characteristics.

Components and equipments required

Zener, resistor, rheostat, voltmeter, ammeter, DC source and bread board.

Theory:

A zener diode functions as an ordinary diode when it is forward biased. It is a specially designed device to operate in the reverse bias. When it is in reverse breakdown region, the zener voltage V_z remains almost constant irrespective of the current I_z through it. A series resistor R_s is used to limit the zener current below its maximum current rating. The current through R_s is given by the expression $I_s = I_z + I_L$, where I_L is the current through the load resistor R_L . The value of R_s must be properly selected to fulfil the following worst condition requirements.

When the input voltage increases I_L remains same, I_s and I_z increase. Similarly if input voltage decreases, I_L remains same, I_s and I_z decrease. But if I_z falls lower than the minimum zener current enough to keep the zener in break down region, the regulation will cease and output voltage decrease. A low input voltage can cause the regulator fail to regulate. The series resistance should be selected between $R_{s\ min}$ and $R_{s\ max}$ which are given by the expressions

$$R_{s\ min} = [V_i(\min) - V_z]/I_s.$$

$$R_{s\ max} = [V_i(\max) - V_z]/I_s$$

Procedure:

1. Wire the circuit on bread board after testing all the components.
2. Note down the output voltage for input voltage varying from 7 V to 10 V in steps of 1 V.

Plot the line regulation graph with V_{in} along x-axis and V_o along y-axis. Calculate % line

regulation using the expression $\Delta V_o / \Delta V_i$

3. Keep the input voltage constant (say 10 V) and note down output voltage for various values of load current starting from 0 to 10 mA or more, by varying R_L using a pot., the load regulation graph with I_L along x-axis and V_o along y-axis.
4. To calculate % load regulation, mark V_{NL} and V_{FL} on y-axis on the load regulation graph. V_{NL} is the output voltage in the absence of load resistor and corresponds to rated I_L (here 5 mA). Calculate the % load regulation V_R as per the equation

$$V_R = (V_{NL} - V_{FL}) / V_{NL} \times 100$$

Design output requirements

$V_o = 5.6V$, $I_L = 5mA$ when input in the range $10 \pm 3V$.

Selection of zener select 5.6V zener ($P_0 = 0.33W$, $V_Z = 5.1V$, $r_d = 8\Omega$ and $I_Z = 10mA$)

Design of load resistor R_L

We know, $R_L = V_o / I_L$

But $V_o = V_Z$. Then $R_L = 5.6V / 5mA = 1.12k$. Use 1.2 k pot.

Design of R_S The series resistance R_S must be selected such a way that

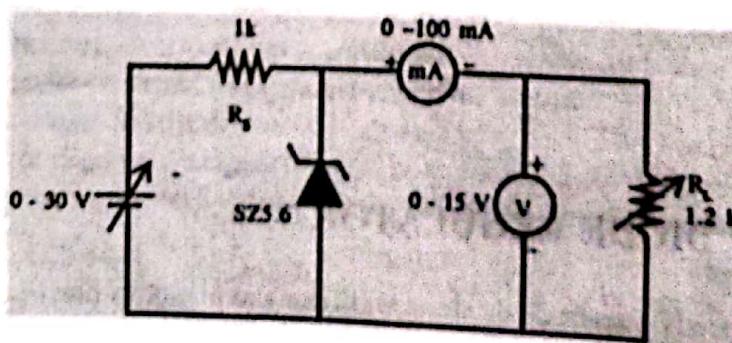
$$R_{S\max} > R_S > R_{S\min}$$

$$R_{S\max} = (V_{imax} - V_Z) / I_S = (13 - 5.6)V / 5mA = 1.48k$$

$$R_{S\min} = (V_{imin} - V_Z) / I_S = (7 - 5.6)V / 5mA = 280\Omega$$

Select $R_S = 1k$.

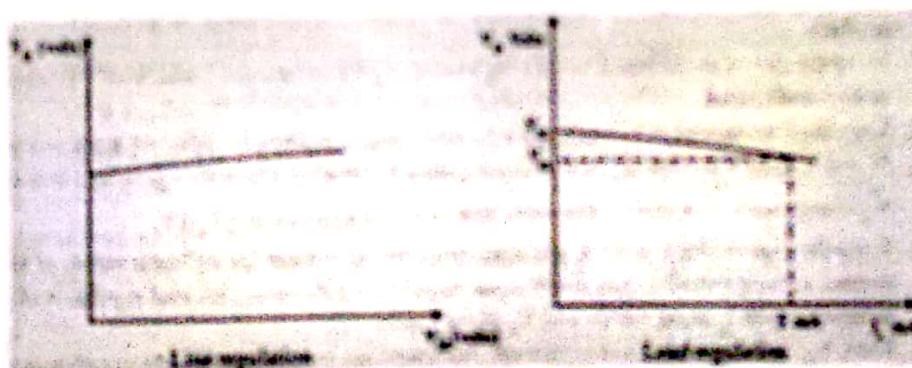
Circuit diagram:



Observation:

I _o = 10mA Line regulation		Load Regulation V _{in} = 10V	
V _{in} (Volts)	V _o (Volts)	I _o (mA)	V _o (Volts)

Expected graph:



Result:

A zener diode shunt regulator was set up and its line and load regulation was calculated.

The % line regulation is -

The % load regulation is -

EXPERIMENT 5

SINGLE STAGE RC COUPLED AMPLIFIER

Aim:

To design and set up an RC-coupled CE amplifier using bipolar junction transistor and plot its frequency response.

Components And Equipments Required:

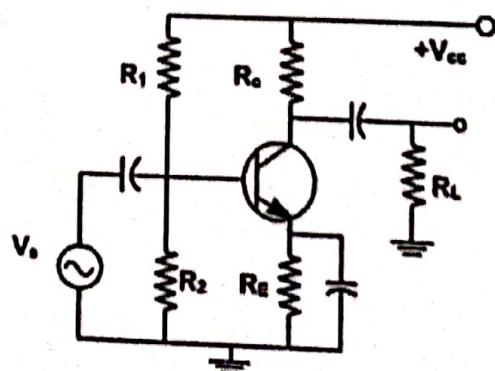
Transistor, dc source, capacitors, resistors, bread board, signal generator, multimeter and CRO

Theory:

RC coupled CE amplifier is widely used in audio frequency applications in radio and TV receiver. It provides current, voltage and power gains. Base current controls the collector current of a common emitter amplifier. A small increase in base current results in a relatively large increase in collector current. Similarly, a small decrease in base current causes large decrease in collector current. The emitter base junction should be forward biased and collector base junction should be in reversed biased for proper functioning of an amplifier. In the circuit diagram ,an NPN transistor is connected as a common emitter ac amplifier.R1 and R2 are employed for the voltage divider bias for the transistor. The input signal V_{in} is coupled through C_{C1} to the base and output voltage is coupled from collector through the capacitor C_{C2} .

Selection Of Supply Voltage V_{cc} :

For distortion less output from an audio amplifier ,the operating point must be kept at middle of the load line selecting $V_{CEQ}=50\%V_{CC}$. However , V_{CC} is selected 20% more than the required voltage swing. For eg, if the required output swing is 10V, V_{cc} is selected 12V.

Circuit Diagram

Design:

Output requirements: Mid-band voltage gain of the amplifier=50

Selection of transistor: Select BC107 since its minimum guaranteed $H_{FE}(100)$ is more than the required gain.(=50) of the amplifier.

DETAILS OF BC107

Type NPN-silicon, Application: In audio frequency

Maximum ratings: $V_{CB}=50V$, $V_{CE}=45V$, $V_{EB}=6V$, $I_C=100mA$

Nominal ratings: $V_{CE}=5V$, $I_C=2mA$, $h_{FE}=100$ to 500

DC BIASING CONDITIONS :

$V_{CC}=12V$, $I_C=2mA$, $V_{RC}=40\%$ of V_{CC} =

$V_{RE}=10\%$ of V_{CC} =

$V_{CE}=50\%$ of V_{CC} =

DESIGN OF R_C : $V_{RC}=I_C \times R_C$

$$R_C = V_{RC}/I_C \\ =$$

DESIGN OF R_E : $V_{RE} = I_E \cdot R_E$

$$R_E = V_{RE}/I_E$$

DESIGN OF VOLTAGE DIVIDER R_1 AND R_2

From the datasheet of BC107 we get H_{FE} min is 100

Assume the current through $R_1 = 10I_B$ and that through $R_2 = 9I_B$ to avoid loading the potential divider network R_1 and R_2 by the base current.

$$V_{R2} = V_{BE} + V_{RE} \\ = 0.7 + 1.2 = 1.9V$$

Also, $V_{R2} = 9I_B R_2$

$$R_2 = V_{R2}/9I_B =$$

$$V_{R1} = V_{CC} - V_{R2} = 12V - 1.9V = 10.1V$$

Also, $V_{R1} = 10I_B R_1 =$

Then $R_1 =$

DESIGN OF R_L :

Gain of the common emitter amplifier is given by the expression $A_v = -(r_o/r_e)$

Where $r_c = R_C // R_L$ and $r_e = 25mV/I_E = 12.5\Omega$

Since the required gain is 50, substituting it in the expression, we get, $R_L =$

DESIGN OF COUPLING CAPACITORS C_{C1} AND C_{C2}

X_{C1} at the lowest frequency (say 100 Hz), should be equal to one-tenth or less of series impedance that being driven by the signal passing through the capacitor. Here R_{in} is the series impedance.

Then $X_{C1} < R_{in}/10$. Here $R_{in} = R_1//R_2//h_{FE}r_e$

We get $R_{in} = 1.1K$ Then $X_{C1} < 110\Omega$

So, $C_{C1} =$

Similarly, $X_{C2} < R_{out}/10$ where $R_{out} = R_C$

Then $X_{C2} =$

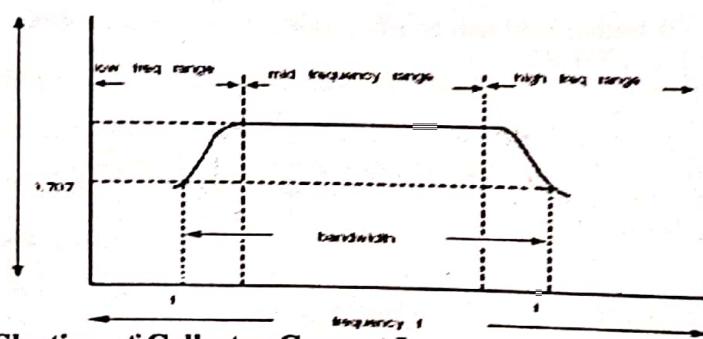
So, $C_{C2} =$

DESIGN OF BYPASS CAPACITORS C_E

To bypass the lowest frequency (say 100 Hz), X_{CE} should be equal to one-tenth or less of the resistance R_E .

Ie, $X_{CE} < R_E/10$, Then $C_E =$

MODEL FREQUENCY RESPONSE



Selection of Collector Current I_c :

The nominal value of I_c can be selected from the data sheet. It is the bias current at which V_{BE} is measured. For BC107 it is 2 mA.

Design Of Emitter Resistor R_E

Current series feedback is used in this circuit using R_E . It stabilizes the operating point against temperature variations. So, as a thumbrule, 10% of V_{CC} is fixed across R_E . Value of R_E is given by the expression

$$R_E = V_{RE}/I_E = V_{RE}/I_C \quad \text{Since } I_E \approx I_C \text{ approximately. } R_E = 0.1 V_{CC}/I_C$$

Design Of Rc Value of R_c can be obtained from the relation $R_c = 0.4 V_{cc}/I_c$ since remaining 40% of V_{cc} is dropped across R_c .

Design Of Potential Divider R_1 And R_2

Value of I_B can be obtained using the expression $I_B = I_c/h_{FE\min}$. At least $10I_B$ should flow through R_1 to have good range of voltage variation across R_1 . When I_B gets branched into the base of transistor, $9I_B$ flows through R_2 . Values of R_1 and R_2 can be calculated from the dc potentials created by the respective currents.

DESIGN OF BYPASS CAPACITOR C_E

The purpose of the bypass capacitor is to bypass signal currents to ground. Its value is chosen as per the following thumb rule. To bypass the lowest frequency, X_{CE} should be equal to one tenth or less of the emitter resistance. ie, $X_{CE} < R_E/10$.

DESIGN OF COUPLING CAPACITOR C_C

Value of the coupling capacitor C_C is obtained such that its reactance X_{C1} at the lowest frequency (say 100Hz or so far an audio amplifier), should be equal to one-tenth or less of the series impedance that being driven by the signal passing through the capacitor. That means X_{C1} must be $< R_{in}/10$. Here $R_{in} = R_1//R_2//h_{fe} r_e$ where r_e is the internal emitter resistance of the transistor given by the expression $= 25mV/I_E$, where 25 mV is temperature equivalent voltage.

PROCEDURE

1. Test all the components using a multimeter. Set up the circuit and verify dc bias conditions. To check dc bias conditions, remove input signal and capacitors in the circuit.
2. Connect capacitors in the circuit. Apply a 100mV peak to peak sinusoidal signal from the function generator to the circuit input. Observe the input and output waveforms on the CRO screen respectively.
3. Keeping the input voltage constant at 100mV, vary the frequency of the input signal from 10 to 1MHz. Measure the output amplitude corresponding to different frequencies and enter it in the Tabular column

4. Plot the frequency response characteristics on a semi log sheet with Gain in dB and Frequency on x-axis. Mark f_L and f_H corresponding to 1/3rd of the maximum gain.
5. Calculate the bandwidth of the amplifier using the expression $BW = f_H - f_L$.
6. Remove the emitter bypass capacitor C_E from the circuit and repeat the steps 1 to 4. Observe that the bandwidth increases and gain decreases in the absence of C_E .

Tabular Column:

Sl. No.	FREQUENCY(Hz)	V _{out} (V)	$\text{Gain} = V_{\text{out}}/V_{\text{in}}$	Comments About Gain

Result:

RC coupled amplifier was designed and its frequency response was plotted

EXPERIMENT 8

LOW FREQUENCY OSCILLATOR A.RC PHASE SHIFT OSCILLATOR

Aim

To design and setup RC phase shift oscillator using opamp for a frequency of 1KHz

Components and equipment required

Sl.. No	Component	Specification	Quantity
1	BJT	BC107	1
2	Resistors	10KΩ	1
		2.2KΩ	1
		4.7KΩ	2
		47KΩ	1
		680Ω	1
3	Capacitors	1μF	1
		0.01μF	3
		22μF	1
4	potentiometer	47KΩ	1

Theory

An oscillator is an electronic circuit for generating an ac signal voltage with a dc supply as the only input requirement. The frequency of the generated signal is decided by the circuit elements. An oscillator requires an amplifier, a frequency selective network, and a positive feedback from the output to the input. The Barkhausen criterion for sustained oscillator is $A\beta = 1$ where A is gain of the amplifier and β is the feedback factor. The unity gain means signal is in phase(If the signal is 180° out of phase , gain will be -1.

If a common emitter amplifier is used, with a resistive collector load, there is a 180° phase shift between the voltage at the base and the collector. Feedback network between the collector and the base must introduce an additional 180° phase shift at a particular frequency. The 3 section of phase shift networks are used so that each section introduce approximately 60° phase shift at resonant frequency. By analysis resonant frequency f can be expressed by the equation,

$$f = \frac{1}{2\pi RC\sqrt{6 + 4Rc/R}}$$

The three section RC network offers a β of 1/29. Hence the gain of the amplifier should be 29. For this the h_{FE} of the transistor is found to be

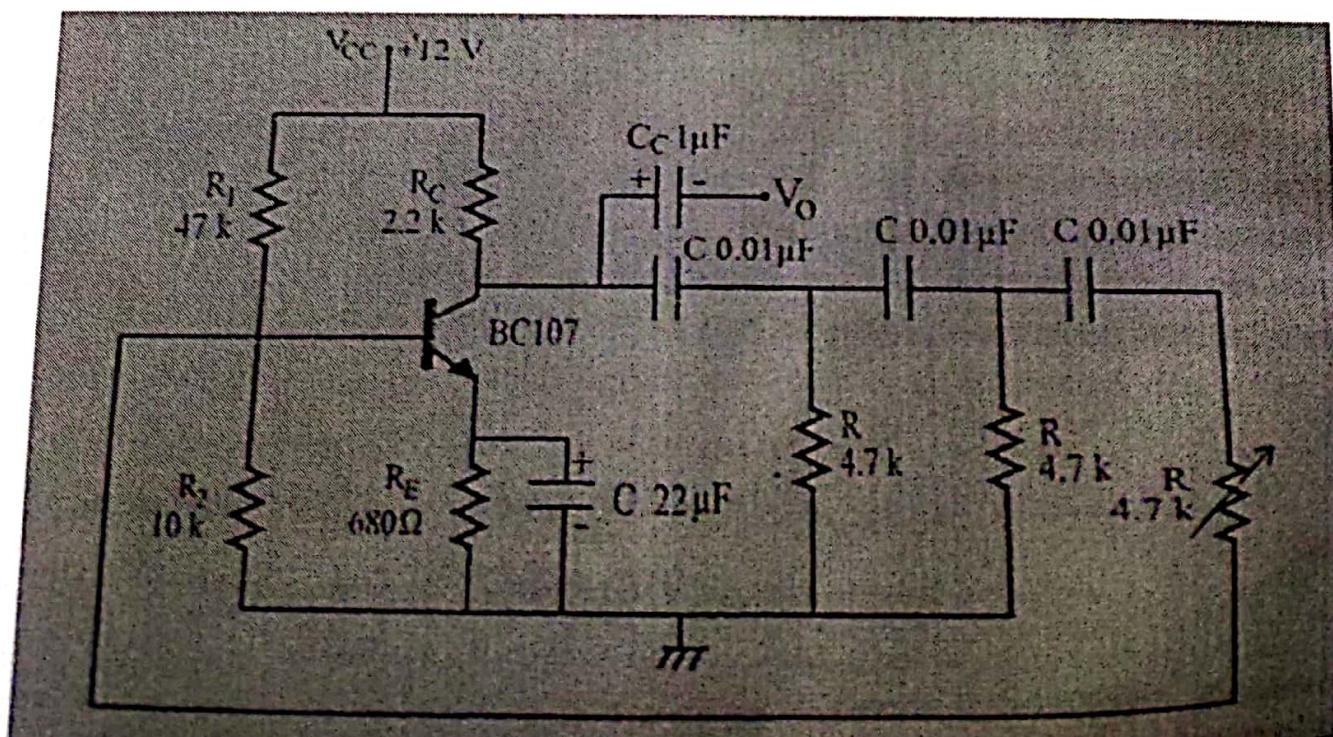
$$h_{FE} \geq 23 + 29(R/Rc) + 4(Rc/R)$$

The phase shift oscillator is particularly useful in the audio frequency range.

Procedure

1. Set up the amplifier part of the oscillator and test the DC conditions. Ensure that the transistor is operating as an amplifier with required gain.
2. Connect the feedback network and observe the sine wave on CRO screen and measure its amplitude and frequency.
3. Observe the waveforms at the base and collector of the transistor simultaneously on CRO screen and notice the phase difference between them.

Circuit Diagram:



Design:

Design of the amplifier : Select transistor BC107. It can provide a gain more than 29 because its minimum h_{FE} is 100.

DC biasing conditions: $V_{CC}=12V$, $I_C=2mA$

$$V_{RC} = 40\% \text{ of } V_{CC} = 4.8V,$$

$$V_{RE} = 10\% \text{ of } V_{CC} = 1.2V$$

$$V_{CE} = 50\% \text{ of } V_{CC} = 6V.$$

Design of R_C : $V_{RC}=I_C \times R_C=4.8V$.

From this, we get $R_C=2.4k$. Use 2.2 k std.

Design of R_E : $V_{RE}=I_E \times R_E=I_C \times R_E=1.2V$.

From this we get, $R_E=600\Omega$. Select 680Ω std.

Design of voltage divider R_1 and R_2 :

From the data sheet of BC 107 we get h_{FE} min is 100.

$$I_B = I_C/h_{FE} = 2mA/100 = 20\mu A.$$

Assume the current through $R_1 = 10 I_B$ and that through $R_2 = 9 I_B$ to avoid loading the potential divider by the base current.

$$V_{R2} = \text{Voltage across } R_2 = V_{BE} + V_{RE}$$

$$\text{i.e. } V_{R2} = V_{BE} + V_{RE} = 0.7 + 1.2 = 1.9V. \text{ Also, } V_{R2} = 9I_B R_2 = 1.9V$$

$$\text{Then } R_2 = \frac{1.9}{9 \times 20 \times 10^{-6}} = 10.6K\Omega. \text{ Select } 10K \text{ std.}$$

$$V_{R1} = \text{voltage across } R_1 = V_{CC} - V_{R2} = 12V - 1.9V = 10.1V$$

$$\text{Also, } V_{R1} = 10 I_B, R_1 = 10.1V,$$

$$\text{Then } R_1 = \frac{10.1}{10 \times 20 \times 10^{-6}} = 50K\Omega. \text{ Select } 47K \text{ pot std}$$

Design of frequency selective network

Required frequency of oscillation is 1KHz

$$F = \frac{1}{2\pi R C \sqrt{6+4R_C/R}} = 1 \text{ KHz}$$

Take $R=4.7K$ to avoid loading of R_C by the RC network. Then $C = 0.01\mu F$

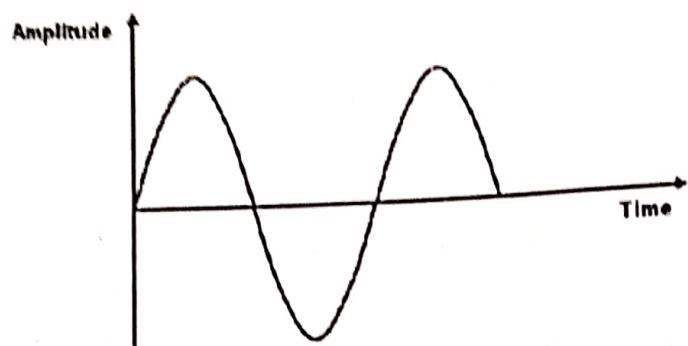
Use 4.7K pot in the last RC stage.

Design of bypass (C_E and $C_{E''}$)

i.e., $X_{CE} \leq R_E/10$. Then $C_E \geq 1/(2\pi \cdot 100 \cdot 68) = 23\mu F$, assuming $f_L = 100\text{Hz}$.

Use $22\mu F$.

Expected Waveform:



Result

RC phase shift oscillator using opamp for a frequency of oscillation of 1 KHz was setup and designed.

The amplitude = V

Time period = ms

Frequency = KHz

EXPERIMENT 11

CLIPPING AND CLAMPING CIRCUITS

Aim:

- (a) To design and set up various shunt clipping circuits using diodes and zener diodes.
- (b) To design and set up various clamping circuits using diodes and capacitors.

Components required:

Sl. No:	Component	Specification	Quantity
1	Diode	1N4001	2
2	Zener diode	SZ5V6	2
3	Resistor	1KΩ	1
4	Resistor	10 KΩ	1
5	Capacitor	1μF	1

Theory:

(a) Clipper

A circuit which removes the peak of a waveform is known as a clipper. A clipper circuit clips a fraction of its input signal keeping the remaining part of the signal unchanged. The circuit limits an input voltage to certain minimum and maximum values. A clipping circuit consists of linear elements like resistors and non-linear elements like junction diodes or transistors, but it does not contain energy-storage elements like capacitors.

1.1 Positive Clipper

In this circuit, the diode is forward biased (cathode more positive than anode) during the positive half cycle of the sinusoidal input waveform. For the diode to become forward biased, it must have the input voltage magnitude greater than +0.7 volts (0.3 volts for a germanium diode).

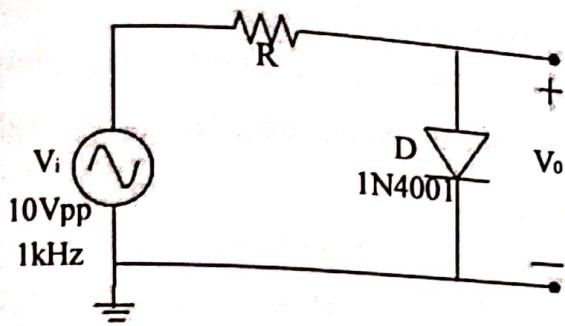
Design:

Choose $I_{max} = 10mA$

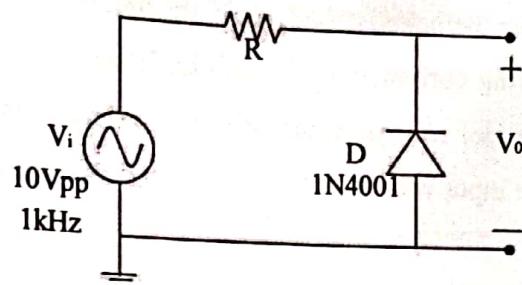
$$R \geq \frac{V}{I_{max}}$$

Circuit diagram:

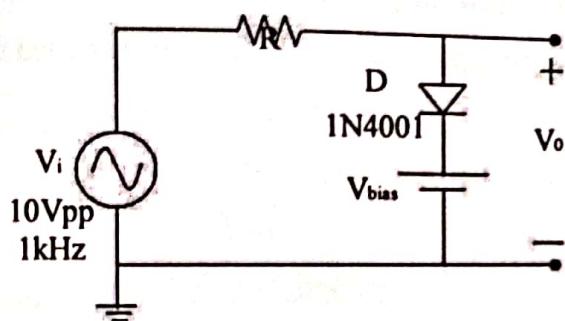
Positive Clipper



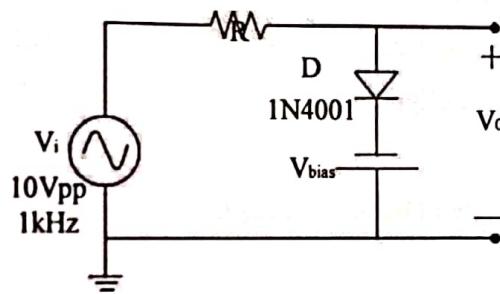
Negative Clipper



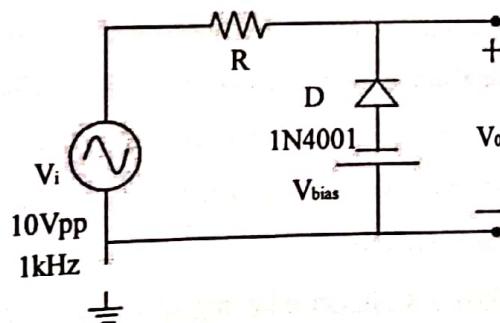
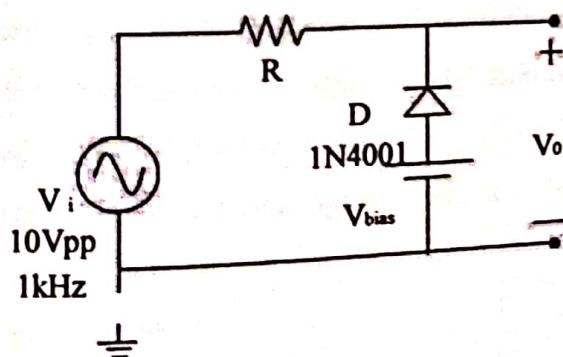
Positive clipper with positive bias



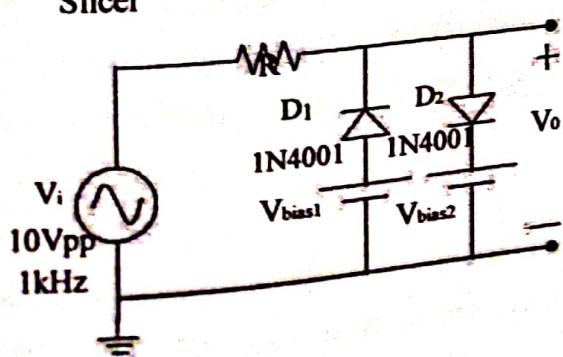
Positive clipper with negative bias



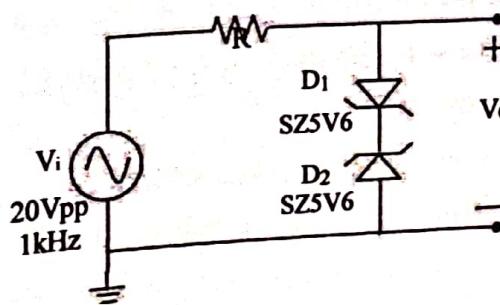
Negative clipper with positive bias Negative clipper with negative bias



Slicer



Combinational clipper using zeners



When this happens the diodes begins to conduct and holds the voltage across itself constant at 0.7V until the sinusoidal waveform falls below this value. Thus the output voltage which is taken across the diode can never exceed 0.7 volts during the positive half cycle.

During the negative half cycle, the diode is reverse biased (anode more positive than cathode) blocking current flow through itself and as a result has no effect on the negative half of the sinusoidal voltage which passes to the load unaltered. Then the diode limits the positive half of the input waveform and is known as a positive clipper circuit.

1.2 Negative Clipper

The diode is forward biased during the negative half cycle of the sinusoidal waveform and clips it to -0.7 volts while allowing the positive half cycle to pass unaltered when reverse biased. As the diode limits the negative half cycle of the input voltage it is therefore called a negative clipper circuit.

1.3 Biased Diode Clipping Circuits

1.3.1 Positive clipper with positive bias

To produce diode clipping circuits for voltage waveforms at different levels, a bias voltage, V_{bias} is added in series with the diode as shown. The voltage across the series combination must be greater than $V_{bias} + 0.7V$ to conduct. For example, if the V_{bias} level is set at 4.0 volts, then the sinusoidal voltage at the diode's anode terminal must be greater than $4.0 + 0.7 = 4.7$ volts for it to become forward biased. Any anode voltage levels above this bias point are clipped off.

1.3.2 Positive clipper with negative bias

The diode is forward biased during the entire duration of the positive half cycle. During the negative half cycle the diode is forward biased till the input is greater than $0.7V - V_{bias}$ otherwise the diode is reverse biased. When the diode is reverse biased the output follows the input.

1.3.2 Negative clipper with positive bias

During the positive half cycle when the input voltage is lesser than V_{bias} the diode becomes forward biased. The corresponding output voltage is at $V_{bias} - 0.7$. During the

negative half cycle the diode is forward biased

1.3.3 Negative clipper with negative bias

During the negative half cycle, when the input voltage becomes less than V_{bias} , diode becomes forward biased and voltage $-(V_{bias}+0.7)$ appears at the output. During the positive half cycle, when the input is greater than V_{bias} , diode is reverse biased and the input appears at the output.

1.3.4 Slicer

A variable diode clipping or diode limiting level can be achieved by varying the bias voltage of the diodes. If both the positive and the negative half cycles are to be clipped, then two biased clipping diodes are used. For a slicer (with reference to figure)two positive bias voltage is required V_{bias1} and V_{bias2} ($V_{bias1} < V_{bias2}$). The output voltage works according to the following condition.

1. $V_{in} < V_{bias1} - 0.7$, $V_{out} = V_{bias1} - 0.7$
2. $V_{bias1} + 0.7 < V_{in} < V_{bias2} + 0.7$, $V_{out} = V_{in}$
3. $V_{in} > V_{bias2}$, $V_{out} = V_{bias2}$

1.3.5 Zener Diode Clipping

One easy way of creating biased diode clipping circuits without the need for an additional emf supply is to use Zener Diodes.

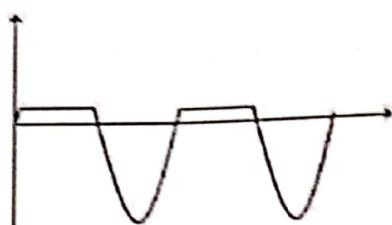
In the given circuit the output waveform will be clipped at the zener voltage plus the 0.7V forward volt drop of the other diode. So for example, the positive half cycle will be clipped at the sum of zener diode, ZD1 plus 0.7V from ZD2 and vice versa for the negative half cycle.

Procedure:

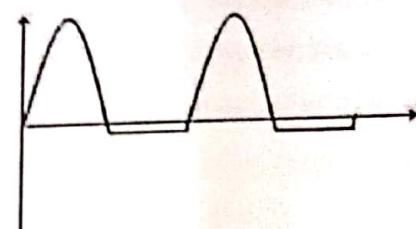
1. Check all the components using multimeter.
2. Set up the circuit as shown in the circuit diagram.
3. Apply a sine wave of amplitude 20 Vpp and frequency 1kHz to the circuit.

Expected waveforms:

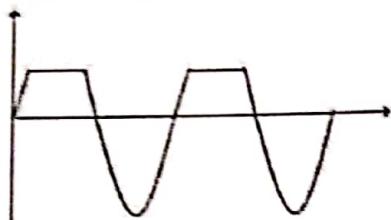
Positive clipper



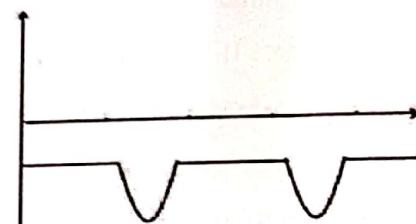
Negative clipper



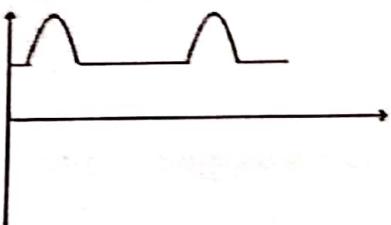
Positive clipper with positive bias



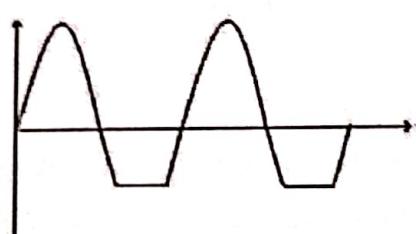
Positive clipper with negative bias



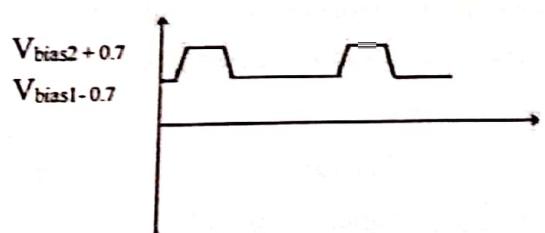
Negative clipper with positive bias



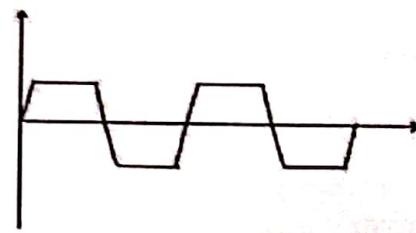
Negative clipper with negative bias



Slicer



Combinational clipper using zeners



(a)Clamper

A clamper is an electronic circuit that moves the whole signal up or down so as to place the peaks at the reference level. A diode clamp consists of a diode, which conducts electric current in only one direction and prevents the signal exceeding the reference value; and a capacitor which provides a DC offset from the stored charge. The capacitor forms a time constant with the resistor load which determines the range of frequencies over which the clamper will be effective.

Positive clamper

In the negative cycle of the input AC signal, the diode is forward biased and conducts, charging the capacitor to the peak negative value of V_{IN} . During the positive cycle, the diode is reverse biased and thus does not conduct. The output voltage is therefore equal to the voltage stored in the capacitor plus the input voltage.

Negative clamper

A negative unbiased clamp is the opposite of the equivalent positive clamp. In the positive cycle of the input AC signal, the diode is forward biased and conducts, charging the capacitor to the peak positive value of V_{IN} . During the negative cycle, the diode is reverse biased and thus does not conduct. The output voltage is therefore equal to the voltage stored in the capacitor plus the input voltage again.

Positive biased

A positive biased voltage clamp is identical to an equivalent unbiased clamp but with the output voltage offset by the bias amount V_{BIAS} .

Negative biased

A negative biased voltage clamp is likewise identical to an equivalent unbiased clamp but with the output voltage offset in the negative direction by the bias amount V_{BIAS} .

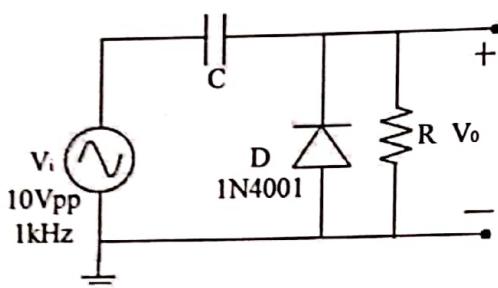
Procedure:

1. Check all the components using multimeter.
2. Set up the circuit as shown in the circuit diagram.

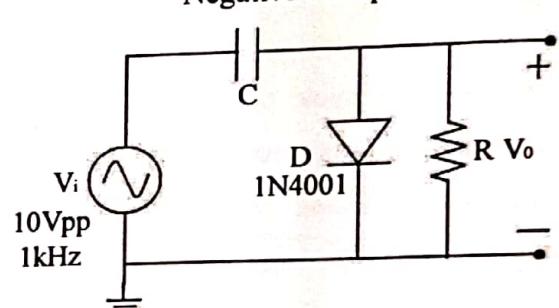
3. Apply a sine wave of amplitude 20 Vpp and frequency 1kHz to the circuit.
4. Keep the CRO in dual mode and connect input to channel 2 and output to channel 1.
5. Observe the output waveform and note down the clamping levels.
6. Keep the CRO in X-Y mode and observe the transfer characteristics.
7. Plot the output waveforms and transfer characteristics .

Circuit diagram

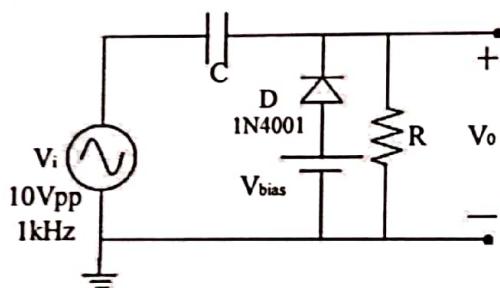
Positive clampper



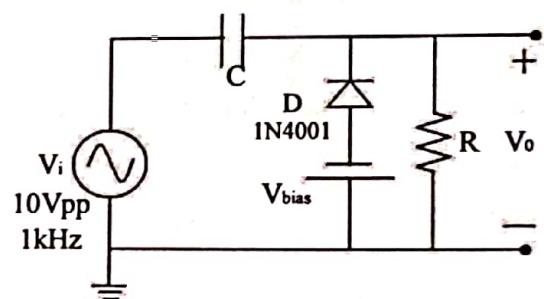
Negative clampper



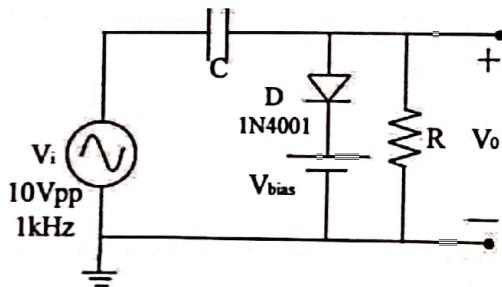
Positive clampper with positive bias



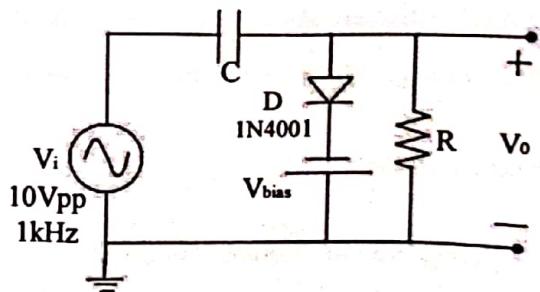
Positive clampper with negative bias



Negative clampper with positive bias



Negative clampper with negative bias



Design:

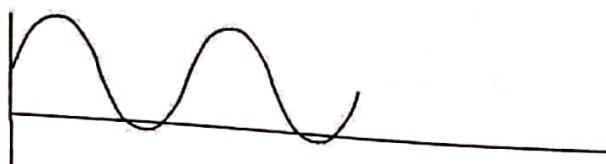
$RC \gg T$ where T is the time period of the input signal.

Here $T=1\text{ms}$.

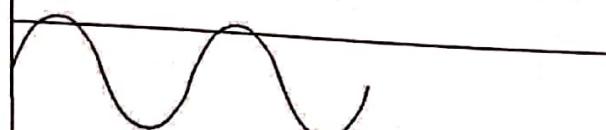
Let $RC=10T$

Assume $C=1\mu F$; then $R=10T/C = 10k\Omega$

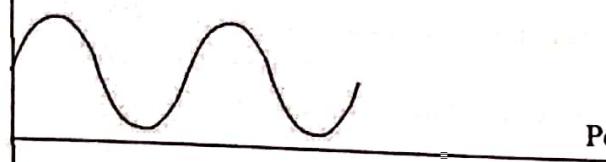
Expected waveforms:



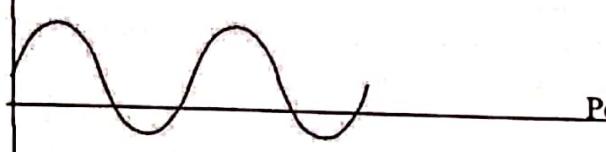
Positive Clamp



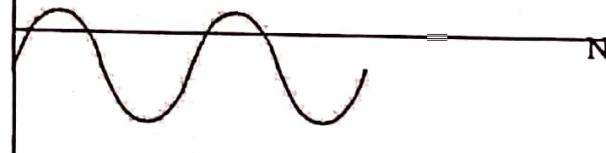
Negative Clamp



Positive Clamp with positive bias



Positive Clamp with negative bias



Negative Clamp with positive bias



Negative Clamp with negative bias

Result:

Designed and set up various clippers and clamping circuits and observed the output waveforms

EXPERIMENT 16

MULTIVIBRATORS

I.ASTABLE MULTIVIBRATOR

Aim:

To design and set up an astable multivibrator using transistors ,study its performance and observe the waveform

Equipments and components required:

Transistors ,resistors ,capacitors ,breadboard,dc supply,multimeter and CRO.

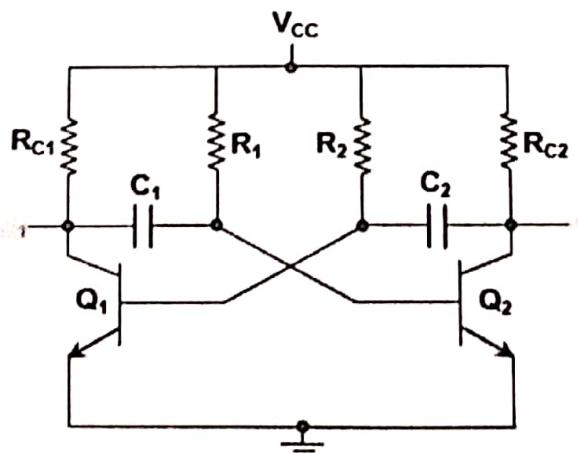
Theory:

Astable multivibrator is also called free running oscillator .It does not have stable state .Astable circuit switches back and forth between two quasi stable states. depending upon the charging and discharging periods of two timing capacitors. Time duration in which Q2 remains in ON state is given by $T_2=0.69R_2C_2$ and time duration in which Q2 remains in ON state is given by $T_1=0.69R_1C_1$.If $R_1=R_2=R$ and $C_1=C_2=C$,Then $T_1=T_2=T=0.69RC$.Now the duty cycle is $\frac{1}{2}$ and the time period of the output $T=T_1+T_2=1.38RC$.

Procedure:

- 1.Verify the condition of all components ,devices and probs.
- 2.Set up the circuit and observe the collector and base waveforms of both transistors.

Circuit diagram



Design

Output requirement-A square wave of amplitude 9V, frequency 1kHz and duty cycle =1/3. Choose transistor BC107.

Take VCC=9V

Design of RC1 and RC2 $RC_1 = V_{CC} - V_{CE\text{ sat}} / I_C = (9 - 0.30) / 2\text{mA} = 4.35\text{k}$. Use 4.7k.

$RC_1 = RC_2 = 4.7\text{k}$.

Design of R1 and R2

$I_{B\text{min}} = I_C / h_{FE} = 20\mu\text{A}$.

$R_1 = (V_{CC} - V_{BE\text{ sat}}) / I_B = 83\text{k}$. Use 82k. Take $R_1 = R_2$.

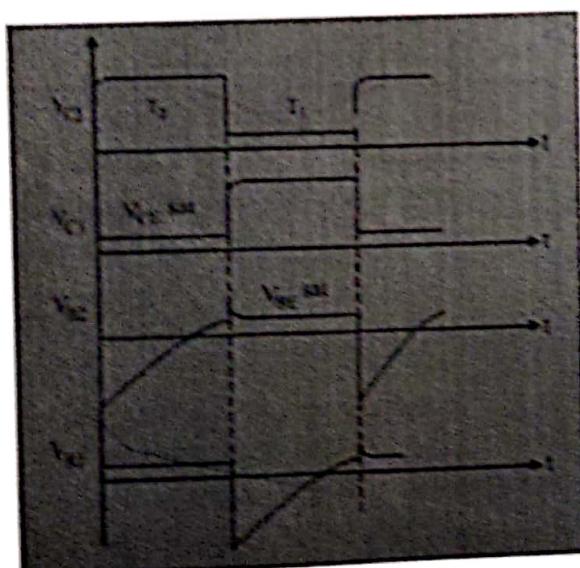
Design of C1 and C2

$T = T_1 + T_2 = 1\text{ms}$ and duty cycle = $T_1 / (T_1 + T_2) = 1/3$.

$T_1 = 0.33\text{ms} = 0.69R_1C_1$. Then $C_1 = 0.006\mu\text{F}$. Use $0.01\mu\text{F}$.

$T_2 = 0.66\text{ms} = 0.69R_2C_2$. Then $C_2 = 0.022\mu\text{F}$.

Waveforms



Result: Design and set up an astable multivibrator has been done.

EXPERIMENT 20

RC INTEGRATING AND DIFFERENTIATING CIRCUITS

RC INTEGRATOR

Aim :

To design and construct RC integrator circuit and study its pulse response.

Components required:

Capacitor, Resistor, Function generator, Oscilloscope, Multimeter, Breadboard.

Theory:

An RC integrator circuit is a wave shaping circuit. It constitutes a resistor in series and a capacitor in parallel to the output. As the name suggests it does the mathematical operation 'integration' on the input signal. The time constant RC of the circuit is very large in comparison with the time period of the input signal. Under this condition the voltage drop across C will be very small in comparison with the voltage drop across R . For satisfactory integration it is necessary that $RC \geq 16T$, where T is time period of the input. When pulse waveform is given at the input, capacitor charges through R and output voltage builds up slowly. Capacitor continues to charge as long as input voltage is present. When input falls to zero, capacitor discharges and output falls to zero slowly. As the value of $RC \gg T$, the charging current is almost constant and the output becomes linear. Hence a square pulse input provides a triangular output.

PROCEDURE

- 1) Test the components
- 2) Assemble the circuit on a breadboard
- 3) Connect the output of a function generator to the input of the differentiator circuit
- 4) Switch on the function generator and set the output at 5V, 1KHz pulse
- 5) Connect the output of the differentiator to an oscilloscope

- 6) Observe the output waveform and its amplitude for the following condition by varying the time period (T) of the input
- 7) Plot all the input and output waveforms

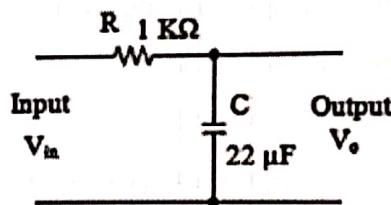
DESIGN

Let the input be a square pulse of 1 KHz Then $T = 1\text{ms}$ For an integrator $RC \geq 16T$ To avoid loading select R as 10 times the output impedance of the function generator If it is 100 Ω , then $R = 1\text{K}\Omega$ Substituting the value of R in the expression, $RC = 16T$, we get C = 16 μF Therefore C should be greater than 16 μF . Hence choose C = 22 μF

OBSERVATIONS To observe the response of the circuit, you can change either the RC value of the circuit or T of the input. Here T of the input is changed.

1. $f = 1\text{ KHz}$, $T = 1\text{ms}$, $RC = 22\text{ms}$ ($RC > T$)
2. $f = 100\text{ KHz}$, $T = 10\text{ms}$, $RC = 22\text{ms}$ ($RC > T$)
3. $f = 10\text{ Hz}$, $T = 100\text{ms}$, $RC = 22\text{ms}$ ($RC < T$)
4. $f = 1\text{ Hz}$, $T = 1\text{s}$, $RC = 22\text{ms}$ ($RC \ll T$)

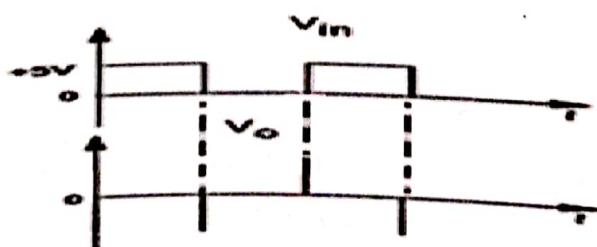
Circuit diagram



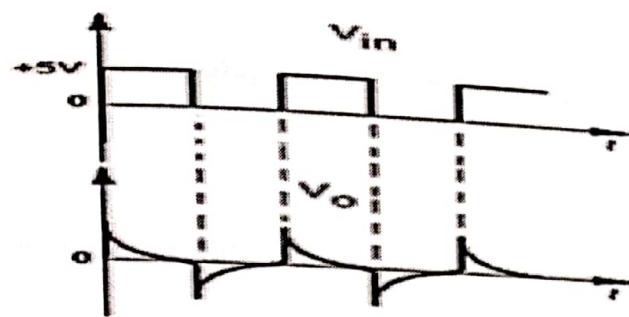
Observations

To observe the response of the circuit, you can change either the RC value of the circuit or T of the input. Here T of the input is changed.

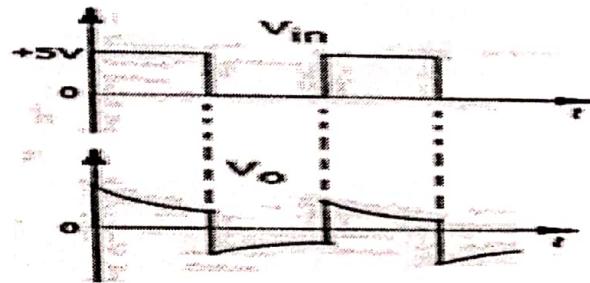
1. $f = 1\text{ KHz}$, $T = 1\text{ms}$, $RC = 22\text{ms}$ ($RC \gg T$)



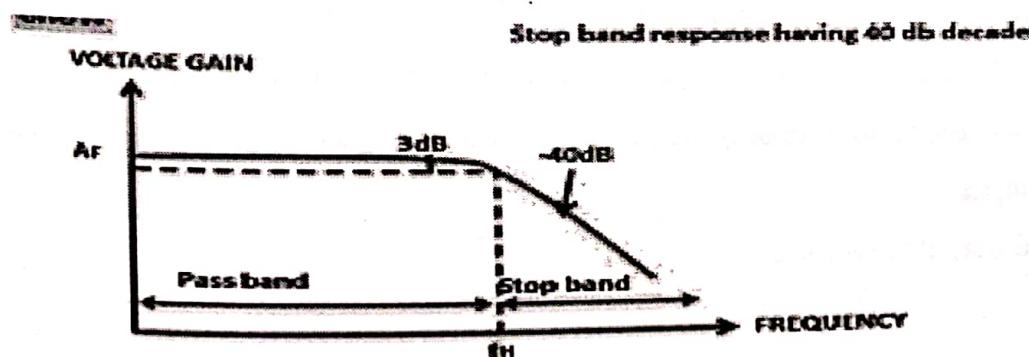
2. $f = 100 \text{ KHz}$, $T = 0.01\text{ms}$, $RC = 1\mu\text{s}$ ($RC < T$)



3. $f = 1 \text{ MHz}$, $T = 1\mu\text{s}$, $RC = 1\mu\text{s}$ ($RC \geq T$)



Frequency response:



Result: Design and construct RC integrator circuit has been done.

RC DIFFERENTIATOR

Aim:

To design and construct RC differentiator circuit and study its pulse response.

Components required:

Capacitor, Resistor ,Function generator,, Oscilloscope ,Multimeter ,Breadboard

Theory:

RC differentiator will simply act as a simple high pass filter (HPF) with a cut-off or corner frequency that corresponds to the RC time constant (τ , τ) of the series network.

Thus when fed with a pure sine wave an RC differentiator circuit acts as a simple passive high pass filter due to the standard capacitive reactance formula of $X_C = 1/(2\pi f C)$.

RC time constant, $\tau = RC$.

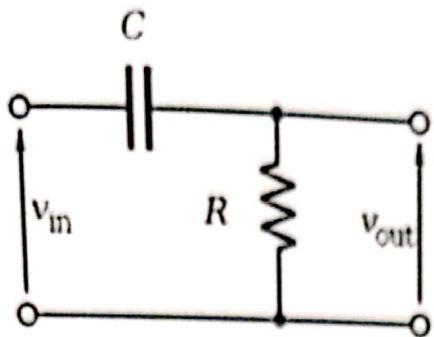
PROCEDURE

- 1) Test the components
- 2) Assemble the circuit on a breadboard
- 3) Connect the output of a function generator to the input of the differentiator circuit
- 4) Switch on the function generator and set the output at 5V, 1KHz pulse
- 5) Connect the output of the differentiator to an oscilloscope
- 6) Observe the output waveform and its amplitude for the following condition by varying the time period (T) of the input.
- 7) Plot all the input and output waveforms.

Design:

Let the input be a square pulse of 1 KHz Then $T = 1\text{ms}$ For an integrator $RC \geq 16T$ To avoid loading select R as 10 times the output impedance of the function generator If it is $100\ \Omega$, then $R = 1\text{K}\Omega$ Substituting the value of R in the expression, $RC = 16T$, we get $C = 16\mu\text{F}$ Therefore C should be greater than $16\mu\text{F}$. Hence choose $C = 22\mu\text{F}$.

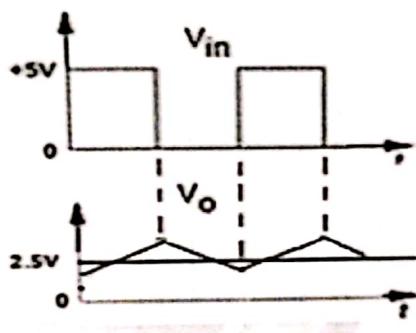
Circuit diagram:



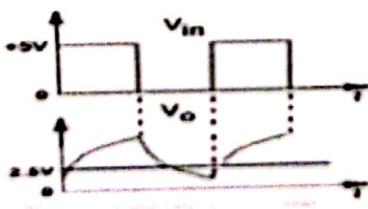
Observations

To observe the response of the circuit, you can change either the RC value of the circuit or T of the input. Here T of the input is changed.

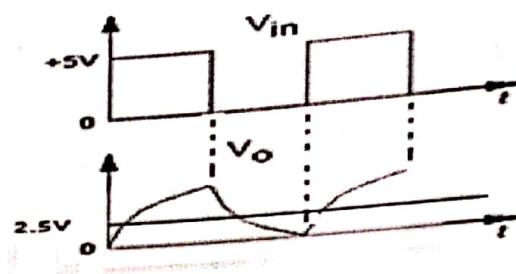
1. $f = 1 \text{ KHz}$, $T = 1\text{ms}$, $RC = 22\text{ms}$ ($RC \gg T$)



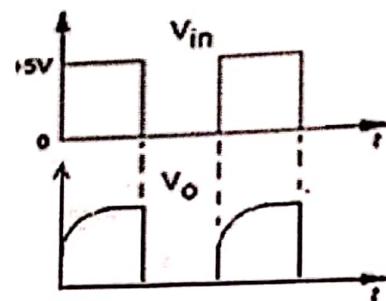
2. $f = 100 \text{ KHz}$, $T = 10\text{ms}$, $RC = 22\text{ms}$ ($RC > T$)



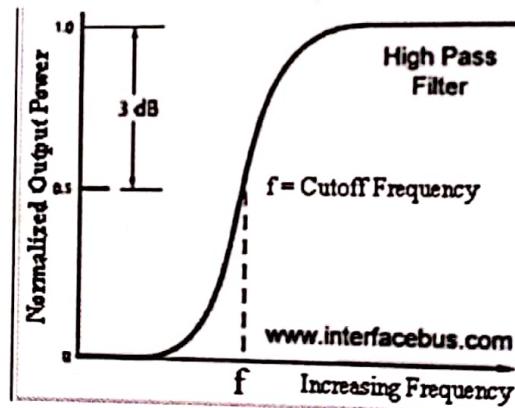
3. $f = 10 \text{ Hz}$, $T = 100\text{ms}$, $RC = 22\text{ms}$ ($RC < T$)



4. $f = 1 \text{ Hz}$, $T = 1 \text{ s}$, $RC = 22\text{ms}$ ($RC \ll T$)



Frequency response



Result: Design and construct RC differentiator circuit has been done.