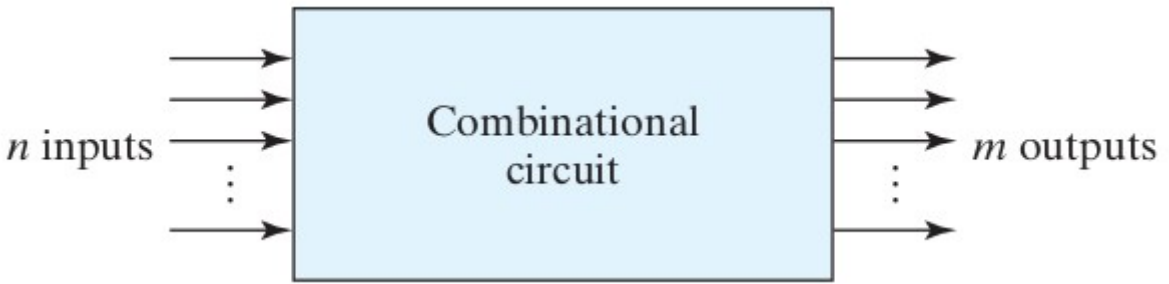
COMBINATIONAL CIRCUITS

COMBINATIONAL CIRCUITS

- A combinational circuit consists of an interconnection of logic gates.
- Combinational logic gates react to the values of the signals at their inputs and produce the value of the output signal, transforming binary information from the given input data to a required output data.
- Block diagram:



- The n input binary variables come from an external source; the m output variables are produced by the internal combinational logic circuit and go to an external destination.

COMBINATIONAL CIRCUITS

- For n input variables, there are $\mathbf{2^n}$ possible combinations of the binary inputs. For each possible input combination, there is one possible value for each output variable.
- Thus, a combinational circuit can be specified with a truth table that lists the output values for each combination of input variables.
- A combinational circuit also can be described by **m** Boolean functions, one for each output variable. Each output function is expressed in terms of the **n** input variables.

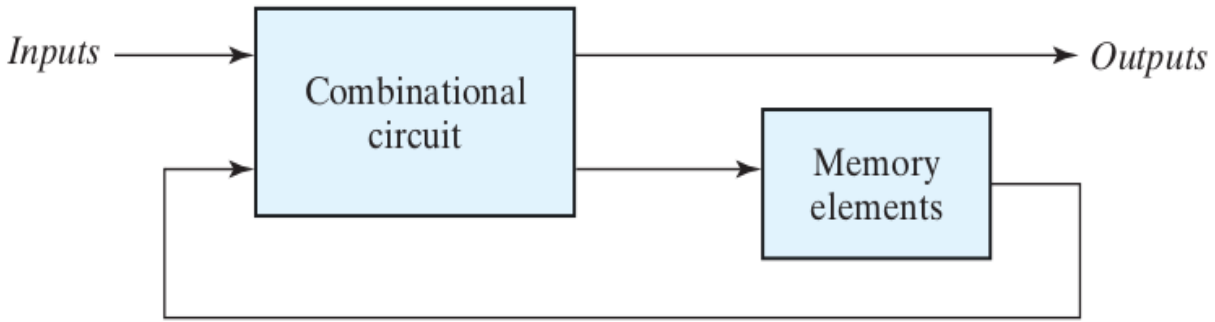
  Eg: adders, subtractors, comparators, decoders, encoders, multiplexers ...
- The diagram of a combinational circuit has logic gates with no feedback paths or memory elements.
- A feedback path is a connection from the output of one gate to the input of a second gate whose output forms part of the input to the first gate.

SEQUENTIAL CIRCUITS

- It consists of a combinational circuit to which storage elements are connected to form a **feedback path**.
- The **storage elements** are devices capable of storing binary information. The binary information stored in these elements at any given time defines the **state** of the sequential circuit at that time.
- The sequential circuit receives binary information from external inputs that, together with the present state of the storage elements, determine the binary value of the outputs.
- These external inputs also determine the condition for changing the state in the storage elements.

SEQUENTIAL CIRCUITS

- Block diagram:



- The block diagram demonstrates that the outputs in a sequential circuit are a function not only of the inputs, but also of the present state of the storage elements.
- The next state of the storage elements is also a function of external inputs and the present state. Thus, a sequential circuit is specified by a time sequence of inputs, outputs, and internal states.
- In contrast, the outputs of combinational logic depend only on the present values of the inputs.

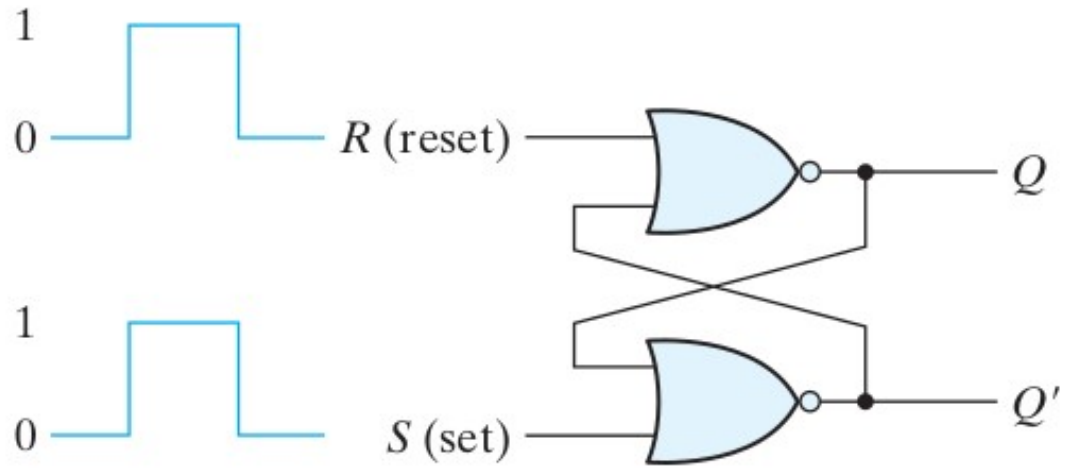
SEQUENTIAL CIRCUITS

- There are two main types of sequential circuits, and their classification is a function of the timing of their signals.
- A **synchronous** sequential circuit is a system whose behavior can be defined from the knowledge of its signals at discrete instants of time.
- The behavior of an **asynchronous** sequential circuit depends upon the input signals at any instant of time and the order in which the inputs change.
- The storage elements commonly used in asynchronous sequential circuits are time-delay devices.
- A synchronous sequential circuit employs signals that affect the storage elements at only discrete instants of time. Synchronization is achieved by a timing device called a **clock generator**, which provides a clock signal having the form of a periodic train of clock pulses.
- In practice, the clock pulses determine when computational activity will occur within the circuit, and other signals (external inputs and otherwise) determine what changes will take place affecting the storage elements and the outputs. Synchronous sequential circuits that use clock pulses to control storage elements are called **clocked sequential circuits** and are the type most frequently encountered in practice.

Storage Elements: Latches

- A storage element in a digital circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit), until directed by an input signal to switch states.
- The major differences among various types of storage elements are in the number of inputs they possess and in the manner in which the inputs affect the binary state.
- Storage elements that operate with signal levels (rather than signal transitions) are referred to as **latches**; those controlled by a clock transition are **flip-flops**.
- **Latches are said to be level sensitive devices; flip-flops are edge sensitive devices.**

SR Latch –
cross-coupled NOR gate implementation

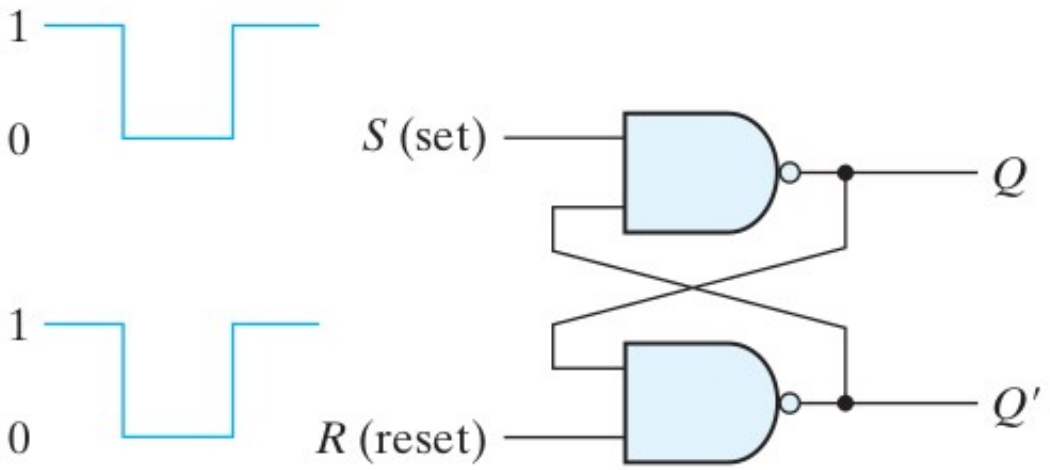


(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden)

(b) Function table

SR Latch –
cross-coupled NAND gate implementation

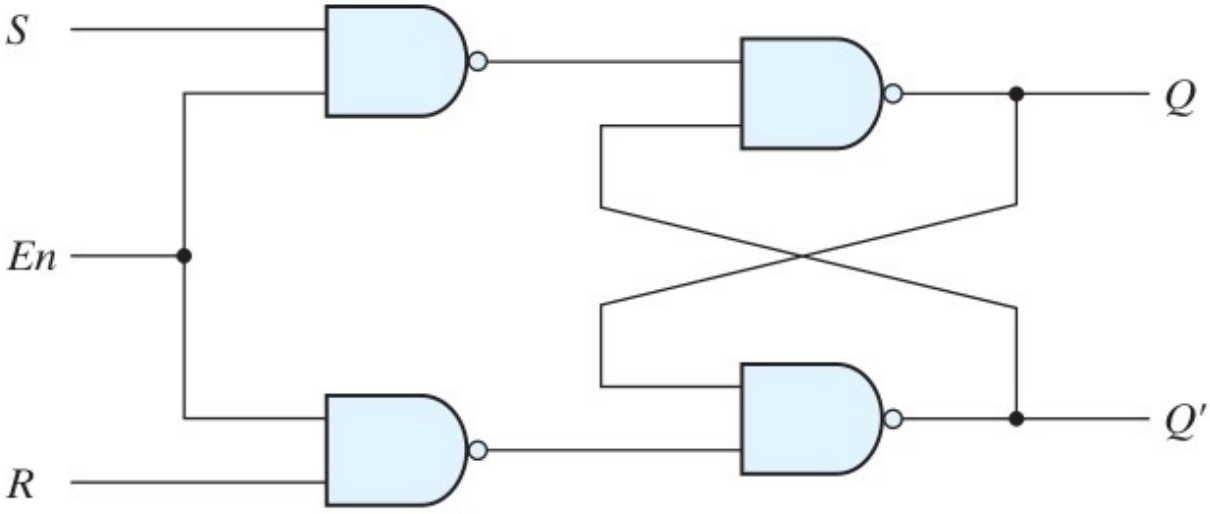


(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

(b) Function table

SR Latch –
with enable/ control input

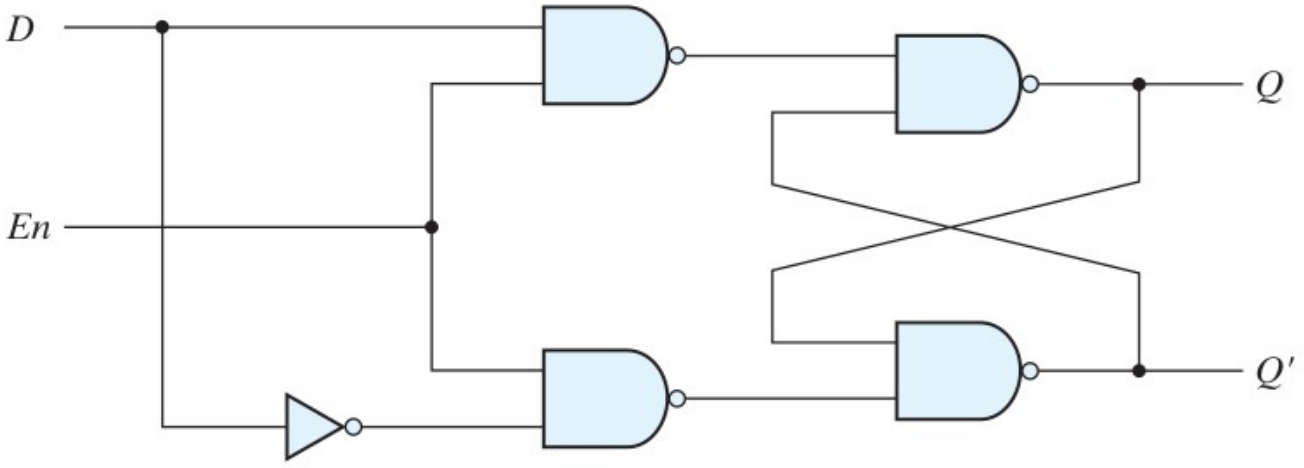


(a) Logic diagram

En	*S*	*R*	Next state of *Q*
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

(b) Function table

D Latch (Transparent Latch)

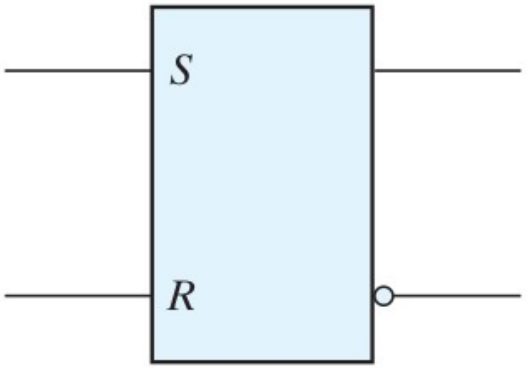


(a) Logic diagram

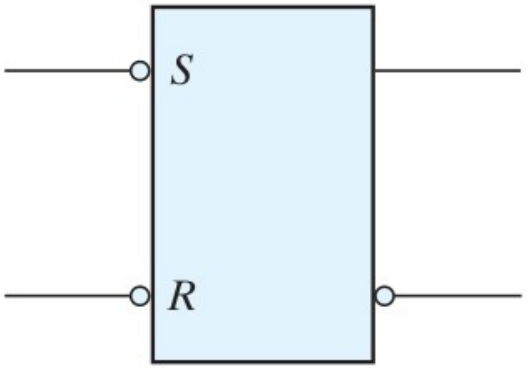
En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

(b) Function table

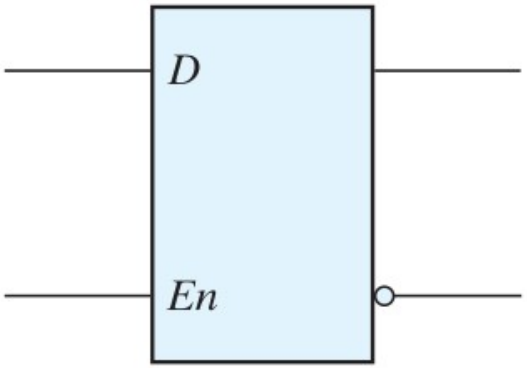
Graphic symbols for latches



SR



$\overline{S}\overline{R}$



D

Storage Elements: Flip-Flops

- The state of a latch or flip-flop is switched by a change in the control input. This momentary change is called a **trigger**, and the transition it causes is said to trigger the flip-flop.
- Flip-flop circuits are constructed in such a way as to make them operate properly when they are part of a sequential circuit that employs a common clock.
- The problem with the latch is that it responds to a change in the level of a clock pulse.
- The key to the proper operation of a flip-flop is to trigger it only during a signal transition .
- A clock pulse goes through two transitions: from 0 to 1 and the return from 1 to 0. The positive transition is defined as the positive edge and the negative transition as the negative edge.
- There are two ways that a latch can be modified to form a flip-flop. One way is to employ two latches in a special configuration that isolates the output of the flip-flop and prevents it from being affected while the input to the flip-flop is changing.
- Another way is to produce a flip-flop that triggers only during a signal transition (from 0 to 1 or from 1 to 0) of the synchronizing signal (clock) and is disabled during the rest of the clock pulse.

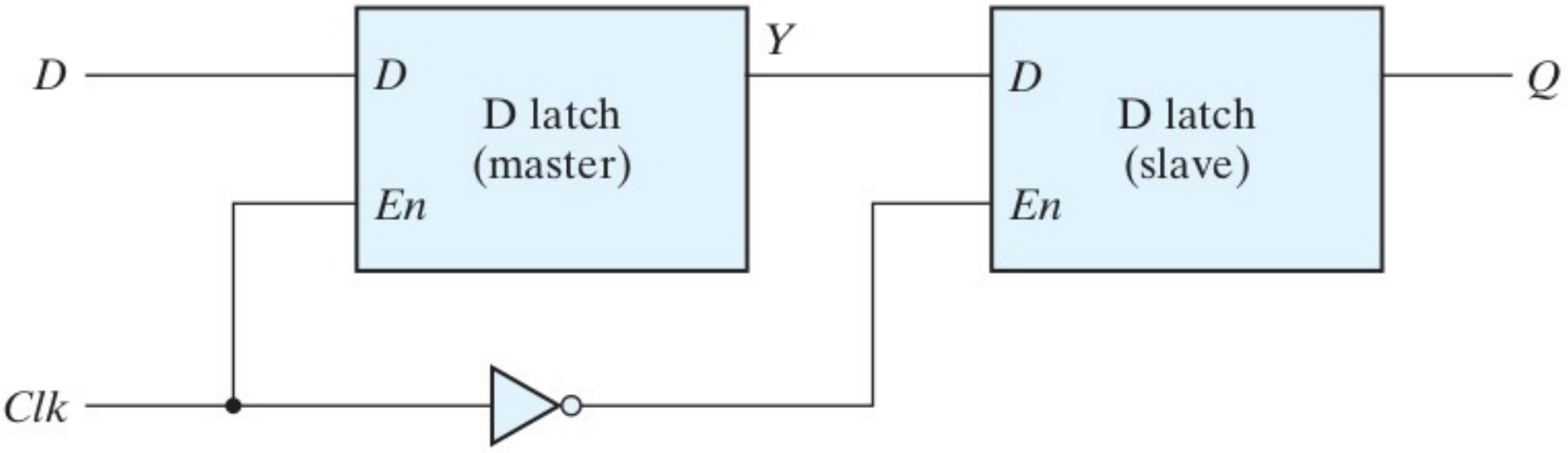
Clock response in latch and flip-flop

(a) Response to positive level

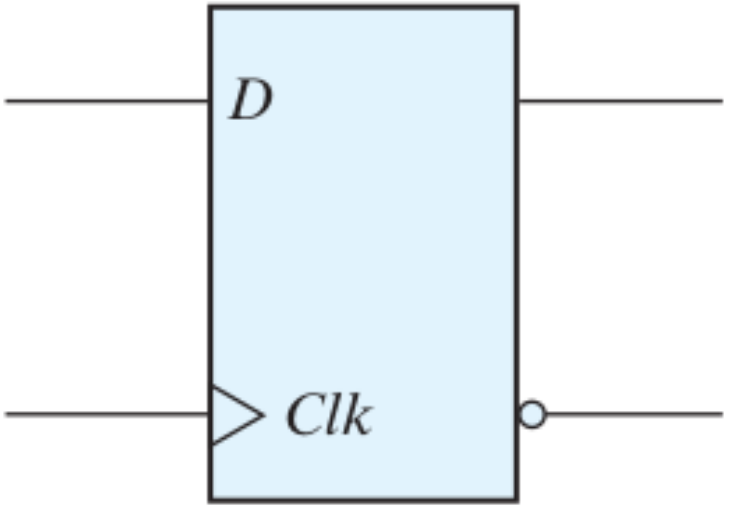
(b) Positive-edge response

(c) Negative-edge response

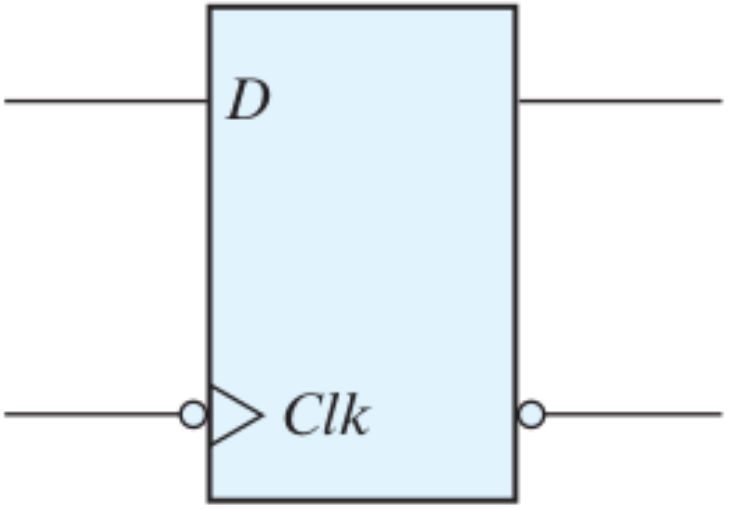
Edge-Triggered D Flip-Flop



Graphic symbol for edge-triggered D flip-flop

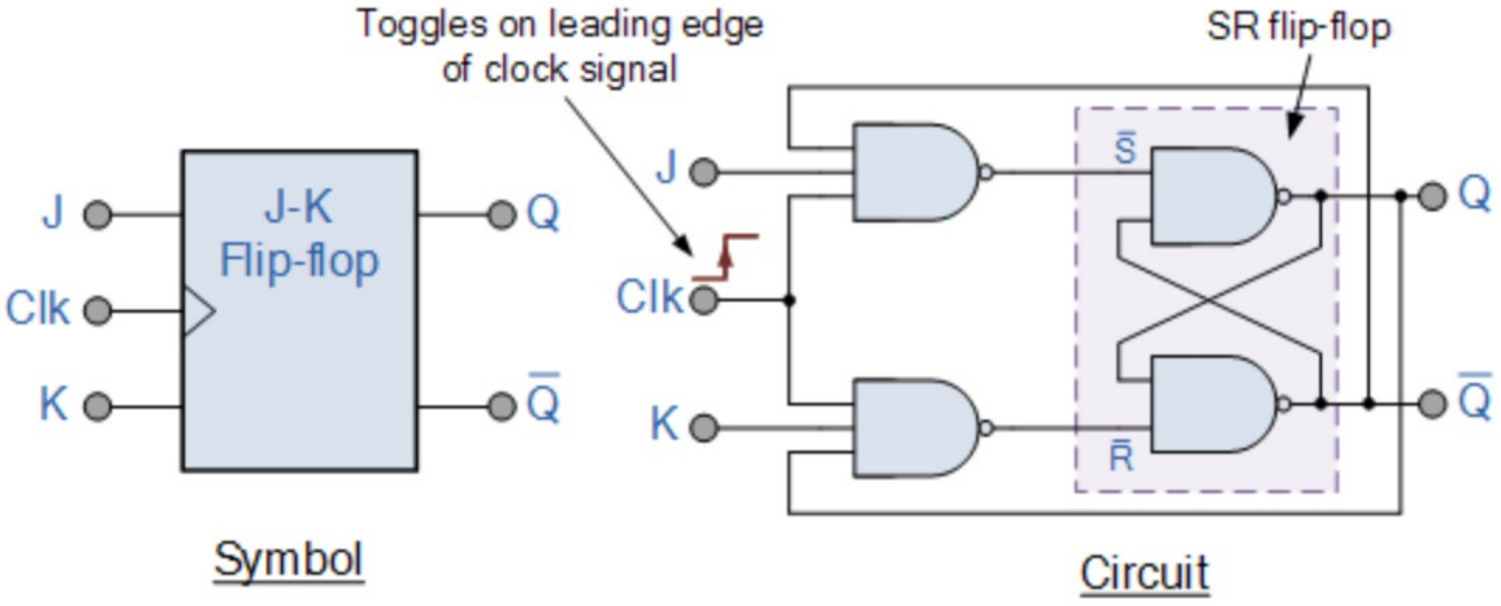


(a) Positive-edge

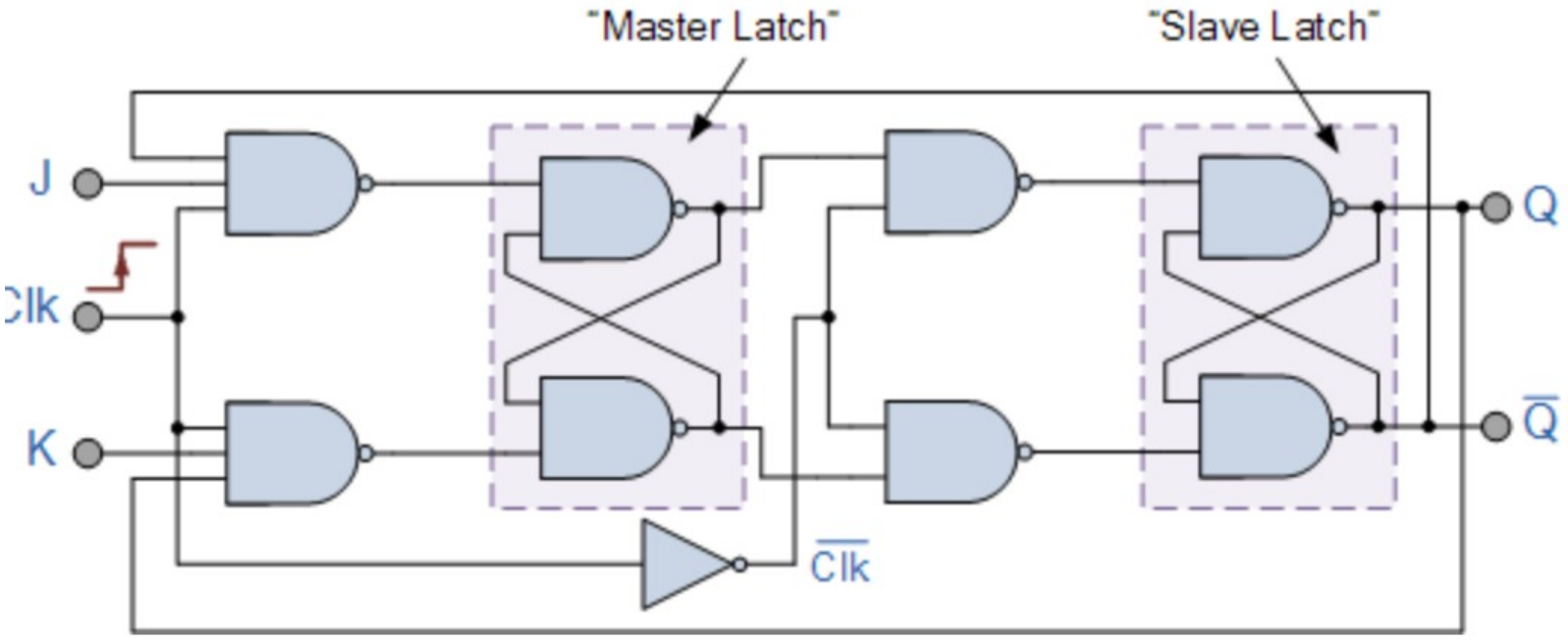


(a) Negative-edge

JK Flip-Flop –
implementation using NAND gates

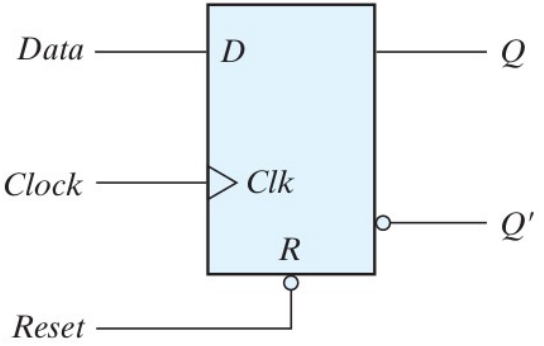


Master Slave JK Flip-Flop



Direct Inputs

- Some flip-flops have asynchronous inputs that are used to force the flip-flop to a particular state independently of the clock.
- The input that sets the flip-flop to 1 is called **preset or direct set** .
- The input that clears the flip-flop to 0 is called **clear or direct reset**.
- When power is turned on in a digital system, the state of the flip-flops is unknown. The direct inputs are useful for bringing all flip-flops in the system to a known starting state prior to the clocked operation.



(b) Graphic symbol

R	*Clk*	*D*	*Q*	*Q′*
0	X	X	0	1
0	↑	0	0	1
0	↑	1	1	0

(b) Function table

Flip-Flop Characteristic Tables

JK Flip-Flop

J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

D Flip-Flop

D	Q(t + 1)	
0	0	Reset
1	1	Set

T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

Flip-Flop Characteristic Equations

- The logical properties of a flip-flop, as described in the characteristic table, can be expressed algebraically with a characteristic equation.
- For the **D flip-flop,** we have the characteristic equation: **Q(t + 1) = D,** which states that the next state of the output will be equal to the value of input D in the present state.
- The characteristic equation for the **JK flip-flop: Q(t + 1) = JQ' + K'Q,** where Q is the value of the flip-flop output prior to the application of a clock edge, i.e. **Q = Q(t).**
- The characteristic equation for the T flip-flop: **Q(t + 1) = TQ' + T'Q = T**

Derive the characteristic equations from the respectivecharacterictic tables ??

Flip-Flop Excitation Tables

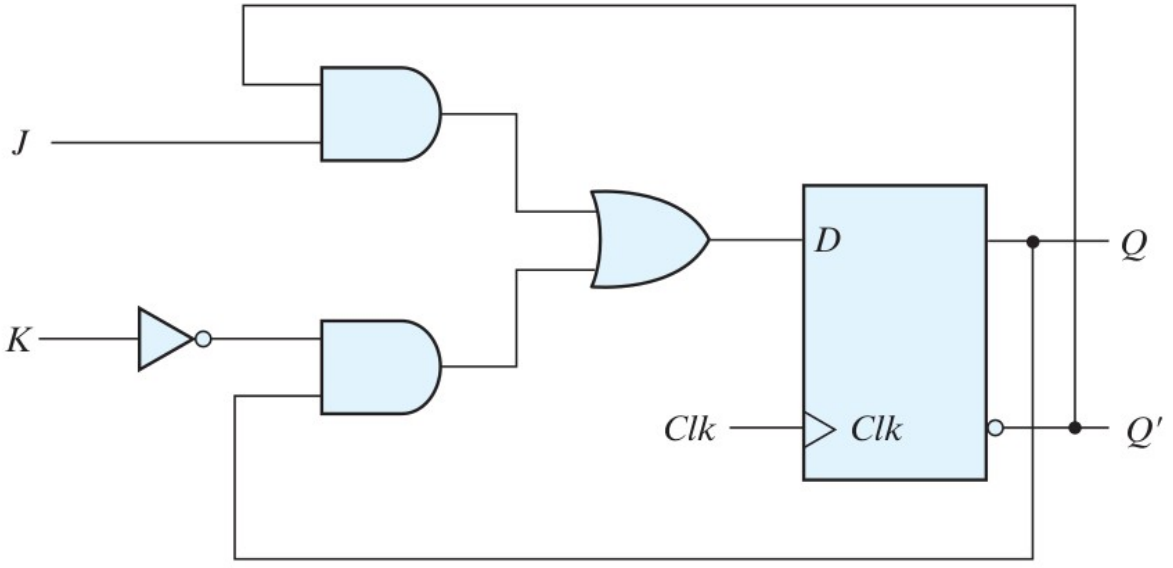
$Q(t)$	$Q(t+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(a) *JK* Flip-Flop

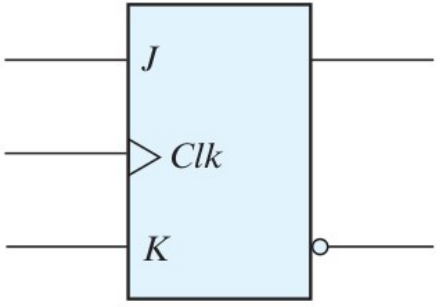
$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

(b) *T* Flip-Flop

JK Flip-Flop –
implementation using D Flip-Flop



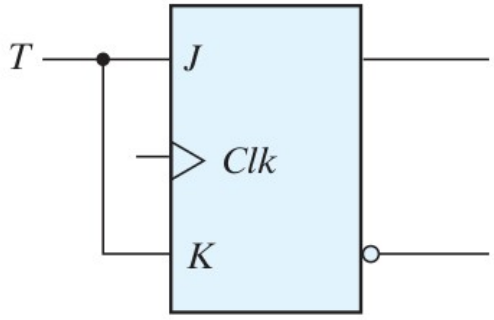
(a) Circuit diagram



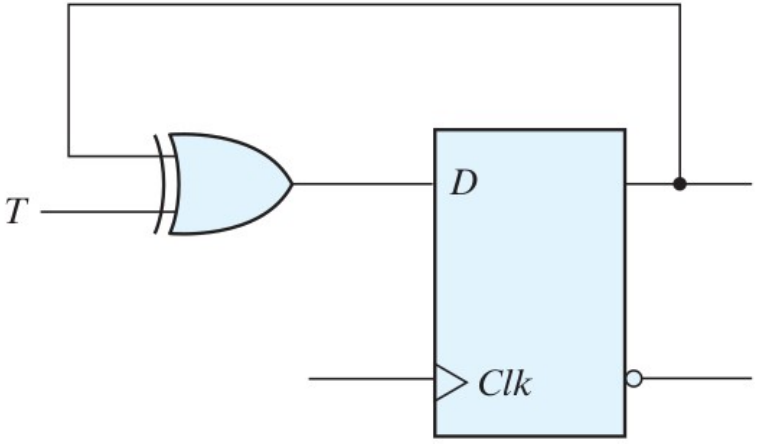
(b) Graphic symbol

T Flip-Flop

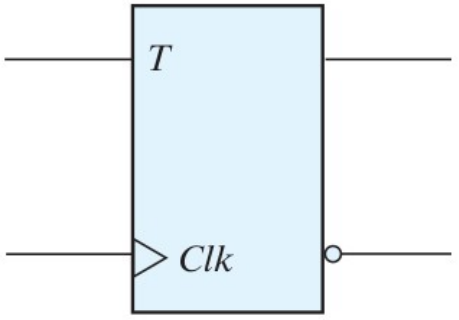
- implementation using D Flip-Flop



(a) From *JK* flip-flop



(b) From *D* flip-flop



(c) Graphic symbol