

Counters University Questions

- ① How does ripple counter differ from synchronous counter? (3)
- ② Design a synchronous counter with the following repeated binary sequence 000, 100, 111, 010, 011 using T flip flops (7)
- ③ Draw the block diagram of a 4-bit ripple counter. Sketch the waveforms at the output of each flip flop. Explain how this waveform is obtained. By what number N does this system divide? (10)
- ④ Design and implement a 4 bit binary synchronous up counter. (10)
- ⑤ Design a Johnson counter and explain its working. (10)
- ⑥ Draw and explain 4 bit Johnson counter. Also draw its timing sequence. (10)

- (7) Design a synchronous counter using JK flip-flop which counts through the states 0, 1, 3, 4, 5, 6, 0 Is the counter self starting? (10)
 - (8) Design a BCD ripple counter. Also verify its operation by means of a timing diagram (10)
 - (9) Design a counter that has a repeated sequence of the following six states: 000, 001, 010, 100, 101, 110. (6)
 - (10) Compare Ring & Johnson counter. (2)
 - (11) Design a synchronous counter using JK flip flops to count the sequence 0, 5, 6, 7, 3, 2 and then repeats. (10)
 - (12) Design a synchronous counter, using edge triggered JK flip flops, that generates the binary sequence: 001, 011, 010, 110, 111, 101, 001, 000, 001, (10)
 - (13) Draw a mod-16 ripple up counter using JK flip flops Show how this counter can be converted to a mod-12 ripple counter. (10)
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Module - 6

① Compare RAM & ROM

② Implement the following Boolean functions using a $3 \times 4 \times 2$ PLA

$$F_1 = \Sigma(0, 1, 3, 4)$$

$$F_2 = \Sigma(1, 2, 3, 4, 5)$$

③ Draw the block diagrams of a 4-bit ripple counter. Sketch the waveforms at the o/p of each flip-flop. Explain how this waveform is obtained. By what no. N does this s/m divider.

④ Write an HDL code for a full adder in all three modelling styles. (10 marks)

⑤ Explain the algorithms for floating point subtraction and addition (10marks)

⑥ Write notes on ROM (5)

⑦ Write notes on RAM (5)

⑧ Draw and explain the flow chart for addition and subtraction of 2 binary numbers in sign magnitude form (10)

- ⑨ Describe the working of Programmable logic array (PLA) with a block diagram and a simple example. (10)
- ⑩ a) Write short note on PLA (2)
 b) Give any 2 applications of ROM (3)
 c) Compare static RAM and dynamic RAM. (4)
- ⑪ Find the minimum size of PLA required to implement the following functions?
 Hence implement the following function using PLA.
 $F_1(A, B, C) = \sum m(0, 2, 4, 7)$
 $F_2(A, B, C) = \sum m(3, 5, 6, 7)$ 10 marks
- ⑫ Explain the construction of a 32×4 ROM with a logic diagram (5)
- ⑬ Explain the various types of ROMs (4)

- (14) Compare static & dynamic.
- (15) A combinational circuit is defined by the functions:

$$F_1(A, B, C) = \Sigma(3, 5, 6, 7)$$

$$F_2(A, B, C) = \Sigma(0, 2, 4, 7)$$

Implement the circuit with a PLA having 8 inputs, 4 product terms and 2 outputs.

Module - 5

- ① What is a Universal shift Register? (2)
- ② Explain how a shift register is used as a converter from (i) serial to parallel data and (ii) parallel to serial data (2)
- ③ Explain how shift registers can be used for serial transfer (5)
- ④ Draw and explain the different types of shift registers. (8)
- ⑤ List down the applications of shift registers. CO₃, L₂ (2)

~~Briefly explain any three~~
- ⑥ Implement a 4-bit bidirectional shift register with parallel load. (6)
- ⑦ Design a serial adder using a full adder and shift registers (5).
- ⑧ Give the logical configuration of shift registers. With a block diagram, explain the use of shift registers for serial transfer of data. (5)

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Lecture Note

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5.
- ⑨ Explain the working of 3-bit Universal shift Register. (8) 9
CO₂, L₂
- ⑩ Give 2 applications of shift registers. (2)