



KTU NOTES APP



www.ktunotes.in

Introduction to Transistor BiasingR_b1) ~~transistor biasing & selection of a point~~2) ~~stability need for B.S.~~3) ~~means of achieving stability & stability factors~~

4)

5) ~~biasing with PNP transistor~~6) ~~Op. point~~7) ~~Min. collector current~~8) ~~Max. collector current~~9) ~~Min. collector voltage~~10) ~~Max. collector voltage~~

The basic function of a transistor is amplification.
 The process of raising the strength of a weak signal without any change in its general shape is referred to as faithful amplification.

For faithful amplification it is essential that

(1) emitter-base junction is foward biased (F.B.)

(2) C-B junction is reverse biased (R.B.)

(3) Proper zero signal collector current

For achieving faithful amplification some basic ^{proper zero signal collector I}
conditions are essential. ^{proper B-E voltage @ an insta}

(1) Proper zero signal collector current: Zero signal collector current should be at least equal to the maximum collector current due to signal alone.

(2) Minimum proper Base-Emitter voltage at any instant:

The base emitter voltage V_{BE} should not fall below

0.2V for germanium & 0.7V for Si for any instant.

If the base emitter voltage V_{BE} falls below these values, during any part of the signal, that part will be amplified to smaller extent due to small collector current and therefore faithful amplification will not be available.

(15) Minimum proper C-E voltage at any instant :
The collector-emitter (C-E) voltage V_{CE} should not fall below knee voltage. With V_{CE} less than knee voltage, the e-B junction is not properly reverse biased and therefore the collector cannot attract the charge carriers emitted by the emitter and hence a large portion of them goes to the base. Consequently collector current decreases and the base current increases. Thus (when V_{CE} falls below knee voltage during any part of the signal, that part will be amplified to lesser extent due to reduced value of β and result in unfaithful amplification.)

$$I_C = \beta \cdot I_B$$

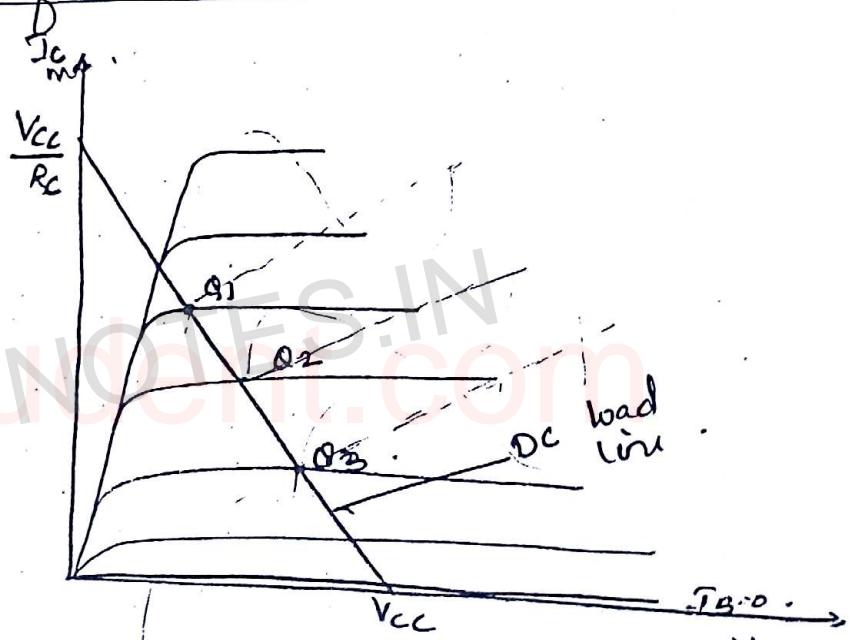
~~x~~ ~~x~~ ~~Transistor Biasing~~ The proper flow of zero signal collector current and maintenance of proper collector-emitter voltage during the passage of signal is called transistor biasing.

If the transistor is not properly biased, it would work inefficiently and produce distortion in the output signal. A transistor is biased either with the help of battery or associating a circuit with a.

transistor. The latter method is more efficient and is frequently used. The circuit used for transistor biasing is called biasing circuit.

* Selection of Operating Point

To study the effect of biasing conditions on the performance of a transistor, it is necessary to draw a dc load line on the output characteristics of the transistor.



In designing the circuit a point on the load line is selected as the dc bias point or quiescent point. This bias pt specifies the collector I_c and collector-emitter voltage V_{CE} .

The output characteristics are as shown in the figure when no signal is applied. When an input signal is applied,

(the base current value according to the
amplitude of the input signal and causes
collector current to vary, consequently producing
an output voltage variation.) (For faithful
amplification of the input signal a judicious
selection of the operating or quiescent point is
of utmost importance.) (In the active region,
the transistor operates linearly. Once an operating
point Q is established, tone varying excursion
of the input signal should cause an output
signal of the same wave form.)

(The figure given shows the output characteristic
with three operating points Q_1 , Q_2 & Q_3 .
The biasing circuit may be designed to set
the device to operate at any of these points
or others within the operating region. The
operating region is the area of the current &
voltage within the max. limits for the
particular device i.e. their $I_{C\max}$, $V_{C\max}$, V_{BE}
& $P_{C\max}$.)

It is necessary to bias the device so
that it can respond & cause change in
current or voltage for the entire range of
an input signal.

Bias Stabilization

Only the fixing of a suitable operating point (I_C and V_B) is not sufficient but it is also to be ensured that the operating point remains stable. (i.e. it does not shift due to change in temperature or due to variations in transistor parameters.)

(The maintenance of the operating point stable is known as stabilization.)

Need for Bias Stabilization

Stabilization of operating point is essential

because of

- ① Temperature dependence of collector current I_C .
- ② Individual variations.
- ③ Thermal runaway.

Temperature dependence of collector current:

$$I_C = \beta I_B + (\beta + 1) I_{C0}$$

$\beta \rightarrow$ Transistor I^{\prime} gain

$I_{C0} \rightarrow$ Reverse sat: I (leakage I')

The variation in temp. is caused by

three factors:

i) Reverse saturation current (leakage current),

I_{C0} , which doubles for every 10°C rise in temperature.

ii) Transistor current gain β , which increases with the increase in temperature.

(iii) Base emitter voltage V_{BE} , which decrease by $2.5\text{mV per }^{\circ}\text{C}$.

(Any or all the above factors can cause the bias point to shift from the values originally fixed by the circuit because of a change in temperature.)

④ Individual Variations

The value of β and V_{BE} are not exactly the same for any two transistors even of same type.

The base width of the transistor ~~may~~.

It is difficult to control the base width of the transistor. So small variations can cause variations in β , V_{BE} etc.

Also when a transistor is replaced by another transistor, then the operating point shifts.

⑤ Thermal Runaway

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

As $I_C = \beta I_B$, so as Temperature T_{es} , $I_{CO} T_{es}$, so

$I_C T_{es}$. This increase in I_C leads to

power dissipation. Being a ~~cumulative~~ which

further T_{es} temp. and this continues. So being a cumulative process it can lead to thermal runaway resulting in burn-out

of the transistor. (The self destruction of an unstabilized transistor is called thermal runaway.)

However if by some modification, I_B is made to fall with increase in temperature α , then decrease in the term βI_B can be made to neutralize the increase in the term βI_B can be made to neutralize the increase in the term $(1+\beta) I_C$, thereby keeping I_C almost constant.)

Means of Achieving Stability For Operating Point

Operating point stability may be achieved by adopting either stabilization techniques or compensation techniques.

I) Stabilizing Technique: makes use of a resistive biasing circuit that permits such variation of base current I_B as to maintain collector current I_C almost constant inspite of variation in reverse saturation current I_{CO} , base emitter voltage V_{BE} and β .

II) Compensation technique: makes use of temp sensitive device such as diodes, transistors etc... Such devices produce compensation voltages, and currents so as to make operating point stable.

Stability factor:

(The degree of success achieved in stabilizing I_c in face of variation in T_{CO} is expressed in terms of stability factor S) and it is defined as the ratio of change of collector current w.r.t T_{CO} keeping V_{BE} & β constant.

$$S = \frac{\partial I_c}{\partial T_{CO}} \approx \frac{dI_c}{dT_{CO}}$$

Small the value of 'S' higher the stability.

The ideal value of 'S' is 1.1

Other stability factors are

(1) $S_V \rightarrow$ ratio of change of I_c w.r.t V_{BE} keeping β & I_{CO} constant.

$$S_V = \frac{dI_c}{dV_{BE}}$$

| β & I_{CO} constant .

(2) $S_\beta \rightarrow$ ratio of change of I_c w.r.t β keeping I_{CO} & V_{BE} const.

$$S_\beta = \frac{dI_c}{d\beta}$$

| I_{CO} & V_{BE} const. .

General Expression for stability Factor S

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

On Differentiating the above eqn w.r.t I_C
considering β to be constant:

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

$$= \beta \frac{dI_B}{dI_C} + \frac{(\beta + 1)}{S}$$

$$1 - \beta \frac{dI_B}{dI_C} = \frac{\beta + 1}{S}$$

$$S = \frac{\beta + 1}{1 - \beta dI_B/dI_C}$$

General Expression for stability factor S_B

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

$$1 = \beta \frac{dI_B}{dI_C} + I_B \cdot \frac{d\beta}{dI_C} + I_{CO} \frac{d\beta}{dI_C}$$

$I_{CO} \& V_{BE} \rightarrow \text{const}$

$$= \beta \frac{dI_B}{dI_C} + \frac{d\beta}{dI_C} (I_B + I_{CO})$$

\rightarrow derivat
regm

$$1 - \beta \frac{dI_B}{dI_C} = \frac{I_B + I_{CO}}{S_B}$$

$$S_B = \frac{I_B + I_{CO}}{1 - \beta dI_B/dI_C}$$

Transistor Biasing Circuit

(There is a large number of circuits for biasing of a transistor. These circuits differ so as to their ability to keep the quiescent point fixed ~~in spite~~ of variations in transistor characteristics.)

Requirement of biasing circuit

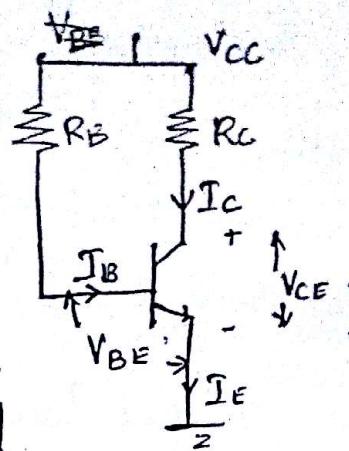
- ① Establish the operating point in the middle of the active region of the characteristics, so that on applying the c.c.p signal the instantaneous operating point does not move either to the cutoff region or to the saturation region.
- ② Stabilize the collector current I_C against temperature variation.
- ③ Making the operating pt. independent of transistor parameter so that replacement of transistor by another transistor of the same type in the ckt. does not shift the operating point.

Fixed Bias Circuit

The circuit diagram of fixed biasing for an npn transistor is shown. In this biasing a high valued resistance is connected between supply and base of the transistor.

between supply and base of the transistor.

The required zero signal base current I_B is provided by V_{CC} . The supply also keeps the base positive with respect to emitter and hence makes the base emitter junction forward biased.)



Analysis

To calculate the stability factor for the given circuit.

Apply KVL to the input section

$$V_{CC} - I_B R_B - V_{BE} = 0 \quad \text{--- (1)}$$

We know that

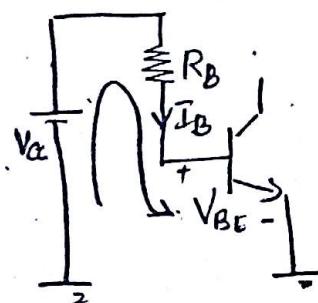
$$I_C = \beta I_B + (\beta + 1) I_{CO} \quad \text{--- (2)}$$

From eqn (1)

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Putting this value of I_B

$$I_C = \left(\frac{V_{CC} - V_{BE}}{R_B} \right) \beta + (\beta + 1) I_{CO}$$

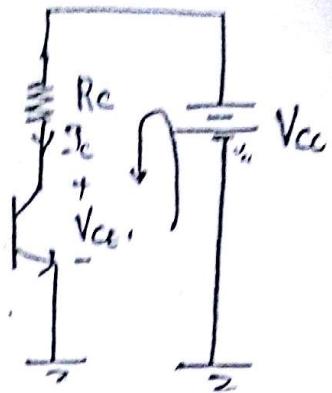


So the collector current is independent of base resistance in the collector circuit. So we can say that collector current is controlled by B-E junction.)

The output loop (collector-emitter loop) is considered.

$$V_{ce} = I_c R_c = V_{cc} \approx 0$$

$$V_{ce} = V_{cc} - I_c R_c$$



The quiescent pt is given by $\underline{I_{cq}, V_{ce}}$.

- Stability factor

$$s = \frac{dI_c}{dI_{co}}$$

$$I_c = \left(\frac{V_{cc} - V_{BE}}{R_B} \right) \beta + (\beta + 1) I_{co} \Rightarrow \text{saturation is required.}$$

$$\frac{dI_c}{dI_{co}} = s = \beta + 1$$

So the value of stability factor is very high.
So its stability factor is very poor.)

Advantages

1. Calculations are simple.
2. Simple in construction as only one resistor R_B is required to set the conditions
3. There is no loading at the source as no resistor is employed at the base-emitter junction.

Disadvantages

1. It provided high stability factor as in other we lose poor thermal stability and therefore chance of thermal runaway.
2. This method provides poor stability against inherent variations of transistor parameters.

Due to these disadvantages, this method is rarely employed in circuits.

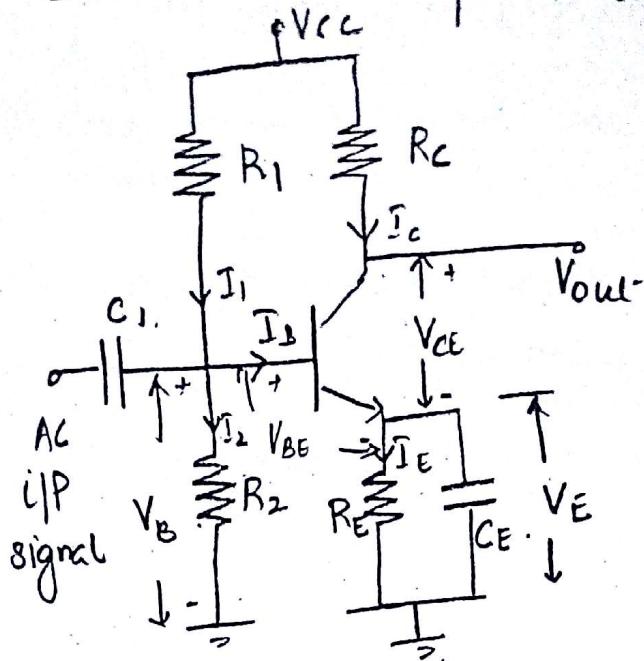
II Self Bias or Potential Divider Bias Circuit

This is the most commonly used arrangement.

This biasing circuit consists of two resistors R_1 and R_2 connected across the supply voltage V_{CC} and provide the necessary biasing. (The emitter resistor R_E provides stabilization (thermal stability)) The emitter resistor R_E causes a voltage drop in a direction so as to reverse bias the emitter junction. Since the E-B junction is to be forward biased, the base voltage is obtained from supply V_{CC} through R_1 - R_2 now. For forward biasing the emitter base for R_1 and R_2 are adjusted that the base terminal becomes more positive than emitter. The net forward bias across the E-B junction ($V_{BE} = V_B - V_E$)

$$V_{BE} = V_B - V_E$$

The dc bias circuit is independent of transistor B.



Circuit Analysis

Assume that current flowing through R_1 is I_1 .

As the base current I_B is very small, the total current flowing through R_2 can be assumed to be almost equal to I_1 .

$$\therefore I_1 \approx \frac{V_{cc}}{R_1 + R_2} \cdot R_2$$

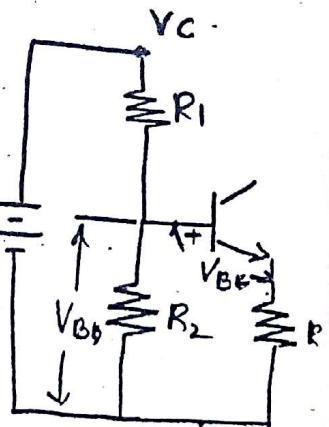
$$\therefore \text{Voltage across } R_2, V_B = \frac{V_{cc}}{R_1 + R_2} \cdot R_2$$

The voltage across the emitter resistor R_E is

$$V_E = V_B - V_{BE} \quad \therefore (V_{BE} = V_B - V_E)$$

$$\therefore \text{Emitter current } I_E = \frac{V_E}{R_E}$$

$$I_E = \frac{V_B - V_{BE}}{R_E}$$

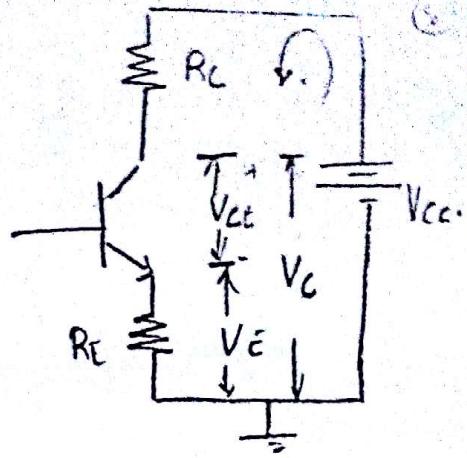


$$I_C \approx I_E = \frac{V_{CC} - V_{BE}}{R_E}$$

The voltage at the collector will be.

$$V_{CC} - I_C R_C - V_C = 0$$

$$V_C = V_{CC} - I_C R_C$$



The collector emitter voltage.

$$V_{CE} = V_C - V_E$$

$$\therefore V_{CE} = V_{CC} - I_C R_C - V_B$$

$$= V_{CC} - I_C R_C - I_E R_E$$

$$I_C = I_E$$

$$\therefore \boxed{\underline{\underline{V_{CE} = V_{CC} - I_C (R_C + R_E)}}}$$

So here it is clear that no expression of B appears. Hence operating point is independent of B . Due to this reason this voltage divider bias circuit is most widely used).

Stabilization of R_E .

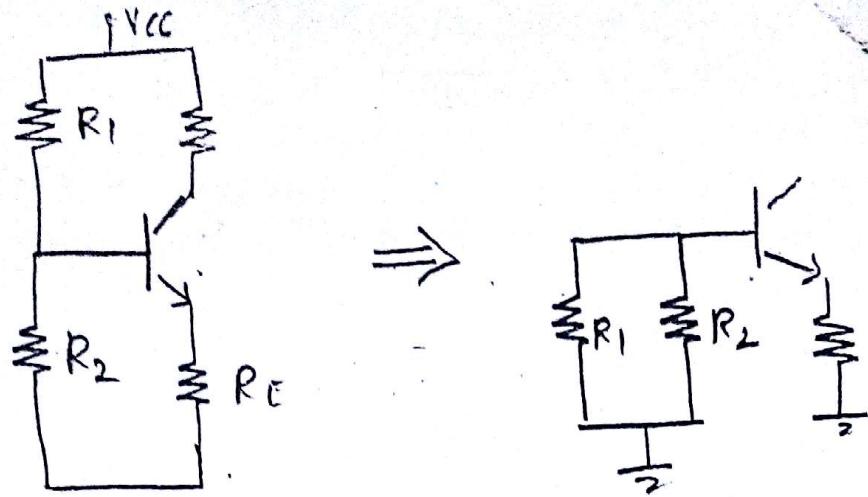
$$V_B = V_{BE} + V_E$$

$$= V_{BE} + I_E R_E$$

$$\underline{\underline{V_B = V_{BE} + I_C R_E}}$$

Circuit Analysis of stability Factor:

Let us consider the base emitter loop of the voltage divider bias circuit. We first apply Thevenin's voltage equivalent model.

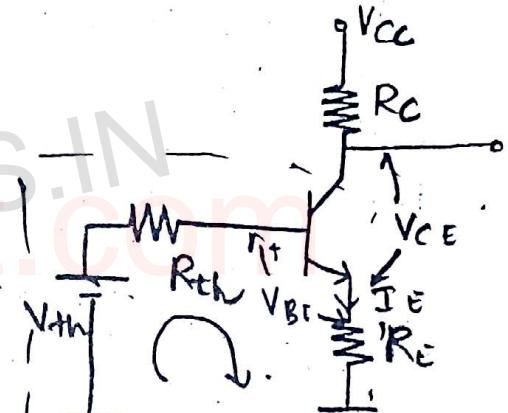


To calculate R_{th}

In Thévenin's equivalent model
we need to calculate R_{th} and V_{th} .

$$R_{th} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

Thevenin's equivalent model..



Now apply KVL to the
circuit section

$$V_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$$

$I_E = ?$

$$I_C = \beta I_E$$

$$V_{th} - V_{BE} - I_B R_{th} - I_E R_E = 0 \quad I_E = I_B + I_C$$

$$V_{th} - V_{BE} - I_B R_{th} - (I_B + I_C) R_E = 0$$

$$V_{th} - V_{BE} = I_B (R_{th} + R_E) + I_C R_E$$

$$I_B = \frac{V_{th} - V_{BE} - I_C R_E}{R_{th} + R_E}$$

$$I_C = \beta I_{B0} + (\beta + 1) I_{CBO}$$

$$I_{CO} = -I_{CBO}$$

6

$$I_C = \beta \left(\frac{V_{th} - V_{BE} - I_C R_E}{R_{th} + R_E} \right) + (\beta + 1) I_{CBO}$$

$S = \frac{dI_C}{dI_{CO}}$ Differentiating the above eqn by w.r.t I_C , we get -

$$1 = \frac{d}{dI_C} \left(\beta \left(\frac{V_{th} - V_{BE} - I_C R_E}{R_{th} + R_E} \right) + (\beta + 1) I_{CBO} \right)$$

$$1 = -\frac{R_E \beta}{R_E + R_{th}} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

$$1 + \frac{\beta R_E}{R_E + R_{th}} = (\beta + 1) \frac{dI_{CO}}{dI_C}$$

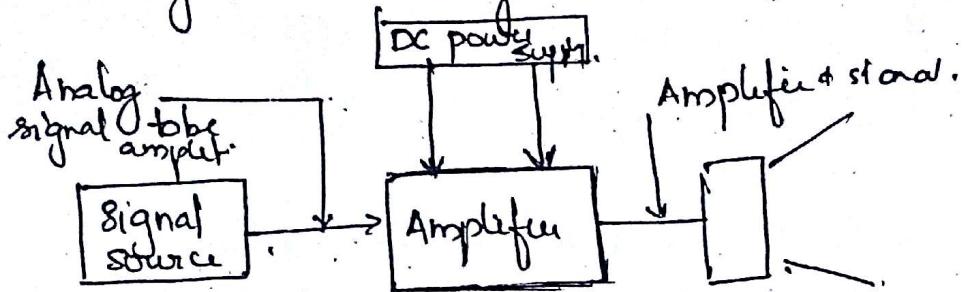
$$\frac{dI_C}{dI_{CO}} = \frac{(\beta + 1)}{1 + \beta R_E / R_E + R_{th}} = S$$

$$S = (1 + \beta) \left(\frac{R_E + R_{th}}{R_E(1 + \beta) + R_{th}} \right)$$

X X

Amplifiers

Next we will discuss about linear amplifiers. (The linear amplifiers are meant to amplify the analog signals.) The magnitude of the analog signal can take any value and the signal can vary continuously with time.



A linear amplifier is supposed to multiply the input signal by a constant to produce the output signal. This multiplying factor is greater than 1 and is known as gain of an amplifier.

Analysis of amplifier can be done of two types.

- (1) DC analysis
- (2) AC analysis

Amplifier characteristics

For comparing the amplifier performance, we have to define certain important characteristics

- (1) Voltage gain A_V
- (2) Current gain A_i
- (3) Input resistance R_i

2. Output resistance (R_o)
 It is the resistance seen looking into the output terminals of an amplifier, when the input signal source is short circuited ($V_i = 0$) and output terminals are open circuited. Thus, current gain, voltage gain, input resistance and output resistance are the four vital parameters of an amplifier.

8.2. TYPES OF BJT AMPLIFIERS

Fig. 8.3. Block diagram of an amplifier is as shown in figure.

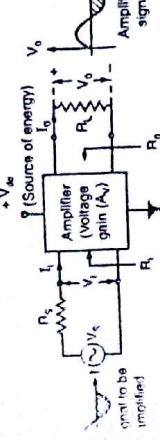


Fig. 8.3. Block diagram of an amplifier showing important parameters

In order to magnify the input signal V_i , all the amplifiers need a source of energy. This may be provided by a battery or dc power supply. The dc power supply is essential for biasing the BJT used in the amplifier. The amplifier should contain at least one active device such as a transistor or field effect transistor (FET). In regenerative amplifier (op-amp) [if a transistor is used, it should be housed in the active region]. In figure, the source V_b represents the ac input signal to be amplified. The amplified signal is applied to the load resistance R_o .

5. Amplifier Characteristics

For comparing the amplifier performance, we have to know certain important characteristics.
 Some of them are:

- (i) The voltage gain A_v
- (ii) The current gain A_I
- (iii) Input resistance R_i
- (iv) Output resistance R_o
- (v) Power gain A_p

Therefore, current gain, $A_I = \frac{I_o}{I_b}$... (8.1)
 The gain of an amplifier is defined as the ratio of output quantity to the input quantity. So, the ratio of output voltage to input voltage will be called as voltage gain A_v . Similarly, the ratio of output current to input current is called as current gain A_I of amplifier.

Also, voltage gain, $A_v = \frac{V_o}{V_i}$... (8.2)
 The voltage and current gain of an amplifier should be as possible.

Now the resistance seen looking into the input terminals of an amplifier. More generally, an input resistance Z_i is defined, however, Z_i is resistive for the amplifiers, hence, it is replaced by R_i .

3. Output resistance (R_o)
 It is the resistance seen looking into the output terminals of an amplifier, when the input signal source is short circuited ($V_i = 0$) and output terminals are open circuited. Thus, current gain, voltage gain, input resistance and output resistance are the four vital parameters of an amplifier.

4. Block Diagram of an Amplifier
 Fig. 8.3. Block diagram of an amplifier is as shown in figure.

The transistor amplifiers are classified into following three categories.

- (i) Common Emitter (CE) amplifier.
- (ii) Common Base (CB) amplifier.
- (iii) Common Collector (CC) amplifier.

Let us discuss them one by one in detail.

8.3. Common Emitter (CE) Amplifier / RC - coupled amp.

Let us consider a practical transistor amplifier circuit, discuss its operation and then analyze the behaviour of this circuit using the dc load line. A single stage RC coupled amplifier using transistor as an active device has been shown in figure 8.4.

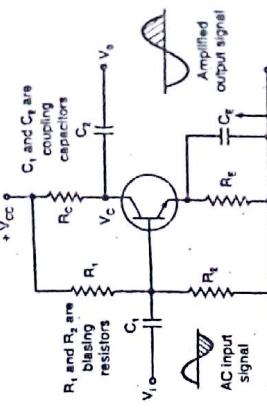


Fig. 8.4. Single stage RC coupled CE amplifier

Description

The capacitors C_1 and C_3 are called as the coupling capacitors. As the load resistor R_o is coupled to the amplifier through the coupling capacitor, this amplifier is called as RC coupled amplifier. The transistor is connected in the common Emitter (CE) configuration. Therefore, this amplifier is called CE amplifier.

Circuit components and their functions

Let us now know about the function of each component in the RC coupled amplifier. Resistors R_1 , R_2 and R_o are used for biasing the transistor in the active region, because for operating the transistor as an amplifier, it is necessary to bias it in the active region. The type of biasing circuit used here is voltage divider bias or self bias. R_c is the collector resistor used for controlling the collector current. Input coupling capacitor C_1 is used for coupling the ac input voltage V_i to the base of the transistor. As capacitors block dc, this capacitor helps to block any dc component present in V_i and couples only the ac component of the input signal. This capacitor also ensures that the dc

5. Biasing conditions of the transistor remain unchanged even after application of the input signal.

Bypass capacitor C_E

The capacitor connected in parallel with the emitter resistor R_e is called as the emitter bypass capacitor. This resistor R_e is a low resistance to the amplified ac signal. Therefore, the emitter resistor R_e gets bypassed. Therefore, C_E for only the ac signal. This will increase the voltage drop $I_c R_E$ across it. This will increase the voltage drop $I_c R_E$ to produce a varying voltage drop $I_c R_E$ across it. This voltage drop $I_c R_E$ is in phase with the collector-emitter current as shown in figure 8.5. The collector voltage is given by,

$$V_C = V_{CC} - I_c R_E$$

Therefore, with changes in the voltage drop $I_c R_E$, the collector voltage also will vary as shown in figure 8.5. The capacitor C_E will vary in exactly opposite manner with respect to each other, because as I_c increases, V_C has to decrease according to equation (8.3).

This collector voltage is then coupled to the load through the coupling capacitor C_2 . It will block the dc part of the amplified signal obtained after C_1 . Thus the ac signal amplitude is much higher than the output voltage. Its magnitude is strictly proportional to that of the input signal and its shape is exactly same as that of the output signal. Thus, the input ac signal has been successfully amplified.

Base relationship between Input and output

As seen from figure 8.5, there is 180° phase shift between the output and input or the output is said to be an inverted version of input. Thus for a CE amplifier there is a phase shift of 180° between V_i and V_o .

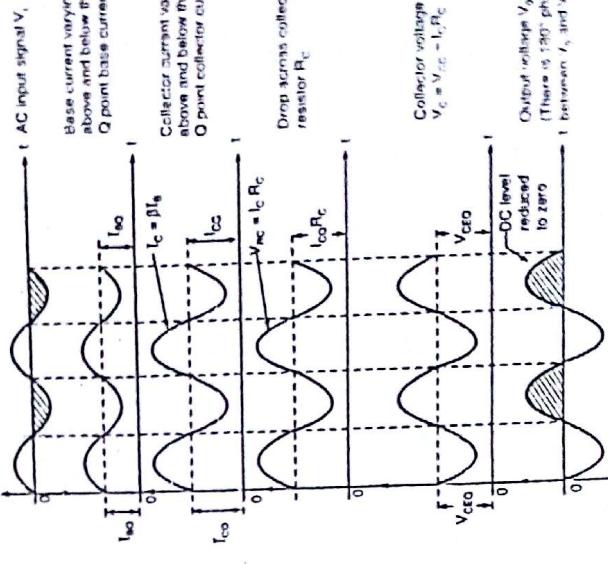


Fig. 8.5. Waveforms showing the process of amplification

Role of coupling capacitor C_2

The coupling capacitor C_2 couples on the ac part of the signal to the output and blocks the dc part as shown in figure 8.5. Therefore, the signal obtained after the coupling capacitor C_2 has a zero DC value.

Does the frequency change in the amplification process?

Comparing the waveforms of V_i and V_o , we conclude that the frequency of the amplified output signal V_o is same as that of the input voltage. Thus, in the amplification process, the frequency of the signal remains unchanged.

Summary of operation of RC coupled CE amplifier

- In the absence of ac input signal, $I_b = I_{BQ}$, $I_c = I_{CQ}$ and $V_{CE} = V_{CQ}$. The Q point is selected to be in the active region of transistor.
- As V_i is applied, the base current varies above and below I_{BQ} .
- Hence, $I_c = \beta I_b$ varies above and below I_{CQ} .
- Therefore, voltage across R_C varies because $V_{RC} = I_c \times R_C$.
- Hence, collector voltage V_C varies above and below V_{CQ} as $V_C = V_{CC} - I_c R_C$.
- Through C_2 only, the ac part of V_C is coupled to the load. V_o is of same shape as V_i but of larger size. Thus, amplification has taken place.

8.2.2 Working of the Amplifier with the help of DC Load Line

The amplifier operation discussed earlier can also be explained with the help of DC load line. Let us consider figure 8.6, which illustrates the amplification process graphically.

Selection of Q-point

The criteria for selecting quiescent point to operate the transistor as an amplifier is as follows:

- The Q point should not be too close to the cut off region.

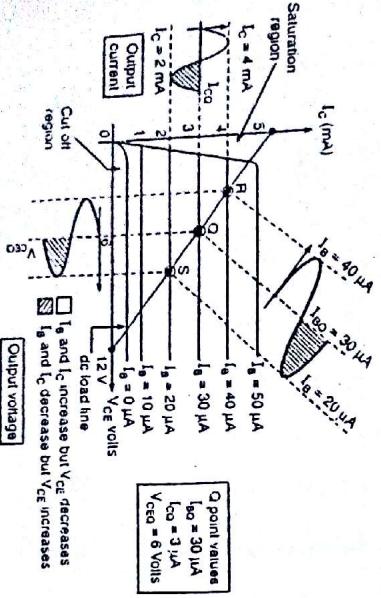


Fig. 8.3. Graphical representation of amplification process

- The Q point should not be too close to the saturation region.
- The conditions (i) and (ii) should be satisfied in order to avoid any waveform distortion in the amplified output signal.

(ii) The Q point should not be too close to the dc load line so that the variation in the amplified voltage is equal corresponding to the positive and negative half cycles of the input signal. This will ensure that the amplified signal will be an exact replica of the input signal. In figure 8.6, the component values are so adjusted that the Q point is situated exactly at the center of the dc load line. The co-ordinates of the Q point are:

$$\text{Q point} = (V_{CQ}, I_{CQ}) = (6V, 3 mA)$$

Amplification Process

As shown in figure 8.6, due to application of the input signal, the base current varies sinusoidally above and below I_{BQ} . The change in base current i.e.,

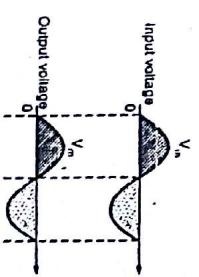
$$\Delta I_B = I_{Bmax} - I_{Bmin}$$

$$= 40 \mu A - 20 \mu A$$

The operating point will move along the load line from Q to R and then from R to S corresponding to change in I_B . Due to this, the collector current I_c will change above and below I_{CQ} as shown in figure 8.6. Here, it may be noted that $\Delta I_c = \beta \Delta I_B = 2 \text{ mA}$ and I_c and I_B are in phase. The collector to emitter voltage V_{CE} (which is same as V_o) will vary above and below its Q point value V_{CQ} . This is the amplified output voltage. Note that V_{CE} is 180° out of phase with I_c and I_B .

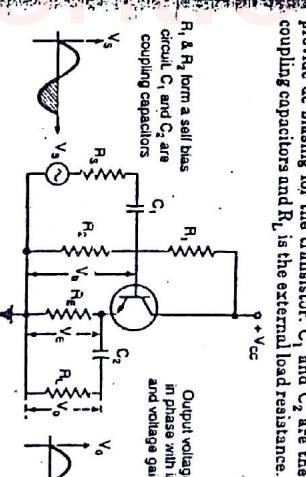
Waveforms

The input voltage is applied at the base with respect to ground and the output of amplifier is taken from the emitter with respect to ground. As the emitter voltage follows the base voltage, the gain of this amplifier is approximately equal to 1. As shown in figure 8.8, the input and output voltage waveforms are in phase with each other. Also observe that the output voltage is exactly equal to the input voltage.



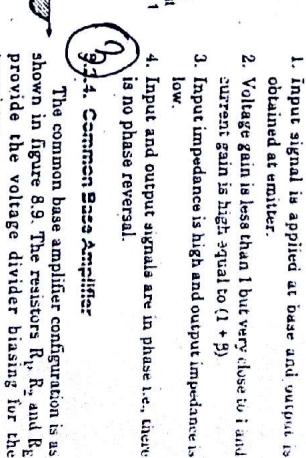
8.2.3 Common Collector or Emitter Follower Amplifier Circuit

The common collector or emitter follower configuration is as shown in figure 8.7. The resistors R_1 , R_2 and R_E provide ac biasing for the transistor. C_1 and C_2 are the coupling capacitors and R_L is the external load resistance.



8.2.4 Common Base Amplifier

The common base amplifier configuration is as shown in figure 8.9. The resistors R_1 , R_2 and R_E provide the voltage divider biasing for the transistor.



Working Operation

The input is applied to the emitter while output is taken from the collector. The base is connected to ground (for ac signals only) via a large capacitor C_1 which acts as a short circuit for ac signals. In the positive half cycle of input signal, the emitter voltage varies sinusoidally above its Q-point value. Hence, V_{be} reduces, hence I_b and I_c will reduce. So the voltage drop across R_C will reduce. Hence the collector voltage will increase above its Q-point value. Thus, we get a positive half cycle at the output corresponding to the positive half cycle of the input as shown in figure 8.10. Similarly, we get a negative half cycle at the output corresponding to the negative half cycle

impedance is low. Input and output signals are in phase i.e., there is no phase reversal.

Applications

The important applications of the emitter follower are

- A buffer amplifier.

- For the impedance matching.

- At the output stage (Power amplifier).

(i) Input impedance is moderately high.

Output impedance is moderately high.

There is a phase shift of 180° between the input and output.

(ii) Voltage gain is high.

Current gain is high.

Output impedance is moderately high.

Output is obtained at the collector.

Amplification Process

Why is it called emitter follower?

As the output (emitter) voltage is equal to the input voltage and in phase with input voltage, it is said that emitter follows the base. Hence, the name emitter follower.

Features of CC amplifier

- Input signal is applied at base and output is obtained at emitter.
- Voltage gain is less than 1 but very close to 1 and current gain is high and output impedance is low.
- Input impedance is high and output impedance is obtained at emitter.
- Input and output signals are in phase i.e., there is no phase reversal.

8.2.5 Common Bass Amplifier

The important advantages of the emitter follower are

1. A buffer amplifier.

2. For the impedance matching.

3. At the output stage (Power amplifier).

Advantages:

Some of these advantages are very high input impedance, large bandwidth, low output resistance, low noise, low distortion. Input impedance is high and output

impedance is low. Input and output signals are in phase i.e., there is no phase reversal.

Due to the voltage series negative feedback present in the emitter follower circuit, it possesses all the advantages of the negative feedback.

Some of these advantages are very high input impedance, large bandwidth, low output resistance, low noise, low distortion. Input impedance is high and output

If the input V_{in} , there is no phase shift between the input and output.

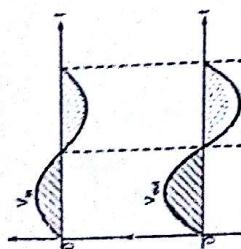


Fig. 8.10. Frequency response of common base amplifier

1. Input resistance of this configuration is very low, hence source loading can take place.
2. Output resistance is very large.
3. Current gain is approximately equal to 1, so there is no current amplification.

Applications

The common base amplifiers are used for the applications where impedance matching is to be achieved. They are also used as wideband amplifiers i.e., the amplifiers having a large bandwidth.

8.2.5. Small Signal Operation

If the amplitude of the input ac signal being applied to the amplifier is small (few mV), then the amplifier is called as a small signal amplifier, and the operation of the amplifier is called as small signal operation. As the input signal is small, the transistor will operate on the linear region of its transfer characteristic and produces a distortionless output as shown in figure 8.11. This is why the small signal amplifiers are also called as linear amplifiers. All the amplifiers (CE, CB and CC) discussed in this chapter are small signal amplifiers.

3.3. CONCEPT OF FREQUENCY RESPONSE

Frequency response of an amplifier is the graph of amplifier gain in decibels plotted against frequency. It shows the variation in amplifier gain with respect to frequency.

Significance of frequency response

An audio frequency amplifier used in a tape recorder is expected to amplify all the audio frequency signals in the range of 20 Hz to 20 kHz, equally i.e., with the same voltage gain. However, it does not happen so in practice. For a practical voltage amplifier, the gain is low at low frequencies as well as at high frequencies. This will affect the quality of music played back on the tape recorder. Hence, to choose an amplifier for such application, we must know its behaviour at different frequencies of the input signal. For this purpose, we need to know about the frequency response of an amplifier.

8.4. TYPICAL FREQUENCY RESPONSE

A typical frequency response of an audio amplifier is shown in figure 8.12. On the X-axis, we plot the frequency in Hz whereas the voltage gain A_v in decibels (dB) is plotted on the Y-axis. The frequency response is generally plotted on a semilog graph paper. Ideally, the frequency response should be flat over the entire frequency range as shown by the dotted line in figure 8.12.

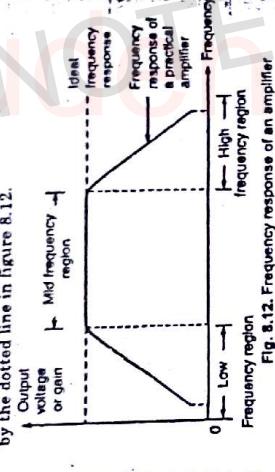


Fig. 8.12. Frequency response of an amplifier

8.4.1. Different Regions In Frequency Response

Practically, the frequency response of an amplifier is not flat over the entire operating frequency region. The practical frequency response can be divided into three regions as follows:

- (i) Low frequency region
- (ii) Mid frequency region
- (iii) High frequency region
- (iv) Various capacitors are responsible for reduction in gain in low and high frequency regions.

Low frequency region

The amplifier gain in the low frequency region decreases due to coupling and bypass capacitors in an amplifier.

Mid frequency region

In this region, gain and output voltage remain constant.

High frequency region

In this region, the output voltage and gain will

decrease due to the transistor internal capacitance, stray capacitance.

How to plot the frequency response?

The frequency response of figure 8.12 can be plotted by following the procedure given as follows:

- (i) First, we apply V_{in} to the amplifier.
- (ii) Then we adjust an ac input voltage so as to get the maximum undistorted output voltage in the mid frequency range (typically at 1 kHz).
- (iii) Next, we keep this input voltage constant throughout the experiment. Now change the frequency of the input or signal in suitable steps and every time note down the corresponding output voltage.
- (iv) Finally, we calculate the gain of the amplifier at each frequency and plot the frequency response.

8.4.2. Bandwidth of an Amplifier

The mid frequency region of the frequency response is useful for amplification as the amplifier gain is constant at a value called midband voltage gain $A_{v(mid)}$. However, as the amplifier gain reduces at low and high frequencies, we need to obtain a range of frequencies over which the voltage gain is close to or equal to $A_{v(mid)}$, because this range of frequencies will be of practical use. We can use the amplifier effectively over this frequency range. Looking at figure 8.12, we come to know that there is a band of frequencies in which the magnitude of output voltage or gain is either equal or relatively close to their mid frequency band value. To fix the frequency range in which the amplifier gain is relatively large, a cut-off level of 0.707 (A_v and 0.707 V_{out}) is chosen. The corresponding frequencies f_L and f_H (see figure 8.13) are known as the half power frequencies. They are known as half power frequencies because the output power at these frequencies becomes 50% of the output power in the mid frequency band. The frequencies f_L and f_H are also known as corner, cut-off, band, break or 3 dB frequencies. These are known as 3 dB frequencies because 50% reduction in output power corresponds to 3 dB reduction on the dB scale. The bandwidth of the amplifier is defined as the difference between the half power frequencies.

$$BW = (f_H - f_L) \text{ Hz} \quad \dots(8.4)$$

The mathematical expression for voltage gain for the low frequency region is given by,

$$A_{v(low)} = \frac{A_{v(mid)}}{\sqrt{1 + [f_L/f_0]^2}} \quad \dots(8.5)$$

Where, f_0 = Upper half power frequency
As the frequency "f" is reduced, the ratio $(f/f_0)^2$ will increase. This will increase the value of denominator of equation (8.5) and the gain $A_{v(low)}$ will reduce below the $A_{v(mid)}$. At $f = f_0$ i.e., the lower half power frequency the equation (8.5) gets modified to,

$$A_{v(low)} = \frac{A_{v(mid)}}{\sqrt{1 + [f_L/f_0]^2}}$$

Where, f_0 = Upper half power frequency
As we increase the frequency "f", the ratio $(f/f_0)^2$ will increase. This will increase the value of denominator of equation (8.5) and the gain $A_{v(low)}$ will reduce below the $A_{v(mid)}$. At $f = f_0$ i.e., the lower half power frequency the equation (8.5) gets modified to,

Fig. 8.13. Frequency response, half power frequencies and bandwidth of an RC coupled amplifier

8.4.3. Definitions of Upper and Lower Cutoff Frequencies

Lower cut off frequency (f_L) or (f_U)

It is the frequency of the input signal at which the amplifier gain or output voltage reduces to 70.7% of their mid frequency range value. Here, f_L is always less than f_0 .

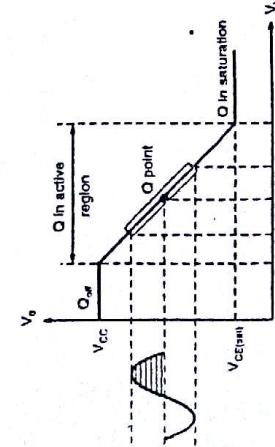


Fig. 8.11. Transfer characteristics

Similarly, at $f = f_{\text{H}}$, i.e., the upper half power frequency, the equation (8.6) gets modified to,

$$A_{V1} = \frac{A_{V(\text{mid})}}{\sqrt{1+(1/\beta)^2}} = 0.707 A_{V(\text{mid})}$$

Hence, $A_{V1} = A_{V2} = 0.707 A_V (\text{mid})$

8.4.6. Factors Affecting the Bandwidth of the RC Coupled Amplifier

The factors affecting the bandwidth of an RC coupled amplifier are as under:

- Coupling capacitors C_1 and C_2
- Bypass capacitor C_E
- Internal capacitances of the BJT.

8.4.7. Effect of Coupling Capacitors

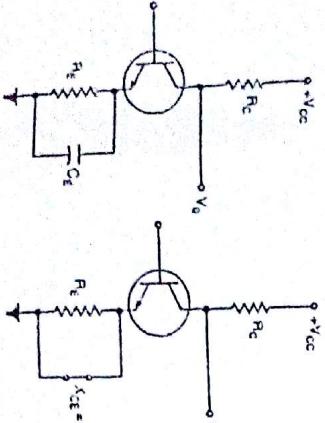
The capacitors C_1 and C_2 are coupling capacitors used for blocking the dc part and allowing only the ac part of the signal to pass through. Reactance of a capacitor is given by,

$$\frac{1}{X_C} = \frac{1}{2\pi f C}$$

Thus, the capacitive reactance will increase with decrease in frequency and it will decrease with increase in frequency. Therefore, the coupling capacitors will offer a very low reactance in mid and high frequency regions and they can be replaced by short circuit, without any problem. So they do not have any effect at medium and high frequencies. At low frequencies, however, the reactance of coupling capacitors will be large. Due to this, the voltage drop across them increases with reduction in frequency. This increased voltage drop will reduce both the output voltage and gain of the amplifier in the low frequency region of the frequency response.

8.4.8. Effect of Bypass Capacitor

The bypass capacitor is connected across the emitter resistance R_E in BJT amplifier as shown in figure 8.14.



(a) Bypass capacitor in the medium and high frequencies

At medium and high frequencies, the bypass capacitor C_E offers a very low reactance. Therefore, it can be replaced by a short circuit as shown in figure 8.14(b). Therefore, the impedance Z_E which is the parallel combination of R_E and X_{CE} will have a zero value. Thus, R_E is bypassed successfully and the bypass capacitor C_E has no effect on the frequency response of the amplifier at medium and high frequencies. But at low frequencies, the reactance X_{CE} is not equal to zero but it has some finite value. Thus, the parallel combination of R_E and C_E will offer a finite impedance. So, R_E is not properly bypassed. Let the impedance of the parallel combination be denoted by R_E' . We know that the gain of CE amplifier with bypassed R_E is given by,

$$A_V = -h_{ie} \frac{R_L}{R_E}$$

And that for a CE amplifier with unbypassed R_E is given by,

$$A_V = -h_{ie} \frac{R_L}{h_{ie}(1 + h_{ie}/R_E)} \quad \dots (8.8)$$

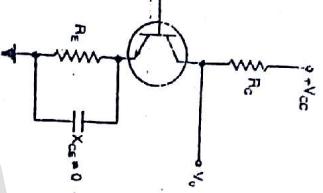
If R_E is not properly bypassed, then, the voltage gain will decrease. Thus, reduction in gain at low frequencies takes place due to the coupling and bypass capacitors.

Effect of bypass capacitor in FET amplifier

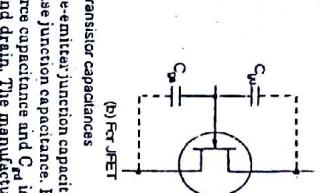
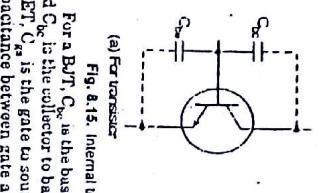
The bypass capacitor is present in the source terminal of the FET. The effect of bypass capacitor in FET is same as that in the transistor amplifier.

8.4.9. Effect of Internal Transistor Capacitances

At high frequencies, the coupling and bypass capacitors act as short circuit due to their low reactance, and do not affect the amplifier response. But, the internal junction capacitances will come into play. They reduce the amplifier gain and introduce unwanted phase shift as the signal frequency is increased. Figure 8.15 shows the internal p-n junction capacitances for a BJT and FET.



(a) For transistor



FEW IMPORTANT SOLVED EXAMPLES

EXAMPLE 8.1. An audio frequency amplifier is to be designed for operating over a range of 10 Hz to 20 kHz. Calculate the value of input coupling capacitor C_1 if the total series resistance is 10 kΩ.

Solution: The capacitor C_1 should have a value such that its reactance even at the lowest frequency, must be negligibly small as compared to the total series resistance. So, $X_{C1} = R_s / 10 \text{ at the lowest frequency i.e., at } 10 \text{ Hz}$.

Therefore, $X_{C1} = 10 \text{ k}\Omega / 10 = 1 \text{ k}\Omega \text{ at } f = 10 \text{ Hz}$

Thus, $\frac{1}{2\pi f C_1} = 1000$

$$\text{or } C_1 = \frac{1}{2\pi \times 10 \times 1000}$$

$$\text{or } C_1 = 7.954 \mu\text{F} \quad \text{Ans.}$$

As this is not a standard value, we select the value of C_1 to 10 μF.

EXAMPLE 8.2. If the mid band gain of an amplifier is 100, and if the half power frequencies are $f_L = 10 \text{ Hz}$ and $f_H = 10 \text{ kHz}$, calculate the amplifier gain at the frequencies of 20 Hz and 20 kHz.

Solution: Given that $A_{V(\text{mid})} = 100$, $f_L = 10 \text{ Hz}$, $f_H = 10 \text{ kHz}$.

(i) Voltage gain at frequency $f = 20 \text{ Hz}$:

$$A_{V(\text{low})} = \frac{A_{V(\text{mid})}}{\sqrt{1 + (f_L/f)^2}} = \frac{100}{\sqrt{1 + (10/20)^2}} = 44.72 \quad \text{Ans.}$$

(ii) Voltage gain at $f = 20 \text{ kHz}$:

$$A_{V(\text{high})} = \frac{A_{V(\text{mid})}}{\sqrt{1 + (f/f_H)^2}} = \sqrt{1 + (10 \text{ kHz} / 10 \text{ kHz})^2} = 100$$

or $A_{V(\text{high})} = 62.47 \quad \text{Ans.}$

EXAMPLE 8.3. The lower 3 dB frequency of an amplifier is 100 Hz and the gain in the mid frequency is 40. Calculate the gain of the amplifier at the lower 0 dB frequency.

Solution: Given: $f_L = 100 \text{ Hz}$, $A_{V(\text{mid})} = 40$

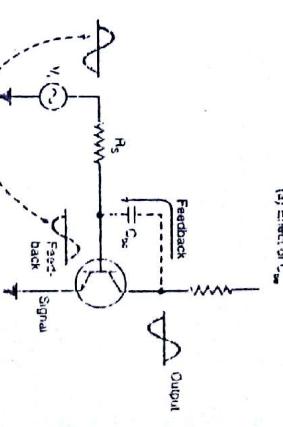
The voltage gain at low frequencies is given by:

$$A_{V(\text{low})} = \frac{A_{V(\text{mid})}}{\sqrt{1 + (f_L/f)^2}}$$

V_i , so the effective input to the amplifier is reduced due to the effect of C_{be} . The input voltage and gain, therefore, is illustrated in Figure 8.15(b). Thus, the internal capacitances reduce the amplifier gain at high frequencies.

Due to small reactance of C_{be} , the input to amplifier reduces to a very small value.

(4) Effect of C_{be}



Important Point: The effects of coupling, bypass and internal capacitors discussed so far are applicable as it is to the JFET amplifiers.

Fig. 8.15. Effect of internal capacitances

(i) Effect of C_{be}

(ii) Effect of C_{be}

(iii) Effect of C_{be}

(iv) Effect of C_{be}

(v) Effect of C_{be}

(vi) Effect of C_{be}

(vii) Effect of C_{be}

(viii) Effect of C_{be}

(ix) Effect of C_{be}

(x) Effect of C_{be}

(xi) Effect of C_{be}

(xii) Effect of C_{be}

(xiii) Effect of C_{be}

(xiv) Effect of C_{be}

(xv) Effect of C_{be}

(xvi) Effect of C_{be}

(xvii) Effect of C_{be}

(xviii) Effect of C_{be}

(xix) Effect of C_{be}

(xx) Effect of C_{be}

(xxi) Effect of C_{be}

(xxii) Effect of C_{be}

(xxiii) Effect of C_{be}

(xxiv) Effect of C_{be}

(xxv) Effect of C_{be}

(xxvi) Effect of C_{be}

(xxvii) Effect of C_{be}

(xxviii) Effect of C_{be}

(xxix) Effect of C_{be}

(xxx) Effect of C_{be}

(xxxi) Effect of C_{be}

Scanned by CamScanner Downloaded from Ktunotes.in To get more study materials click here > www.ktustudent.com

13

Cascaded Amplifiers : Multistage Amplifiers

INSIDE THIS CHAPTER

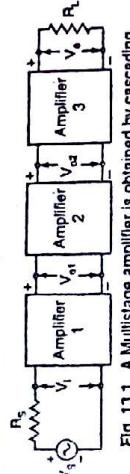
- Introduction; ➤ Need of Cascading; ➤ How for Select Amplifier? Configurations for Cascade Connection? ➤ Methods of Coupling Multistage Amplifiers; ➤ Procedure to Analyze the Multistage Amplifier; ➤ CE-CEB (Cascade) Amplifier; ➤ Effect of Cascading on Bandwidth; ➤ Techniques to Improve the Input Impedance of Emitter Follower; ➤ Bootstrap Emitter Follower; ➤ Darlington Connection

13.1 INTRODUCTION

The meaning of the word **cascading** is to connect a number of amplifier stages to each other with the output of the previous stage to the input of next stage as shown in figure 13.1. Thus, a multistage amplifier is obtained by cascading a number of amplifiers.

13.2 NEED OF CASCADING

The amplifier circuits analyzed earlier, using transistors, were single stage circuits. Practically, there is a limitation on the maximum value of voltage gain that can be obtained from a single stage amplifier. So, in order to increase gain of the amplifier, it is necessary to use a multistage amplifier that provides higher voltage gain as compared to single stage amplifiers.



Many times, a single stage amplifier is not capable of providing input and output impedances of correct magnitudes.

- (i) The most important parameters of an amplifier are its input impedance, voltage gain, bandwidth and output resistance.

(ii) The required values of these parameters are dependent on the particular application.

- (iii) It is generally not possible for a single stage amplifier to fulfil all the requirements. Hence, we have to use a multistage amplifier, which deals with these requirements.

- (iv) In such cases, if more than one amplifier stages are cascaded, then, the input stage takes care of the input impedance while the output stage takes care of the output impedance matching.

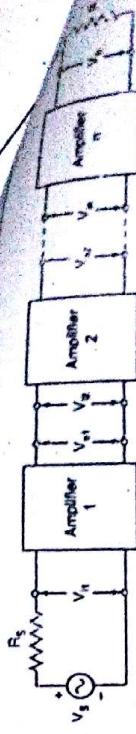


Fig. 13.2. 3-stage cascaded voltage amplifier

Substituting these values into equation (13.1), we get,

$$A_v = A_{v1} \times A_{v2} \times A_{v3}$$

Important Point: Thus, the overall voltage gain of a cascaded multistage amplifier is equal to the product of the voltage gains of the individual amplifier stages.

Overall Current Gain

Similarly, we can prove that the total overall current gain of a multistage amplifier is given by,

$$A_i = A_{i1} \times A_{i2} \times A_{i3}$$

where, A_i = Overall current gain of the multistage amplifier. A_{i1}, A_{i2} and A_{i3} are the current gains of the individual amplifiers.

Here, it may be noted that equation (13.3) may not always be true. If biasing resistors for each stage are included, then, current division takes place and equation (13.3) will no more be valid.

Overall Input Resistance (R_i)

The overall input resistance of a cascaded configuration is equal to the input resistance of the first stage. Overall Output Resistance (R_o)

The overall output resistance of a cascaded amplifier is equal to the output resistance of the last stage.

13.2.3 n-stage Cascaded Amplifier

Figure 13.1 shows a cascaded amplifier with three stages. But, there is no restriction on the number of stages to be cascaded. So, in general it is possible to cascade n-number of stages as shown in figure 13.2. All the principles of a three stage cascaded amplifiers are applicable to the n-stage cascaded amplifiers as well.

Thus, the voltage gain of the overall cascade connection is,

$$A_v = A_{v1} \times A_{v2} \times \dots \times A_{vn}$$

13.2.4 Gain in Decibels

The gain expressed as a ratio of output voltage and input voltage is called as the linear gain. But, sometimes, it is more convenient to express the gain on the logarithmic scale rather than on the linear scale. Therefore, gain is defined in decibels as follow:

$$\text{On the logarithmic scale, the gain is expressed as:}$$

$$(i) \text{Power gain in dB} = 10 \log_{10} \left[\frac{P_o}{P_i} \right] \quad \dots (13.1)$$

where P_o = Output power of the amplifier
 P_i = Input power to the amplifier

$$(ii) \text{Overall voltage gain in}$$

$$\text{dB} = 20 \log_{10} \left[\frac{V_o}{V_i} \right] \quad \dots (13.5)$$

where V_o = Output voltage of the amplifier
 V_i = Input voltage of the amplifier

Fig. 13.2. 3-stage cascaded amplifier

Substituting these values into equation (13.1), we get,

$$A_v = A_{v1} \times A_{v2} \times A_{v3}$$

Important Point: Thus, the overall voltage gain of a cascaded multistage amplifier is equal to the product of the voltage gains of the individual amplifier stages.

EXAMPLE 13.1

A voltage amplifier provides an output voltage of 5V when an input voltage of 1mV is applied to it. Calculate its voltage gain in dB.

$$\text{Solution: Voltage gain in dB} = 20 \log_{10} \left(\frac{V_o}{V_i} \right) \quad \dots (13.2)$$

Ans.

EXAMPLE 13.2

Derive the expression for the overall gain in decibels of an n-stage cascaded amplifier.

Solution (i): Let n amplifier stages are connected in series. Let their individual voltage gains be denoted as $A_{v1}, A_{v2}, \dots, A_{vn}$. Therefore, overall voltage gain

$$A_v = A_{v1} \times A_{v2} \times \dots \times A_{vn}$$

(ii) The overall voltage gain is expressed in dB as A_v in dB = $20 \log_{10} (A_v)$.

Hence, A_v in dB = A_{v1} dB + A_{v2} dB + ... + A_{vn} dB

(iii) Taking log on both the sides of equation (i) after multiplying both sides by 20, we get,

Important Point: Thus, the overall voltage gain in dB of a cascaded amplifier is equal to the sum of the gains in dB of the individual stages in the cascade connection.

13.2.5 Why to Express Gain in dB

The reasons for expressing gain in dB are as follows:

(i) On the logarithmic scale, we can conveniently express very small as well as very large values of a gain. For example, a voltage gain of 100000 can be represented as +120 dB, while a voltage gain of 1/100000 can be expressed as -120 dB.

(ii) The overall gain of a cascaded amplifier in dB can be obtained just by adding the individual stage gains.

(iii) Human ears have a logarithmic response. Therefore, the sound levels are expressed in decibels. So, if an amplifier is driving loud speakers at a fixed level, then, it is convenient to express the gain in decibels.

13.3 HOW TO SELECT AMPLIFIER CONFIGURATIONS FOR CASCADE CONNECTION?

The cascaded amplifier should match the source polarization with the input impedance of the first stage for maximum power transfer. **Secondly**, the gain of the cascaded amplifier should be sufficient, high, and its output impedance of the final stage should match the load impedance of a **CE** or **CB** configuration of a transistor amplifier are available to the designer. He has to select proper configurations to meet the requirements mentioned above.

13.4 GAIN IN DECIBLES

The gain expressed as a ratio of output voltage and input voltage is called as the linear gain. But, sometimes, it is more convenient to express the gain on the logarithmic scale rather than on the linear scale. Therefore, gain is defined in decibels as follow:

$$(i) \text{Power gain in dB} = 10 \log_{10} \left[\frac{P_o}{P_i} \right] \quad \dots (13.1)$$

where P_o = Output power of the amplifier
 P_i = Input power to the amplifier

$$(ii) \text{Overall voltage gain in}$$

$$\text{dB} = 20 \log_{10} \left[\frac{V_o}{V_i} \right] \quad \dots (13.5)$$

where V_o = Output voltage of the amplifier
 V_i = Input voltage of the amplifier



For the selection of configuration for the input stage, we must compare the input impedances offered by the three configurations as shown in table 13.1.

Table 13.1. Input resistance of various amplifier configurations

S.No.	Configuration	Input resistance	Select
1.	Common Base (CB)	Very low ($20\text{ }\mu\Omega$)	✓
2.	Common Emitter (CE)	Low ($1\text{ k}\Omega$)	✓
3.	Common Collector (CC)	High (Few hundred $\text{k}\Omega$)	—

Thus, if the source resistance is low, then, CB configuration should be selected for the input stage and if source resistance is medium, then, CE configuration should be selected.

13.2 Selection of Configuration for the Output Stage

(i) For the selection of configuration for the output stage, we must compare the output impedances of the three amplifier configurations, as shown in table 13.2.

Table 13.2. Output resistance of various amplifier configurations

S.No.	Configuration	Output resistance	Select
1.	Common Base (CB)	High ($1\text{ M}\Omega$ or higher)	—
2.	Common Emitter (CE)	High (Few hundred $\text{k}\Omega$)	—
3.	Common Collector (CC)	Low (Few ohms)	✓

Therefore, for loads such as loud speakers, which have a very low resistance, a common collector configuration should be used as the output stage.

13.3 Selection of Configuration for the Middle Stages

The middle stages are supposed to provide the required voltage gain of the cascaded configuration. The selection of configuration for the middle stages should be based on the comparison of the voltage and current gains of the various configurations.

The voltage and current gains of various configurations are given in table 13.3.

Table 13.3. Voltage and current gains of various amplifier configurations

S.No.	Configuration	Voltage gain	Current gain	Select
1.	Common Base	Medium	Low (less than 1)	—
2.	Common Emitter	Medium	High	✓
3.	Common Collector	Low (less than 1)	High	—

Therefore, for a high voltage gain, the CE configuration is preferred for the middle stages of a cascaded amplifier.

13.4 METHODS OF COUPLING MULTISTAGE AMPLIFIERS

In the multistage amplifiers, the output signal of preceding stage is to be connected to the input of the next stage. This is called as interstage coupling. The interstage coupling can be achieved by using any one of the following coupling techniques.

The coupling techniques are:

- R-C coupling
- Transformer coupling
- Direct coupling

13.4.1 R-C Coupled Amplifiers

A typical R-C coupled transistor amplifier is as shown in figure 13.3. Let us carefully look at the way the output signal of first stage is being coupled to the input of the second stage. The coupling takes place through coupling capacitor and resistive load at the output of the first stage. Therefore, this is known as the R-C coupling.

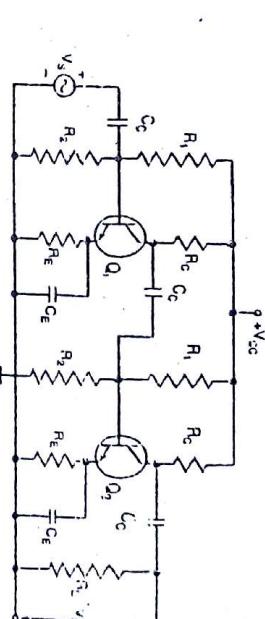


Fig. 13.3. Two stage R-C coupled transistor amplifier

Important points about the R-C coupled amplifiers are:

- R_1 , R_2 and R_3 are the biasing resistors used separately for the two stages. Voltage divider biasing is being used.
- Due to the use of coupling capacitors, the dc voltages will not be coupled from one stage to the other. Therefore, the quiescent point of the next stage will not be affected due to coupling. Thus, due to RC coupling, the dc operating conditions in any stage remain unaffected.

- The R-C network gives a wideband frequency response without introduction of peaks at any frequencies. Therefore, RC coupling can be used for the AF amplifiers.
- The frequency response drops off (reduces in magnitude) at low frequencies due to the coupling capacitors and at high frequencies, due to the shunting effects of the internal capacitances of the transistor and stray capacitances.
- The R-C coupling can be used in the multistage JFET amplifiers as well.
- The typical frequency response of an RC coupled amplifier has been shown in figure 13.4.

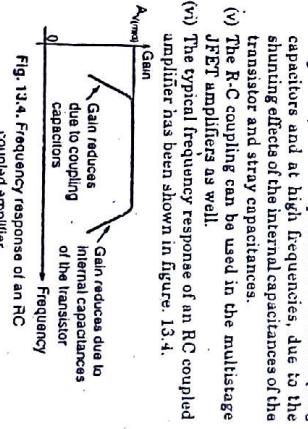


Fig. 13.4. Frequency response of an RC coupled amplifier

Advantages of RC coupled amplifiers

The advantages of RC coupled amplifiers are:

- Wide frequency response (large bandwidth)
- It is the most convenient coupling.
- It is an inexpensive way of coupling.
- Due to the capacitor, the dc biasing of individual stages will remain unchanged even after cascading.
- It is a high fidelity amplifier.
- The distortion in the output is low.
- No core distortion.

Disadvantages

- No impedance matching

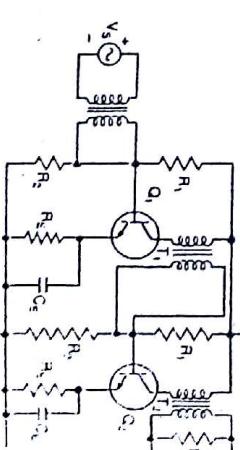


Fig. 13.5. RC coupled FET amplifier

13.4.2 Transformer Coupled Amplifiers

A transformer coupled two stage amplifier using transistors is as shown in figure 13.6. Note the important points about this type of coupling.

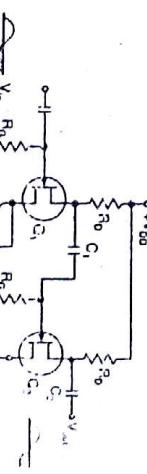


Fig. 13.6. A two stage transformer coupled amplifier using transistors.

Fig. 17.10 (a) Block diagram of a voltage series feedback amplifier is shown in figure 17.10(a). Here, we use the combination of voltage sampling and series mixing.

Therefore, **Voltage Series Feedback = Voltage Sampling + Series Mixing**

The voltage series feedback is present in the voltage amplifiers.

17.4.2. Voltage Shunt Feedback

The block diagram of an amplifier with voltage shunt feedback is shown in figure 17.10(b). Voltage shunt feedback is a combination of voltage sampling and shunt mixing.

The voltage series feedback is present in the voltage amplifiers.

17.4.3. Current Shunt Feedback

This is a combination of current sampling and series mixing. The block diagram of a feedback amplifier with current shunt feedback is shown in figure 17.10(c).

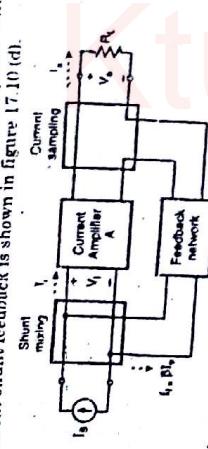


Fig. 17.10. (a) Voltage amplifier with voltage series feedback

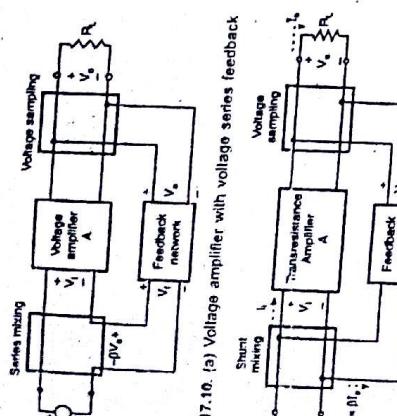


Fig. 17.10. (b) Transconductance amplifier with voltage shunt feedback

Therefore, **Voltage Shunt Feedback = Voltage Sampling + Shunt Mixing**

The voltage shunt feedback is present in the transresistance amplifier.

17.4.3. Current Series Feedback

Applying the same logic, the current series feedback is a combination of current sampling and series mixing. The block diagram of a amplifier with current series feedback is as shown in figure 17.10(c).

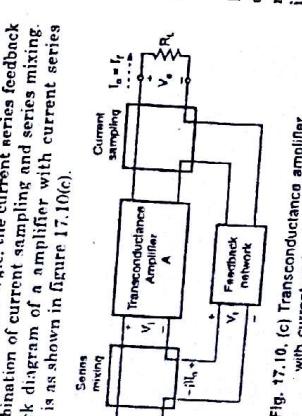


Fig. 17.10. (c) Transconductance amplifier with current series feedback

17.5. GENERAL CHARACTERISTICS OF NEGATIVE FEEDBACK AMPLIFIERS

17.5.1. Expression for Transfer Gain with Feedback (\$A_f\$)

Let us consider figure 17.9 which shows the schematic diagram of a negative feedback amplifier.

A = Transfer gain of the basic amplifier without feedback and

\$A_f = Transfer gain of the basic amplifier with feedback.

Therefore, \$A = \frac{X_o}{X_s}\$ and \$A_f = \frac{X_o}{X_s}\$... (17.28)

where, \$X_o\$ = Output signal (Voltage or current)

\$X_s\$ = Input signal (Voltage or current)

\$X_f\$ = Source signal (Voltage or current)

Step-2 Again considering figure 17.9, we can write that,

where, \$X_f = X_s - X_t\$... (17.29)

Substituting the value of \$X_f\$ from equation (17.29) in equation (17.28) we write,

$$A_f = \frac{X_o}{X_s + X_t}$$

Dividing numerator and denominator by \$X_t\$, we write,

$$A_f = \frac{X_o / X_t}{(X_s / X_t) + 1} \quad \dots (17.30)$$

Step 3: But,

$$\frac{X_o}{X_t} = A$$

Because \$\beta = \frac{X_f}{X_s}\$, it is called as feedback factor or feedback ratio. It is always less than 0 and 1.

Transfer gain with feedback = \$A_f = \frac{A}{1 + \beta}\$

Conclusions: From equations (17.28), it is clear that without feedback (\$A\$),

Hence, \$A_f < A\$

As we increase the value of \$\beta\$, then \$A_f\$ will decrease.

17.5.2. Stabilization of Gain

The amplifier gain does not remain stable due to variation in circuit component values and temperature characteristics. The variation in component values of transistor characteristics takes place due to the temperature changes, replacement of component etc. The lack of stability of gain can be reduced by using negative feedback.

Let us obtain the expression for the expression for with feedback.

Expression for \$dA_f / dA_f\$

The amplifier gain with feedback is given by,

$$A_f = \frac{A}{1 + \beta}$$

Differentiating both sides with respect to \$A\$, we get,

$$\frac{dA_f}{dA} = \frac{(1 + \beta) A - A(1 + \beta)}{(1 + \beta)^2} = \frac{1}{(1 + \beta)^2}$$

Dividing both the sides by \$A_f\$, we get,

$$\frac{dA_f}{A_f} = \frac{1}{(1 + \beta)^2} - \frac{1}{A_f}$$

Substituting the expression for \$A_f\$, we get,

$$\frac{dA_f}{A_f} = \frac{dA}{(1 + \beta)^2} - \frac{1}{A_f}$$

Therefore, \$\frac{dA}{A_f} = \frac{dA}{A} - \frac{1}{(1 + \beta)^2}\$

Hence, \$\frac{dA}{A} = \frac{dA_f}{A_f} + \frac{1}{(1 + \beta)^2}\$

Conclusion from Equation (17.30)

From equation (17.34), we can conclude that the fractional change in \$A_f\$ is less than that in \$A\$ and changes by a factor \$(1 + \beta)\$.

Thus, the gain is stabilized due to negative feedback.

Current series feedback is present in the transconductance amplifiers.

17.4.4. Current Shunt Feedback

This is a combination of current sampling and series mixing.

Therefore, **Current Shunt Feedback = Current Sampling + Series Mixing**

The current shunt feedback is present in the current series feedback amplifiers.

17.4.5. Loop Gain

Let us consider figure 17.9. The signal \$X_d\$ is multiplied by \$A\$ when it is passed through the amplifier, it is again multiplied by \$\beta\$ when passed through the feedback network path discussed above takes us from input terminal around the loop that consists of the amplifier and feedback network back to the input. The signal \$X_d\$ gets multiplied by \$-\beta A\$ while travelling on this path. The product \$-\beta A\$ is called as the loop gain or return ratio. The return difference \$D\$ is defined as,

$$D = 1 - \text{loop gain} = 1 + A\beta \quad \dots (17.26)$$

The amount of feedback introduced into an amplifier is expressed in decibels as follows:

$$N = \text{dB of feedback} = 20 \log \left| \frac{A_f}{A} \right| \quad \dots (17.27)$$

17.4.6. Basic Assumptions

Following are the basic assumptions in the analysis of feedback amplifier:

(i) The input signal is always transmitted through the amplifier and not through the feedback network.

(ii) The feedback signal is transmitted from the output to input through the feedback network and not through the amplifier.

(iii) The feedback factor \$\beta\$ is independent of the load and source resistances \$R_L\$ and \$R_S\$.

17.4.7. Advantages of using Negative Feedback

We know that with the introduction of negative feedback, the amplifier gain reduces. This is an important reduction in amplifier gain. Inspite of it offers some of the advantages as follows:

- (i) Negative feedback stabilizes the gain of the amplifier.

$$\text{Sensitivity} = \frac{1}{1 + \beta A} \quad \dots(17.35)$$

Thus, stability of the transfer gain is defined as the reciprocal of sensitivity.

Approximate expression for A_f

We have $A_f \approx \frac{A}{1 + \beta A}$

If $\beta A > 1$, then $1 + \beta A \approx \beta A$

$$A_f \approx \frac{A}{\beta A} \approx \frac{1}{\beta} \quad \dots(17.37)$$

Hence, A_f is dependent only on the factor β .

This equation shows that A_f is independent of the active device amplifier gain.

17.5.2. Effect of Negative Feedback on the Input Resistance

To understand the effect of negative feedback on the input resistance, let us divide the four configurations into two groups:

Group 1: Voltage series and current shunt feedback.

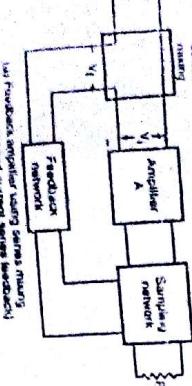
Group 2: Voltage shunt and Current Series

(i) Effect of Voltage Series and Current Series Feedback

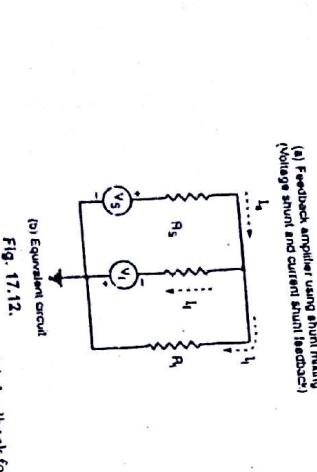
The block diagram of shunt type feedback amplifier has been shown in figure 17.12(a). This type of amplifier uses shunt mixing on the input side. The equivalent circuit of shunt mixing type amplifier is shown in figure 17.12(b).

With increase in negative feedback, V_i increases, therefore, I_o will increase. In order to supply this increased current, I_s will increase and the input resistance R_{if} will decrease because $R_{if} = V_s/I_s$.

The equivalent circuit of series mixing type amplifiers is shown in figure 17.12(b).



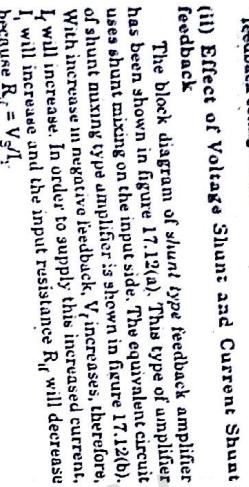
(a) Shunt type feedback amplifier using shunt mixing
(Voltage source and current source feedback)



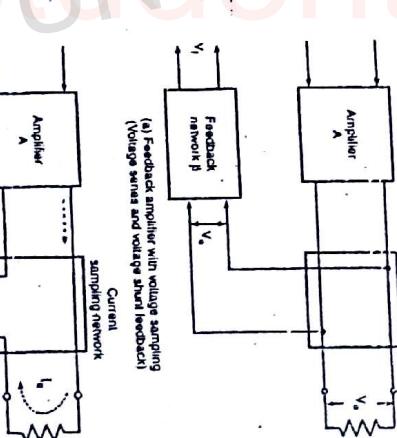
(b) Series type feedback amplifier using series mixing
(Voltage source and current source feedback)

Thus, input resistance decreases with feedback for the voltage shunt and current shunt feedback configurations. This is an undesired effect.

Fig. 17.12.



(a) Feedback amplifier using shunt mixing
(Voltage series and current shunt feedback)



(b) Feedback amplifier with voltage shunt feedback
(Voltage series and current series feedback)

Thus, input resistance decreases with feedback for the voltage shunt and current shunt feedback configurations. This is an undesired effect.

Fig. 17.13.

Fig. 17.13.

The feedback network will decrease the output resistance because when we connect two resistors R_1 and R_2 in parallel to each other, their parallel combination has a value less than R_1 as well as R_2 . Thus, output resistance decreases for voltage series and voltage shunt type feedback amplifiers.

The feedback signal V_f is in series opposition with the signal voltage V_s as shown in figure 17.11(b). Therefore, the current I_s will decrease with increase in negative feedback. The input resistance with feedback is given by:

$$R_{if} = \frac{V_s}{I_s} \quad \dots(17.38)$$

From above table, it is clear that the negative feedback has the desired effect on the input resistance for voltage series and current series feedback but it has an adverse effect for the voltage series and current shunt feedback.

17.5.4. Effect on the Output Resistance

To understand the effect of negative feedback on the output resistance, let us divide the four feedback configurations into two groups based on the type of sampling:

Group 1: Voltage series and current shunt feedback.

Group 2: Current series and voltage shunt feedback.

(i) Effect on Current Series and Current Shunt Feedback

The first group uses voltage sampling while the second one uses the current sampling. In the voltage sampling type amplifiers, the feedback network appears in parallel with R_L as shown in figure 17.13 (a).

Increase in input resistance R_{if} will increase the output resistance and reduce the output voltage V_o .

(ii) Effect on Current Series and Current Shunt Feedback

The second group uses current sampling while the feedback network appears in series with the load resistance. Hence, the output voltage V_o will increase.

(iii) Effect on Current Series and Current Shunt Feedback

Now, let us consider figure 17.13(b) which shows the current sampling type feedback. Here, the feedback network appears in series with the load resistance. When two resistors R_1 and R_2 are connected in series, the value of series combination is $(R_1 + R_2)$. Applying the same concept here, we can say that the output resistance increases with feedback for the current series and current shunt type feedback configurations. Table 17.4 summarizes the effect of negative feedback on the input and output resistances of various feedback configurations.

Table 17.4. Summary of effect of negative feedback on R_{if} and R_o .

Type of feedback	Voltage series	Current series	Voltage shunt	Current shunt
Voltage series	Increases	Increases	Decreases	Decreases
Current series	Increases	Increases	Increases	Increases
Voltage shunt	Decreases	Decreases	Decreases	Decreases
Current shunt	Decreases	Decreases	Increases	Increases

Increase in the input resistance and reduction in the output resistance are desired features of an amplifier. We can obtain them by using the voltage series feedback. Hence, the voltage series feedback is the most widely used type of negative feedback.

17.5.5. Effect on Bandwidth

One of the most important advantages of the negative feedback is that it increases the bandwidth of the amplifier. For any amplifier, the product of voltage gain and bandwidth always remains constant.

Thus, $\text{Gain} \times \text{Bandwidth} = \text{Constant}$

With the negative feedback, gain reduces therefore, to keep the value of the product constant, bandwidth of the amplifier increases proportionally. It is possible to obtain the desired bandwidth by selecting a proper feedback factor β . The increase in bandwidth due to the negative feedback is shown in figure 17.14. Also, note the reduction in gain due to negative feedback.

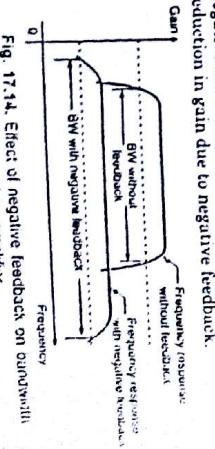


Fig. 17.14. Effect of negative feedback on bandwidth of an amplifier

EXAMPLE 17.1. An amplifier has a bandwidth of 100 Hz and voltage gain of 30 . What will be the bandwidth at gain with a 4 percent negative feedback?

SOLUTION: $BW = 100 \text{ Hz}$, $A = 30$, $\beta = 0.04$

Important Point: This expression indicates that the non-linear distortion decreases due to introduction of negative feedback.

$$\text{HW} = \text{HW}_{\text{eff}} \cdot (1 + \beta A_V) \quad \text{Ans.}$$

$$\text{HW}_{\text{eff}} = 100 \cdot (1 + 0.04 \cdot 50)$$

Effect of Non-linear Distortion

In linear distortion takes place due to the non-linearity in the transfer characteristic of the transistor of FET. Suppose that a large amplitude signal is applied to the amplifier so that the operation of the device extends in the saturation distortion or harmonic distortion. Due to introduction of negative feedback, the effective input is reduced so that the non-linearity distortion is reduced. As a consequence that the negative feedback helps it to operate in the linear region. This reduces the non-linearity distortion.

The input signal is increased by the same amount by which the second harmonic component. Let the second harmonic component of feedback be denoted by H_2 and due to feedback let the second harmonic component acting in the circuit be H'_2 .

It is evident that the negative feedback is introduced, and the distortion consists of only one term, i.e., the non-linear distortion. If $(1 + \beta A_V) \gg 1$, then, the noise will be reduced to a considerable extent. Thus noise reduction will take place for any type of negative feedback.

17.5.7. Effect on Noise

It can be shown that the noise introduced in the amplifier is multiplied by the factor $1/(1 + \beta A_V)$ if the negative feedback is introduced. If $(1 + \beta A_V) \gg 1$, then, the noise will be reduced to a considerable extent. Thus noise reduction will take place for any type of negative feedback.

17.5.8. Effect on Frequency Distortion

Equation (17.37) states that, $A_V = \frac{1}{\beta}$

It follows from this equation that if the feedback network does not contain any reactive elements, then the overall gain with feedback (A_V) will not be the function of frequency i.e., the amplifier gain will remain constant for all the frequencies. This will reduce the frequency distortion. Thus, irrespective of the type of feedback, the negative feedback reduces the frequency distortion. If the feedback network is frequency selective, then, β depends on frequency, and the amplification will be dependent on frequency. It is possible to design a feedback amplifier which gives a minimum feedback at the center frequency of the band to obtain a frequency selective characteristics.

Table 17.5 summarizes the effect of negative feedback on various amplifier characteristics.

$$\text{Hence, } V_{\text{in}} = \frac{V_{\text{b}}}{(1 + \beta A_V)} = \frac{V_{\text{b}}}{D} \quad \text{... (17.41)}$$

Table 17.5. Effect of negative feedback on amplifier characteristics

Sl. No.	Parameter/Characteristics	Type of feedback			
		Voltage series	Current series	Voltage shunt	Current shunt
1	Gain (A_V)	Reduces	Reduces	Reduces	Reduces
2	Gain stability	Improved	Improved	Improved	Improved
3	Output resistance	Increases	Decreases	Decreases	Decreases
4	Non-linear distortion	Decreases	Decreases	Decreases	Decreases
5	Noise	Decreases	Decreases	Decreases	Decreases
6	Frequency distortion	Decreases	Decreases	Decreases	Decreases
7	Bandwidth	Increases	Increases	Increases	Increases

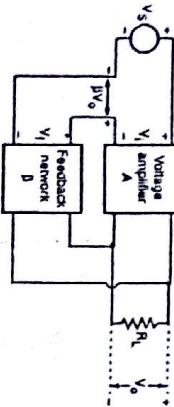
17.6. EFFECT OF NEGATIVE FEEDBACK ON R_{out} AND R_{in}

Let us discuss the effect of negative feedback on input and output resistances of various amplifier configurations.

EXAMPLE 17.2. For a voltage series feedback type amplifier prove that the input impedance is increased due to introduction of negative feedback.

ANSWER: For a voltage series feedback type amplifier, we have

$$\text{A}_{\text{Vf}} = \text{A}_{\text{V}} = R_L \rightarrow \text{A}_{\text{V}}$$
 ... (17.42)



(a) Voltage amplifier with voltage series feedback

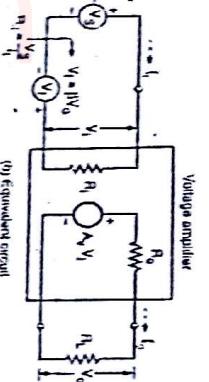


Fig. 17.15. Equivalent circuit

Solution: (i) Thevenin's equivalent circuit
The amplifier in figure 17.16(a) is replaced by its Thevenin's equivalent model to obtain the equivalent circuit of figure 17.16(b). V_s is the fed back voltage which comes in series opposition with the source voltage V_s . Note that A_{Vf} is the open circuit voltage gain taking R_L as account. Open circuit voltage gain means the voltage gain with R_L open circuited. Throughout the discussion on feedback amplifiers, we will consider A_{Vf} to be the gain of the amplifier. Hence, the subscript S will not be used. Therefore, A_{Vf} actually $A_{\text{Vf}} G_m$ is actually G_{mS} and so on.

(ii) The expression for V_s
Looking at figure 17.16(b), the expression for input resistance with feedback is given by,

But the $a = \beta A_{\text{Vf}}$ is given by,

Applying KVL to the input side of figure 17.16(b), we write,

$$V_s - I_s R_s - V_{\text{in}} = 0 \quad \text{or}$$

$$V_s = V_{\text{in}} + I_s R_s \quad \text{... (i)}$$

Substituting in value of $I_s = \beta A_{\text{Vf}} V_{\text{in}}$ we get,

$$V_s = V_{\text{in}} + \beta A_{\text{Vf}} V_{\text{in}} \quad \text{... (ii)}$$

Therefore,

$$1 = \frac{V_s - A_{\text{Vf}} V_{\text{in}}}{R_s} = \frac{V_{\text{in}}(1 + \beta A_{\text{Vf}})}{R_s} \quad \text{... (iii)}$$

(iii) The expression for V_{in}
Looking at figure 17.16, we can write that,

$$V_{\text{in}} = V_{\text{f}} = -V_{\text{in}} - \beta V_{\text{in}} = -\beta V_{\text{in}} \quad \text{... (iv)}$$

Substituting equation (iv) in equation (iii) we get,

$$1 = \frac{V_s + \beta A_{\text{Vf}} V_{\text{in}}}{R_s} = \frac{V_{\text{in}}(1 + \beta A_{\text{Vf}})}{R_s} \quad \text{... (v)}$$

Therefore,

$$R_{\text{in}} = \frac{V_s}{I_s} = \frac{R_s}{(1 + \beta A_{\text{Vf}})} \quad \text{... (17.43)}$$

In this expression, A_{Vf} is the open circuit voltage gain. R_{in} is the input resistance with feedback but without considering the load resistance R_L . Equation (17.43) indicates that R_{in} is output resistance without feedback is being divided by $(1 + \beta A_{\text{Vf}})$, i.e., the de-generative factor which contains the open circuit voltage gain A_{Vf} with out V_{in} .

This output resistance with feedback R'_{in} which includes R_L is given as $R'_{\text{in}} = R_{\text{in}} / (1 + \beta A_{\text{Vf}}) R_L$. R'_{in} which is equal to the parallel combination of R_{in} and R_L .

Thus,

$$R_{\text{in}} = R_{\text{in}} \parallel R_L = \frac{R_{\text{in}} R_L}{(R_{\text{in}} + R_L)}$$

$$= \frac{\frac{R_s}{(1 + \beta A_{\text{Vf}})} R_L}{\frac{R_s}{(1 + \beta A_{\text{Vf}})} + R_L}$$

Hence,

$$R_{\text{in}} = \frac{R_s R_L}{R_s + R_L (1 + \beta A_{\text{Vf}})}$$

$$= \frac{R_s R_L}{R_s + R_L + \beta A_{\text{Vf}} R_L}$$

Dividing the numerator and denominator by $(R_s + R_L)$, we get,

$$R_{\text{in}} = \frac{R_s / R_L / (1 + \beta A_{\text{Vf}})}{1 + \frac{R_L / R_s}{(1 + \beta A_{\text{Vf}})}} = \frac{(R_s / R_L)^2}{1 + \beta A_{\text{Vf}}}$$

where,

$$A_{\text{Vf}} = \frac{R_L A_{\text{V}}}{R_s + R_L}$$

Important Point: Thus, we have proved that the input resistance of an amplifier with voltage series feedback is always higher than that without feedback. OR, Input resistance increases due to the negative feedback.

However, it may be noted that A_{Vf} represents the open circuit voltage gain whereas, A_{V} is the ratio of V_{in} and V_{out} . Hence, A_{Vf} represents the voltage gain without feedback taking into account the load resistance R_L . The relation between A_{Vf} and A_{V} is as follows:

$$A_{\text{Vf}} = A_{\text{V}} = \lim_{R_L \rightarrow \infty} A_{\text{V}}$$

EXAMPLE 17.3. For an amplifier using voltage series feedback, derive the expression for the output resistance

$$R_{\text{out}} = \frac{R_s}{(1 + \beta A_{\text{Vf}})} R_L \quad \text{... (17.44)}$$

$\frac{1}{(1+A\beta)}$ \rightarrow represents sensitivity.

For +ve feedback $(1+A\beta) \gg 1$.

i.e. % gain with feedback is less than
% gain without ".

This \uparrow stability.

(2) Reduction in frequency distortion with
+ve feedback.

For +ve feedback having $A\beta \approx 1$, the gain
with feedback $A_f = \frac{1}{\beta}$. If feedback is
purely resistive.

So gain with feedback becomes independent
of freq. even though the amplifi. is freq.
dependent.

(3) Reducton in non-linear distortion with negative
feedback.

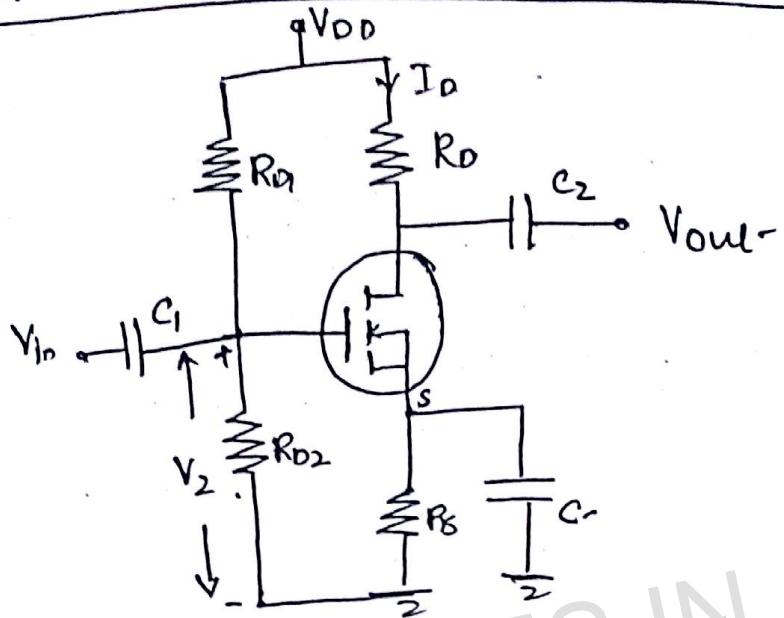
(4) Reducton in noise with negative feedback.

MOSFET Amplifiers

Common Source

MOSFET Amplifier

Common Source Enhancement MOSFET Amplifier

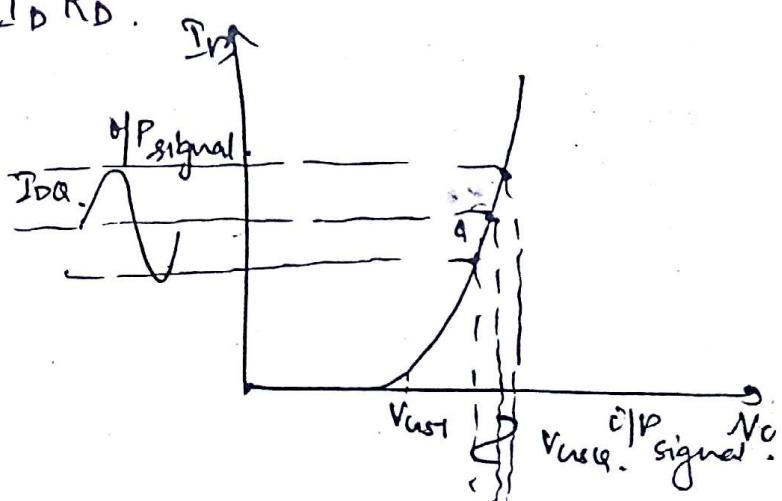


Voltage divider biasing technique is used in CS Amplifier. Here the dc stability is obtained by feedback through source resistance R_S .

$$V_{GS} = V_2 = \frac{V_{DD} \cdot R_{D2}}{R_{D1} + R_{D2}} \quad I_G = 0.$$

$$V_{DS} = V_{DD} - I_D R_D.$$

Gate is biased such that $V_{GS} > V_{Gst}$.

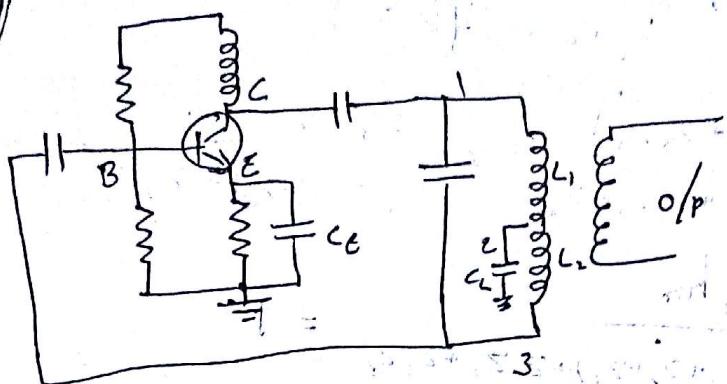


$\times = X$

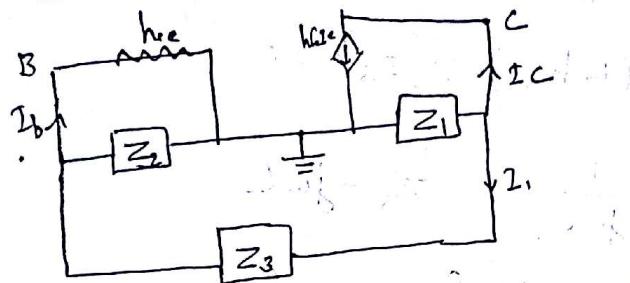
$V_{GS} + \Delta V_{GS}$ C/P Signal No.



Hartley oscillator



$$L = L_1 + L_2$$



$$Z_L = Z_1 \parallel \left[Z_3 + Z_2 \parallel h_{ie} \right]$$

$$= Z_1 \parallel \left[Z_3 + \frac{Z_2 h_{ie}}{Z_2 + h_{ie}} \right]$$

$$= Z_1 \parallel \left[\frac{Z_3 (Z_2 + h_{ie}) + Z_2 h_{ie}}{Z_2 + h_{ie}} \right]$$

$$= Z_1 \left[\frac{h_{ie} (Z_2 + Z_3) + Z_2 Z_3}{Z_2 + h_{ie}} \right] / \frac{Z_3 (Z_2 + h_{ie}) + Z_2 h_{ie}}{Z_2 + h_{ie}}$$

$$= \frac{Z_1 \left[h_{ie} (Z_2 + Z_3) + Z_2 Z_3 \right]}{Z_1 Z_2 + Z_1 h_{ie} + Z_2 h_{ie} + Z_3 Z_2 + Z_3 h_{ie}} = \frac{Z_1 \left[h_{ie} (Z_2 + Z_3) + Z_2 Z_3 \right]}{h_{ie} (Z_1 + Z_2 + Z_3) + Z_2 Z_3}$$

$$A = -\frac{h_{fe} Z_L}{h_{ie}}$$

$$V_o = \left[Z_3 + \frac{Z_2 h_{ie}}{Z_2 + h_{ie}} \right] I_1, \quad V_p = \frac{Z_2 h_{ie}}{Z_2 + h_{ie}} I_1$$

$$\beta = \frac{V_p}{V_o} = \frac{Z_2 h_{ie}}{Z_3 (Z_2 + h_{ie}) + Z_2 h_{ie}} = \frac{Z_2 h_{ie}}{h_{ie} (Z_2 + Z_3) + Z_2 Z_3}$$