EXPERIMENT 5

SINGLE STAGE RC COUPLED AMPLIFIER

Aim:

To design and set up an RC-coupled CE amplifier using bipolar junction transistor and to plot its frequency response.

Components And Equipments Required:

Transistor, dc source, capacitors, resistors, bread board, signal generator, multimeter and CRO

Theory:

RC coupled CE amplifier is widely used in audio frequency applications in radio and TV receiver. It provides current, voltage and power gains. Base current controls the collector current of a common emitter amplifier. A small increase in base current results in a relatively large increase in collector current. Similarly, a small decrease in base current causes large decrease in collector current. The emitter base junction should be forward biased and collector base junction should be in reversed biased for proper functioning of an amplifier. In the circuit diagram ,an NPN transistor is connected as a common emitter ac amplifier.R1 and R2 are employed for the voltage divider bias for the transistor. The input signal Vin is coupled through CC1 to the base and output voltage is coupled from collector through the capacitor CC2.

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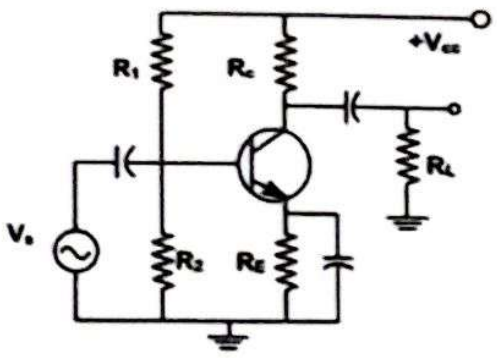
Selection Of Supply Voltage Vcc:

For distortion less output from an audio amplifier ,the operating point must be kept at middle of the load line selecting VCEQ=50%VCC.. However , VCC is selected 20% more than the required voltage swing. For eg, if the required output swing is 10V,V_{CC} is selected 12V.

Circuit Diagram



Design:

Output requirements: Mid-band voltage gain of the amplifier=50

Selection of transistor:Select BC107 since its minimum guaranteed Hfe(100)is more than the required gain.(=50) of the amplifier.

DETAILS OF BC107

Type NPN-silicon,Application: In audio frequency

Maximum ratings:V_{CB}=50V,V_{CE}= 45V, V_{EB}=6V , I_C= 100mA

Nominal ratings: V_{CE}= 5V, I_C = 2 mA, h_{fe}=100 to 500

DC BIASING CONDITIONS :

VCC=12V, I_C=2 mA, V_{RC}= 40% of Vcc=

V_{RE}= 10% of VCC =

V_{CE}= 50%of VCC =

DESIGN OF R_C: $V_{RC}=I_C \times R_C$

$R_C = V_{RC}/I_C$

=

DESIGN OF R_E : $V_{RE} = I_E * R_E$

$R_E = V_{RE}/I_E$

DESIGN OF VOLTAGE DIVIDER R1 AND R2

From the datasheet of BC107 we get H_{FE} min is 100

Assume the current through R_1 = 10IB and that through R_2 =9I_B to avoid loading the potential divider network R_1 and R_2 by the base current.

V_{R2} = V_{BE}+ V_{RE}

= 0.7+ 1.2 = 1.9 V

Also, $V_{R2} = 9I_BR_2$

$R_2 = VR_2/9I_B$ =

VR_1= Vcc-V_{R2} = 12V - 1.9 V = 10.1 V

Also, V_{R1} = 10 I_B R_1 =

Then R_1 =

DESIGN OF R_L:

Gain of the common emitter amplifier is given by the expression A_V=-(r_c/r_e)

Where rc = R_C// R_L and re = 25 mV/ I_E = 12.5 Ω

Since the required gain is 50, substituting it in the expression , we get ,R_L =

series impedence that being driven by the signal passing through the capacitor. Here
the series impedence.

Then $X_{c1} < R_{in}/10$. Here $R_{in}=R_1//R_2//h_{fe}re$

We get R_{in}= 1.1K Then $X_{c1} < 110\Omega$

So,C_{c1} =

Similarly, $X_{c2} < R_{out}/10$ where $R_{out} = Rc$

Then X_{c2} =

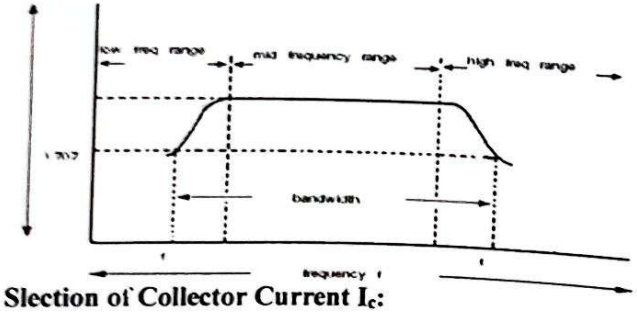
So,Cc2 =

DESIGN OF BYPASS CAPACITORS C_E

To bypass the lowest frequency (say 100 Hz), X_{CE} should be equal to one-tenth or less the resistance R_E.

Ie,$X_{CE} < R_E/10$,Then C_E =

MODEL FREQUENCY RESPOSE



Slection of Collector Current I_c:

The nominal value of Ic can be selected from the data sheet. It is the bias current at which h is measured. For BC107 it is 2 mA.

Design Of Emitter Resistor R_E

Current series feedback is used in this circuit using R_E. It stabilizes the operating poi against temperature variations. So, as a thumbrule, 10% of Vcc is fixed across R_E. Value R_E is given by the expression

$R_E = V_{RE}/I_E = V_{RE}/I_C$ Since $I_E = I_C$ approximately. $R_E = 0.1\ V_{cc}/I_C$

Design Of Rc Value of Rc can be obtained from the relation Rc=0.4 Vcc/Ic since remaining 40% of Vcc is dropped across Rc.

Design Of Potential Divider R1 And R2

Value of IB can be obtained using the expression $IB=Ic/h_{FEmin}$. At least 10IB should flow through R1 to have good range of voltage variation across R1. When IB gets branched into the base of transistor,9IB flows through R2.Values of R1 and R2 can be calculated from the dc potentials created by the respective currents.

DESIGN OF BYPASS CAPACITOR C_E

The purpose of the bypass capacitor is to bypass signal currents to ground. Its value is chosen as per the following thumb rule. To bypass the lowest frequency, XCE should be equal to one tenth or less of the emitter resistance. ie, XCE<RE/10.

DESIGN OF COUPLING CAPACITOR C_C

Value of the coupling capacitor Cc is obtained such that its reactance Xc1at the lowest frequency (say 100Hz or so far an audio amplifier),should be equal to one-tenth or less of the series impedance that being driven by the signal passing through the capacitor. That means Xc1 must be < Rin/10.Here $Rin=R_1//R_2//hfe$ re where re is the internal emitter resistance of the transistor given by the expression=$25mV/I_E$, where 25 mV is temperature equivalent voltage.

PROCEDURE

1. Test all the components using a multimeter. Set up the circuit and verify dc bias conditions. To check dc bias conditions, remove input signal and capacitors in the circuit.
2. Connect capacitors in the circuit. Apply a 100mV peak to peak sinusoidal signal from the function generator to the circuit input. Observe the input and output waveforms on the CRO screen respectively.
3. Keeping the input voltage constant at 100mV,vary the frequency of the input signal from 10 to MHz. easure the output amplitude corresponding to different frequencies and enter it in the Tabular column

EXPERIMENT 8

LOW FREQUENCY OSCILLATOR
RC PHASE SHIFT OSCILLATOR

Aim

To design and setup RC phase shift oscillator using opamp for a frequency of 1KHz

Components and equipment required

Sl. No	Component	Specification	Quantity
1	IC	IC 741	1
2	Resistors	10KΩ	1
		2.2KΩ	1
		4.7KΩ	2
		47KΩ	1
		680Ω	1
3	Capacitors	1μF	1
		0.01μF	1
		22μF	1
4	potentiometer	47KΩ	1

Theory

An oscillator is an electronic circuit for generating an ac signal voltage with a dc supply as the only input requirement. The frequency of the generated signal is decided by the circuit elements. An oscillator requires an amplifier, a frequency selective network, and a positive feedback from the output to the input. The Barkhausen criterion for sustained oscillator is $A\beta = 1$ where A is gain of the amplifier and β is the feedback factor. The unity gain means signal is in phase(If the signal is 180° out of phase , gain will be -1.

a common emitter amplifier is used, with a resistive collector load, there is a 180^0 phase ıift between the voltage at the base and the collector. Feedback network between the ›llector and the base must introduce an additional 180^0 phase shift at a particular frequency. he 3 section of phase shift networks are used so that each section introduce approximately 0^0 phase shift at resonant frequency. By analysis resonant frequency f can be expressed by ıe equation,

$$f = \frac{1}{2\pi RC\sqrt{6+4Rc/R}}$$

he three section RC network offers a β of 1/29. Hence the gain of the amplifier should be 9. For this the h_{FE} of the transistor is found to be

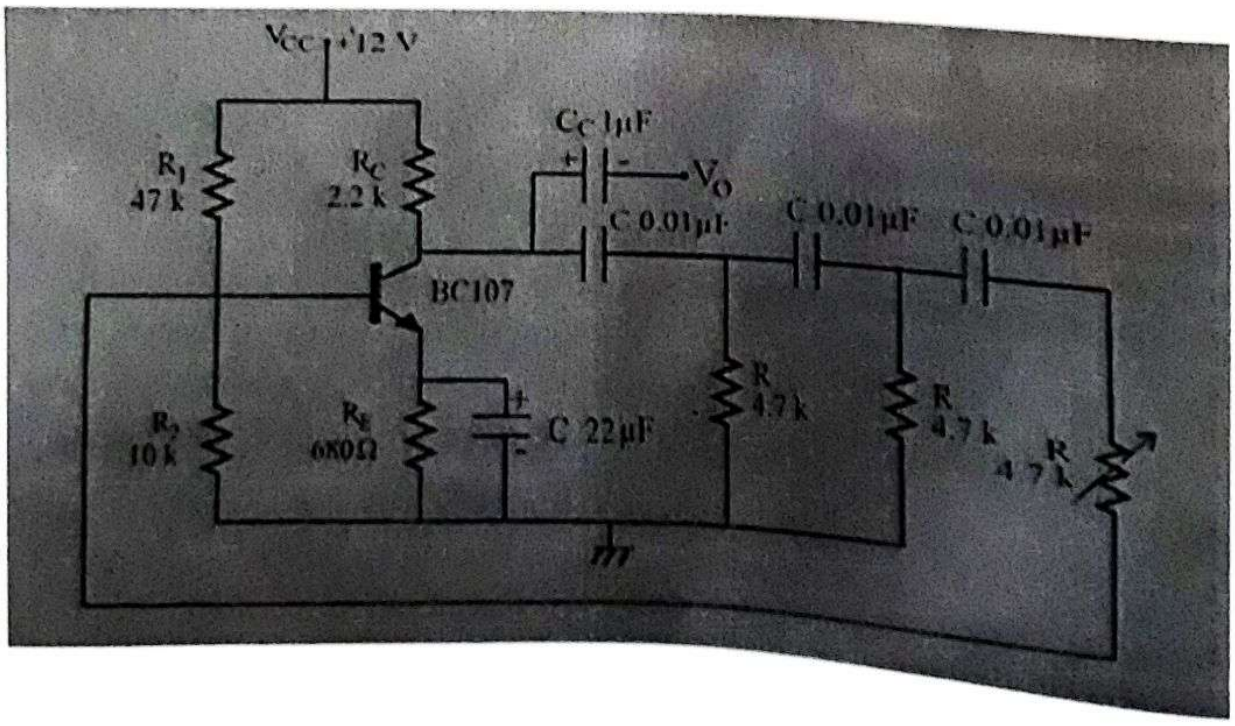
$$h_{FE} \geq 23+29(R/Rc)+4(Rc/R)$$

he phase shift oscillator is particularly useful in the audio frequency range.

Procedure

1. Set up the amplifier part of the oscillator and test the DC conditions. Ensure that the transistor is operating as an amplifier with required gain.
2. Connect the feedback network and observe the sine wave on CRO screen and measure its amplitude and frequency.
3. Observe the waveforms at the base and collector of the transistor simultaneously on CRO screen and notice the phase difference between them.

Circuit Diagram:



Design:

Design of the amplifier : Select transistor BC107. It can provide a gain more than 29 because its minimum h_{FE} is 100.

DC biasing conditions: V_{CC}=12V, I_C=2mA

V_{RC}= 40% of V_{CC}= 4.8V,

V_{RE}=10% of V_{CC} =1.2V

V_{CE} = 50% of V_{CC} =6 V.

Design of R_C: $V_{RC}=I_C \times R_C$=4.8 V.

From this, we get R_C=2.4k. Use 2.2 k std.

Design of R_E: $V_{RE}= I_E \times R_E= I_C \times R_E$ =1.2 V.

From this we get, R_E= 600Ω. Select 680 Ω std.

Design of voltage divider R_1 and R_2:

From the data sheet of BC 107 we get h_{FE} min is 100.

$I_B = I_C/h_{FE}$=2 mA/100=20μ A.

Assume the current through R_1= 10 I_B and that through R_2= 9 I_B to avoid loading the potential divider by the base current.

V_{R2}= Voltage across $R_2= V_{BE} + V_{RE}$

i.e $V_{R2}= V_{BE}+V_{RE}$=0.7+1.2=1.9V. Also, $V_{R2}=9I_B R_2$= 1.9 V

Then $R_2 = \frac{1.9}{9\times20\times10^{-6}} = 10.6K\Omega. Select\ 10\ K\ std.$

V_{R1}= voltage across $R_1= V_{CC} - V_{R2}$= 12V- 1.9 V= 10.1 V

Also, $V_{R1}= 10\ I_B R_1$= 10.1 V,

Then $R_1 = \frac{10.1}{10\times20\times10^{-6}} = 50K\Omega. Select\ 47\ K\ pot\ std$

Design of frequency selective network

Required frequency of oscillation is 1KHz

$$F = \frac{1}{2\pi RC\sqrt{6+4R_C/R}} = 1 \text{ KHz}$$

Take R=4.7K to avoid loading of R_C by the RC network. Then C = 0.01μF

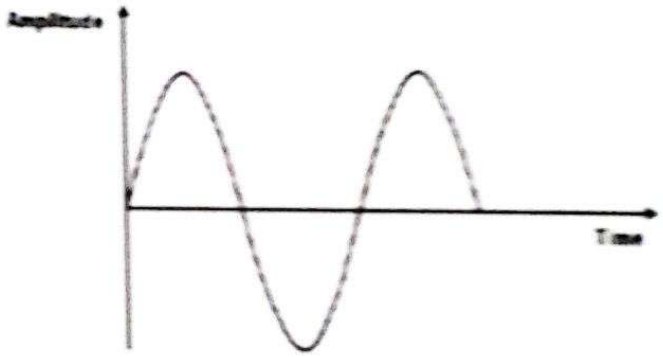
Use 4.7K pot in the last RC stage.

frequency of operation $f = \frac{1}{2\pi\sqrt{L_{eq}C}}$ where L_{eq}= L1 + L2

consider f=50KHz. Assume C=0.01μF. $\therefore 50KHz = \frac{1}{2\pi\sqrt{L_{eq} \times 0.01 \times 10^{-6}}}$

L1=L2=470μH, Ground the inductor L1 and L2 through a capacitor C_1 of value 1μ

Expected Waveform



Result

Designed and setup Hartley oscillator and observed the output waveform.

Frequency of oscillation=

EXPERIMENT 11

CLIPPING AND CLAMPING CIRCUITS

Aim:

(a) To design and set up various shunt clipping circuits using diodes and zener diodes.
(b) To design and set up various clamping circuits using diodes and capacitors.

Components required:

Sl. No:	Component	Specification	Quantity
1	Diode	1N4001	2
2	Zener diode	SZ5V6	2
3	Resistor	1KΩ	1
4	Resistor	10 KΩ	1
5	Capacitor	1μF	1

Theory:

(a) Clipper

A circuit which removes the peak of a waveform is known as a clipper. A clipper circuits clips a fraction of its input signal keeping the remaining part of the signal unchanged. The circuit limits an input voltage to certain minimum and maximum values. A clipping circuit consists of linear elements like resistors and non-linear elements like junction diodes or transistors, but it does not contain energy- storage elements like capacitors.

1.1 Positive Clipper

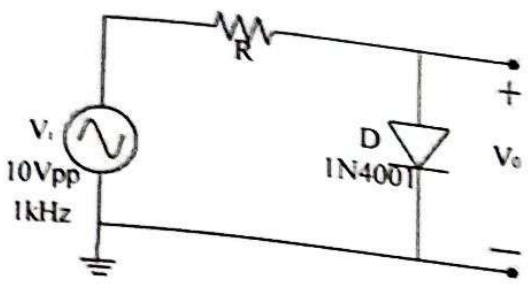
In this circuit, the diode is forward biased (cathode more positive than anode) during the positive half cycle of the sinusoidal input waveform. For the diode to become forward biased, it must have the input voltage magnitude greater than +0.7 volts (0.3 volts for a germanium diode).

Design:

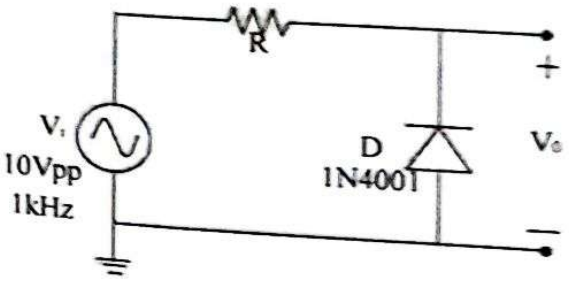
Choose I_{max} = 10mA $\qquad R \geq \frac{V_{R(max)}}{I_{max}}$

Circuit diagram:

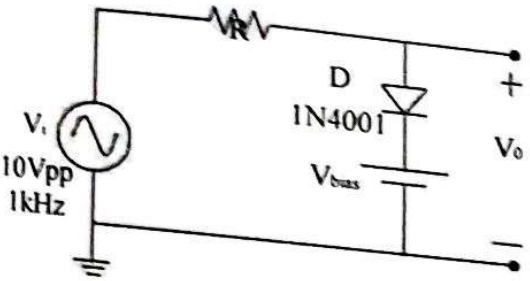
Positive Clipper



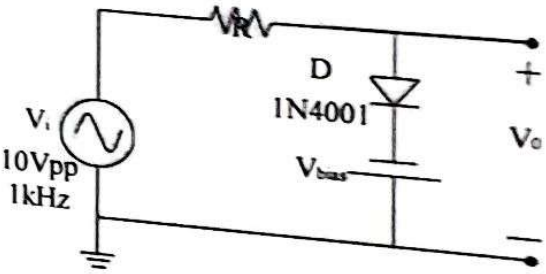
Negative Clipper



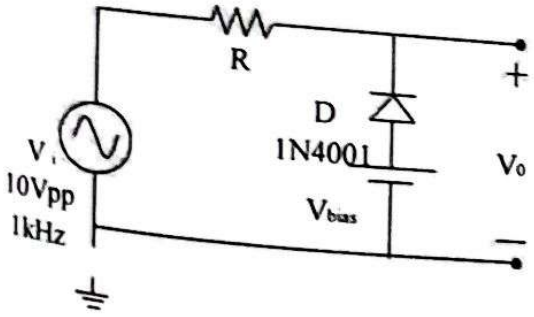
Positive clipper with positive bias



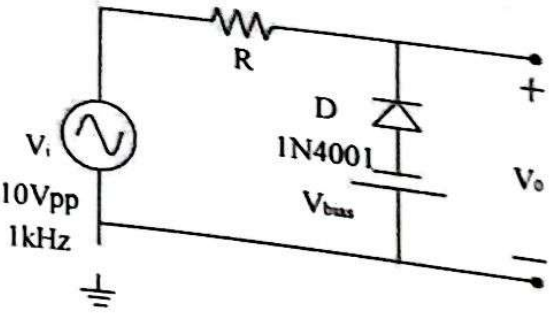
Positive clipper with negative bias



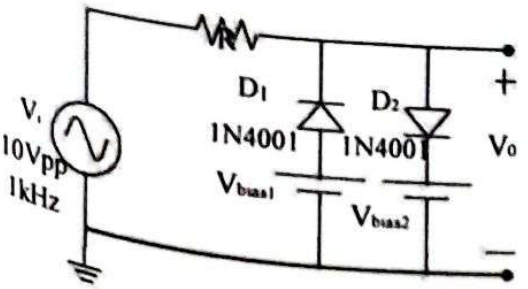
Negative clipper with positive bias



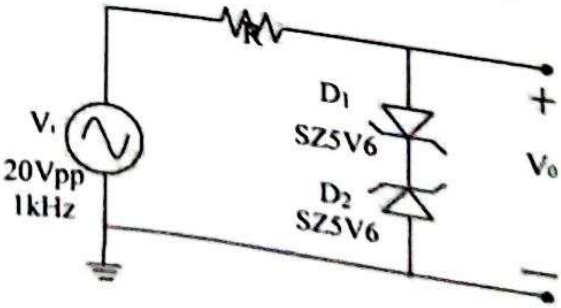
Negative clipper with negative bias



Slicer



Combinational clipper using zeners



When this happens the diodes begins to conduct and holds the voltage across itself constant at 0.7V until the sinusoidal waveform falls below this value. Thus the output voltage which is taken across the diode can never exceed 0.7 volts during the positive half cycle.
During the negative half cycle, the diode is reverse biased (anode more positive than cathode) blocking current flow through itself and as a result has no effect on the negative half of the sinusoidal voltage which passes to the load unaltered. Then the diode limits the positive half of the input waveform and is known as a positive clipper circuit.

1.2 Negative Clipper

The diode is forward biased during the negative half cycle of the sinusoidal waveform and clips it to -0.7 volts while allowing the positive half cycle to pass unaltered when reverse biased. As the diode limits the negative half cycle of the input voltage it is therefore called a negative clipper circuit.

1.3 Biased Diode Clipping Circuits

1.3.1 Positive clipper with positive bias

To produce diode clipping circuits for voltage waveforms at different levels, a bias voltage, V_{bias} is added in series with the diode as shown. The voltage across the series combination must be greater than V_{bias} + 0.7V to conduct. For example, if the V_{bias} level is set at 4.0 volts, then the sinusoidal voltage at the diode's anode terminal must be greater than 4.0 + 0.7= 4.7 volts for it to become forward biased. Any anode voltage levels above this bias point are clipped off.

1.3.2 Positive clipper with negative bias

The diode is forward biased during the entire duration of the positive half cycle. During the negative half cycle the diode is forward biased till the input is greater than 0.7V-V_{bias} otherwise the diode is reverse biased. When the diode is reverse biased the output follows the input.

1.3.2 Negative clipper with positive bias

During the positive half cycle when the input voltage is lesser than V_{bias} the diode becomes forward biased. The corresponding output voltage is at V_{bias}–0.7. During the

negative half cycle the diode is forward biased

1.3.3 Negative clipper with negative bias

During the negative half cycle, when the input voltage becomes less than V_{bias}, diode becomes forward biased and voltage $-(V_{bias}+0.7)$ appears at the output. During the positive half cycle, when the input is greater than V_{bias}, diode is reverse biased and the input appears at the output.

1.3.4 Slicer

A variable diode clipping or diode limiting level can be achieved by varying the bias voltage of the diodes. If both the positive and the negative half cycles are to be clipped, then two biased clipping diodes are used. For a slicer (with reference to figure)two positive bias voltage is required Vbias1and V_{bias2} (Vbias1< Vbias2). The output voltage works according to the following condition.

1. $V_{in} < V_{bias1} - 0.7$, $V_{out} = V_{bias1} - 0.7$
2. $V_{bias1} + 0.7 < Vin < V_{bias2} + 0.7$, $V_{out} = V_{in}$
3. $V_{in} > V_{bias2}$. $V_{out} = V_{bias2}$

1.3.5 Zener Diode Clipping

One easy way of creating biased diode clipping circuits without the need for an additional emf supply is to use Zener Diodes.

In the given circuit the output waveform will be clipped at the zener voltage plus the 0.7V forward volt drop of the other diode. So for example, the positive half cycle will be clipped at the sum of zener diode, ZD1 plus 0.7V from ZD2 and vice versa for the negative half cycle.

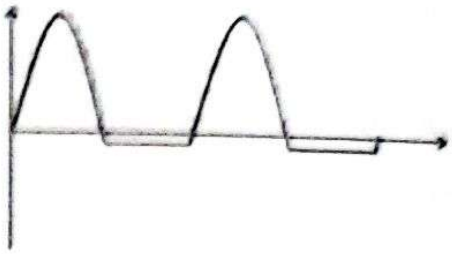
Procedure:

1. Check all the components using multimeter.
2. Set up the circuit as shown in the circuit diagram.
3. Apply a sine wave of amplitude 20 Vpp and frequency 1kHz to the circuit.

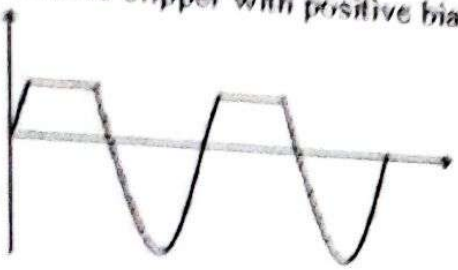
Expected waveforms:

Positive clipper

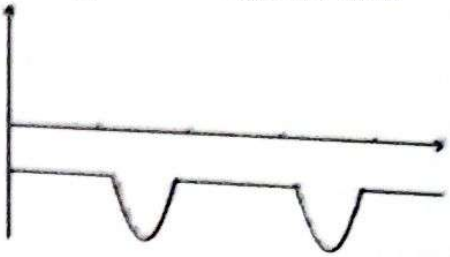
Negative clipper



Positive clipper with positive bias

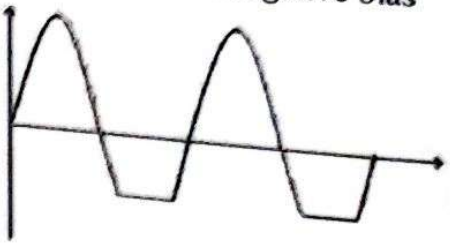


Positive clipper with negative bias



Negative clipper with positive bias

Negative clipper with negative bias

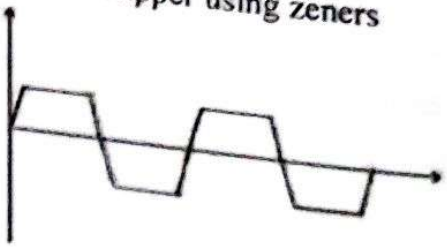


Slicer

$V_{bias2} + 0.7$

$V_{bias1} - 0.7$

Combinational clipper using zeners



(a)Clamper

A clamper is an electronic circuit that moves the whole signal up or down so as to place the peaks at the reference level. A diode clamp consists of a diode, which conducts electric current in only one direction and prevents the signal exceeding the reference value; and a capacitor which provides a DC offset from the stored charge. The capacitorforms a time constant with the resistor load which determines the range of frequencies over which the clamper will be effective.

Positive clamper

In the negative cycle of the input AC signal, the diode is forward biased and conducts, charging the capacitor to the peak negative value of V_{IN}. During the positive cycle, the diode is reverse biased and thus does not conduct. The output voltage is therefore equal to the voltage stored in the capacitor plus the input voltage.

Negative clamper

A negative unbiased clamp is the opposite of the equivalent positive clamp. In the positive cycle of the input AC signal, the diode is forward biased and conducts, charging the capacitor to the peak positive value of V_{IN}. During the negative cycle, the diode is reverse biased and thus does not conduct. The output voltage is therefore equal to the voltage stored in the capacitor plus the input voltage again.

Positive biased

A positive biased voltage clamp is identical to an equivalent unbiased clamp but with the output voltage offset by the bias amount V_{BIAS}.

Negative biased

A negative biased voltage clamp is likewise identical to an equivalent unbiased clamp but with the output voltage offset in the negative direction by the bias amount V_{BIAS}.

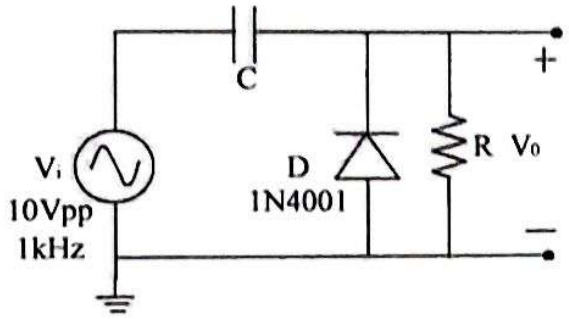
Procedure:

1. Check all the components using multimeter.
2. Set up the circuit as shown in the circuit diagram.

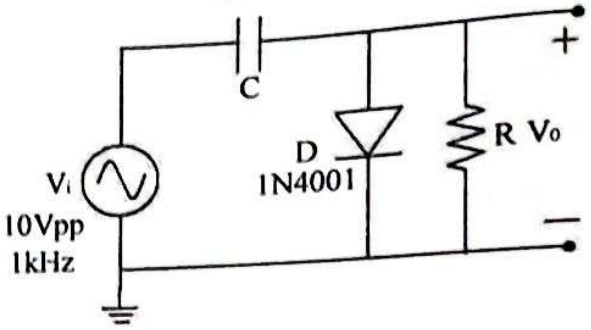
3. Apply a sine wave of amplitude 20 Vpp and frequency 1kHz to the circuit.
4. Keep the CRO in dual mode and connect input to channel 2 and output to channel 1.
5. Observe the output waveform and note down the clamping levels.
6. Keep the CRO in X-Y mode and observe the transfer characteristics.
7. Plot the output waveforms and transfer characteristics .

Circuit diagram

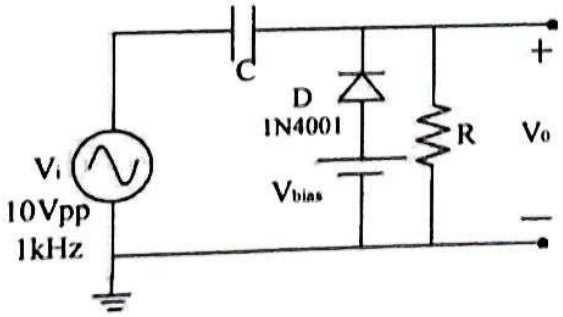
Positive clamper



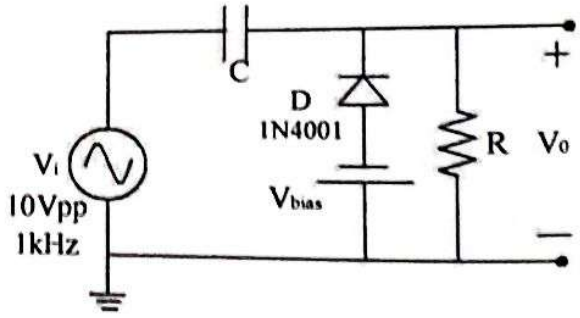
Negative clamper



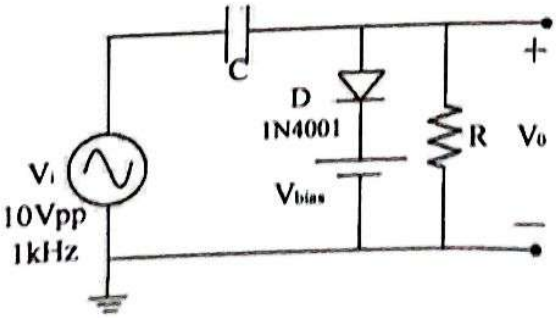
Positive clamper with positive bias



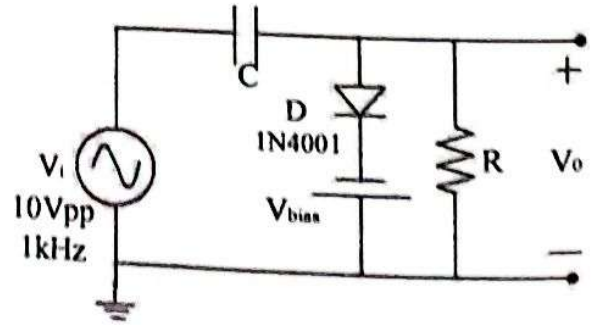
Positive clamper with negative bias



Negative clamper with positive bias



Negative clamper with negative bias



Design:

RC>>T where T is the time period of the input signal.

Here T=1ms.

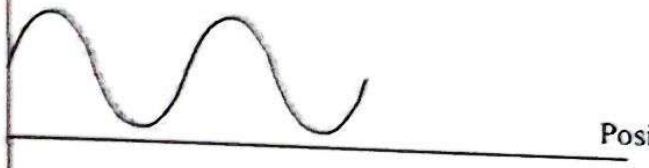
Let RC=10T

Assume C=1μF; then R=10T/C = 10kΩ

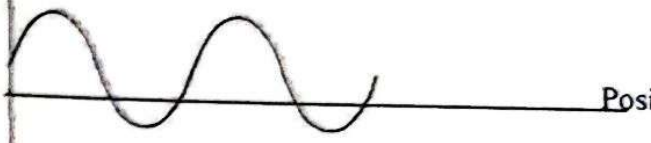
Expected waveforms:

Positive Clamper

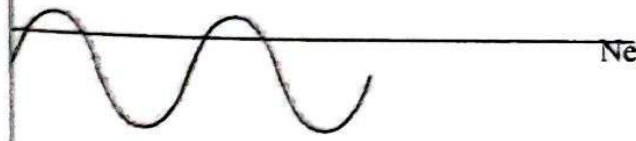
Negative Clamper



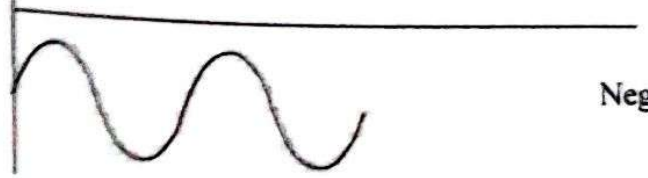
Positive Clamper with positive bias



Positive Clamper with negative bias



Negative Clamper with positive bias



Negative Clamper with negative bias

Result:

Designed and set up various clippers and clamping circuits and observed the output waveforms

EXPERIMENT 16

MULTIVIBRATORS

I.ASTABLE MULTIVIBRATOR

Aim:

To design and set up an astable multivibrator using transistors ,study its performance and observe the waveform

Equipments and components required:

Transistors ,resistors ,capacitors ,breadboard,dc supply,multimeter and CRO.

Theory:

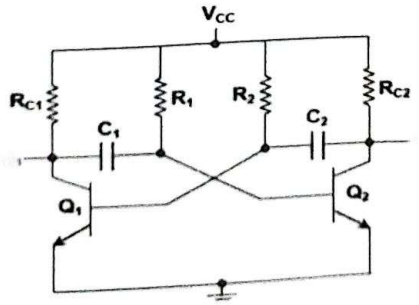
Astable multivibrator is also called free running oscillator .It does not have stable state .Astable circuit switches back and forth between two quasi stable states. depending upon the charging and discharging periods of two timing capacitors. Time duration in which Q2 remains in ON state is given by T2=0.69R2C2 and time duration in which Q2 remains in ON state is given by T2=0.69R1C1.If R1=R2=R and C1=C2=C,Then T1=T2=T=0.69RC.Now the duty cycle is ½ and the time period of the output T=T1+T2=1.38RC.

Procedure:

1.Verify the condition of all components ,devices and probs.

2.Set up the circuit and observe the collector and base waveforms of both transistors.

Circuit diagram



Design

Output requirement-A square wave of amplitude 9V ,frequency 1kHz and duty cycle =1/3.Choose transistor BC107.

Take VCC=9V

Design of RC1 and RC2 RC1=VCC-VCE1 sat/IC1=(9-0.30/2mA = 4.35k.Use 4.7k.

RC1=RC2=4.7k.

Design of R1 and R2

$I_{Bmin}=I_C/h_{FE}$ = 20μA.

$R_1=(V_{CC}-V_{BE\ sat})/I_B$=83k .Use 82k.Take R1=R2.

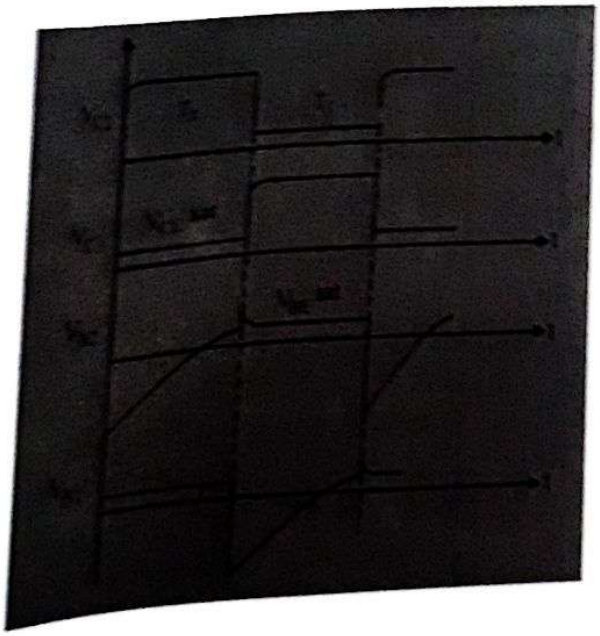
Design of C1 and C2

T=T1+T2=1ms and duty cycle =T1/(T1+T2)=1/3.

T1=0.33ms=0.69R1C1.Then C1=0.006μF.Use 0.01μF.

T2=0.66ms=0.69R2C2.Then c2=0.022μF.

Waveforms



Result: Design and set up an astable multivibrator has been done.

EXPERIMENT 20

RC INTEGRATING AND DIFFERENTIATING CIRCUITS

RC INTEGRATOR

Aim :

To design and construct RC integrator circuit and study its pulse response.

Components required:

Capacito,. Resistor ,Function generator,. Oscilloscope ,Multimeter ,Breadboard .

Theory:

An RC integrator circuit is a wave shaping circuit. It constitutes a resistor in series and a capacitor in parallel to the output. As the name suggests it does the mathematical operation 'integration' on the input signal. The time constant RC of the circuit is very large in comparison with the time period of the input signal. Under this condition the voltage drop across C will be very small in comparison with the voltage drop across R. For satisfactory integration it is necessary that $RC \geq 16T$, where T is time period of the input. When pulse waveform is given at the input, capacitor charges through R and output voltage builds up slowly. Capacitor continues to charge as long as input voltage is present. When input falls to zero, capacitor discharges and output falls to zero slowly. As the value of $RC >> T$, the charging current is almost constant and the output become linear. Hence a square pulse input provides a triangular output.

PROCEDURE

1)Test the components

2) Assemble the circuit on a breadboard

3) Connect the output of a function generator to the input of the differentiator circuit

4) Switch on the function generator and set the output at 5V, 1KHz pulse

5) Connect the output of the differentiator to an oscilloscope

6) Observe the output waveform and its amplitude for the following condition by varying the time period (T) of the input

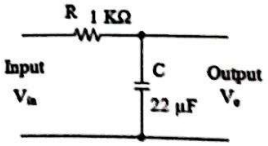
7) Plot all the input and output waveforms

DESIGN

Let the input be a square pulse of 1 KHz Then T = 1ms For an integrator RC ≥ 16T To avoid loading select R as 10 times the output impedance of the function generator If it is 100 Ω, then R = 1KΩ Substituting the value of R in the expression, RC = 16T, we get C = 16μF Therefore C should be greater than 16μF. Hence choose C = 22μF

OBSERVATIONS To observe the response of the circuit, you can change either the RC value of the circuit or T of the input. Here T of the input is changed. 1. f = 1 KHz, T = = 1ms, RC = 22ms (RC >> T) 11 2. f = 100 KHz, T = = 10ms, RC = 22ms (RC > T) 3. f = 10 Hz, T = = 100ms, RC = 22ms (RC < T) 4. f = 1 Hz, T = = 1s, RC = 22ms (RC << T):

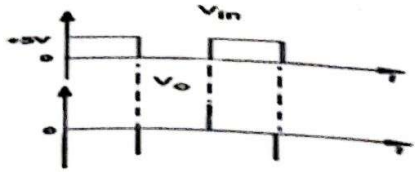
Circuit diagram



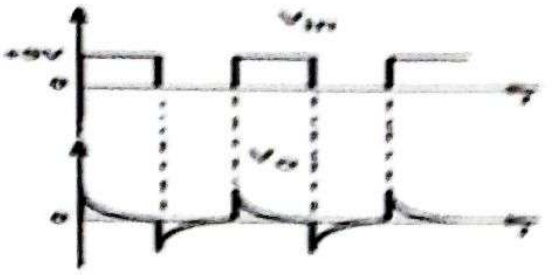
Observations

To observe the response of the circuit, you can change either the RC value of the circuit or T of the input. Here T of the input is changed.

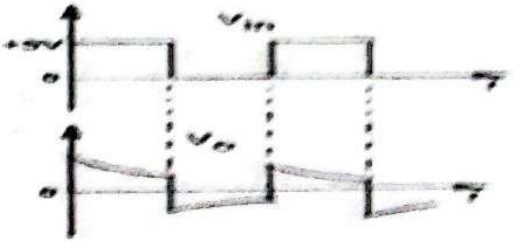
1. f = 1 KHz, T = = 1ms, RC = 22ms (RC >> T)



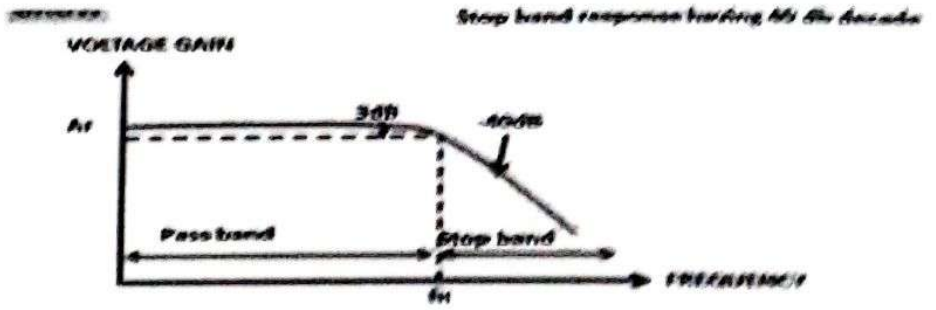
2. f = 100 KHz, T = = 0.01ms, RC = 1μs (RC < T)



3. f = 1 MHz, T = = 1μs, RC = 1μs (RC ≥ T)



Frequency response:



Result: Design and construct RC integrator circuit has been done.

RC DIFFERENTIATOR

Aim:

To design and construct RC differentiator circuit and study its pulse response.

Components required:

Capacitor, Resistor ,Function generator,. Oscilloscope ,Multimeter ,Breadboard

Theory:

RC differentiator will simply act as a simple high pass filter (HPF) with a cut-off or corner frequency that corresponds to the RC time constant (tau, τ) of the series network.

Thus when fed with a pure sine wave an RC differentiator circuit acts as a simple passive high pass filter due to the standard capacitive reactance formula of $X_C = 1/(2\pi fC)$.

RC time constant, $\tau = RC$.

PROCEDURE

1) Test the components

2) Assemble the circuit on a breadboard

3) Connect the output of a function generator to the input of the differentiator circuit

4) Switch on the function generator and set the output at 5V, 1KHz pulse

5) Connect the output of the differentiator to an oscilloscope

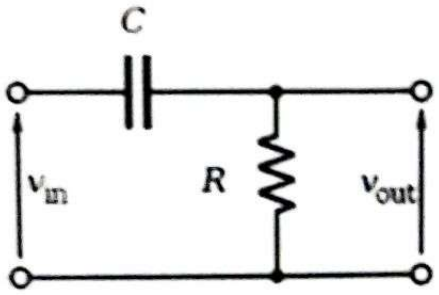
6) Observe the output waveform and its amplitude for the following condition by varying the time period (T) of the input.

7) Plot all the input and output waveforms.

Design:

Let the input be a square pulse of 1 KHz Then T = 1ms For an integrator $RC \geq 16T$ To avoid loading select R as 10 times the output impedance of the function generator If it is 100 Ω, then R = 1KΩ Substituting the value of R in the expression, RC = 16T, we get C = 16μF Therefore C should be greater than 16μF. Hence choose C = 22μF.

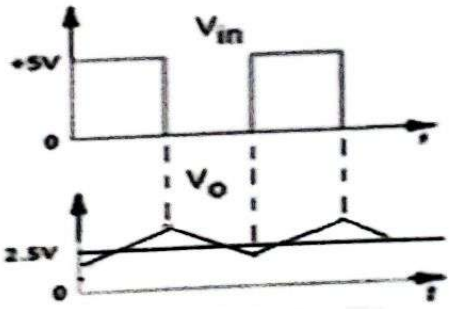
Circuit diagram:



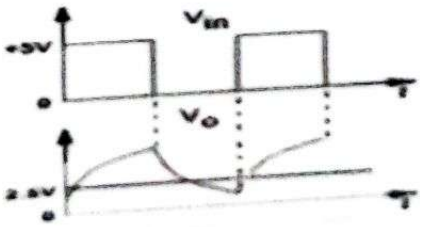
Observations

To observe the response of the circuit, you can change either the RC value of the circuit or T of the input. Here T of the input is changed.

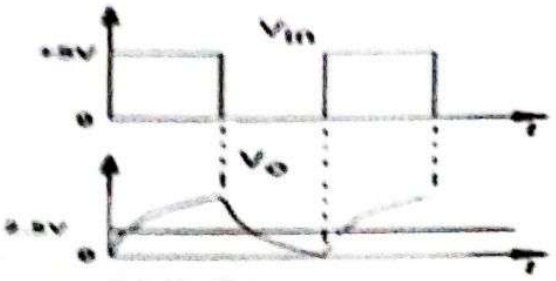
1. f = 1 KHz, T = = 1ms, RC = 22ms (RC >> T)



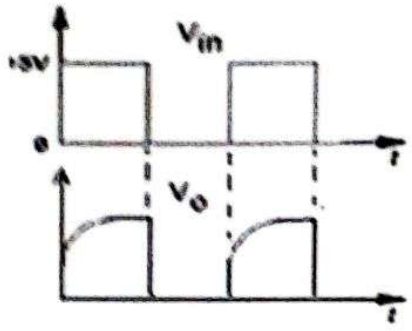
2. f = 100 KHz, T = = 10ms, RC = 22ms (RC > T)



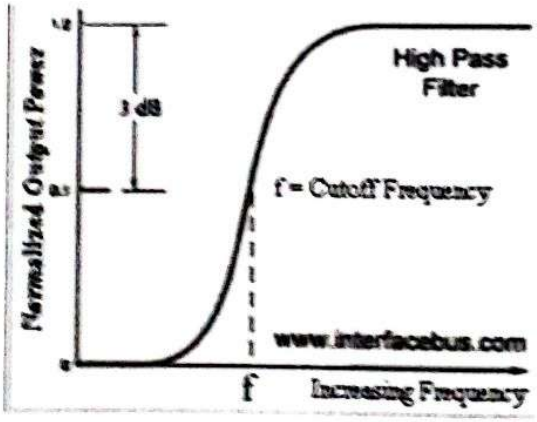
3. f = 10 Hz, T = = 100ms, RC = 22ms (RC < T)



4. f = 1 Hz, T = = 1s, RC = 22ms (RC << T)



Frequency response



Result: Design and construct RC differentiator circuit has been done.