		CS203-DETAILED-SCHEME	Total Pages:

Reg No.: Name:

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
THIRD SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code: CS203

Course Name: **SWITCHING THEORY AND LOGIC DESIGN**

Max. Marks: **100** Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

1 **Find the 9's and 10's complement of $(24579.12)_{10}$.** (3)

(9's complement -1.5 marks 10's complement -1.5 marks)

9's complement

99999.99-

24579.12

75420.87

10's complement

9's complement + 1=75420.88

By definition, 10's complement is 10^n- N and 9's complement is 10^n - 10^-m - N where n and m are number of digits in the integer and fractional part and N is the given number.

Thus 10's complement is 100000-25479.12 and 9's complement is 100000-1/100-24579.12

2 **Convert $(455)_{10}$ to base-4,8 and 16.** (3)

(1 mark each for each conversion)

Number 455 (base 10) is in base 4: ***13013***

Number 455 (base 10) is in base 8: ***707.***

Number 455 (base 10) is in base 16: ***1c7.***

3 **Express the following functions as product of max-terms:** (3)

a) F(X,Y,Z) = Y' +XZ' + XY'Z' b) F(A,B,C) = C (A+B') (A' +B' + C')

!Expects an algebraic manipulation. However marks can be given if the terms are properly exapned to minterms (in case of (a)) and max terms (in case of (b)) before arriving at the final result.

(1.5 marks, 1.5 marks)

a) **F(X,Y,Z) = Y' +XZ' + XY'Z'**

=000+001+100+101+110

=∑ m(0,1,4,5,6)

=Π_M (2,37)=(X+Y'+Z)(X+Y'+Z')(X'+Y'+Z')

b) **F(A,B,C) = C (A+B') (A' +B' + C')**

=(0+0+0)(0+1+0)(1+0+0)(1+1+0)(0+1+1)(1+1+1)

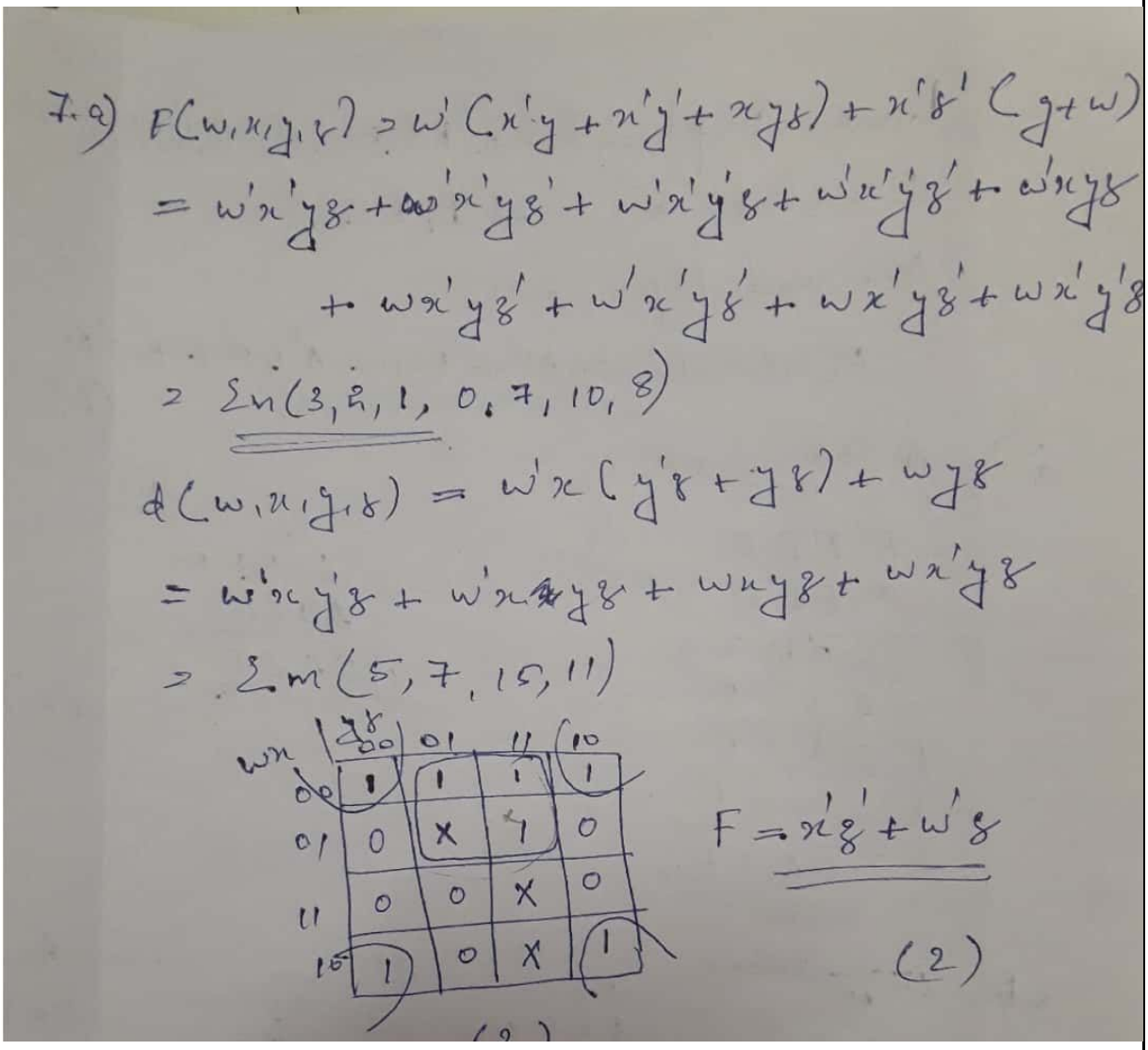
=Π_M (0,2,3,4,6,7)=(A+B+C)(A+B'+C)(A+B'+C')(A'+B+C)(A'+B'+C) (A' +B' + C')

4 **Use Boolean Algebra to show that A'BC'+AB'C'+AB'C+ABC'+ ABC = A+BC'** (3)

(Proof using postulates and theorems)

RHS

		A+BC'=(A+BC')(A+A') *A+A'=1 and A.1=A* *= A.A+A.A'+ABC'+A'BC'* *applying Distributive Law* *=A+ABC'+A'BC'* *A.A=A AND A.A'=0* *=A(B+B')(C+C')+ ABC'+A'BC'* *A+A'=1 and A.1=A* *=ABC+AB'C+ABC'+AB'C'+ABC'+A'BC'* *applying distributive law* *=ABC+AB'C+ABC'+AB'C'+A'BC'* *A+A=A, Commutative Law* *** We can start from LHS and can use boolean postulates and theorems to reach RHS*	
PART B			
Answer any two full questions, each carries 9 marks.			
5		**Simplify F(A,B,C,D)=Σ(1,4,6,7,8,9,10,11,15) using Tabulation method and determine the prime implicants, essential prime implicants and the minimized Boolean expression.** *(Tabulation steps - 5 marks Prime implicants-1 marks essential prime implicant- 2 marks , Minimized Boolean expression-1 marks)* *Essential Prime Implicants:* BCD , A'BD' , B'C'D , AB' *Minimized Boolean expression:* BCD+A'BD'+B'C'D+AB'	(9)
6	**a)**	**Subtract $(9F2C)_{16}$ from $(A96B)_{16}$ using 15's and 16's complement method.** *(Each method- 2 marks.)* Answer :A3F *15's complement of 9F2C is =60D3* *A96B+60D3=10A3E 0A3E+1 = 0A3F or A3F* *16's complement of 9F2C is =60D4* *A96B+60D4=10A3F Answer is 0A3F or A3F*	(4)
	b)	**Subtract 366 from 170 in BCD using 10's complement addition.** *(BCD using 10's complement addition)* *10's complement of 366 : 999-366=633+1=634* *0001 0111 0000+* *0110 0011 0100* *0111 1010 0100* *Here second nibble is >9 so add 0110* *0111 1010 0100 +* *0000 0110 0000* *1000 0000 0100 =804* *No carry takes 10's complement of 804 =999-804=195+1=196* *So answer is -196*	(3)
	c)	**Perform $(417)_8 - (232)_8$ using *8's complement addition*.** *(8's complement addition)* *8's complement of* **232** **7's complement =777-232=545** **8's complement =545+1=546** **$(417)_8 - (232)_8$ =417+546=1165** ***Alternate answer: discard the carry , 165***	(2)

7	a)	**Using K-map simplify the Boolean function F as Sum of Products using the don't care conditions d.** **F(w,x,y,z)=w'(x'y+ x'y' +xyz) + x'z'(y+w) d(w,x,y,z)=w'x(y'z + yz) +wyz** *(K-map grouping – 2 marks simplification-2 marks)*  	(4)
	b)	**Represent the following decimal numbers in signed 2's complement 8-bit numbers: i) +43 ii) –19** *(i) +43 - 1 mark ii) –19 - 2 marks)* *(i) +43 =**0010 1011*** *ii) –19 =* *Binary equivalent of 19 =0001 0011* *1's complement =1110 1100* ***2's complement =1110 1101***	(3)
	c)	**Convert the decimal number 3.248 x 10 4 to IEEE 754 standard single precision floating point binary number.** *(IEEE 754 format- 2 mark Any other valid format-1 mark.)* ***Single Precision frame format (32 bit)***	(2)

Sign (1 bit)	*Exponent (8 bit)*	*Fractional (23 bit)*

$1.11111011100000x2^{14}$ exponent =141

Here,

S=0 (+ve number)

E=10001101

F=11111011100000

0	*10001101*	*11111011100000000000000*

Alternate answer: Fraction F in 23 bits, append zeroes on left side

00000000011111011100000

PART C

Answer all questions, each carries 3 marks.

8 **Differentiate combinational and sequential circuits** (3)

(Min 3 differences- 1 mark each)

Combinational Logic Circuits

Output is a function of the present inputs

Do not have the ability to store data (state)

It does not require any feedback. It simply outputs the input according to the logic designed

Example: Adder

Sequential Logic Circuits

Output is a function of clock, present inputs and the previous states of the system.

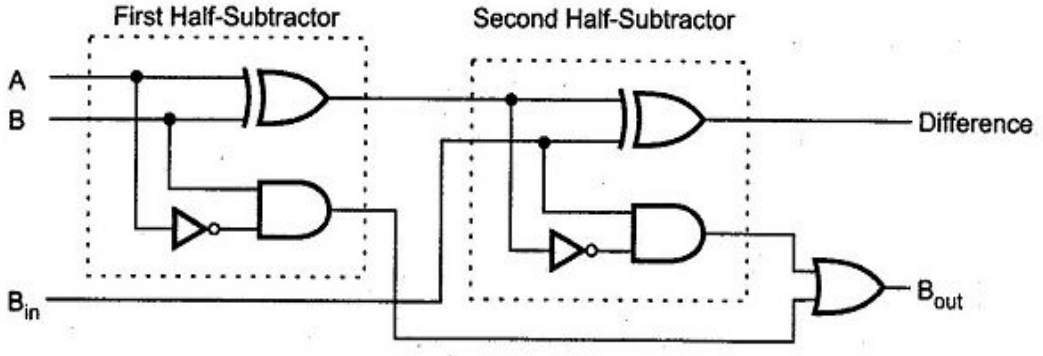
Have memory to store the present states that is sent as control input (enable) for the next operation.

It involves feedback from output to input that is stored in the memory for the next operation.

Example: Counter

9 **Given the block diagram of half-subtractor, imp lement a full-subtractor using half-subtractors.** (3)

(2 half subtractors and OR gate- 3 mark)



10 **Write the excitation tables of SR, JK and T flip-flops.** (3)

(Excitation tables of SR, JK and T flip-flops- 1 mark each)

Excitation table of SR FF

Qn (PS)	*Qn+1 (NS)*	*S*	*R*
0	*0*	*0*	*X*

			0	*1*	*1*	*0*
			1	*0*	*0*	*1*
			1	*1*	*X*	*0*

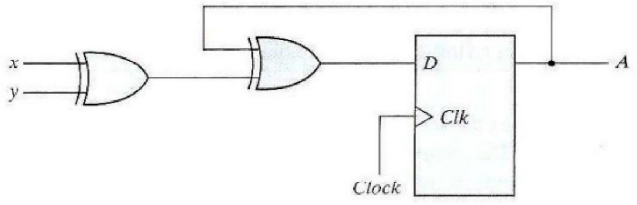
Excitation table of JK FF

Qn (PS)	*Qn+1 (NS)*	*J*	*K*
0	*0*	*0*	*X*
0	*1*	*1*	*X*
1	*0*	*X*	*1*
1	*1*	*X*	*0*

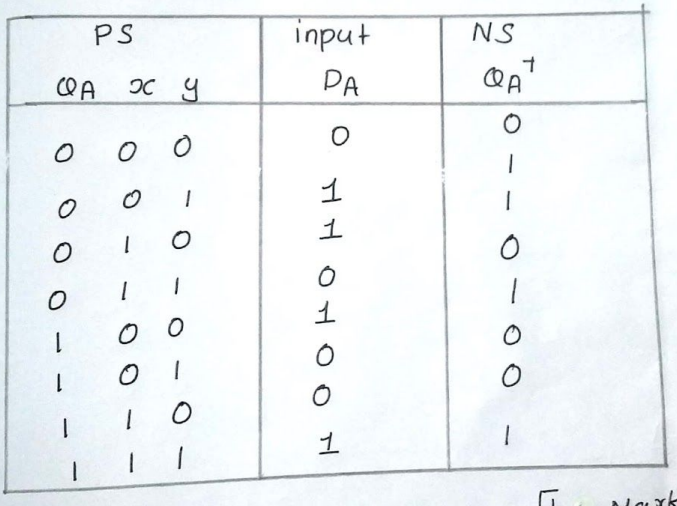
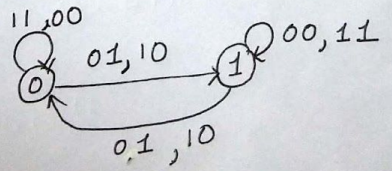
Excitation table of T FF

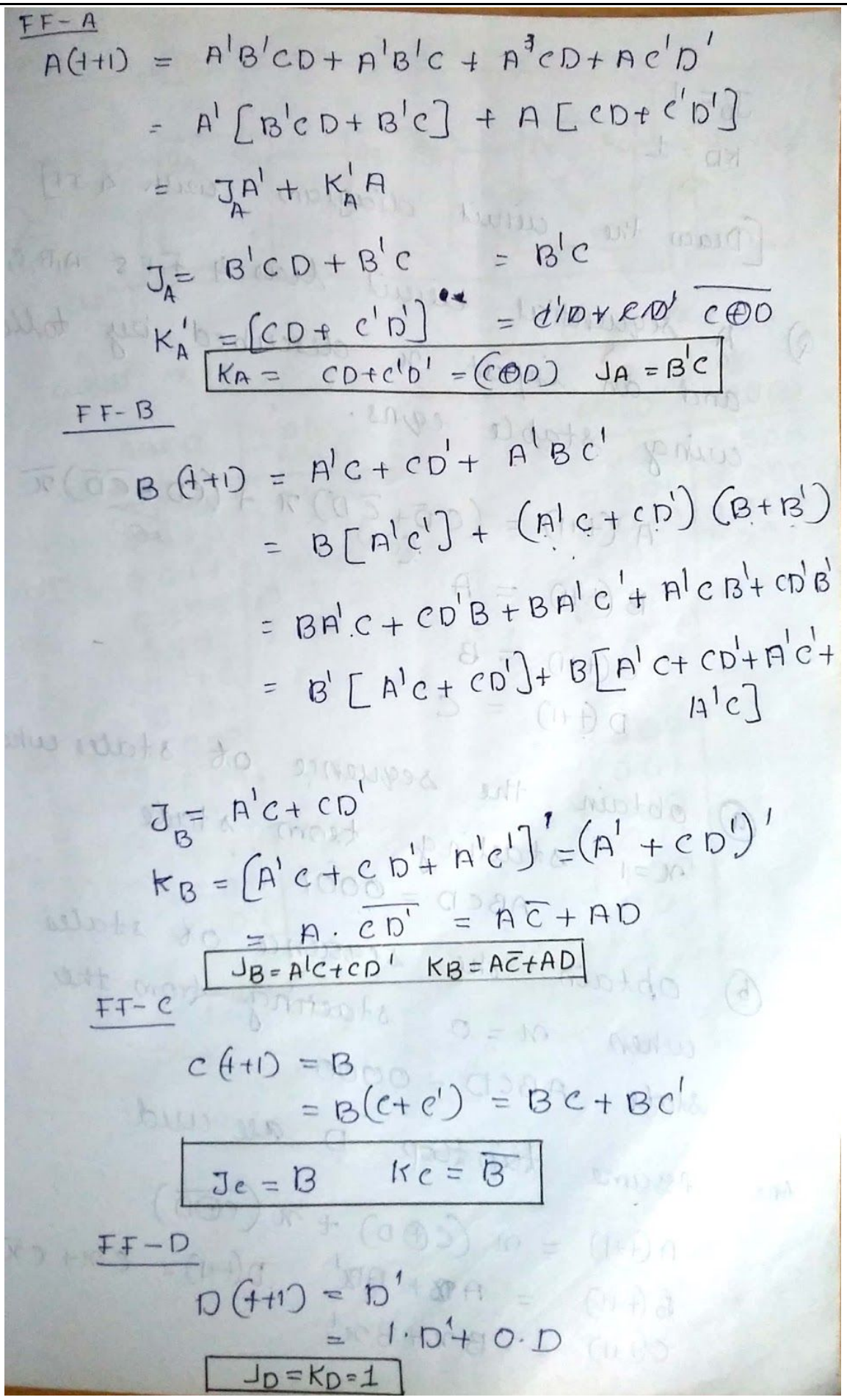
Qn (PS)	*Qn+1 (NS)*	*T*
0	*0*	*0*
0	*1*	*1*
1	*0*	*1*
1	*1*	*0*

11		**Given below is a sequential circuit using D flip-flop. Write the state table and draw a state diagram.**	(3)



(State table – 2 mark State diagram- 1 mark)

		Step 1 : Find out input Equation $D_A = x \oplus y \oplus A$ [2 Mark] Step 2 : State Table Here $Q_A = A$ Q_A^+ is NS.  [1 Mark] Step 3 : State Diagram  	
		PART D	
		Answer any two full questions, each carries 9 marks.	
12	**a)**	**Design a sequential circuit with JK Flip flops to satisfy the following state equation. A(t+1)=A'B'CD + A'B'C + ACD + AC'D' B(t+1)= A'C + CD' + A'BC' C(t+1)= B D(t+1)=D'** *(Full design – 5 marks)*	(5)



FF-A

$A(t+1) = A'B'CD + A'B'C + A'CD + AC'D'$

$= A'[B'CD + B'C] + A[CD + C'D']$

$= J_A A' + K_A' A$

$J_A = B'CD + B'C = B'C$

$K_A' = [CD + C'D']' = C'D + CD'$ $\overline{C \oplus D}$

$K_A = CD + C'D' = (C \oplus D)$ $J_A = B'C$

FF-B

$B(t+1) = A'C + CD' + A'BC'$

$= B[A'C'] + (A'C + CD')(B + B')$

$= BA'C + CD'B + BA'C' + A'CB' + CD'B'$

$= B'[A'C + CD'] + B[A'C + CD' + A'C' + A'C]$

$J_B = A'C + CD'$

$K_B = [A'C + CD' + A'C']' = (A' + CD')'$

$= A \cdot \overline{CD'} = A\bar{C} + AD$

$J_B = A'C + CD'$ $K_B = A\bar{C} + AD$

FF-C

$C(t+1) = B$

$= B(C + C') = BC + BC'$

$J_C = B$ $K_C = \bar{B}$

FF-D

$D(t+1) = D'$

$= 1 \cdot D' + 0 \cdot D$

$J_D = K_D = 1$

Draw the Circuit diagram using 4 FF based on above equations

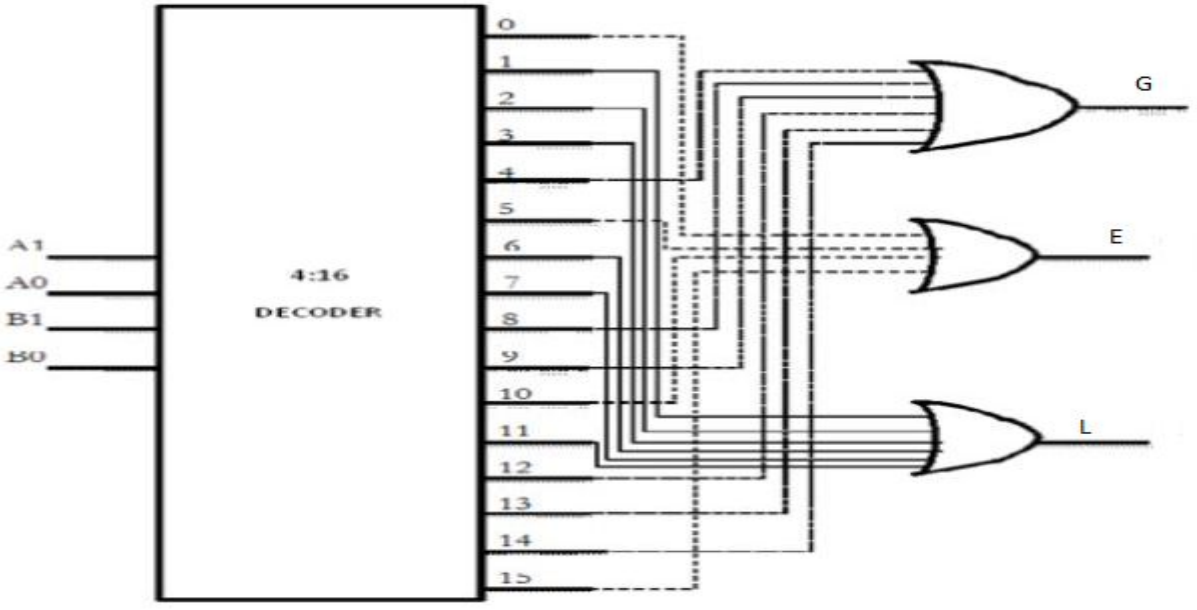
	b)	**Design and implement a decoder that decodes BCD digits (0000 to 1001).** *(Design- 2 marks Implementation- 2 marks)* *Since implementation method is not mentioned in the question, marks can be awarded for both BCD to seven segment display or BCD to decimal decoder*	(4)
13	**a)**	**Design and implement a 2-bit magnitude comparator using 4X16 decoder.** *(Design – 3 marks Implementation -2 marks.)* 1) Truth Table:	(5)

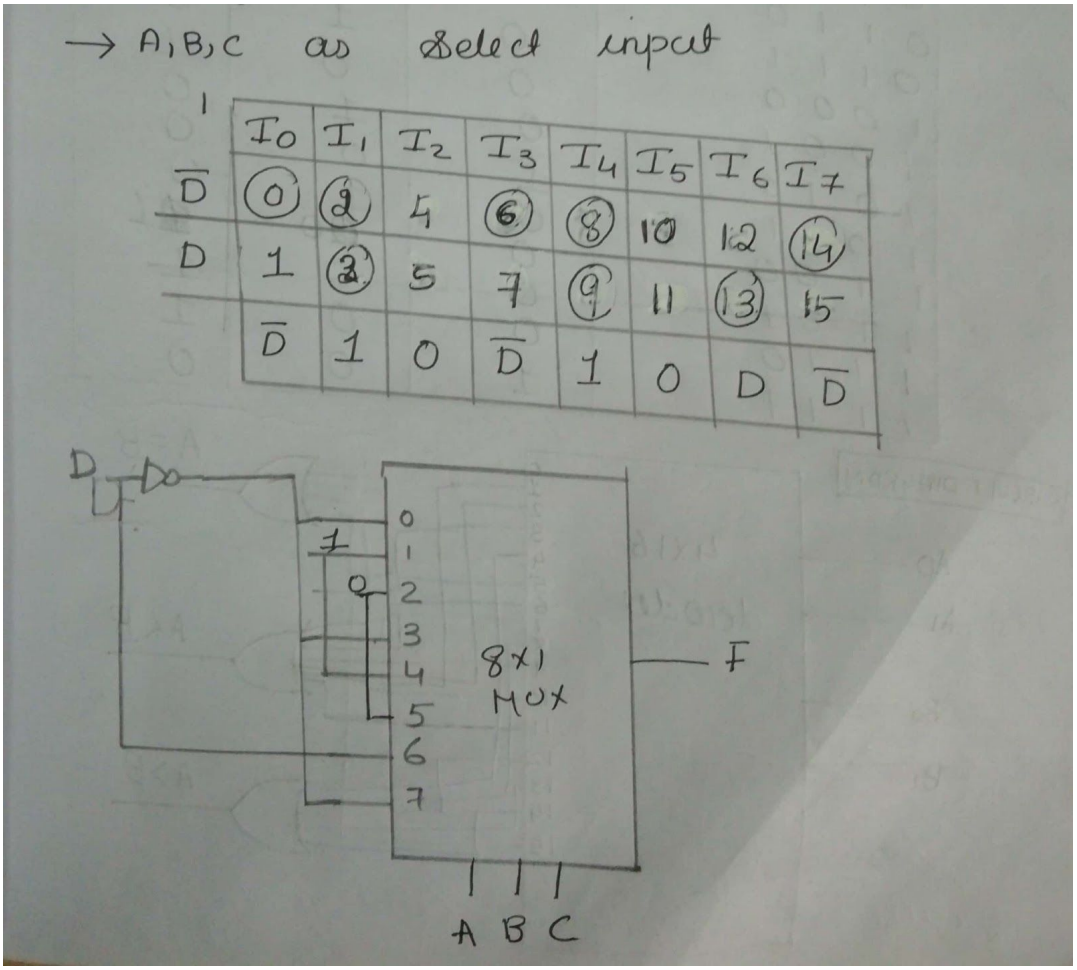
Inputs				Outputs		
A		B		G(A>B)	E(A=B)	L(A<B)
A1	A0	B1	B0			
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

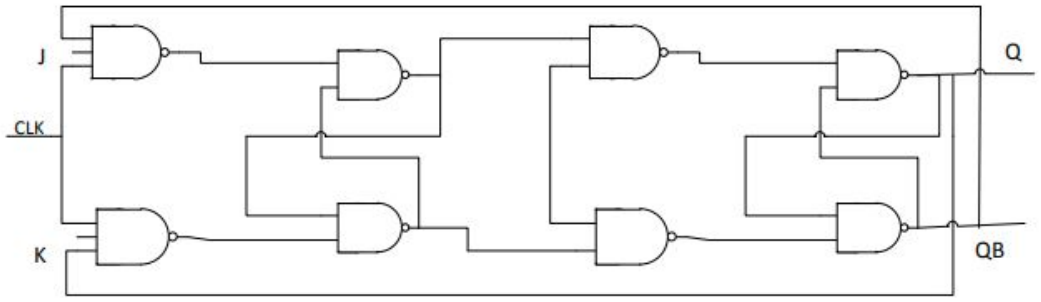
G=Σm(4,8,9,12,13,14)

E=Σm(0,5,10,15)

L=Σm(1,2,3,6,7,11)



	b)	**Implement f(A,B,C,D)= Σ(0,2,3,6,8,9,13,14) using 8 x 1 MUX .** *(Design using 8 x 1 MUX -4 marks)* 	(4)
14		**What is race around condition? Why does it occur? Discuss how master-slave flip-flop eliminates it.** *(Race around condition-2 marks Reason for Occurrence- 2 marks. Master-slave flip-flop working- 3 marks Diagram – 2 marks .)* *For a given clock pulse, the output will oscillate between '0' & '1' when both J & K are high. The condition is referred to as "race around".* *The race around can be avoided* *1) if the width of the clock pulse (T) is less than the propagation delay.* *2) Edge triggering* *3) Master - Slave FF* ***Master Slave Flip Flop:** This is cascade of two JK flip flops with a feedback from output to input. The clock pulses for the two stages are compliments of each. So when first stage is active, second is inactive & vice versa. The First one changes as per the inputs applied. When the clock goes low, the second is enabled and first one is disabled. The Second stage follows the first, hence the name master-slave.*	(9)

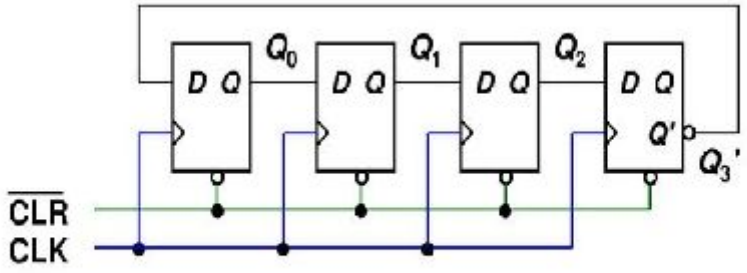


PART E

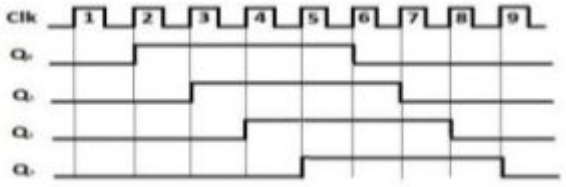
Answer any four full questions, each carries 10 marks.

15 a) **Draw the logic diagram of a 4-bit Johnson counter and explain the working with a timing diagram.** (8)

(Logic diagram of a 4-bit Johnson counter -3 marks Working- 2 marks Timing diagram- 3 marks)



Clock	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

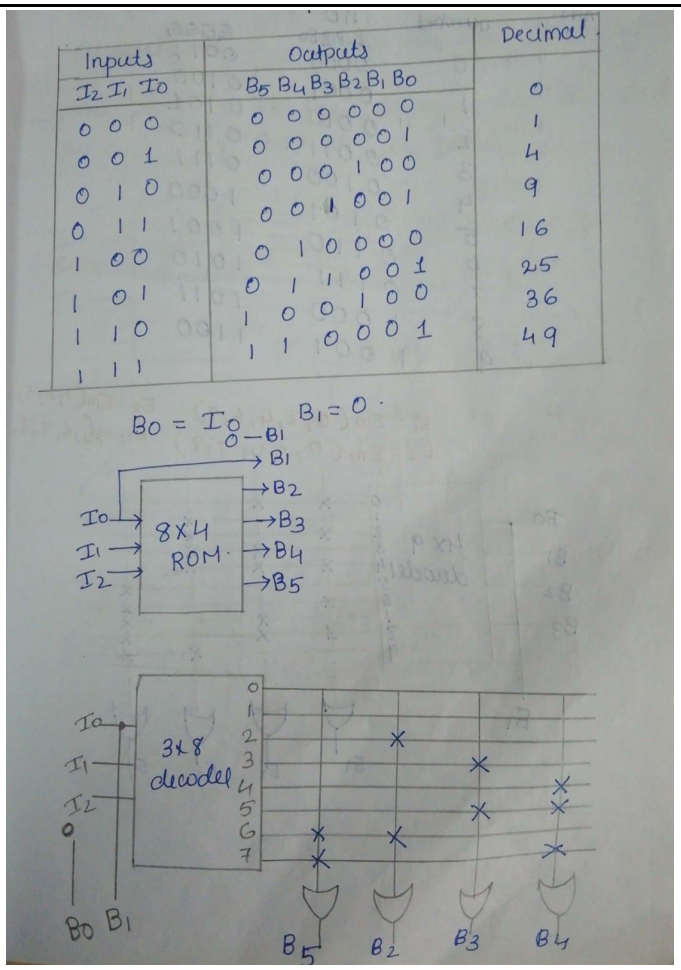


b) **Compare Ring counter and Johnson counter.** (2)

(Any 2 differences- 1 mark each)

Ring counter	Johnson counter
Output of last flip flop (Q) is connected to the input of the first flip flop	*Output of last flip flop (Q') is connected to the input of first flip flop.*

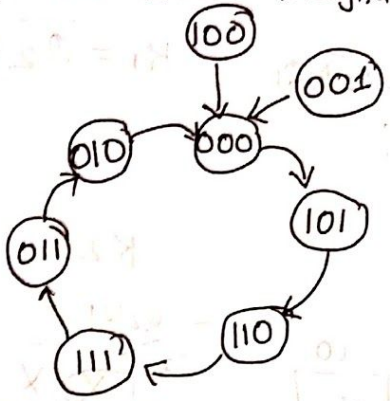
		If 'n' is the number of flip flops that is used in ring counter,number of possible states are also 'n'.That means the number of states is equal to the number of flip flops used.	*If 'n' is the number of flip flop used,then the total number of states used is '2n'.*
		Decoding is easy in ring counter as the number of states is equal to number of flip flops	*Decoding circuit is complex as compared to ring counter.*
16	**a)**	**Explain the working of 3-bit Universal Shift Register.** *(Working of 3-bit Universal Shift Register-5 marks. Diagram- 3 marks)* *	(8)
	b)	**Give 2 applications of shift register.** *(Any 2 applications of shift register- 1 mark each)* 1. *Time Delays* 2. *Serial /Parallel data conversion* 3. *Ring counter* 4. *Johnson Counter* 5. *Universal asynchronous receiver transmitter (UART)* 6. *Adder*	(2)
17	**a)**	**Design a combinational circuit using ROM that accepts a 3-bit binary number and generates output equal to the square of the input number. Use decoder of suitable size to implement ROM.** *(Truth table – 3 marks Rom using decoder – 4 marks)*	(7)

			
	b)	**What size of ROM would it take to implement** **i. A BCD adder/subtractor with a control input to select between the addition and subtraction.** **ii. A binary multiplier that multiplies two 4-bit numbers.** **iii. Dual 4-line to 1-line multiplexers with common selection inputs.** *(1 mark each)* *i) This circuit has 8 data inputs(two BCD Number), a control input and a carry input, so the ROM must have 2^{10} words. It also has 4 data outputs(BCD number) and a carry output, so it must have 5 bits per word* *ii)This circuit has two 4 bit inputs and 8 bit outputs, so the ROM must have 2^{8} words with 8 bits each.* *iii)This circuit has 10 bit inputs and 4 bit outputs, so the ROM must have 2^{10} words with 4 bits each.*	(3)

18	**a)**	**Design a synchronous counter using JK flip-flops to count the sequence 0,5,6,7,3,2 and then repeats.** *(State table – 2 marks Design using K-map- 6 marks Diagram- 2 marks)*	(10)

Step 1 : no of FF : 3

Step 2 : The state Diagram

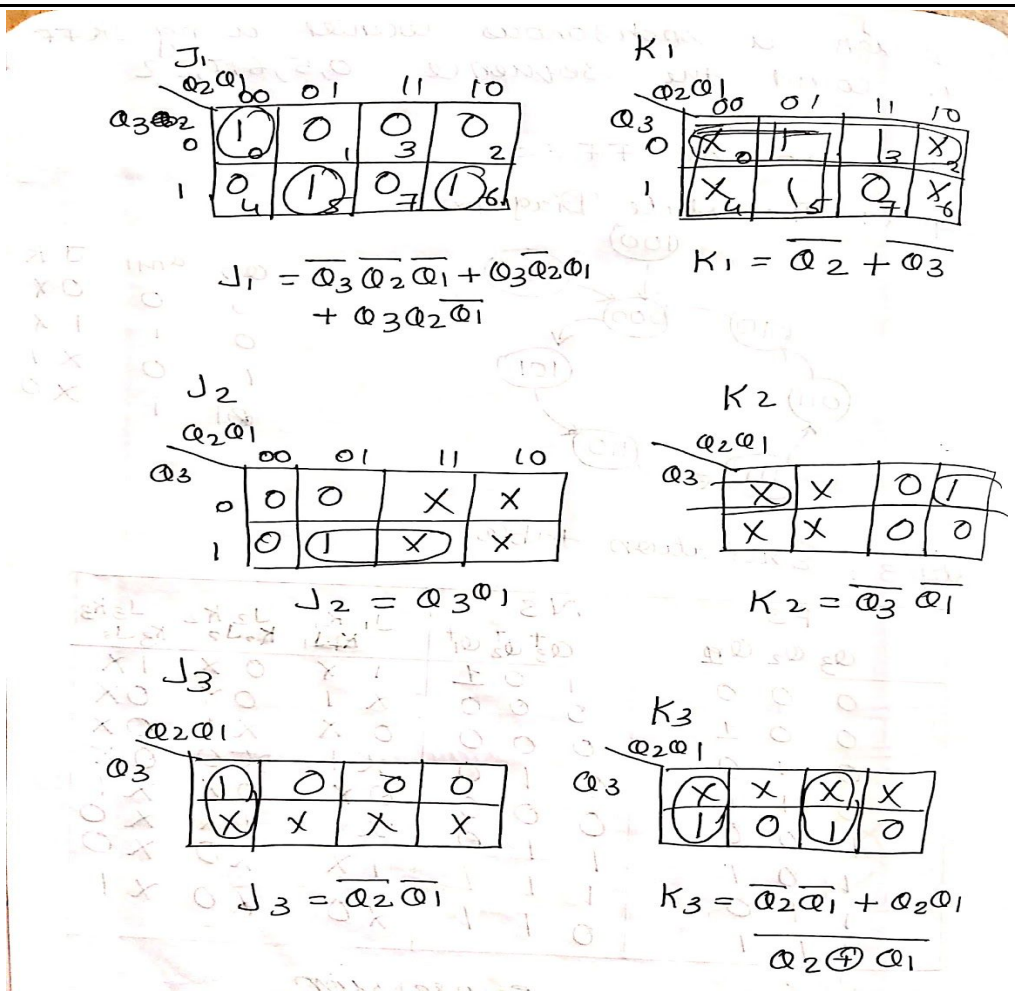


Q_n	Q_{n+1}	J K
0	0	0 X
0	1	1 X
1	0	X 1
0	1	X 0

Step 3 : Excitation table

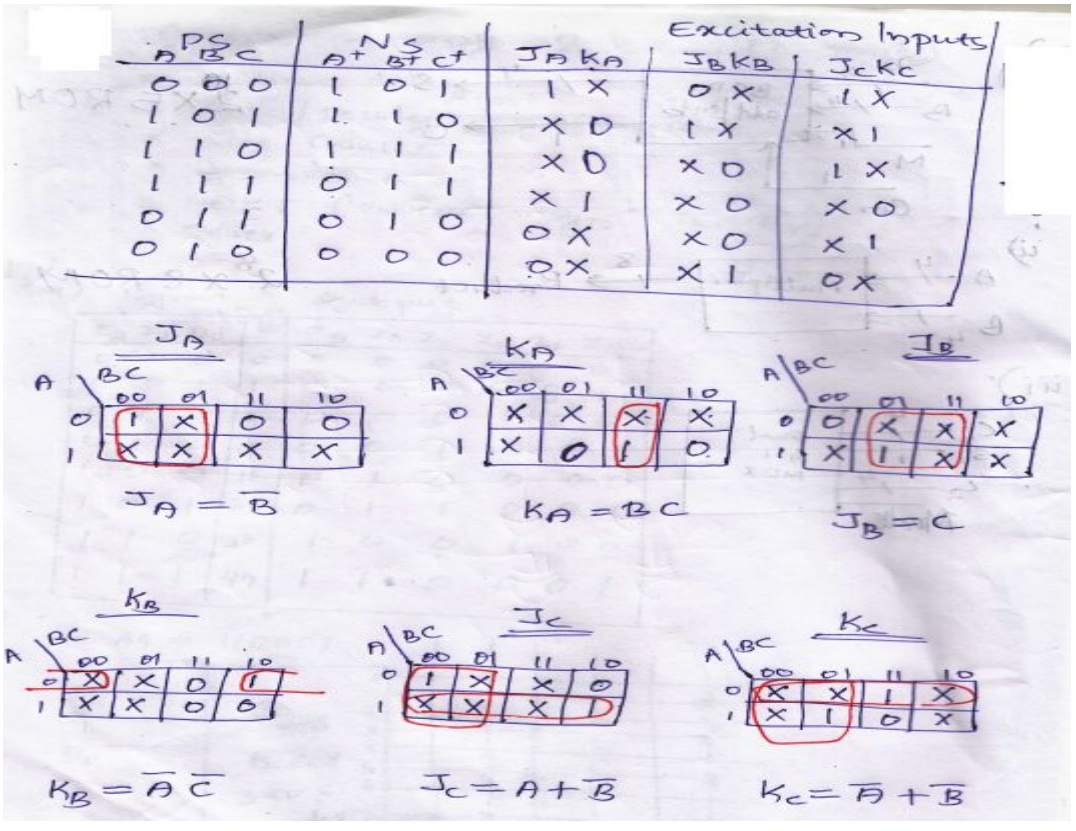
PS $Q_3\ Q_2\ Q_1$	NS $Q_3^+\ Q_2^+\ Q_1^+$	$J_1\ K_1$	$J_2\ K_2$	$J_3\ K_3$
0 0 0	1 0 1	1 X	0 X	1 X
0 0 1	0 0 0	X 1	0 X	0 X
0 1 0	0 0 0	0 X	X 1	0 X
0 1 1	0 1 0	X 1	X 0	0 X
1 0 0	0 0 0	0 X	0 X	X 1
1 0 1	1 1 0	X 1	1 X	X 0
1 1 0	1 1 1	1 X	X 0	X 0
1 1 1	0 1 1	X 0	X 0	X 1

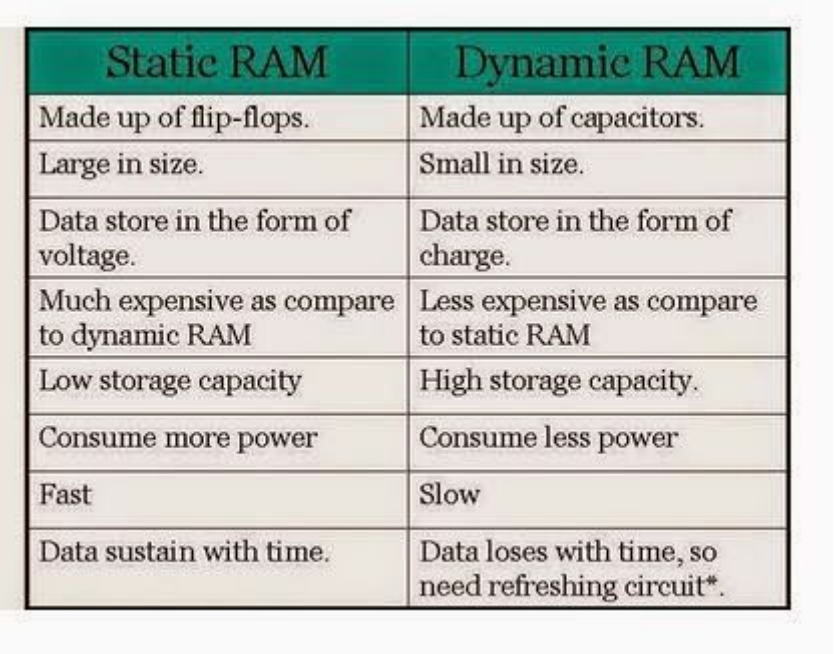
Step 4 : Minimal Expression



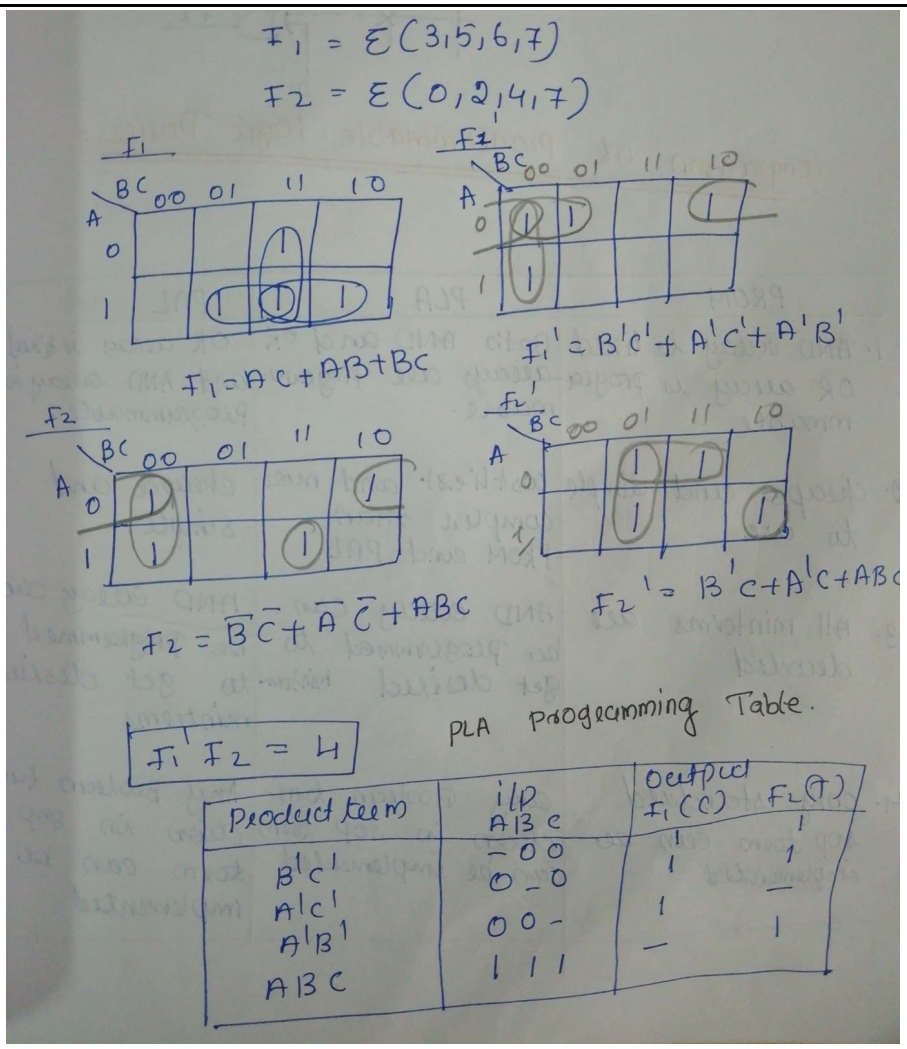
Draw the circuit diagram using this equation

**** It is not specified as a self starting counter. So it can be designed with the specified states only*

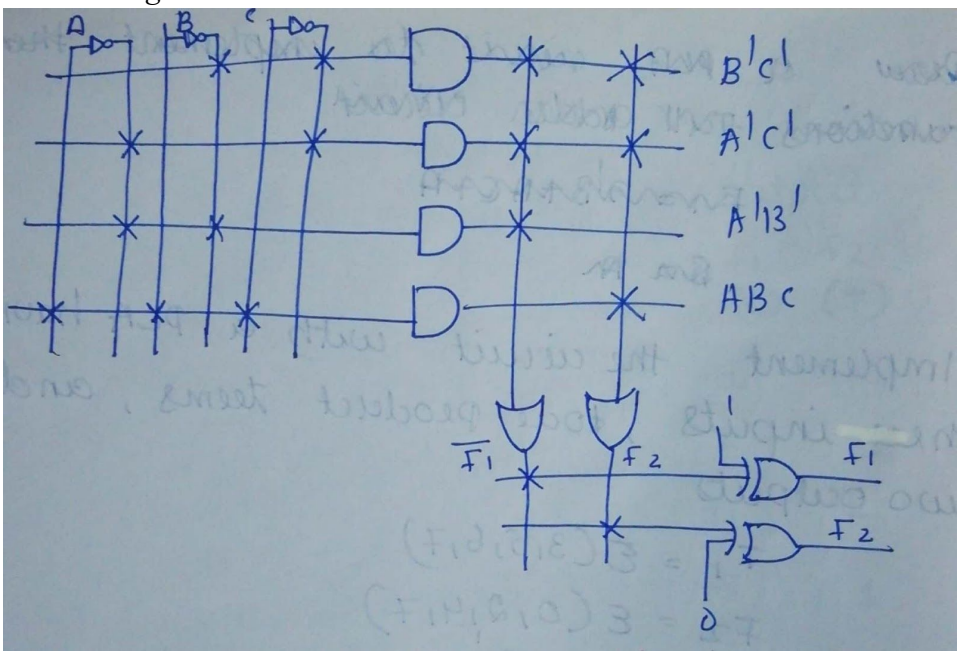


19	**a)**	**Compare static and dynamic RAMs.** *(3 differences- 1 mark each)* 	(3)
	b)	**A combinational circuit is defined by the functions: F1(A,B,C)=Σ(3,5,6,7) F2= Σ(0,2,4,7) .Implement the circuit with a PLA having 3 inputs, four product terms and 2 outputs.** *(Implementation of the circuit with a PLA- 3 marks)*	(7)

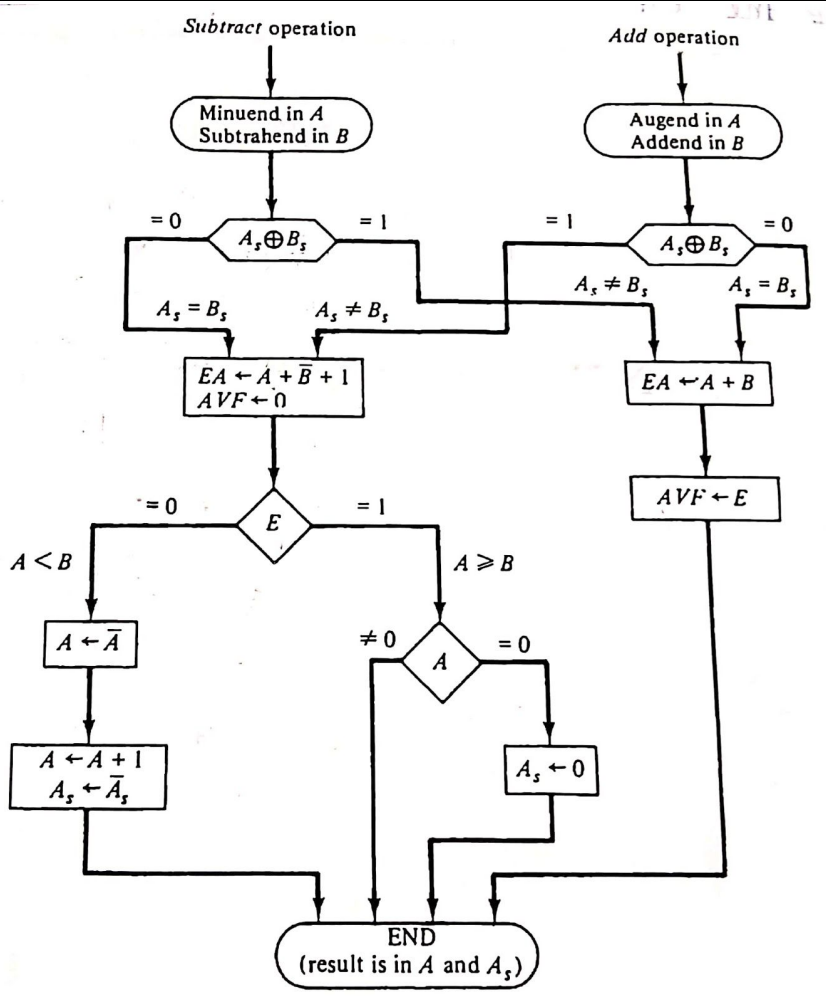
Static RAM	Dynamic RAM
Made up of flip-flops.	Made up of capacitors.
Large in size.	Small in size.
Data store in the form of voltage.	Data store in the form of charge.
Much expensive as compare to dynamic RAM	Less expensive as compare to static RAM
Low storage capacity	High storage capacity.
Consume more power	Consume less power
Fast	Slow
Data sustain with time.	Data loses with time, so need refreshing circuit*.



Circuit Diagram



20		**With the help of a flowchart explain the addition/subtraction of binary numbers in sign magnitude form.** *(Addition-5 marks Subtraction- 5 marks.(Flow chart/Algorithm)*	(10)


Subtract operation
Minuend in A
Subtrahend in B
= 0
$A_s \oplus B_s$
= 1
$A_s = B_s$
$A_s \neq B_s$
$EA \leftarrow A + \bar{B} + 1$
$AVF \leftarrow 0$
= 0
E
= 1
$A < B$
$A \geqslant B$
$A \leftarrow \bar{A}$
$A \leftarrow A + 1$
$A_s \leftarrow \bar{A}_s$
$\neq 0$
A
= 0
$A_s \leftarrow 0$
END
(result is in A and A_s)
Add operation
Augend in A
Addend in B
= 1
$A_s \oplus B_s$
= 0
$A_s \neq B_s$
$A_s = B_s$
$EA \leftarrow A + B$
$AVF \leftarrow E$

****