CH32V103 Data sheet

V1.0

Overview

The 32-bit RISC processor RISC-V3A is based on the RISC-V open source instruction set design, and its system architecture achieves the best balance of low-cost, low power consumption and functional application of the hardware platform.

CH32V1 series general-purpose microcontrollers use this processor as the core and mount a wealth of peripheral interface and function modules, including clock security mechanism, multi-level power management, general-purpose DMA controller, multi-channel 12-bit ADC conversion module, multi-channel Touch key capacitance detection (TKey), advanced and general timers, USB2.0 host controller and device controller, multi-channel I2C/USART/SPI interface, etc. The microcontroller is equipped with a complete hardware and software platform and debugging interface tools, which can meet various needs in the industrial, medical, consumer and other markets.

Product Features

- **Core:**
  - Support RV32IMAC instruction set combination, hardware multiplication and division
  - Fast programmable interrupt controller + hardware on-site preservation and recovery
  - Static branch prediction and conflict handling mechanism
  - Low-power two-stage pipeline
  - Up to 80MHz system frequency
- **Memory:**
  - 20KB volatile data storage area SRAM
  - 64KB user application storage area CodeFlash
  - 3.75KB system boot program storage area BootLoader
  - 128B system non-volatile configuration information storage area
  - 128B user-defined information storage area
- **Power management and low power consumption:**
  - Power supply range: 2.7V ~ 5.5V, GPIO synchronous power supply voltage
  - Multiple low-power modes: sleep/stop/standby

  -V_{BAT} Power supply independently powers RTC and backup registers
- **System clock, reset**
  - Built-in factory-adjusted 8MHz RC oscillator
  - Built-in 40KHz RC oscillator
  - Built-in PLL, optional CPU clock up to 80MHz
  - External support 4MHz ~ 16MHz high speed oscillator
  - External support for 32.768KHz low speed oscillator
  - Power-on/power-off reset (POR/PDR), programmable voltage monitor (PVD)
- **Real-time clock RTC:** 32-bit independent timer
- **General DMA controller**
  - Provides 7 channels
  - Support peripherals and memory, memory and memory
  - Support ring buffer management
  - Support peripherals: TIM/ADC/USART/I2C/SPI
- **12-bit ADC**
  - Conversion range: 0 ~ V_{DDA} , The fastest 1us conversion is completed
  - 16 external signal channels + 2 internal signal channels
  - On-chip temperature sensor
- **16-channel Touch-Key channel detection**
- **7 timers**
  - 1 16-bit advanced timer, including general-purpose timer function, with dead zone control and emergency braking, providing PWM for motor control
  - Three 16-bit general-purpose timers, providing up to four channels for input capture/output comparison/PWM/pulse count and incremental encoder input
  - 2 watchdog timers (independent and window type)
  - System time timer: 64-bit self-incrementing counter
- **8 standard communication interfaces** :
  - USB2.0 host/device interface (full speed and low speed)
  - 2 I2C interfaces (support SMBus/PMBus)
  - 3 USART interfaces (support ISO7816 interface, LIN, IrDA interface and modem control)
  - 2 SPI interfaces (support Master and Slave mode)
- **Fast GPIO port**
  - Up to 51 I/O ports, and can be mapped to 16 external interrupts
- **Security features:** CRC calculation unit, 96-bit chip unique ID
- **Debug mode:** Serial 2-wire debug interface
- **Package form**
  - LQFP64M (LQFP64-10*10)
  - LQFP48 (LQFP48-7*7)
  - QFN48X7 (QFN48-7*7)

Chapter 1 Specification Information

CH32V1 series MCU products use RISC-V3A processor and architecture, and support RV32IMAC open source instruction. The maximum operating frequency is 80MHz, built-in high-speed memory, and the pre-fetch method is used to increase the instruction access speed. In the system structure, multiple buses work synchronously, providing rich peripheral functions and enhanced I/O ports. This series of products have built-in RTC, clock security mechanism, a 12-bit ADC conversion module, multiple sets of timers, 16-channel touch key capacitance detection (TKey) and other functions, and also include standard communication interfaces: 2 I2C interfaces, 2 SPI Interface, 3 USART interfaces, 1 USB2.0 full speed host/device interface (full/low speed communication).

The power supply voltage of this series of products is 2.7V ~ 5.5V, and the working temperature range is -40℃ ~ 85℃ industrial grade. Support a variety of power-saving operating modes to meet product low-power application requirements. The products in this series are different in terms of resource allocation, number of peripherals, peripheral functions, etc., select as needed. Several package types of LQFP64M/LQFP48/QFN48X7 are provided. It can be widely used in: motor drive and application control, medical and handheld devices, PC gaming peripherals and GPS platforms, programmable controllers, inverters, printers, scanners, alarm systems, video intercom, heating, ventilation and air conditioning systems, etc. .

1.1 Model comparison

Table 1-1 CH32V103x product resource allocation

Resource differences \ Product number		CH32V103 C6T6	CH32V103 C8T6	CH32V103 C8U6	CH32V103 R8T6
Number of chip pins		48	48	48	64
Flash memory (bytes)		32K	64K	64K	64K
SRAM (bytes)		10K	20K	20K	20K
GPIO ports		37	37	37	51
Timer	General	2	3	3	3
	advanced	1	1	1	1
	Watchdog	2	2	2	2
	System clock	1	1	1	1
ADC/TKey (number of channels)		10	10	10	16
Communication interface	SPI	1	2	2	2
	I2C	1	2	2	2
	USART	2	3	3	3
mouth	USBHD 2.0FS	1	1	1	1
CPU frequency		Typical: 72MHz			
Operating Voltage		2.7V ~ 5.5V			
Operating temperature		Industrial grade: -40℃ ~ 85℃			
Package form		LQFP48		QFN48X7	LQFP64M (10*10)

1.2 System architecture

CH32V1 series products are general-purpose microcontrollers designed based on the RISC-V3A processor. The core, arbitration unit, DMA module, SRAM storage and other parts of the architecture realize interaction through multiple sets of buses. The core adopts 2-stage pipeline processing, and sets static branch prediction and instruction prefetching mechanisms to achieve the best performance ratio of low power consumption, low cost and high-speed operation of the system. The controller has a general DMA controller to reduce the

Burden and improve efficiency. The hierarchical management of the clock tree reduces the total operating power consumption of peripherals. At the same time, it also includes data protection mechanisms and clock security system protection mechanisms to increase system stability.

The following figure is a block diagram of the internal architecture of a series of products.

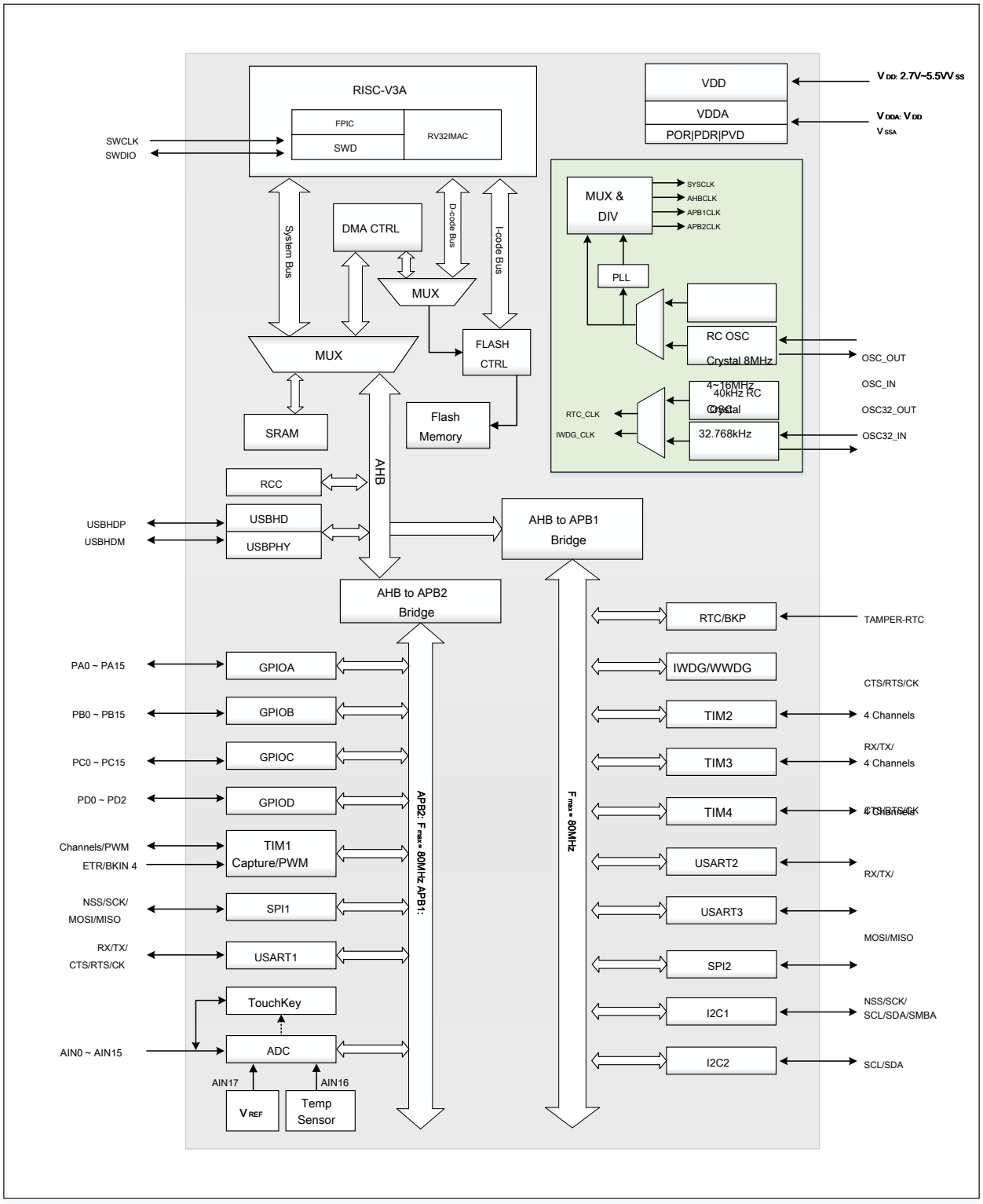

Figure 1-1 System block diagram

1.3 Memory Map

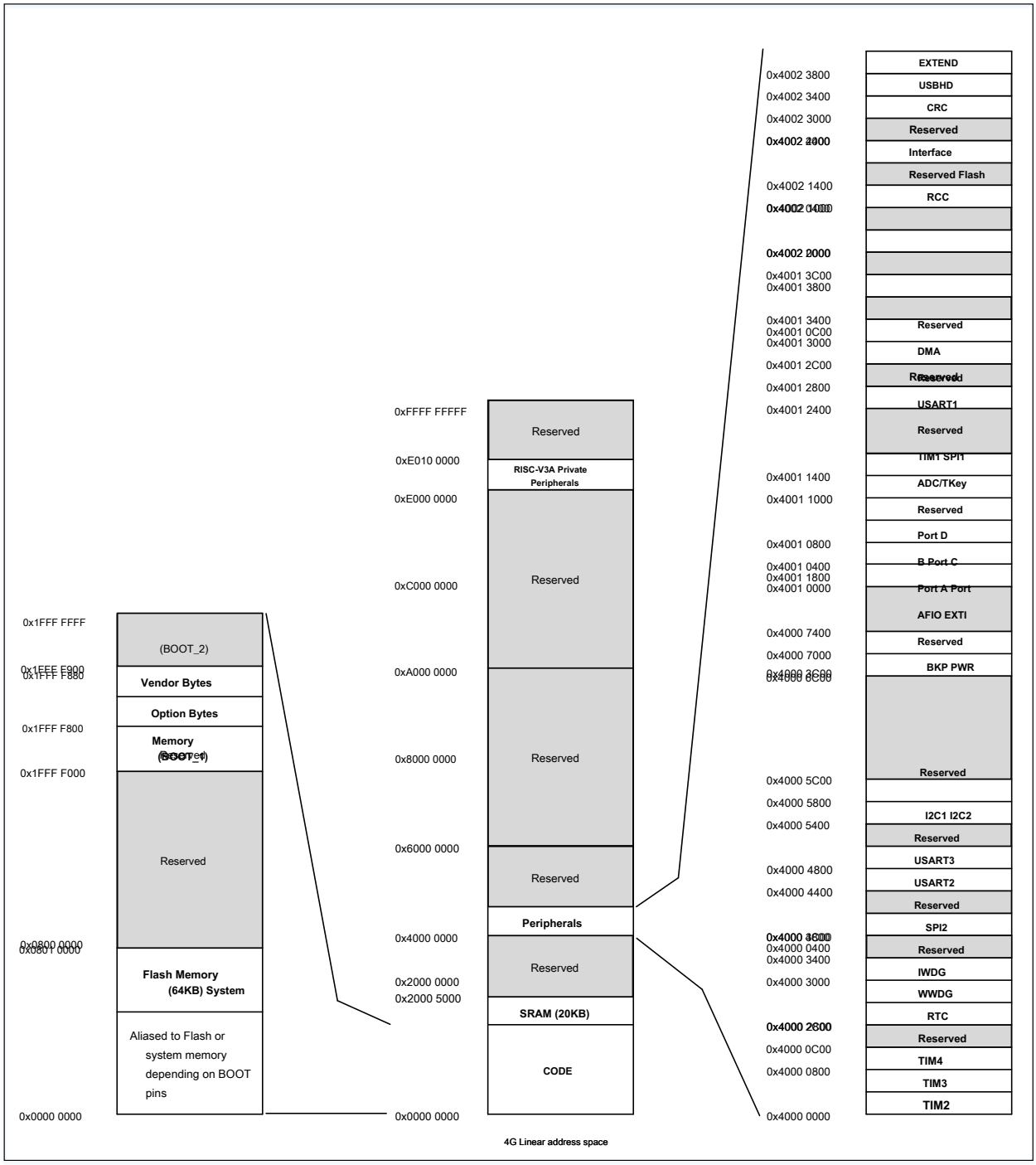

Figure 1-2 Memory address mapping

1.4 Clock Tree

The system provides 4 sets of clock sources: internal high frequency RC oscillator (HSI), internal low frequency RC oscillator (LSI), external high frequency oscillator or clock signal (HSE), external low frequency oscillator or clock signal (LSE). Among them, the system bus clock (SYSCLK) comes from a high-frequency clock source (HSI/HSE) or a higher clock generated after it is multiplied by the PLL. The AHB domain, APB1 domain, and APB2 domain are obtained by dividing the system clock or the previous stage through the corresponding prescaler.

The low frequency clock source provides a clock reference for RTC and independent watchdog.

The PLL multiplied clock directly provides the working clock reference of the USBHD module at 48MHz through the frequency divider.

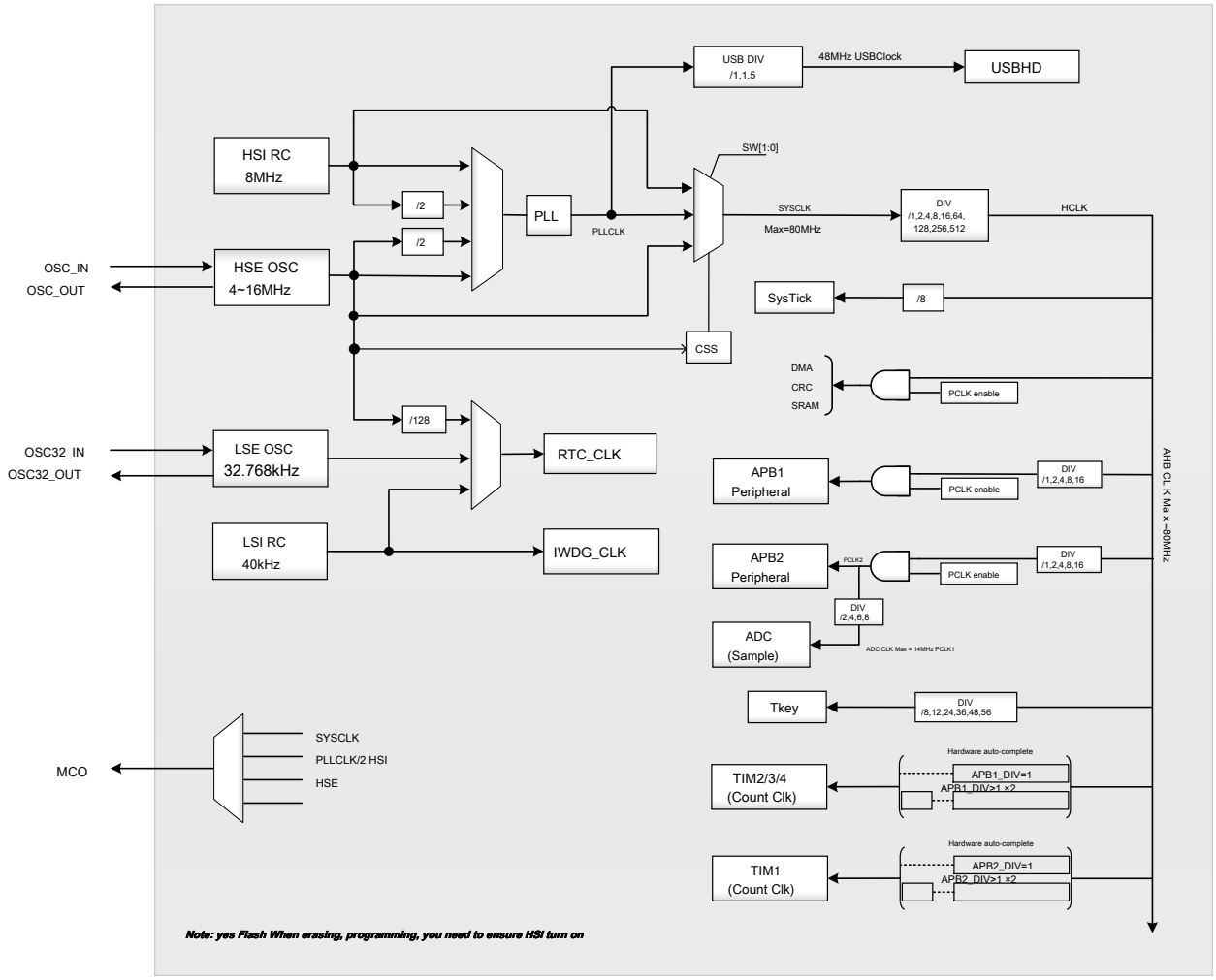

Figure 1-3 Clock tree block diagram

Note:

When using the USB function, the PLL must be used at the same time, and the CPU frequency must be 48MHz or 72MHz. When the ADC sampling time is 1us, APB2 must be set at 14MHz, 28MHz or 56MHz. When the system wakes up from sleep, the system will automatically switch to HSI as the main frequency. When erasing and programming Flash, HSI must be turned on.

1.5 Functional Overview

1.5.1 RISC-V3A processor

RISC-V3A is a 32-bit embedded processor with internal modular management that supports the RISC-V open source instruction set IMAC subset. Contains fast programmable interrupt controller (FPIC), provides 4 vector programmable fast interrupt channels and 44 common interrupts with configurable priority, and realizes the shortest cycle response of interrupts through hardware on-site storage and recovery; includes 2 Wire serial debugging interface, support users to upgrade and debug online; including multiple sets of bus connection processor external unit modules, to achieve the interaction of external function modules and kernel.

- RV32IMAC instruction set, little-endian data mode
- Low-power two-stage pipeline
- Support machine and user privilege mode
- Fast Programmable Interrupt Controller (FPIC), Tail-Chaining tail-chain interrupt handling, 2-level hardware push stack
- Serial 2-wire debug interface

- Branch prediction, efficient jump, conflict detection mechanism

The processor based on this design can be flexibly applied to the design of microcontrollers in different scenarios due to its minimal instruction set, multiple working modes, modular customization and expansion, such as small-area low-power embedded scenarios and high-performance application operating system scenarios. Wait.

CH32V1 series controller adopts RISC-V3A core, equipped with a complete hardware and software platform and tools, and supports online downloading, debugging and tracking of application codes.

1.5.2 On-chip memory and bootstrap mode

Built-in 20K bytes SRAM area for storing data.

Built-in 64K byte program flash storage area (CodeFlash), used for user application storage. Built-in 3.75K byte system storage area (BootLoader), used for system boot program storage (factory solidified bootloader). In addition, 128 bytes are used for manufacturer configuration word storage, and 128 bytes are used for user-selected word storage. At startup, one of three bootstrap modes can be selected through the bootstrap pins (BOOT0 and BOOT1):

- Boot from program flash memory
- Boot from system memory
- Boot from internal SRAM

The bootloader is stored in the system storage area, and the contents of the program flash storage area can be reprogrammed through the USART1 and USB interface.

1.5.3 Power supply scheme

- **V_{DD} - 2.7 ~ 5.5V: V_{DD} The pins power the I/O pins, RC oscillator, reset module, and internal voltage regulator.**
- **V_{DDA} - 2.7 ~ 5.5V: supply power for the analog part of ADC, temperature sensor and PLL. V_{DDA} And V_{SSA} Must be connected to V separately$_{DD}$ And V_{SS} .**
- **V_{BAT} - 1.8 ~ 5.5V: when V_{DD} When removed or not working, V_{BAT} Separate power supply for RTC, external 32KHz oscillator and backup register.**

1.5.4 Power supply monitor

This product integrates a power-on reset (POR)/power-down reset (PDR) circuit, which is always in a working state to ensure that the system works when the power supply **exceeds 2.7V; when V_{DD} Below the set threshold (V_{PORPDR}) At this time, the device is placed in a reset state without using an external reset circuit.**

There is also a programmable voltage monitor (PVD), which needs to be turned on by software to compare V_{DD}/ V_{DDA} Power supply and set threshold V_{PVD} The size of the voltage. Turn on the corresponding edge interrupt of PVD.$_{DD}$ When it falls to the PVD threshold or rises to the PVD threshold, an interrupt notification is received. About V_{PORPDR} And V_{PVD} Refer to Table 3-4 for the value.

1.5.5 Voltage regulator

After reset, the regulator automatically turns on, and there are three operation modes according to the application mode

- Open mode: normal operation, providing stable core power
- Low power consumption mode: When the CPU enters the stop mode, the regulator can be selected to run at low power consumption
- Shutdown mode: when the CPU enters the standby mode, the regulator is automatically switched to this mode, the voltage regulator output is in a high-impedance state, the power supply of the core circuit is cut off, and the voltage regulator is in a zero consumption state

The voltage regulator is always in the on mode after reset, and is turned off in the off mode in the standby mode, which is a high-impedance output.

1.5.6 Low power mode

The series products support three low-power modes, and can choose to achieve the best balance under the conditions of low power consumption, short start-up time and multiple wake-up events.

- Sleep mode

Execute WFI/WFE instruction to enter. In sleep mode, only the CPU clock is stopped, but all peripheral clock power is normal, and the peripherals are in working state. This mode is the shallowest low-power mode, but can achieve the fastest wake-up.

Exit condition: any interrupt or wake-up event.

- Stop mode

Clear the PDDS bit, set the SLEEPDEEP bit, choose to clear/set the LPDS bit, and execute the WFI/WFE instruction to enter. In the stop mode, FLASH enters the low-power mode. The LPDS bit determines whether to turn off the power supply to the core part. The PLL, HSI RC oscillator, and HSE crystal oscillator are turned off. In the case of keeping the contents of SRAM and registers not lost, the stop mode can achieve the lowest power consumption.

Exit conditions: any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset, a rising edge on the WKUP pin, where the EXTI signal includes one of 16 external I/O ports, the output of PVD, RTC alarm clock or USB wake-up signal.

- Standby mode

Set the PDDS and SLEEPDEEP bits and execute the WFI/WFE instruction to enter. The power supply of the core part is turned off; PLL, HSI's RC oscillator and HSE crystal oscillator are also turned off; in this mode, the lowest power consumption can be achieved, but the system is reset after waking up.

Exit conditions: any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset, a rising edge on the WKUP pin, where the EXTI signal includes one of 16 external I/O ports, the output of PVD, RTC alarm clock or USB wake-up signal.

1.5.7 CRC (Cyclic Redundancy Check) calculation unit

The CRC (Cyclic Redundancy Check) calculation unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. In many applications, CRC-based technology is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC 60335-1 standard, it provides a means of detecting flash memory errors. The CRC calculation unit can be used to calculate the signature of the software in real time and compare it with the signature generated when linking and generating the software.

1.5.8 Fast programmable interrupt controller (FPIC)

The product has a built-in fast programmable interrupt controller (FPIC) that supports up to 255 interrupt vectors. CH32V1 controller provides 5 core private interrupts and 44 peripheral interrupt management, other interrupt sources are reserved. FPIC registers can be accessed in user and machine privilege modes.

- 44+3 individually shieldable interrupts
- Provide a non-maskable interrupt NMI
- 16-level priority programming, dynamic modification.
- 2-level nested interrupt entry and exit hardware automatically pushes and restores without instruction overhead
- 4 programmable fast interrupt channels, custom interrupt vector address
- Support break link function
- Provide the first response of non-maskable interrupt

The module provides flexible interrupt management functions with minimal interrupt delay.

1.5.9 External interrupt/event controller (EXTI)

The external interrupt/event controller contains 20 edge detectors for generating interrupt/event requests. Each interrupt line can independently configure its trigger event (rising edge or falling edge or bilateral edge), and can be individually masked; the suspend register maintains all interrupt request states. EXTI can detect that the pulse width is less than the internal APB2 clock period. Up to 51 general-purpose I/O ports can be optionally connected to 16 external interrupt lines.

1.5.10 General DMA controller

Flexible general-purpose DMA can manage high-speed data transfer from memory to memory, peripheral to memory and memory to peripheral, provides 7 channels, and supports ring buffer management. Each channel has dedicated hardware DMA request logic, supports one or more peripherals to access memory requests, memory-to-memory data transfer, configurable access priority, transfer length, source address and destination address of the transfer, etc.

DMA is used for the main peripherals including: general/advanced control timers TIM, ADC, USART, I2C, SPI.

1.5.11 Clock and Start

The system clock source HSI is turned on by default. After the clock is not configured or reset, the internal 8MHz RC oscillator is used as the default CPU clock, and then an external 4-16MHz clock or PLL clock can be selected. When the clock security mode is turned on, if HSE is used as the system clock (direct or indirect), the external clock is detected to be invalid at this time, the system clock will automatically switch to the internal RC oscillator, and HSE and PLL will be automatically turned off; In power consumption mode, the system will automatically switch to the internal RC oscillator after waking up. If the clock interrupt is enabled, the software can receive the corresponding interrupt.

Multiple prescalers are used to configure the AHB bus clock, high-speed APB2, and low-speed APB1 regional bus clocks. Refer to Figure 1-2 for the clock tree block diagram.

1.5.12 RTC (Real Time Clock) and Backup Register

The RTC and backup registers are in the backup power supply area inside the product, at V_{DD} When valid, V_{DD} Power supply, otherwise the internal automatically switches to V_{BAT} Pin power supply.

The RTC real-time clock is a group of 32-bit programmable counters. The time base supports 20-bit prescaler and is used for long time period measurement. The clock reference source is a high-speed external clock divided by 128 (HSE/128), an external crystal 32.768KHz oscillator (LSE) or an internal low-power RC oscillator (LSI). There is also a backup power supply area for LSE, so when LSE is selected as the RTC time base, the RTC setting and time can remain unchanged after the system resets or wakes up from standby mode.

The backup register contains 10 16-bit registers that can be used to store 20 bytes of user application data. This data can be maintained and will not be reset after wake-up from standby, or when the system is reset or the power is reset. When the intrusion detection function is enabled, once the intrusion detection signal is valid, all contents in the backup register can be cleared.

1.5.13 ADC (Analog/Digital Converter) and Touch Key Capacitance Detection (TKey)

The product is embedded with a 12-bit analog/digital converter (ADC), which provides up to 16 external channels and 2 internal channels sampling, programmable channel sampling time, can achieve single, continuous, scanning or discontinuous mode conversion . Providing analog watchdog function allows very accurate monitoring of one or more selected channels for monitoring the signal voltage of the channel. Support external event trigger conversion, the trigger source includes the internal signal of the on-chip timer and the external pin (EXTI line 11). Supports the use of DMA operations.

ADC internal channel sampling includes one internal temperature sensor sampling and one internal reference power sampling. The temperature sensor generates a **voltage that varies linearly with temperature, and the power supply range is 3.0V <V_{DDA}< Between 5.5V. The temperature sensor is internally connected to the input channel of** ADC_IN16 and is used to convert the output of the sensor to a digital value.

Touch button capacitance detection function, multiplexing the external channels of the ADC, provides up to 16 detections. The application determines the state of the touch key by the amount of change in the digital value.

1.5.14 Timer

The timer includes 1 advanced 16-bit timer, 3 general-purpose 16-bit timers, 2 watchdog timers and 1 system time-base timer.

1.5.14.1 Advanced Control Timer (TIM1)

The advanced control timer (TIM1) is a 16-bit auto-loading counter with a programmable prescaler. In addition to the complete general-purpose timer function, it can be regarded as a three-phase PWM generator distributed to 6 channels, with a complementary PWM output function with dead-zone insertion, allowing the timer to be updated to repeat after a specified number of counter cycles Count cycle, brake function, etc. Many functions of the advanced control timer are the same as the general-purpose timer, and the internal structure is also the same. Therefore, the advanced control timer can cooperate with the TIM timer through the timer link function to provide synchronization or event link function.

1.5.14.2 General-purpose timer (TIM2/3/4)

The system has built-in up to 3 standard timers (TIM2, TIM3 and TIM4) that can run synchronously. Each timer has a 16-bit auto-loading up/down counter, a programmable 16-bit prescaler and 4 independent channels, each of which can be used for input capture, output comparison, PWM generation and Single pulse mode output.

It can also work with the advanced control timer through the timer link function to provide synchronization or event link functions. In debug mode, the counter can be frozen and the PWM output is disabled, thereby cutting off the switches controlled by these outputs. Any general-purpose timer can be used to generate the PWM output. Each timer has an independent DMA request mechanism.

These timers can also handle signals from incremental encoders and digital outputs from 1 to 3 Hall sensors.

1.5.14.3 Independent Watchdog (IWDG)

The independent watchdog is a free-running 12-bit down counter with an 8-bit prescaler. The clock is provided by an internal independent 40KHz RC oscillator; because this RC oscillator is independent of the main clock, it can run in stop and standby modes. IWDG can work completely independently from the main program, so it is used to reset the entire system when a problem occurs, or as a free timer to provide timeout management for applications. The option byte can be configured to be a software or hardware boot watchdog. In debug mode, the counter can be frozen.

1.5.14.4 Window Watchdog (WWDG)

The window watchdog is a 7-bit down counter and can be set to run freely. Can be used to reset the entire system when a problem occurs. It is driven by the main clock and has an early warning interrupt function; in debug mode, the counter can be frozen.

1.5.14.5 System Time Base Timer (SysTick)

This is a timer that comes with the kernel controller. It is used to generate SYSTICK exceptions. It can be used exclusively for real-time operating systems to provide a "heartbeat" rhythm for the system. It can also be used as a standard 64-bit up-counter. The AHB clock is divided by 8 as the reference clock source. When the counter increments to the set comparison value, a maskable system interrupt is generated.

1.5.15 Standard communication interface

1.5.15.1 Universal Synchronous/Asynchronous Transceiver (USART)

3 sets of universal asynchronous transceivers USART, support full duplex asynchronous communication, synchronous unidirectional communication and half duplex single line communication, also support LIN (local interconnection network), ISO7816 compatible smart card protocol and IrDA SIR ENDEC transmission codec specification, and modem (CTS/RTS hardware flow control) operation. It also allows multiprocessor communication. It uses a fractional baud rate generator system, the USART1 interface is up to 4.5Mbits/s, USART2/3 can reach 2.25Mbits/s. Support DMA operation continuous communication.

1.5.15.2 Serial Peripheral Interface (SPI)

2 sets of serial peripheral SPI interface, providing master or slave operation, dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. The clock frequency can be up to 36MHz, programmable clock polarity and phase, the data bit width provides 8 or 16 bit selection, reliable communication hardware CRC generation/check, support DMA operation continuous communication.

1.5.15.3 I2C bus

Up to 2 I2C bus interfaces can work in multi-master mode or slave mode, complete all I2C bus specific timing, protocol, arbitration, etc. It supports both standard and fast communication speeds, and is compatible with SMBus2.0.

The I2C interface provides 7-bit or 10-bit addressing, and supports dual-slave addressing in 7-bit slave mode. Built-in hardware CRC generator/checker. Can use DMA operation and support SMBus bus version 2.0/PMBus bus.

1.5.15.4 Universal Serial Bus (USB)

The product is embedded with a USB2.0 host controller and device controller (USBHD), following the USB2.0 Fullspeed standard. Provide 16 configurable USB device endpoints and a set of host endpoints. Support control/batch/synchronization/interrupt transmission, double buffer mechanism, USB bus suspend/resume operation, and provide standby/wake-up function. The 48MHz clock dedicated to the USBHD module is directly generated by the internal main PLL frequency division (PLL must be 72MHz or 48MHz).

1.5.16 General Purpose Input and Output Interface (GPIO)

The system provides 4 groups of GPIO ports, a total of 51 GPIO pins. Each pin can be configured by software as an output (push-pull or open-drain), input (with or without pull-up or pull-down), or multiplexed peripheral function port. Most GPIO pins are shared with digital or analog multiplexed peripherals. Except for the ports with analog input function, all GPIO pins have large current passing capability. A locking mechanism is provided to freeze the IO configuration to avoid accidental writes to I/O registers.

1.5.17 2-wire serial debugging interface (SWD)

Built-in SWD interface, this is a 2-wire serial debugging interface. The hardware includes SWDIO and SWCLK pins and supports online code upgrade and debugging.

Chapter 2 Pin Information

2.1 Pin arrangement

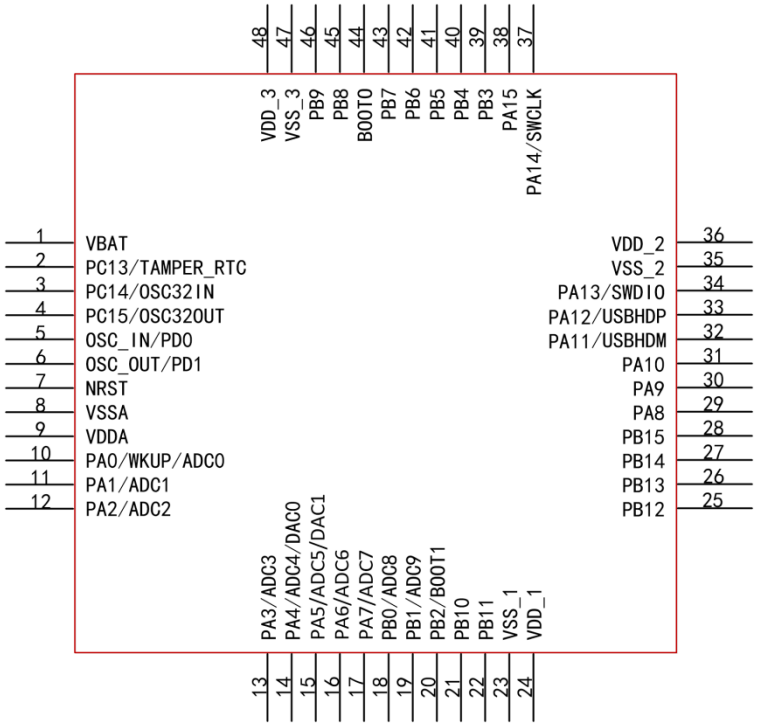

Figure 2-1 CH32V103Cx (LQFP48/QFN48X7) pin layout

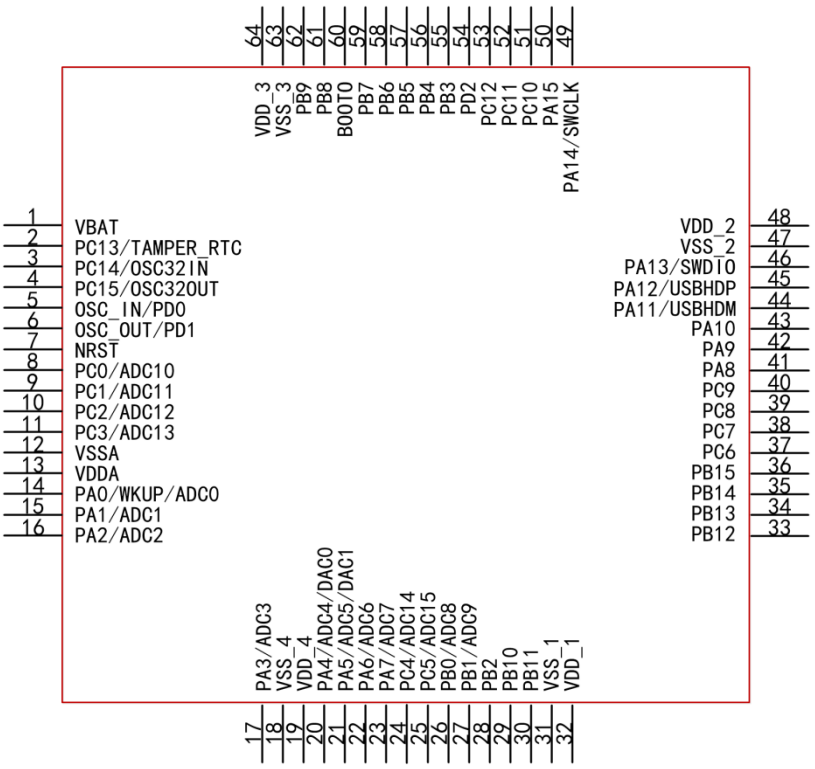

Figure 2-2 CH32V103Rx (LQFP64M) pin layout

2.2 Pin description

Table 2-1 CH32V103x8x6 pin definition guide Foot

number			Pin name	Pin type	Main function (after reset)	Default reuse function	Remap function
LQFP48	QFN48X7	LQFP64M					
1	1	1	V_{BAT}	P	V_{BAT}		
2	2	2	PC13-TAMPER-RTC	I/O	PC13	TAMPER-RTC	
3	3	3	PC14OSC32_IN	I/O/A	PC14	OSC32_IN	
4	4	4	PC15-OSC32_OUT	I/O/A	PC15	OSC32_OUT	
5	5	5	OSC_IN	I/A	OSC_IN		PD0
6	6	6	OSC_OUT	O/A	OSC_OUT		PD1
7	7	7	NRST	I/O	NRST		
-	-	8	PC0	I/O/A	PC0	ADC_IN10	
-	-	9	PC1	I/O/A	PC1	ADC_IN11	
-	-	10	PC2	I/O/A	PC2	ADC_IN12	
-	-	11	PC3	I/O/A	PC3	ADC_IN13	
8	8	12	V_{SSA}	P	V_{SSA}		
9	9	13	V_{DDA}	P	V_{DDA}		
10	10	14	PA0-WKUP	I/O/A	PA0	WKUP/USART2_CTS/ADC_IN0 /TIM2_CH1/TIM2_ETR	
11	11	15	PA1	I/O/A	PA1	USART2_RTS/ADC_IN1 /TIM2_CH2	
12	12	16	PA2	I/O/A	PA2	USART2_TX/ADC_IN2 /TIM2_CH3	
13	13	17	PA3	I/O/A	PA3	USART2_RX/ADC_IN3 /TIM2_CH4	
-	-	18	V_{SS_4}	P	V_{SS_4}		
-	-	19	V_{DD_4}	P	V_{DD_4}		
14	14	20	PA4	I/O/A	PA4	SPI1_NSS/USART2_CK /ADC_IN4	
15	15	twenty one	PA5	I/O/A	PA5	SPI1_SCK/ADC_IN5	
16	16	twenty two	PA6	I/O/A	PA6	SPI1_MISO/ADC_IN6 /TIM3_CH1	TIM1_BKIN
17	17	twenty three	PA7	I/O/A	PA7	SPI1_MOSI/ADC_IN7 /TIM3_CH2	TIM1_CH1N
-	-	twenty four	PC4	I/O/A	PC4	ADC_IN14	
-	-	25	PC5	I/O/A	PC5	ADC_IN15	
18	18	26	PB0	I/O/A	PB0	ADC_IN8/TIM3_CH3	TIM1_CH2N
19	19	27	PB1	I/O/A	PB1	ADC_IN9/TIM3_CH4	TIM1_CH3N

20	20	28	PB2	I/O	PB2 /BOOT1		
twenty one	twenty one	29	PB10	I/O	PB10	I2C2_SCL/USART3_TX	TIM2_CH3
twenty two	twenty two	30	PB11	I/O	PB11	I2C2_SDA/USART3_RX	TIM2_CH4
twenty three	twenty three	31	V_{SS_1}	P	V_{SS_1}		
twenty four	twenty four	32	V_{DD_1}	P	V_{DD_1}		
25	25	33	PB12	I/O	PB12	SPI2_NSS/I2C2_SMBAI /USART3_CK/TIM1_BKIN	
26	26	34	PB13	I/O	PB13	SPI2_SCK/USART3_CTS /TIM1_CH1N	
27	27	35	PB14	I/O	PB14	SPI2_MISO/USART3_RTS /TIM1_CH2N	
28	28	36	PB15	I/O	PB15	SPI2_MOSI/TIM1_CH3N	
-	-	37	PC6	I/O	PC6		TIM3_CH1
-	-	38	PC7	I/O	PC7		TIM3_CH2
-	-	39	PC8	I/O	PC8		TIM3_CH3
-	-	40	PC9	I/O	PC9		TIM3_CH4
29	29	41	PA8	I/O	PA8	USART1_CK/TIM1_CH1/MCO	
30	30	42	PA9	I/O	PA9	USART1_TX/TIM1_CH2	
31	31	43	PA10	I/O	PA10	USART1_RX/TIM1_CH3	
32	32	44	PA11	I/O/A	PA11	USART1_CTS/USBHDM/TIM1_CH4	
33	33	45	PA12	I/O/A	PA12	USART1_RTS/USBHDP/TIM1_ETR	
34	34	46	PA13	I/O	SWDIO		PA13
35	35	47	V_{SS_2}	P	V_{SS_2}		
36	36	48	V_{DD_2}	P	V_{DD_2}		
37	37	49	PA14	I/O	SWCLK		PA14
38	38	50	PA15	I/O	PA15		TIM2_CH1/TIM2_ETR /SPI1_NSS
-	-	51	PC10	I/O	PC10		UASRT3_TX
-	-	52	PC11	I/O	PC11		USART3_RX
-	-	53	PC12	I/O	PC12		USART3_CK
-	-	54	PD2	I/O	PD2	TIM3_ETR	
39	39	55	PB3	I/O	PB3		TRACESWO/TIM2_CH2 /SPI1_SCK
40	40	56	PB4	I/O	PB4		TIM3_CH1/SPI1_MISO
41	41	57	PB5	I/O	PB5	I2C1_SMBAI	TIM3_CH2/SPI1_MOSI
42	42	58	PB6	I/O/A	PB6	I2C1_SCL/TIM4_CH1	USART1_TX
43	43	59	PB7	I/O/A	PB7	I2C1_SDA/TIM4_CH2	USART1_RX
44	44	60	BOOT0	I	BOOT0		
45	45	61	PB8	I/O/A	PB8	TIM4_CH3	I2C1_SCL
46	46	62	PB9	I/O/A	PB9	TIM4_CH4	I2C1_SDA
47	47	63	V_{SS_3}	P	V_{SS_3}		
48	48	64	V_{DD_3}	P	V_{DD_3}		

Table 2-2 CH32V103x6x6 pins Define the pin

number		Pin name	Pin type	Main function (after reset)	Default reuse function	Remap function
LQFP48	LQFP64M					
1	1	V_{BAT}	P	V_{BAT}		
2	2	PC13-TAMPER-RTC	I/O	PC13	TAMPER-RTC	
3	3	PC14-OSC32_IN	I/O/A	PC14	OSC32_IN	
4	4	PC15-OSC32_OUT	I/O/A	PC15	OSC32_OUT	
5	5	OSC8M_IN	I/A	OSC8M_IN		PD0
6	6	OSC8M_OUT	O/A	OSC8M_OUT		PD1
7	7	NRST	I/O	NRST		
-	8	PC0	I/O/A	PC0	ADC_IN10	
-	9	PC1	I/O/A	PC1	ADC_IN11	
-	10	PC2	I/O/A	PC2	ADC_IN12	
-	11	PC3	I/O/A	PC3	ADC_IN13	
8	12	V_{SSA}	P	V_{SSA}		
9	13	V_{DDA}	P	V_{DDA}		
10	14	PA0-WKUP	I/O/A	PA0	WKUP/USART2_CTS/ADC_IN0/TIM2_CH1/TIM2_ETR	
11	15	PA1	I/O/A	PA1	USART2_RTS/ADC_IN1/TIM2_CH2	
12	16	PA2	I/O/A	PA2	USART2_TX/ADC_IN2/TIM2_CH3	
13	17	PA3	I/O/A	PA3	USART2_RX/ADC_IN3/TIM2_CH4	
-	18	V_{SS_4}	P	V_{SS_4}		
-	19	V_{DD_4}	P	V_{DD_4}		
14	20	PA4	I/O/A	PA4	SPI1_NSS/USART2_CK/ADC_IN4	
15	twenty one	PA5	I/O/A	PA5	SPI1_SCK/ADC_IN5	
16	twenty two	PA6	I/O/A	PA6	SPI1_MISO/ADC_IN6/TIM3_CH1	TIM1_BKIN
17	twenty three	PA7	I/O/A	PA7	SPI1_MOSI/ADC_IN7/TIM3_CH2	TIM1_CH1N
-	twenty four	PC4	I/O/A	PC4	ADC_IN14	
-	25	PC5	I/O/A	PC5	ADC_IN15	
18	26	PB0	I/O/A	PB0	ADC_IN8/TIM3_CH3	TIM1_CH2N
19	27	PB1	I/O/A	PB1	ADC_IN9/TIM3_CH4	TIM1_CH3N
20	28	PB2	I/O	PB2/BOOT1		
twenty one	29	PB10	I/O	PB10		TIM2_CH3
twenty two	30	PB11	I/O	PB11		TIM2_CH4
twenty three	31	V_{SS_1}	P	V_{SS_1}		
twenty four	32	V_{DD_1}	P	V_{DD_1}		

25	33	PB12	I/O	PB12	TIM1_BKIN	
26	34	PB13	I/O	PB13	TIM1_CH1N	
27	35	PB14	I/O	PB14	TIM1_CH2N	
28	36	PB15	I/O	PB15	TIM1_CH3N	
-	37	PC6	I/O	PC6		TIM3_CH1
-	38	PC7	I/O	PC7		TIM3_CH2
-	39	PC8	I/O	PC8		TIM3_CH3
-	40	PC9	I/O	PC9		TIM3_CH4
29	41	PA8	I/O	PA8	USART1_CK/TIM1_CH1/MCO	
30	42	PA9	I/O	PA9	USART1_TX/TIM1_CH2	
31	43	PA10	I/O	PA10	USART1_RX/TIM1_CH3	
32	44	PA11	I/O/A	PA11	USART1_CTS/USBHDM/TIM1_CH4	
33	45	PA12	I/O/A	PA12	USART1_RTS/USBHDP/TIM1_ETR	
34	46	PA13	I/O	SWDIO		PA13
35	47	V_{SS_2}	P	V_{SS_2}		
36	48	V_{DD_2}	P	V_{DD_2}		
37	49	PA14	I/O	SWCLK		PA14
38	50	PA15	I/O	PA15		TIM2_CH1/TIM2_ETR/SPI1_NSS
-	51	PC10	I/O	PC10		
-	52	PC11	I/O	PC11		
-	53	PC12	I/O	PC12		
-	54	PD2	I/O	PD2	TIM3_ETR	
39	55	PB3	I/O	PB3		TRACESWO/TIM2_CH2/SPI1_SCK
40	56	PB4	I/O	PB4		TIM3_CH1/SPI1_MISO
41	57	PB5	I/O	PB5	I2C1_SMBAI	TIM3_CH2/SPI1_MOSI
42	58	PB6	I/O/A	PB6	I2C1_SCL	USART1_TX
43	59	PB7	I/O/A	PB7	I2C1_SDA	USART1_RX
44	60	BOOT0	I	BOOT0		
45	61	PB8	I/O/A	PB8		I2C1_SCL
46	62	PB9	I/O/A	PB9		I2C1_SDA
47	63	V_{SS_3}	P	V_{SS_3}		
48	64	V_{DD_3}	P	V_{DD_3}		

Note: Pin type:

I = TTL/CMOS level Schmitt input; O = CMOS level tri-state output; A = analog signal input or output; P = power supply;

Chapter 3 Electrical Characteristics

3.1 Test conditions

Unless otherwise specified and marked, all voltages are in V_{SS} As a benchmark.

All minimum and maximum values will be guaranteed under the worst ambient temperature, supply voltage and clock frequency. Typical values are based on room temperature and V_{DD}. It can be used for design guidance in 3.3V environment.

The data obtained through comprehensive evaluation, design simulation or process characteristics will not be tested on the production line. On the basis of comprehensive evaluation, the minimum and maximum values are obtained statistically after sample testing.

Normal temperature

environment: 25℃ Power supply scheme:

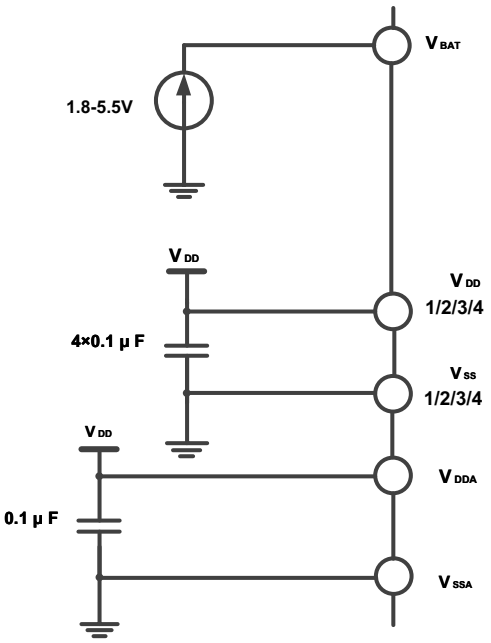

Figure 3-1 Typical circuit of conventional power supply

3.2 Absolute maximum

Critical or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged.

Table 3-1 Absolute maximum parameter table

symbol	description	Min	Max	unit
T_A [1]	Ambient temperature when working	-40	85	℃
T_S	Ambient temperature during storage	-40	105	℃
V_{DD}- V_{SS}	External main supply voltage (including V_{DDA} And V_{DD})	- 0.3	5.5	V
V_{IN} [1]	Input voltage on the pin	V_{SS}- 0.3	5.5	V
$\|\Delta V_{DDx}\|$	Voltage difference between different power supply pins		50	mV
$\|V_{SSx}$- $V_{SS}\|$	Voltage difference between different ground pins		50	mV
$V_{ESD(HBM)}$ [1]	ESD electrostatic discharge voltage (human body model, non-contact type)	2000		V
I_{VDD} [2]	After V_{DD}/ V_{DDA} The total current of the power cord (supply current)		50	mA

I_{Vss} [2]	After V_{SS} Total current of ground wire (outflow current)		50	
I_{IO} [1]	Sink current on any I/O and control pins		-25	
	Output current on any I/O and control pins		25	

Note: 1. Design parameters.

2. Normal operation can reach the maximum current value.

3.3 Electrical parameters

3.3.1 Working conditions

Table 3-2 General working conditions

symbol	parameter	condition	Min	Max	unit
F_{SYSCLK}	Internal system clock frequency			80	MHz
F_{HCLK}	Internal AHB domain bus clock frequency			80	MHz
F_{PCLK1}	Internal APB1 domain bus clock frequency			80	MHz
F_{PCLK2}	Internal APB2 domain bus clock frequency			80	MHz
V_{DD}	Standard working voltage		2.7	5.5	V
V_{DDA}	The working voltage of the analog part (not using ADC) must be the same as V_{DD} the same		2.7	5.5	V
	Analog part working voltage (using ADC)		3.0		
V_{BAT} [2]	Working voltage of backup unit	Cannot be greater than V_{DD}	1.8	5.5	V
T_A [1]	Ambient temperature		-40	85	℃

Note: 1. Design parameters.

2. Battery to V_{BAT} The wiring should be as short as possible.

Table 3-3 Power-on and power-off conditions

symbol	parameter	condition	Min	Max	unit
t_{VDD}	V_{DD} Ascent rate		0	∞	us/V
	V_{DD} Rate of descent		50	∞	us/V

Note: battery to V_{BAT} The wiring should be as short as possible.

3.3.2 Embedded reset and power control module features

Table 3-4 Reset and voltage monitor

symbols	parameter	condition	Minimum value	Typical value	maximum unit	
V_{PVD} [2]	Programmable voltage detector Flat selection	PLS[2:0] = 000 (rising edge)		2.65		V
		PLS[2:0] = 000 (falling edge)		2.5		V
		PLS[2:0] = 001 (rising edge)		2.87		V
		PLS[2:0] = 001 (falling edge)		2.7		V
		PLS[2:0] = 010 (rising edge)		3.07		V
		PLS[2:0] = 010 (falling edge)		2.89		V
		PLS[2:0] = 011 (rising edge)		3.27		V
		PLS[2:0] = 011 (falling edge)		3.08		V
		PLS[2:0] = 100 (rising edge)		3.46		V
		PLS[2:0] = 100 (falling edge)		3.27		V
		PLS[2:0] = 101 (rising edge)		3.76		V

		PLS[2:0] = 101 (falling edge)		3.55		V
		PLS[2:0] = 110 (rising edge)		4.07		V
		PLS[2:0] = 110 (falling edge)		3.84		V
		PLS[2:0] = 111 (rising edge)		4.43		V
		PLS[2:0] = 111 (falling edge)		4.18		V
$V_{PVDhyst}$ [1]	PVD hysteresis			0.2		V
$V_{POR/PDR}$ [1]	Rising edge of power-on/power-down reset threshold			2.5		V
		Falling edge		2.42		V
$V_{PDRhyst}$ [1]	PDR hysteresis		40		110	mV
$t_{RSTTEMPO}$ [1]	Reset duration		16		44	mS

Note: 1. Design parameters

2. Normal temperature test value.

3.3.3 Built-in reference voltage

Table 3-5 Built-in reference voltage

symbol	parameter	condition	Min	Max	unit
V_{REFINT}	Built-in reference voltage	T_A = -40℃~85℃	1.12	1.28	V
$T_{S\_vrefint}$	When reading the internal reference voltage, the sampling time of the ADC		0.107	17.1	us

3.3.4 Supply current characteristics

Current consumption is a comprehensive indicator of various parameters and factors, including operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin turnover rate, and program in memory The position in the code and the executed code, etc.

The current consumption measurement method is as follows:

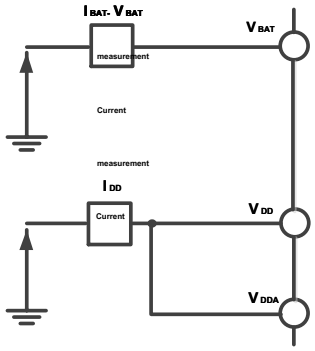

Figure 3-2 Current consumption measurement

The microcontroller is in the following conditions:

At normal temperature, V_{DD} - 3.3V, all IO ports are configured with pull-up inputs to enable or disable all peripheral clocks (excluding GPIO Set), there is no initialization peripheral function.

Table 3-6 Running mode Typical current under Consumption, data processing code runs from internal flash memory

symbol	parameter	condition	Typical value		unit
			Enable all peripherals and	turn off all peripherals	

I_{DD}	Supply current in operating mode	External clock	F_{SYSCLK}= 72MHz	13.56	8.88	mA
			F_{SYSCLK}= 48MHz	9.76	6.64	
			F_{SYSCLK}= 36MHz	8.51	5.85	
			F_{SYSCLK}= 24MHz	6.38	4.62	
			F_{SYSCLK}= 16MHz	5.11	3.88	
			F_{SYSCLK}= 8MHz	3.15	2.61	
			F_{SYSCLK}= 4MHz	2.50	2.26	
			F_{SYSCLK}= 500KHz	1.99	1.96	
		Runs on high speed internal RC oscillator (HSI), using AHB prescaler to reduce frequency	F_{SYSCLK}= 64MHz	12.63	7.63	
			F_{SYSCLK}= 48MHz	9.92	6.17	
			F_{SYSCLK}= 36MHz	7.90	5.08	
			F_{SYSCLK}= 24MHz	5.75	3.98	
			F_{SYSCLK}= 16MHz	4.57	3.31	
			F_{SYSCLK}= 8MHz	2.82	2.23	
			F_{SYSCLK}= 4MHz	2.19	1.88	
			F_{SYSCLK}= 500KHz	1.61	1.58	

Note: The above are measured parameters

Table 3-7 Sleep mode Typical current under Consumption, data processing code runs from internal flash or SRAM

symbol	parameter	condition		Typical value		unit
				Enable all peripherals and	turn off all peripherals	
I_{DD}	Supply current in sleep mode (peripheral power supply and clock hold)	External clock	F_{SYSCLK}= 72MHz	10.98	5.33	mA
			F_{SYSCLK}= 48MHz	8.05	4.27	
			F_{SYSCLK}= 36MHz	6.87	4.06	
			F_{SYSCLK}= 24MHz	5.30	3.42	
			F_{SYSCLK}= 16MHz	4.34	3.08	
			F_{SYSCLK}= 8MHz	2.83	2.21	
			F_{SYSCLK}= 4MHz	2.37	2.06	
			F_{SYSCLK}= 500KHz	1.97	1.93	
		Runs on high speed internal RC oscillator (HSI), using AHB prescaler to reduce frequency	F_{SYSCLK}= 64MHz	9.71	4.69	
			F_{SYSCLK}= 48MHz	7.73	3.96	
			F_{SYSCLK}= 36MHz	6.24	3.41	
			F_{SYSCLK}= 24MHz	4.76	2.87	
			F_{SYSCLK}= 16MHz	3.83	2.57	
			F_{SYSCLK}= 8MHz	2.47	1.84	
			F_{SYSCLK}= 4MHz	2.00	1.68	
			F_{SYSCLK}= 500KHz	1.59	1.55	

Note: The above are measured parameters

Table 3-8 Typical current consumption in stop and standby modes

symbol	parameter	condition	Typical value	unit

I_{DD}	Supply current in stop mode	The voltage regulator is in running mode, and the low-speed and high-speed internal RC oscillators and external oscillators are off (no separate watchdog)	455	uA
		The voltage regulator is in low-power mode, and both the low-speed and high-speed internal RC oscillators and external oscillators are off (no separate watchdog)	1.6	
	Supply current in standby mode	Low speed internal RC oscillator and independent watchdog are on	2.8	
		Low-speed internal RC oscillator is on, independent watchdog is off	2.7	
		Low speed internal RC oscillator and independent watchdog are off, low speed external oscillator and RTC are off	1.6	
I_{DD_VBAT}	Supply current in the backup area (remove V_{DD} And V_{DDA} , Use only V_{BAT} powered by)	Low-speed external oscillator and RTC are on	2.4	

Note: The above are measured parameters

3.3.5 External clock source characteristics

Table 3-9 From external high-speed clock

symbol	parameter	condition	Minimum	Typical Value	Maximum	Unit
F_{HSE_ext}	External clock frequency			8	25	MHz
V_{HSEH} [1]	OSC_IN input pin high voltage		$0.8V_{DD}$		V_{DD}	V
V_{HSEL} [1]	OSC_IN input pin low voltage		0		$0.2V_{DD}$	V
$C_{in(HSE)}$	OSC_IN input capacitance			5		pF
$DuCy_{(HSE)}$	Duty cycle			50		%

Note: 1. Failure to meet this condition may cause level recognition errors.

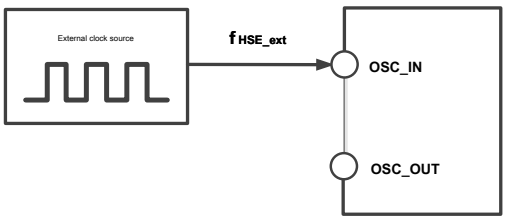

Figure 3-3 External high-frequency clock source circuit

Table 3-10 From external low-speed clock

symbol	parameter	condition	Minimum	Typical Value	Maximum	Unit
F_{LSE_ext}	User external clock frequency			32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high voltage		$0.8V_{DD}$		V_{DD}	V

V_{LSEL}	OSC32_IN input pin low voltage		0		0.2V_{DD}	V
$C_{in(LSE)}$	OSC32_IN input capacitance			5		pF
DuCy(LSE)	Duty cycle			50		%

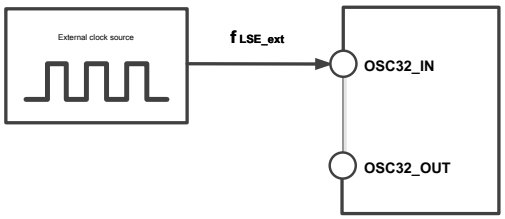

Figure 3-4 External low-frequency clock source circuit

Table 3-11 Use A crystal/ceramic resonator produces high-speed external Clock

symbol	parameter	condition	Minimum	Typical Value	Maximum	Unit
F_{OSC_IN}	Resonator frequency		4	8	16	MHz
I_2 [1]	HSE drive current	V_{DD} = 3.3V, 20p load		0.2		mA
g_m [1]	Oscillator Transconductance	start up		4.6		mA/V
$t_{SU(HSE)}$	Start Time	V_{DD} Is stable		1		ms

Note: 1. Design parameters

Circuit reference design and requirements:

The load capacitance of the crystal is generally 20pF (C_{L1} C_{L2} , Recommended 5 ~ 25pF), please refer to the manufacturer's data manual of the crystal used in practice.

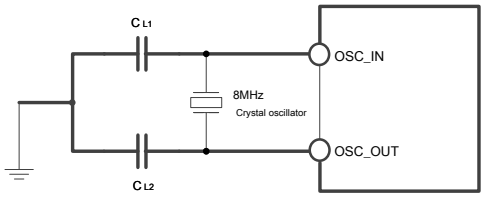

Figure 3-5 Typical circuit of external 8M crystal

Table 3-12 Use Low speed external produced by a crystal/ceramic resonator Clock (f(LSE) 32.768KHz) symbol

	parameter	condition	Minimum	Typical Value	Maximum	Unit
i_2 [1]	LSE drive current	V_{DD} = 3.3V		0.5		uA
g_m [1]	Oscillator Transconductance	start up		13.5		uA/V
$t_{SU(LSE)}$	Start Time	V_{DD} Is stable		200		mS

Note: 1. Design parameters.

Circuit reference design and requirements:

The load capacitance of the crystal is generally not more than 15pF (C_{L1} C_{L2} , Recommended 5 ~ 15pF), in fact, please refer to the manufacturer's data manual of the

crystal used.

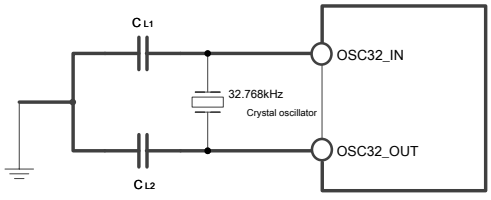

Figure 3-6 Typical circuit with external 32.768K crystal

Note: Load capacitance C_L Calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, Where C_{stray} It is the capacitance of the pin and the capacitance related to the PCB or

PCB. Its typical value is between 2pF and 7pF.

3.3.6 Internal clock source characteristics

Table 3-13 Characteristics of the internal high-speed (HSI) RC oscillator

symbol	parameter	condition	Minimum	Typical Value	Maximum	Unit
F_{HSI}	frequency			8		MHz
$DuCy_{HSI}$ Duty cycle			45	50	55	%
ACC_{HSI}	Accuracy of HSI oscillator	T_A= 0℃~70℃	- 1.5		1.5%	
		T_A=- 40℃~85℃	- 2		2	%
$t_{SU(HSI)}$	HSI oscillator start-up time				2.6 us	
$I_{DD(HSI)}$	HSI oscillator power consumption			200		uA

Table 3-14 Internal low speed (LSI) RC oscillator characteristics

symbol	parameter	condition	Minimum	Typical Value	Maximum	Unit
F_{LSI}	frequency		25	36	60	KHz
$DuCy_{LSI}$ Duty cycle			45	50	55	%
$t_{SU(LSI)}$	LSI oscillator start-up time				82	us
$I_{DD(LSI)}$ [1]	LSI oscillator power consumption			0.6		uA

Note: 1. Design parameters

3.3.7 PLL characteristics

Table 3-15 PLL characteristics

symbol	parameter	condition	Typical minimum value	maximum	Value	unit
F_{PLL_IN}	PLL input clock		4	8	16	MHz
	PLL input clock duty cycle [1]		40		60	%
F_{PLL_OUT}	PLL frequency multiplied output clock				80	MHz
t_{LOCK} [1]	PLL lock time				1000	$1/F_{PLL\_IN}$

Note: 1. Design parameters

3.3.8 Time to wake up from low power mode

Table 3-16 Time symbols for wake-up in

low-power mode	parameter	condition	Typical	unit
$t_{wusleep}$ Wake up from sleep mode		Wake up using HSI RC clock	5.8 us	
t_{wustop}	Wake up from stop mode (voltage regulator is in run mode)	HSI RC clock wakeup	253	us
	Wake up from stop mode (voltage regulator in low power mode)	Voltage regulator wake-up time from low power mode + HSI RC clock wake-up + flash boot	253	us
$t_{WUSTDBY}$ Wake up from standby mode		Voltage regulator wake-up time from low power mode + HSI RC clock wake-up + flash boot	340	us

3.3.9 Memory characteristics

Table 3-17 Flash memory characteristics

symbol	parameter	condition	Minimum	Typical Value	Maximum	Unit
t_{ERASE_128}	Page (128 bytes) programming time	T_A=-40℃~85℃	2.5	2.75	3	ms
t_{ERASE}	Page (128 bytes) erase time	T_A=-40℃~85℃	2.5	2.75	3	ms
t_{prog}	16-bit programming time	T_A=-40℃~85℃	2.5	2.75	3	ms
t_{ERASE}	Page (1K byte) erase time	T_A=-40℃~85℃	20	twenty two	twenty four	ms
t_{ME}	Chip erase time	T_A=-40℃~85℃	2.5	2.75	3	ms
V_{prog}	Programming voltage		2.7		5.5 V	

Table 3-18 Flash memory Memory life and data retention period

symbol	parameter	condition	Minimum	Typical Value	Maximum	Unit
N_{END}	Erasing times	T_A=25℃	10K	80K[1]		Times
t_{RET}	Data retention period		10			year

Note: The measured times of operation and erasure are not guaranteed.

3.3.10 I/O port characteristics

Table 3-19 General I/O Static Characters

number	parameter	condition	Minimum	Typical Value	Maximum	Unit
V_{IL}	Input low voltage	TTL port	- 0.3		0.8 V	
V_{IH}	Standard I/O pin, input high voltage	TTL port 2.7V<V_{DD}< 4.2V	2		V_{DD}+ 0.3	V
		TTL port 4.2V≤V_{DD}< 5.5V	0.55V_{DD}		V_{DD}+ 0.3	V
V_{IL}	Input low voltage	CMOS port	- 0.3		0.8 V	
V_{IH}	Input high voltage		0.65V_{DD}		V_{DD}+ 0.3	V
V_{hys}	Standard I/O pin Schmitt trigger voltage hysteresis			330		mV
I_{lkg}	Input leakage current				±1	uA
R_{PU}	Weak pull-up equivalent resistance		30	42	55	KΩ
R_{PD}	Weak pull-down equivalent resistance		30	42	55	KΩ
C_{IO}	I/O pin capacitance			5		pF

Note: The above are design parameters

Output drive current characteristics

GPIO (General Purpose Input/Output Port) can sink or output up to ±8mA current, and sink or output ±20mA current (not strictly up to V_{OL}/V_{OH}). In user applications, the total current driven by all IO pins must not exceed the absolute maximum ratings given in Section 3.2:

Table 3-20 Output voltage characteristics

symbol	parameter	condition	Minimum	Maximum	Unit
V_{OL}	Low level output, single pin sinks current	TTL port, I_{IO}=+8mA		0.4 V	
V_{OH}	Output high level, single pin output current	2.7V< V_{DD}< 5.5V	V_{DD}-0.4		V
V_{OL}	Low level output, single pin sinks current	CMOS port, I_{IO}=+8mA		0.4 V	
V_{OH}	Output high level, single pin output current	2.7V< V_{DD}< 5.5V	2.3		V

V_{OL}	Low level output, single pin sinks current	$I_{IO=+}$ 20mA		1.3 V	
V_{OH}	Output high level, single pin output current	2.7V< $V_{DD<}$ 5.5V	V_{DD-} 1.3		V

Note: If multiple IO pins are driven simultaneously under the above conditions, the sum of the currents cannot exceed the absolute maximum ratings given in Table 3.2. In addition, when multiple IO pins are driven at the same time, the current on the power/ground point is very large, which will cause a voltage drop so that the internal IO voltage does not reach the power supply voltage in the table, resulting in the drive curr

Table 3-21 Input input AC characteristics

MODEx[1:0] Configuration	symbol	parameter	condition	Minimum and maximum units		
10 (2MHz)	$F_{max(IO)out}$	Maximum frequency	CL=50pF, VDD=2.7-5.5V		2	MHz
	$t_{f(IO)out}$	Output high to low fall time	CL=50pF, VDD=2.7-5.5V		125	ns
	$t_{r(IO)out}$	Output low to high rise time			125	ns
01 (10MHz)	$F_{max(IO)out}$	Maximum frequency	CL=50pF, VDD=2.7-5.5V		10	MHz
	$t_{f(IO)out}$	Output high to low fall time	CL=50pF, VDD=2.7-5.5V		25	ns
	$t_{r(IO)out}$	Output low to high rise time			25	ns
11 (50MHz)	$F_{max(IO)out}$	Maximum frequency	CL=30pF, VDD=2.7-5.5V		50	MHz
			CL=50pF, VDD=2.7-5.5V		30	MHz
	$t_{f(IO)out}$	Output high to low fall time	CL=30pF, VDD=2.7-5.5V		20	ns
			CL=50pF, VDD=2.7-5.5V		5	ns
	$t_{r(IO)out}$	Output low to high rise time	CL=30pF, VDD=2.7-5.5V		8	ns
			CL=50pF, VDD=2.7-5.5V		12	ns
	t_{EXTIpw}	EXTI controller detects the pulse width of an external signal		10		ns

Note: The above are design parameters

3.3.11 NRST pin characteristics

Table 3-22 External reset pin characteristics

symbol	parameter	condition	Minimum	Typical Value	Maximum	Unit
$V_{IL(NRST)}$ [1]	NRST input low voltage		- 0.3		0.8 V	
$V_{IH(NRST)}$ [1]	NRST input high voltage		0.65V_{DD}		V_{DD+} 0.5	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			330		mV
R_{PU} [2]	Weak pull-up equivalent resistance		30	42	55	KΩ
$T_{F(NRST)}$ [1]	NRST input filter pulse				4	ns
$T_{NF(NRST)}$ [1]	NRST input unfiltered pulse		20			ns

Note: 1. Design parameters

2. The pull-up resistor is a real resistor connected in series with a switchable PMOS. The resistance of this PMOS/NMOS switch is very small (about 10%).

Circuit reference design and requirements:

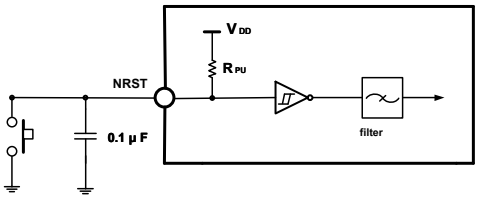

Figure 3-7 Typical circuit of external reset pin

3.3.11 TIM timer features

Table 3-23 TIMx characteristics

symbol	parameter	condition	Minimum and maximum units		
$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	13.9		ns
F_{EXT}	Timer external clock frequency of CH1 to CH4		0	$f_{TIMxCLK}$/ 2	MHz
		$f_{TIMxCLK}$ = 72MHz	0	36	MHz
R_{esTIM}	Timer resolution			16	Bit
$t_{COUNTER}$	When the internal clock is selected, the 16-bit counter clock period		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	0.0139	910	us
t_{MAX_COUNT}	Maximum possible count			65535	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz		59.6	s

Note: The above are design parameters

3.3.12 I2C interface characteristics

Table 3-24 I2C interface features

symbol	parameter	Standard I2C		Fast I2C		unit
		Min	Max	Max	Min	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.2		us
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		us
$t_{SU(SDA)}$	SDA data establishment time	250		100		ns
$t_{h(SDA)}$	SDA data retention time	0		0	900	ns
$t_{r(SDA)}$/ $t_{r(SCL)}$	SDA and SCL rise time		1000	20		ns
$t_{F(SDA)}$/ $t_{F(SCL)}$	SDA and SCL fall time		300			ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		us
$t_{SU(STA)}$	Repeated start condition establishment time	4.7		0.6		us
$t_{SU(STO)}$	Stop condition establishment time	4.0		0.6		us
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.7		1.2		us
C_b	Capacitive load per bus		400		400	pF

Note: The above are design parameters

3.3.12 SPI interface features

Table 3-25 SPI interface features

symbol	parameter	condition	Minimum and maximum units		
f_{SCK}	SPI clock frequency	Main mode		36	MHz
		Slave mode		36	MHz
$t_{r(SCK)}$/ $t_{f(SCK)}$	SPI clock rise and fall time load capacitance: C = 30pF			20	ns
$t_{SU(NSS)}$	NSS establishment time	Slave mode	$2t_{PCLK}$		ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{PCLK}$		ns
$t_{w(SCKH)}$/ $t_{w(SCKL)}$	SCK high and low time main mode, f_{PCLK} = 36MHz, prescaler Coefficient = 4		40	60	ns
$t_{SU(MI)}$	Data input establishment time	Main mode	5		ns

		Slave mode	5		ns
$t_{h(MI)}$	Data input hold time	Main mode	5		ns
		Slave mode	4		ns
$t_{a(SO)}$	Data output access time	**Slave mode, f_{PCLK}= 20MHz**	0	$1t_{PCLK}$	ns
$t_{dis(SO)}$	Data output prohibition time	Slave mode	0	10	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enabling edge)		25	ns
$t_{v(MO)}$	Data output valid time	Master mode (after enabling edge)		5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enabling edge)	15		ns
$t_{h(MO)}$		Master mode (after enabling edge)	0		ns

3.3.13 USB interface features

Table 3-26 USB module features

symbol	parameter	condition	Minimum and maximum units		
V_{DD}	USB operating voltage	Disable USB5VSEL control bit	3.0	3.6 V	
		Enable USB5VSEL control bit	4.0	5.5	
V_{SE} [1]	Single-ended receiver threshold	**V_{DD}= 3.3V**	1.2	1.9 V	
		V_{DD}= 5V	1.2	2	
V_{OL}	Static output low level			0.3 V	
V_{OH}	Static output high level		2.8	3.6 V	

Note: 1. Design parameters

3.3.14 12-bit ADC features

Table 3-27 ADC characteristics

symbol	parameter	condition	Minimum Typical Value Maximum Unit			
V_{DDA}	Supply voltage		3.0		5.5 V	
f_{ADC}	ADC clock frequency				14	MHz
f_S	Sampling rate				1	MHz
f_{TRIG}	External trigger frequency	**f_{ADC}= 14MHz**			875	KHz
					16	**$1/f_{ADC}$**
V_{AIN}	Conversion voltage range		0		v_{DDA}	V
R_{AIN}	External input impedance				58	KΩ
R_{ADC}	Sampling switch resistance			0.6	0.75 KΩ	
C_{ADC}	Internal sample and hold capacitor			30		pF
t_{lat}	Injection trigger conversion delay	**f_{ADC}= 14MHz**			0.143	us 2
						$1/f_{ADC}$
t_{latr}	Regular trigger conversion delay	**f_{ADC}= 14MHz**			0.143	us 2
						$1/f_{ADC}$
t_s	sampling time	**f_{ADC}= 14MHz**	0.107		17.1 us	
			1.5		239.5	**$1/f_{ADC}$**
t_{STAB}	Power on time				1	us
t_{CONV}	**Total conversion time (including sampling time) f_{ADC}= 14MHz**		1		18	us
			14		252	**$1/f_{ADC}$**

Note: The above are design parameters

Formula: Max R_{AIN}

$$R_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln 2^{N+2}} - R_{ADC}$$

The above formula is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. N=12 (indicating 12-bit resolution).

Table 3-28 f_{ADC} - Maximum R at 14MHz $_{AIN}$

T_{S}(cycle)	t_{S}(us)	Max R_{AIN}(KΩ)
1.5	0.11	0 (not recommended)
7.5	0.54	1.1
13.5	0.96	2.6
28.5	2.04	6.2
41.5	2.96	9.4
55.5	3.96	12.9
71.5	5.11	16.8
239.5	17.1	58

Note: The above are design parameters

C_p Indicates the parasitic capacitance (approximately 5pF) on the PCB and the pad, which may be related to the quality of the pad and PCB layout. Larger C_p The value will reduce the conversion accuracy, the solution is to reduce f_{ADC} value.

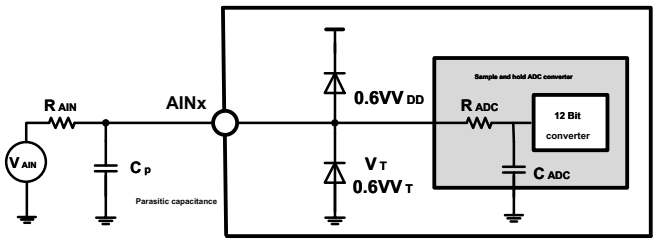

Figure 3-8 ADC typical connection diagram

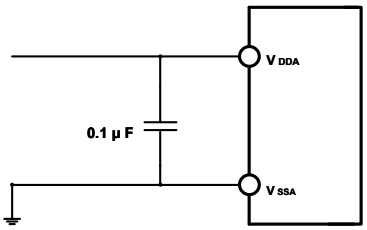

Figure 3-9 Analog power supply and decoupling circuit reference

3.3.15 Temperature sensor characteristics

Table 3-29 Temperature sensor characteristics

symbol	parameter	condition	Minimum	Typical Value	Maximum	Unit
Avg_Slope	Mean slope		3.3	4.3	5.3	mV/℃
V_{25}	Voltage at 25℃		1.11	1.34	1.57	V
T_{S_temp}	When reading the temperature, the ADC sampling time f_{ADC} - 14MHz				17.1	us

Note: The above are design parameters.

3.3.16 TKey module features

Table 3-29 TKey module features

symbol	parameter	condition	Minimum	Typical Value	Maximum	Unit
I_{TKey}	Module working current	V_{DD}= 3.3V	211	270	421	uA

Chapter 4 Packaging Information

Chip package

Package width of plastic body		Lead pitch		Package description	Order model
LQFP48	7*7mm	0.5mm	19.7mil Standard LQFP48 foot patch	CH32V103C6T6	
LQFP48	7*7mm	0.5mm	19.7mil Standard LQFP48 foot patch	CH32V103C8T6	
QFN48X7	7*7mm	0.5mm	19.7mil Square leadless 48-pin patch	CH32V103C8U6	
LQFP64M	10*10mm	0.5mm	19.7mil LQFP64M (10*10) patch	CH32V103R8T6	

Note: The unit for dimensioning is mm (millimeters), the center distance between the pins is always the nominal value, there is no error, and the other dimension error is not greater than ±0.4mm or 15%.

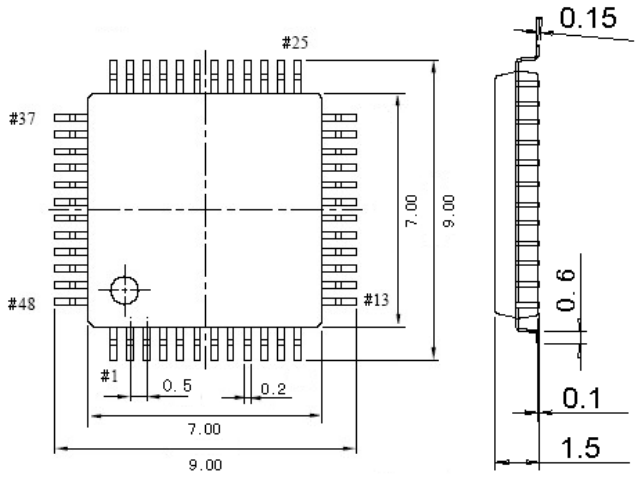

Figure 4-1 LQFP48 package

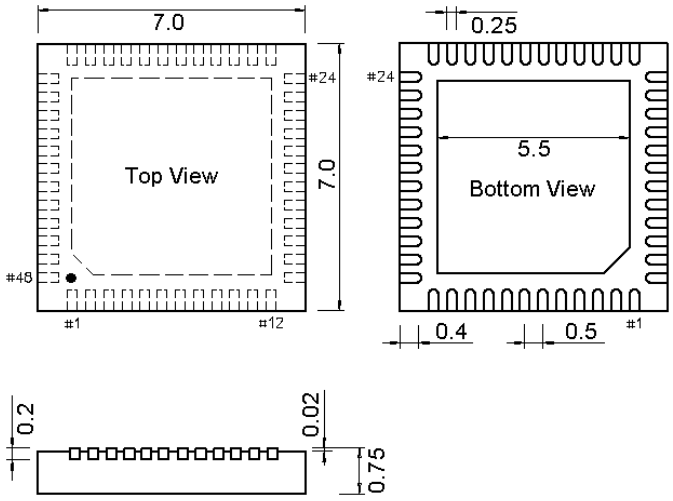

Figure 4-2 QFN48X7 (QFN48-7*7) package

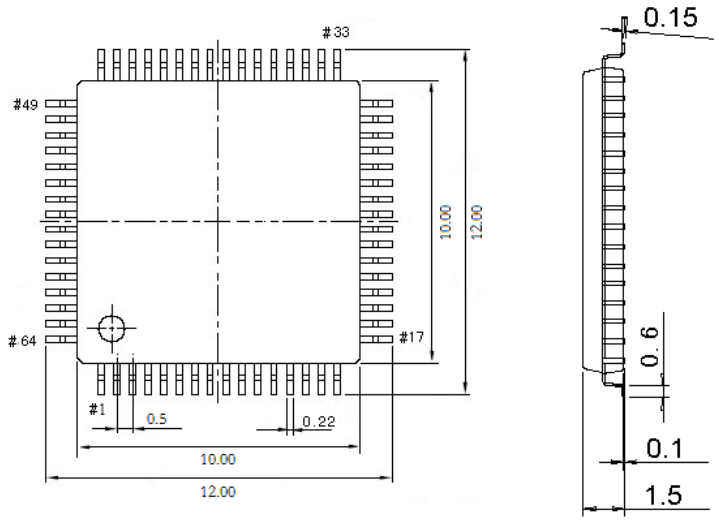

Figure 4-3 LQFP64M (LQFP64-10*10) package