

Bucket Brigade Devices: MN3007 (/mn3007-bucket-brigade-devices)

The Bucket Brigade Device *BBD* chip was invented by F. Sangster and K. Teer at the Philips Research Labs between 1968-1969. This affordable solid state device provides signal delay and soon found many applications in a wide range of products, especially guitar effects being a midpoint between the bulky old *pure analog* delay circuits based on magnetic tape and the modern *digital* systems based in Analog to Digital converters and signal processors.

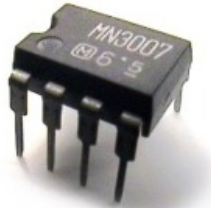


Table of Contents.

1. BBD Functionality. (/mn3007-bucket-brigade-devices#link1)
2. BBD Internal Circuit Topologies. (/mn3007-bucket-brigade-devices#link2)
 - 2.1 Basic Topology. (/mn3007-bucket-brigade-devices#link21)
 - 2.2 Tetrode Isolation Topology. (/mn3007-bucket-brigade-devices#link22)
 - 2.3 Complementary Output Topology. (/mn3007-bucket-brigade-devices#link23)
 - 2.4 Dual Topology. (/mn3007-bucket-brigade-devices#link24)
 - 2.5 Tapped Output Topology. (/mn3007-bucket-brigade-devices#link25)
3. BBD Chips Comparison. (/mn3007-bucket-brigade-devices#link3)
4. Bucket Brigade Device Clock Drivers. (/mn3007-bucket-brigade-devices#link4)
 - 4.1 BBD Clock Limitations. (/mn3007-bucket-brigade-devices#link41)
5. BBD Circuits Architecture. (/mn3007-bucket-brigade-devices#link5)
 - 5.1 Filter Implementation. (/mn3007-bucket-brigade-devices#link51)
6. The MN3007. (/mn3007-bucket-brigade-devices#link6)
 - 6.1 MN3007 VS MN3207. (/mn3007-bucket-brigade-devices#link61)
7. Resources. (/mn3007-bucket-brigade-devices#link7)
 - 7.1 BBDs Datasheets. (/mn3007-bucket-brigade-devices#link71)

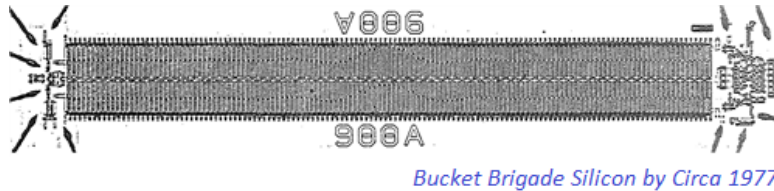
1. BBD Functionality.

BBDs are given their name because of the similarity in their functionality to a line of people passing buckets of water to fight a fire. The chip was licensed to Matsushita from mid-70s, Roland/Boss was the first customer and they used it in the Roland JC120 Amplifier, the Chorus CE-1 pedal and later on the Chorus CE-2 (/boss-ce-2-analysis).



Fire Bucket Brigade by Monroe Historical Society

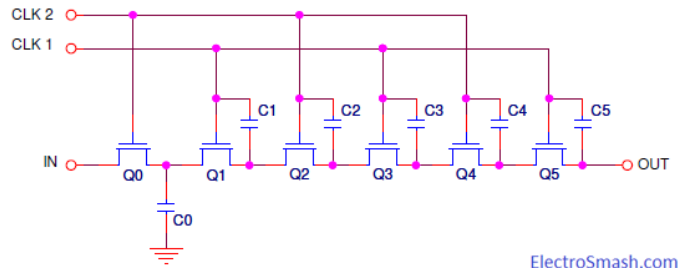
(<http://www.stepneyct.org/history/ht/stop17.html>)



(/images/tech/mn3007/bbd-topology-basic.png)

They consist of a series of capacitors sections which carry the analog signal. The charge in each cap stage is passed into the subsequent stage using transistors as switches at a rate determined by an external clock.

In this way, the output delayed signal is discrete in time due to the external clock sampling and analog in amplitude because of the capacitor storage element.



(/images/tech/mn3007/bbd-basic.png)

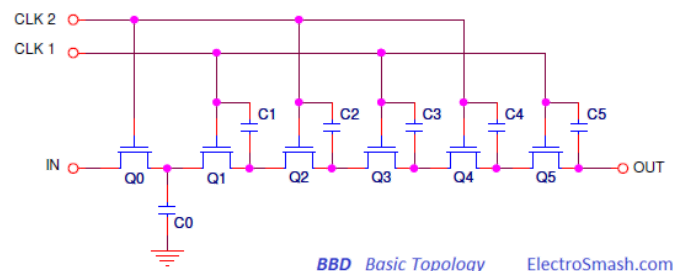
With the high level of CLK2, the input signal is gated through Q_0 to the capacitor C_0 . At the next clock transition, C_0 is isolated and the last voltage applied to C_0 is held. As CLK2 goes down, CLK1 rises allowing the charge on C_0 to be gated to the storage capacitor C_1 . On the next clock transition, gating transistor Q_1 is disabled and Q_2 is enabled to allow the charge in C_1 to pass the next stage C_2 . The process is repeated through the circuit until the same voltage appears at the output.

2. BBD Internal Circuit Topologies.

The basic BBD internal schematic is made of a series of typically thousands of capacitors and MOS transistor switches. The design suffered some modifications to enhance its performance:

2.1 The Basic Topology.

The basic model invented by Sangster at Philips in 1968. It was the first attempt to make a practical implementation of an analog delay structure. This initial design had a poor transfer efficiency being limited to few stages and low-frequency applications.

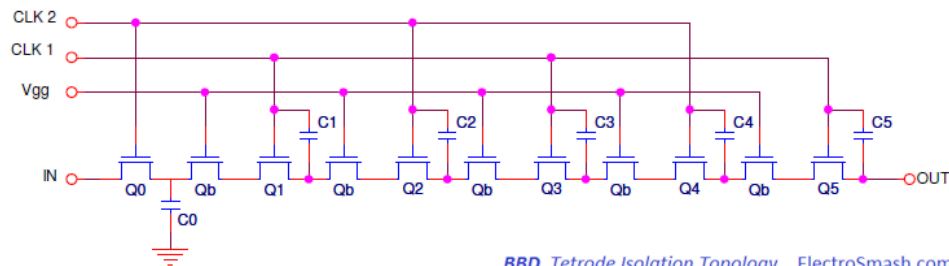


(/images/tech/mn3007/bbd-topology-basic.png)

2.2 The Tetrode Isolation Topology.

The first major advance also by Sangster at Reticon Corporation, introduces an isolation of tetrode structure with a DC biased gate NMOS transistor separating each clock element.

Two out of phase clk lines are required: one to govern the even-numbered caps and the other to drive the odd-numbered ones. The performance was enhanced being able to use it in audio applications.

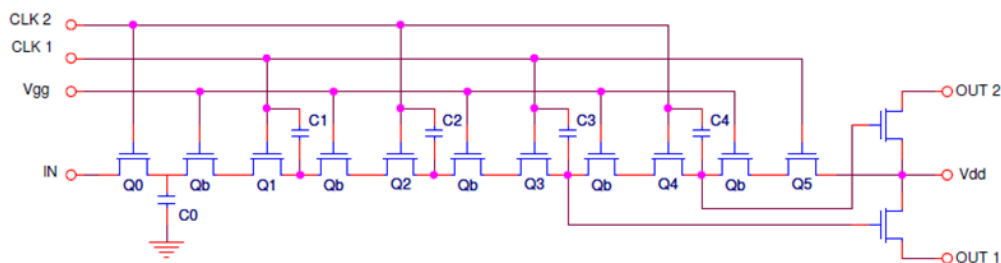


BBD Tetrode Isolation Topology ElectroSmash.com

(/images/tech/mn3007/bbd-topology-tetrode-isolation.png) Between each of this switch transistors, there is a capacitor (charge-holding element) which is separated by a DC-biased gate transistor, which greatly improves transfer efficiency. Only half of the caps carry information, the other half remain charged

2.3 The Complementary Output Topology.

The output architecture was enhanced using two source follower transistors connected to the last two consecutive capacitors, resulting in a full wave output. Mixing these two outputs a more continuous output waveform is generated, providing a means of improved suppression of clocking glitches.

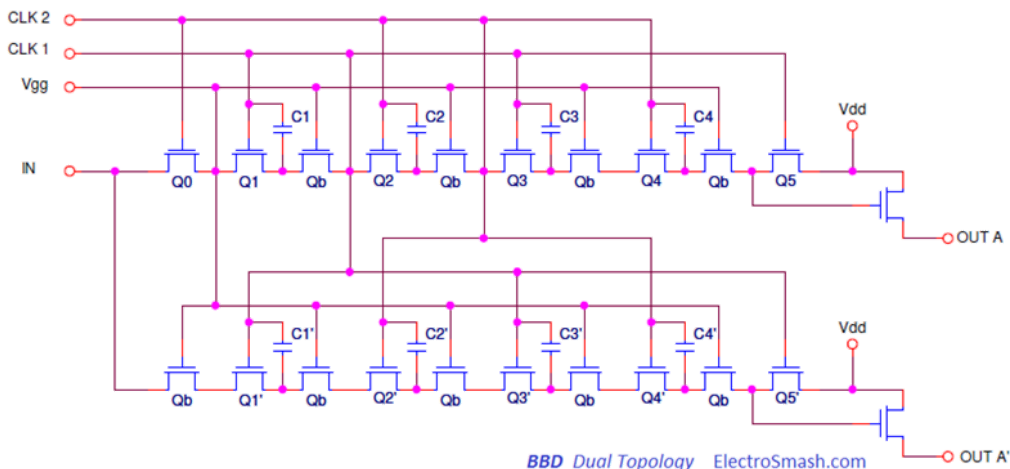


BBD Complementary Outputs Topology ElectroSmash.com

(/images/tech/mn3007/bbd-topology-complementary-outputs.png) Some designs use a trim-pot to vary the load termination between the two output followers to minimize clock frequency component due to V_{GS} between them. This could be useful if running very low clock frequencies, and tight filter skirts to passband.

2.4 Dual Topology.

Another well-known topology is the *Dual Delay Line* which is made of two delay sections running in parallel:



BBD Dual Topology ElectroSmash.com

(/images/tech/mn3007/bbd-topology-dual.png)

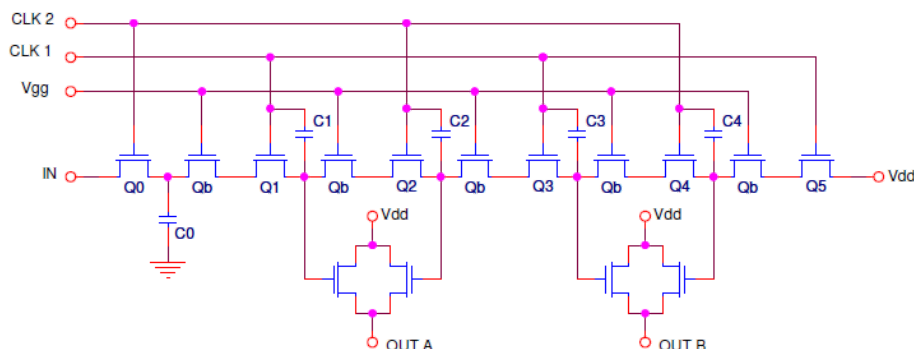
This approach offers flexible performance:

- Each section can be used independently, only sharing the power supply.
- Each section can be connected in series to get double delay time for a given sample rate.
- Each section can be multiplexed to double the sample rate.
- Each section can be operated in differential mode in order to reduce even harmonic distortion.
- Several devices can be connected in series.

For more details about these configurations check the Reticon SAD1024 datasheet.

2.5 The Tapped Output Topology.

A buffer amplifier (NMOS source follower) can be used for non-destructive sampling of the capacitors. These measure points or *taps* permit to have multiple outputs with a different delay, which is very interesting in order to model reverb effects, mixing the different delayed output signals properly.

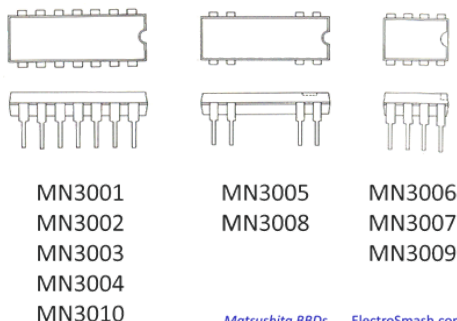


BBD Output Tapper Topology ElectroSmash.com

(/images/tech/mn3007/bbd-output-tapper-topology.png)

3. BBD Chips Comparison.

The most common BBD chips come from Panasonic/Matsushita MN3xxx series, with variants for high/low supply voltage and the number of stages.



Matsushita BBDs ElectroSmash.com

(/images/tech/mn3007/bbds-matsushita.png)

Besides Panasonic/Matsushita, other companies were licensed to make BBD clones like Behringer which bankroll Coolaudio and started producing MN3207/3208/3205 clones for their own production needs. Visual Sound recommissioned production of MN3102/MN3207 in 2009. Shangai Beilling Co LTD manufactures pin compatible parts with Panasonic/Matsushita chips, labeled with BL instead of MN.

	Item	Symbol	MN3001	MN3002	MN3003	MN3004	MN3005	MN3006	MN3007	MN3008	MN3009	MN3010	MN3011	MN3012	Unit	
	Number of BDD	N	Dual-512	512	Dual-64	512	4096	128	1024	2048	256	Dual-512	3328 6-Tap	190, 3, 5 3-Tap	Stage	
Circuit Construction	Clock Generator		External		Built-in	External								Built-in		
	Output Terminal				Pair								6 Different Taps	3 Different Taps		
Operating Conditions	Drain Supply Voltage	V _{DD}	-15		-9	-15	-15	-15	-15	-15	-15	-15	-15	-15	V	
	Gate Supply Voltage	V _{GG}	-14		-8	-14	-14	-14	-14	-14	-14	-14	-14	-	V	
	Back-Gate Bias Voltage	V _{BB}	+5		Not Needed									V		
	Clock Voltage "H" Level	V _{CPH}	0		0	0	0 ~ -1	0 ~ -1	0 ~ -1	0 ~ -1	0 ~ -1	0 ~ -1	0 ~ -1.3	-0 ~ -0.4	V	
	Clock Voltage "L" Level	V _{CPH}	-15		-9	-15	-15	-15	-15	-15	-15	-15	-15	-15	V	
	Input DC Bias	V _{Bias}	-3.3 ~ -4.9		-2.5 ~ -6	-5 ~ -10	-5 ~ -10	-5 ~ -10	-5 ~ -10	-5 ~ -10	-5 ~ -10	-5 ~ -10	-	-3 ~ -12	V	
Electrical Characteristics	Input Signal Frequency	f _i	12				10	12				14	12	10	12	kHz [max.]
	Input Signal Swing	V _i	1.8		0.8	1.8	1.2	1.8	1.5	1.5	1.7	1.8	1.0	1.2	V _{rms} [max.]	
	Insertion Loss	L _i	8.5		3.5	1.5	0	0	0	0	0	0	0	0	dB [typ.]	
	Total Harmonic Distortion	THD	0.4		0.5	0.4	1	0.2	0.5	0.5	0.3	0.4	0.4	0.4	% [typ.]	
	Noise Voltage	V _{no}	250 (typ.)		140	210	400	200	300	300	150	210	0.4	0.4	μV _{rms} [max.]	
	Signal to Noise Ratio	S/N	70		75	85	75	90	80	78	88	85	76	0.01 = 90 0.475 = 85 0.0125 = 97 0.012 = 98	dB [typ.]	
	Signal Delay Time	t _D	51.2	25.6	6.4	25.6	204.8	6.4	51.2	102.4	12.8	51.2	¹⁰ max 198, 201 50.7 max 3, 129.5, 166.4	0.0125 ~ 0.25 0.0075 ~ 0.15	msec [max.]	
Package (Molded Package)		14-Pin DIP					Larger 8-Pin DIP	8-Pin DIP		Larger 8-Pin DIP	8-Pin DIP	14-Pin DIP	12-Pin DIP	14-Pin DIP		

[Matsushita BBDs Comparison Table](#) [ElectroSmash.com](#)

(/images/tech/mn3007/bbd-comparison.png) Reticon manufactured the popular BBD chips SAD512, SAD1024 and SAD4096, whose suffix represents the number of BBD stages.

Less common chips include the Reticon R51xx and RD51xx series and the Philips TDA1022.

4. Bucket Brigade Devices Clock Drivers.

In order to make a BBD system fully working, a complementary clock signal generator driver is needed. Matsushita/Panasonic MN31xx series have a convenient small footprint package designed to match with their respective BBD and providing:

- A two-phase clock with low impedance and the proper capacitance. The frequency value is selected by a simple RC network.
- Stable V_{GG} power supply used to DC bias the base of the charge-holding elements, which greatly improves transfer efficiency, $V_{GG} = 4/15 * V_{CC}$.

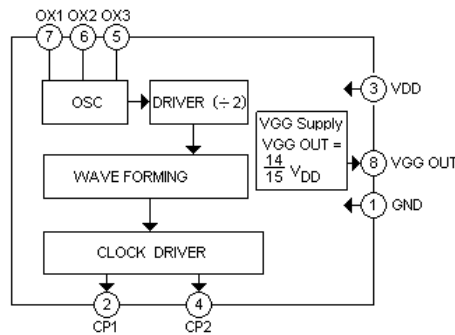


Image by CBTricks.com

(/images/tech/mn3007/bbd%20clock.gif)

The usage of these devices is not mandatory, some designers in order to reduce costs, have more flexibility or achieve higher clock rates use simple voltage dividers to get V_{GG} and oscillator parts like CD4046 (used in Zombie Chorus), CD4047 (used in Small Clone, Carbon Copy, and A/DA Flanger) or 4013 (used in Electric Mistress) to generate the double clock signal.

4.1 BBD Clock Limitations.

Following the datasheet recommendations, BBDs guaranteed a correct behavior under a certain clock frequency (100~200KHz). It is because the input capacitance of the clock pins causes progressive degradation of clock pulses above the frequency limit: The clock pulses change from square to a trapezoidal/sawtooth waveform. When that happens the switching action is not perfectly synchronized resulting in a signal degradation.

The clock frequency limitation is the reason why the Reticon SAD1024 chip was a largely preferred choice for flangers effects which involve short delay and fast clock: the input capacitance on the clock pins was much lower (110pF) than on the MN3007 (700pF), allowing it to be clocked at much higher frequencies.

When suitably buffered, though, there are reports of it clocking MN3xxx chips up well past 1MHz, which takes the device close the zero-delay zone, being convenient for fine flanger effects.

BBD Sampling Time Limitations: For any BBD, the total delay time can be calculated as:

where:

N: is the number of stages.

f_{clock} : is the circuit clock frequency.

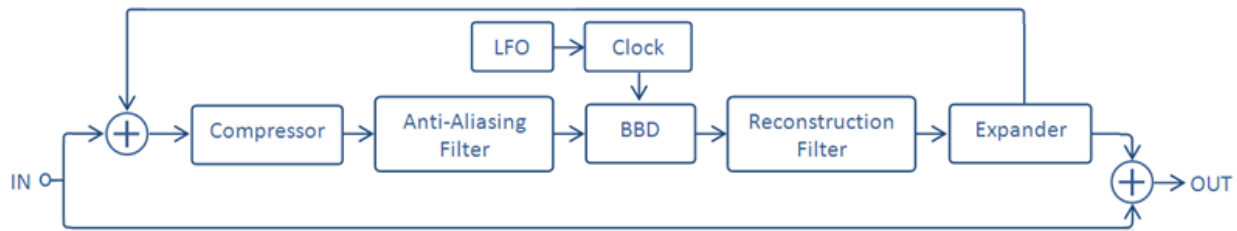
The clock signals applied to the BBD will determine the signal sampling time, this sampling time should respect the Nyquist-Shannon Theorem:

$$f_{\text{sampling}} < 2 \cdot f_{\text{signal}}$$

- For short delay effects like flanging, the input signal can be oversampled, there is no penalty in terms of signal degradation. If the clock signal goes beyond the BBD clock boundary, the clk signal can be degraded as explained above and the audio waveform corrupted.
- For long delay effects like delay, the input signal is can be undersampled, the resulting processed signal will be degraded but the total delay time is extended.

5. Typical Circuit with BBD Architecture.

The BBDs are found in delay based effects such as echo, chorus, reverb, vibrato, flanging or delay all of them share the same general circuit architecture:



BBD Circuit Architecture ElectroSmash.com

(/images/tech/mn3007/bbd-architecture.png)

Part of the input signal is processed through the BBD chain. Depending on the clock circuit the specific effect is created: the Low-Frequency Oscillator *LFO* is used for flanger/chorus/vibrato effects to automatically modify the delay time. For other effects like a simple delay, it is not needed.

The output of the delay line or part of it can be feedbacked into the input with variable gain, generating trailing echoes. Before and after the BBD action, there are some stages needed to avoid signal degradation: Dynamic Range compression/expansion, Anti-Aliasing Filter and Reconstruction Filter:

- **Dynamic Range Companding (compression + expansion):** These circuits allow wider dynamic range signals to be processed at the cost of altering the signal dynamics. In order to obtain low THD and good Signal to Noise ratio, the input signal has to be close to the maximum input level of the BBD.

In some cases, the compression and expansion take place outside of the anti-aliasing and reconstruction filters, while in others, the compander is implemented directly at the input and output of the BBD. Some BBD systems that require companding utilize the 570/571 series chips. This integrated circuit consists of a pair of variable gain amplifiers and signal level averagers.

- **Anti-Aliasing Filter:** It is low pass filter used before a signal sampler, to restrict the bandwidth of a signal to approximately satisfy the Nyquist-Shannon sampling theorem. The sampled input signal must be bandlimited to prevent aliasing (meaning waves of higher frequency being recorded as a lower frequency).
- **Reconstruction Filter:** Also called *Anti-Imaging Filter* is again a low pass filter used to construct a smooth analog signal from a sampled input. The output signal must be bandlimited, to prevent aliasing (meaning Fourier coefficients being reconstructed as low-frequency waves, not as higher frequency aliases).
- **Feedback path:** The feedback path also varies from system to system; different circuits place it inside or outside of the compression and expansion circuitry.

Finally, the *wet* or processed signal is mixed with the *dry* original one, depending on this mix ratio the effect over the original signal will be more or less dramatic.

Drawbacks of Bucket Brigade Devices:

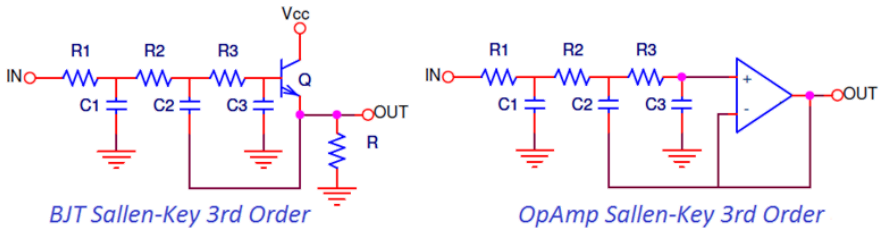
First of all, there is degradation of the capacitors charge as it passes through the bucket brigade, these losses deteriorate the quality of the delayed signal by introducing noise and distortion. The signal is slightly modified, but this is not a drawback necessarily, some players consider that this feature is unique in BBDs and contribute to create a warm or organic tone.

The process of passing the charge from bucket to bucket creates clocking noise in the signal. The output signal, therefore, looks like the audio signal, but there are "spikes" in the wave that corresponds to the clock frequency. The solution to this problem is to remove the spikes with a low pass filter, typically 30 or 36 dB per octave with a -3 dB point of around 3 kHz.

5.1 Filter Implementation.

The low pass filters used for Anti-Aliasing and Reconstruction must be strict to avoid signal distortion and keep the clock signal out of the audio path. Common configurations implement high order (2nd, 3rd, 4th) active filters using op-amps or transistors in Sallen-key configuration because of their simplicity.

In this, so called, *standard strategy* the cut-off frequency of the filters before and after the BBD is fixed according to the effect delay time:

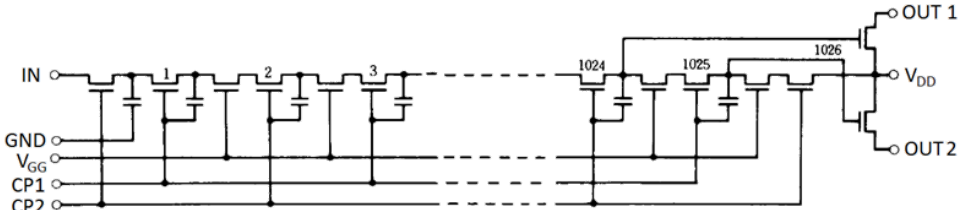


BBDs Low Pass Filters ElectroSmash.com

(/images/tech/mn3007/bbd-low-pass-filters.png)Another less common technique use switched capacitor filters, controlling the cut-off frequency by the signal clock frequency and therefore limiting the pass-band only to the necessary for a given clock frequency and improving the signal fidelity for shorter delay times.

6. The MN3007.

The MN3007 core is based on the Bucket Brigade Delay circuit with an isolated triode and a differential output. It was included in popular designs like the DM-1 and CE-2 by Boss (/boss-ce-2-analysis), Small Clone and Memory Man by Electro-Harmonix, AD-999 by Maxon or Analog Delay by MXR:



MN3007 Internal Circuit ElectroSmash.com

(/images/tech/mn3007/mn3007-internal-circuit.png)It consists of a 1024 PMOS silicon stage that provides a signal delay from 5.12 to 51.2ms. The S/N is 80dB typ, THD of 0.5% typ ($V_{in}=0.78V_{rms}$), supporting a clock frequency range from 10 to 100KHz. The supply voltage range is from -10 to -15V.

6.1 MN3007 vs MN3207.

There is some controversy among the MN3007 and MN3207 BBDs: some designers prefer to use the MN3007 because it has more headroom (higher levels/dynamic range without signal clipping) and therefore less distortion.

	MN3007	MN3207
Technology	PMos	NMos
S/N Ratio	80dB	73dB
THD	0.5% ($V_{in}=0.78V_{rms}$)	0.4% ($V_{in}=0.25V_{rms}$)
Max. Freq.	100KHz	200KHz
Delay Time	5.12 ~ 51.2ms	2.56 ~ 51.2ms
Power Supply	-10 to -15V	+5 to +10V

MN3207 is based in NMOS technology while MN3007 is PMOS (that is why it needs negative supply). Both are 1024-stage BBDs sharing the same internal circuit.

- S/N ratio is slightly better in MN3007 (80 vs 73dB).
- THD levels are similar 0.4-0.5% under different input V_{rms} (0.25V vs 0.78V), MN3007 accept input signals 3 times wider, having, in fact, better dynamic range and less noise.
- Maximum Clock frequency is better in MN3207 200 vs 100KHz, allowing shorter delays 2.56 vs 5.12ms.
- Regarding the power supply, the 3007 is made for high voltage (10 to 15V) and in a usual 9V pedals supply is below the ideal voltage and then ends up not with the performance which it was designed to work. The 3207 operates from 4 to 10V, being suitable for 9V powered effects and within the optimal supply range and also the 9V can be easily regulated to 5V giving a reliable standard behavior under all conditions.

Summarizing, using MN3007 will provide light advantages in terms of THD, and more dynamic headroom. In a guitar pedal, the chip will work at 9V, below the optimum supply range. So far seems that the performance in this conditions is good and preferred over the MN3207.

However, in BBD circuit design there are many other other factors that can improve the performance more than the chip itself:

- The use of compander circuitry to keep a ceiling on input signal levels.
- The bias voltage fine adjustment.
- The filtering applied, and the support circuitry (quality of clock pulse, mixing of complementary outputs, etc.)

7. Resources:

Official Panasonic Bucket Brigade Devices Databook (<http://www.sdiy.org/BBDHell/>) by Harry Bissell.

Practical Modeling of Bucket Brigade Device Circuits (http://dafx10.iem.at/papers/RaffelSmith_DAFx10_P42.pdf) by Raffael & Smith.

Anti-Aliasing Filters Application Note (<http://ww1.microchip.com/downloads/en/AppNotes/00699b.pdf>) by Microchip.

PAiA Phlanger (http://hammer.ampage.org/files/PAiA_Phlinger.PDF) in Hammer AmpPage.

Bucket Brigade Delay Line Application Note (<http://www.uk-electronic.de/PDF/mn3004.pdf>)

Bucket-brigade electronics - new possibilities for delay, time-axis conversion, and scanning by F. L. J. Sangster and K. Teer. (IEEE Journal vol. 4, no. 3, pp. 131-136, 1969.)

Bucket Brigade Devices Circa 1977.

(<http://www.imagesensors.org/Past%20Workshops/Marvin%20White%20Collection/1977%20Short%20Course/1977%203%20Weckler.pdf>)

- Bucket Brigade Devices Circa 1976.

(<http://www.imagesensors.org/Past%20Workshops/Marvin%20White%20Collection/1977%20Short%20Course/1977%203%20Weckler.pdf>)

The PT-80 Digital Delay (<http://www.generalguitargadgets.com/effects-projects/modulationecho/pt-80-delay/>) by General Guitar Gadgets.

www.CircularScience.com (<http://www.CircularScience.com>) by John Roberts.

7.1 Datasheets:

All MN3XXX, SAD512-1024-4096 and TDA1022 Datasheets (<http://www.experimentalistsanonymous.com/diy/Datasheets/>) by ExperimentalistAnonymous.

All MN3XXX, SAD512-1024-4096 and TDA1022 Datasheets (<http://hammer.ampage.org/files/BBDementia.zip>) by Mark Hammer.

Thanks for reading, all feedback is appreciated info@ElectroSmash.com

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