HTPA32x31L10/1.0S

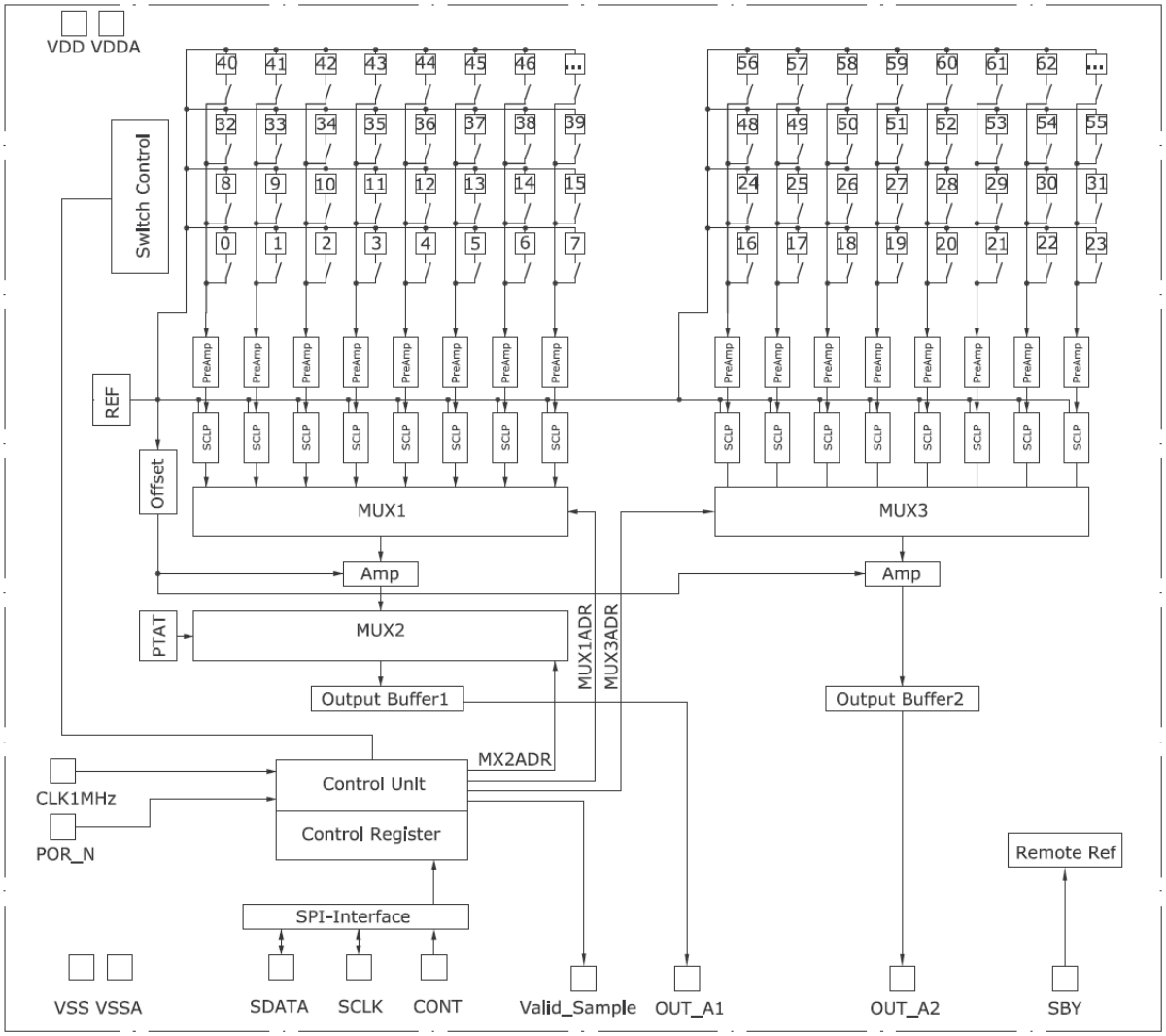
Thermopile Array With Lens Optics

Rev.2: 2014.08.12 Forg/Schnorr

This datasheet is valid for following parts:

HTPA32x31L10/1.0HiS[Si]
HTPA32x31L10/1.0S[Si]
HTPA32x31L10/1.0HiS
HTPA32x31L10/1.0S

Principal Schematic for HTPA32x31:



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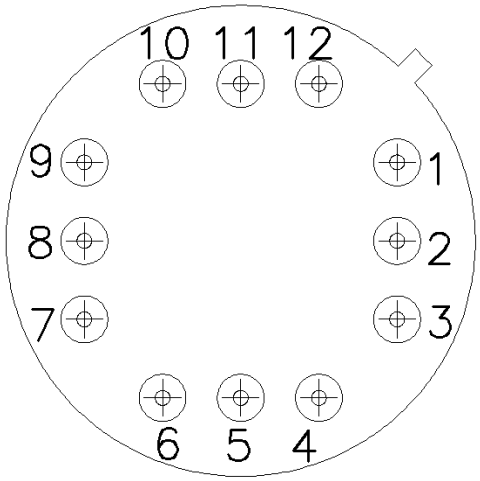
Pin Assignment in TO8 – Bottom View:



Connect all reference voltages via 100 nF capacitors to VSS.

Pin Assignment 32x31			
Pin	Name	Description	Type
1	MCLK	master clock	Digital Input
2	SCLK_IO	clock input/output for SPI	Digital Input/Output **
3	SBY	Standby	Digital Input***
4	VSAM	valid sample	Digital Output
5	DATA_IO	data input/output for SPI	Digital Input/Output **
6	OUT_A2	Analog Output	Analog Output
7	VCM_C	common mode voltage	Reference Voltage*
8	VREF_1225V	1.225V reference voltage	Reference Voltage*
9	OUT_A1	Analog Output	Analog Output
10	VSS	negative power supply voltage	Power
11	VDD	positive power supply voltage	Power
12	CONT	Control Pin for SPI	Digital Input

*) Connect via 100 nF to VSS
**) The HTPA32x31 has no ADC, but the valid sample cycle number is delivered.
***) Connect to VSS or NC for internal reference voltages. Connect to VDD if VREF_1225V and VCM_C are applied from external. See “Application Note HTPA” for details.

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Internal Register Map:

Num	Name	Function	Default	Notes
0	R	Reset	0	In case of 1, the mux pixel counter is reset. ASIC stays in reset.
1		spare	1	-not used- write '1' to this location
2		spare	0	-not used- write '0' to this location
3	MA0	Multiplexer address 0	0	-not used- write '0' to this location
4	MA1	Multiplexer address 1	0	-not used- write '0' to this location
5	MA2	Multiplexer address 2	0	-not used- write '0' to this location
6	MA3	Multiplexer address 3	0	-not used- write '0' to this location
7	MA4	Multiplexer address 4	0	-not used- write '0' to this location
8	MA5	Multiplexer address 5	0	-not used- write '0' to this location
9	MA6	Multiplexer address 6	0	-not used- write '0' to this location
10	AIM	Automatic increment mode	1	1 : auto increment mode
				0: manual mode (not used)
11	AMPL	Amplification high bit	0	0: low amplification
				1: high amplification
12		spare	0	-not used- write '0' to this location
13		spare	0	-not used- write '0' to this location
14		spare	0	-not used- write '0' to this location
15	BDUR	Break Duration	0	0: 64clks of MCLK
				1: 32clks of MCLK

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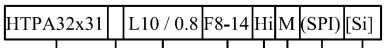
Order Code Example



Type:	
HTPA32x31	Please contact support for all available HTPA and module combinations.
Output:	
d	HTPA sensor with digital output
Not declared	HTPA sensor with analogous output
Optics:	
L	Focal length: In example L2,1 = 2,1 mm focal length
/	F-Number: In example /0.85
	For optics see also “HTPA standard optics”
Filter:	
F	Filter characteristics. In example F8-14 (µm, Bandpass)
Not declared	Broad band ARC
Sensitivity:	
Hi	Increased sensitivity
Not declared	Standard sensitivity
Version:	
A	Application set: comes with GUI, housing, power supply. Always UDP Interface.
M	Module: HTPA sensor soldered to PCB, calibrated stream
S	HTPA sensor only. Raw voltage output, not calibrated
Interface:	
SPI	SPI device; Two variants: Analog HTPA, 14bit ADC Digital HTPA, 12bit ADC
LC	SPI,Only Analogous HTPA. low speed, external processing required
UDP	Ethernet, CAT5 cable connection
Lens Material:	
Si	Silicon
Not declared	Germanium

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Characteristics:

Common Specifications:	
Technology	n-poly/p-poly Si
Element Resistance	approx. 80 kOhms
Sensitivity	approx. 100 V/W without optics and filter
Thermal pixel time constant	<4 ms
MUX preamplifier noise	approx. 30 $nV/\sqrt{Hz}$
Pixel + amplifier noise	approx. 50 $nV/\sqrt{Hz}$
Digital Interface	SPI
Analog Output	Yes
2 point selectable Gains	880x / 2640 x

Pitch	220 µm
Absorber size	150 µm
Max. Framerate (without Averaging)	25 Hz

16 internal Amps + MUX
992 sensitive elements

Optical characteristics:

Focal length:	10 mm (“L” equals the focal length of the lens)
F-Number:	1.0
Field of view:	39 x 38 deg
Lens coating:	AR-Coating; average reflectance per surface < 3% for 8µm < λ < 11.5 µm Environment acc. for MIL-C-48497

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Electric Specifications:

Absolute Maximum Ratings:

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{DD}		-0.5		6	V
Voltage at All inputs and outputs	V_{IO}		-0.5		V_{DD}+0.5	V
Storage Temperature	T_{STG}		-20		85	Deg. C

Operating Conditions:

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{DD}		4.5		5.5	V
Operation Temperature	T_A		0		85	Deg. C
ESD-Protection		Human body model 100pF + 1k5Ohm	1.5			kV

Electrical Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Digital Input						
Frequency of MCLK	MCLK		100k	1M	TBD	Hz
Input voltage high	V_{IH}		V_{DD}-1.2			V
Input voltage low	V_{IL}				1.2	V
PTAT						
Temperature range			0		85	Deg. C
PTAT gradient			37.4	39.1	40.5	K/V
Signal Processing						
First amplifier stage gain	G0		TBD	880	TBD	V/V
Second amplifier stage gain	G1	AMPL=0	TBD	1	TBD	V/V
Second amplifier stage gain	G1	AMPL=1	TBD	3	TBD	V/V
Analog path 1 Output ripple	V_{PPSENS}	AMPL=0 MCLK=1MHz	16	18	22	mV
Analog path 2 Output ripple	V_{PPSENS}	AMPL=0 MCLK=1MHz	64	69	74	mV
Temp. coefficient Thermopile path output voltage	TCO_{OUTA}		-0.07	0.02	0.10	mV/K

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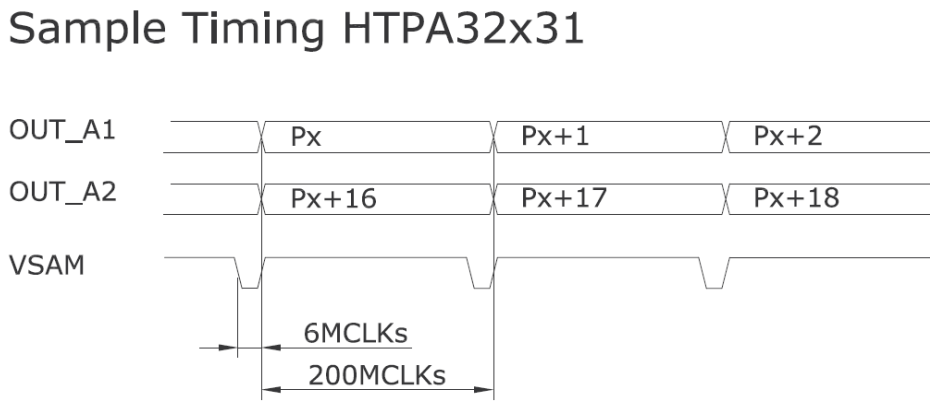
Electrical Characteristics (continued)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
VoltageReference						
VREF_1225	V_{REF}	V_{dd}=5V, T_{amb}=25°C SBY=1	1.31	1.32	1.34	V
Temp. coeff. of V_{REF}	TC_{REF}		41	128	217	ppm/K
Analog Output						
Output voltage swing	V_{OUTA}	load 10kOhm	0.5		V_{DD}-0.8	V
Power supply rejection ratio	P_{SRR}	AMPL=0, VDD<5V MCLK=1MHz	-14.5	-13.8	-13.3	dB
Output current limit	I_{OUTA}	OUT_A	0.15			mA
General Parameters						
Overall current consumption	I_{DD}	MCLK=1MHz 25° C	7.1	7.4	8.2	mA
Start up time	T_{POR}	Power On to first VSAM transition		1610		cycles

Timings HTPA32x31:



For the HTPA32x31 every analogous voltage is stable in the whole time domain.

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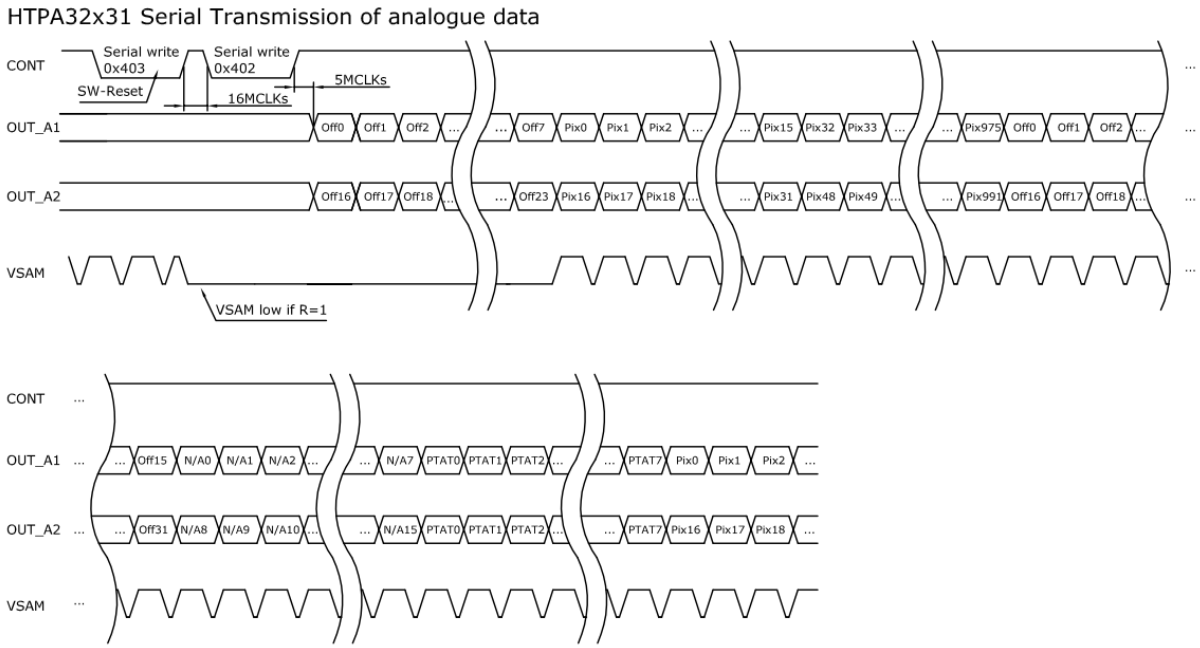
Serial Transmission:



Off0…Off16	Electric offset of amplifier 0 to amplifier 16
Pix0…Pix991	Amplified pixel voltage of Pixel0 to Pixel991
PTAT0…PTAT7	PTAT-Signal

The numeration of the pixels is in all cases line by line.

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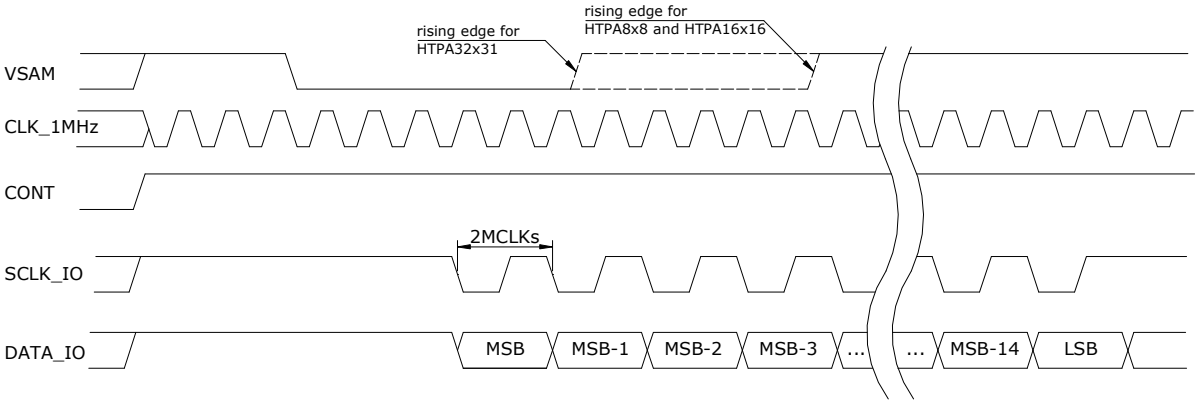
SPI Communication:

Data sampled at rising edge of SCLK, MSB first.
In case of ASIC as master device the frequency of the SCLK_IO is equal to the frequency of MCLK/2.

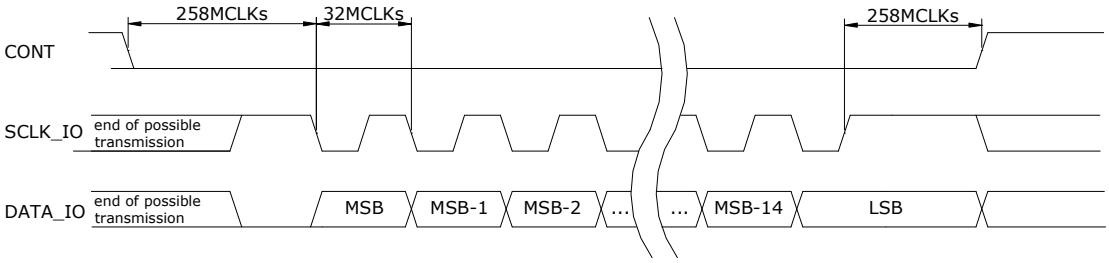
The valid sample cycle numbers are expensed in the least 10 bits. The value runs from 0 to 527.

The output drivers for SCLK_IO and DATA_IO are enabled by CONT.
If CONT is low the data can be written serially from external controller through DATA_IO. In that case the external controller has to wait a minimum delay time, until SCLK_IO and DATA_IO output drivers are disabled. After programming, the positive slope of CONT stores the contents, when the number of SCLK-pulses is equal 16. While the output driver of the ASIC is disabled a weak pull up ensures that the SCLK_IO pin is at high level. To execute a reset command, the µC has to write a logical "1" to the R-Bit in to configuration and afterwards a "0" into the R-bit, which requires two write cycles in this special case.

Serial Read from ASIC



Serial Write to ASIC



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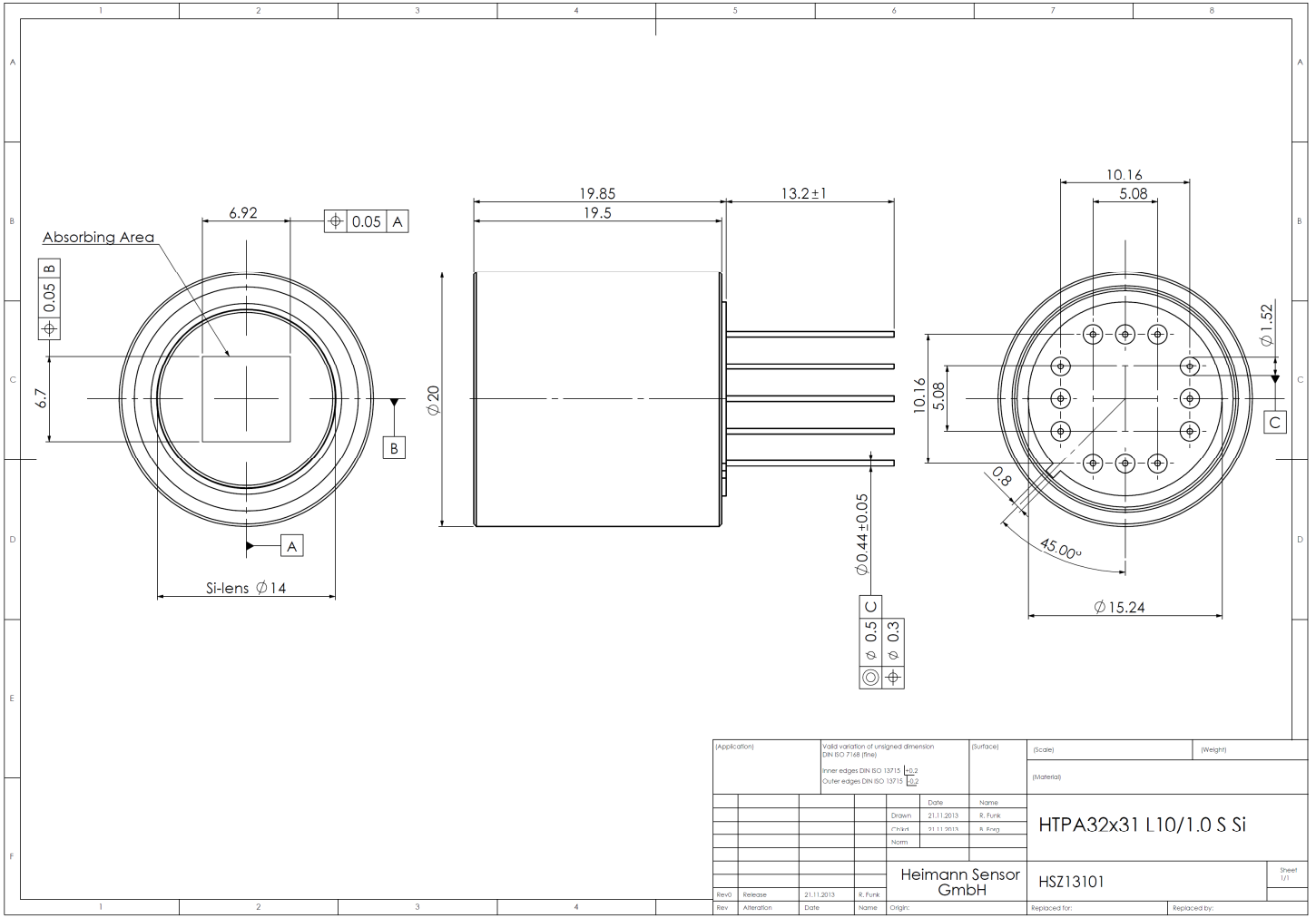
HTPA32x31L10/1.0S

Thermopile Array With Lens Optics

Rev.2: 2014.08.12 Forg/Schnorr

Outer Dimensions:

HTPA32x31L10/1.0 (dual Germanium Spherical/Spherical lens combination, focal length 10mm):



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