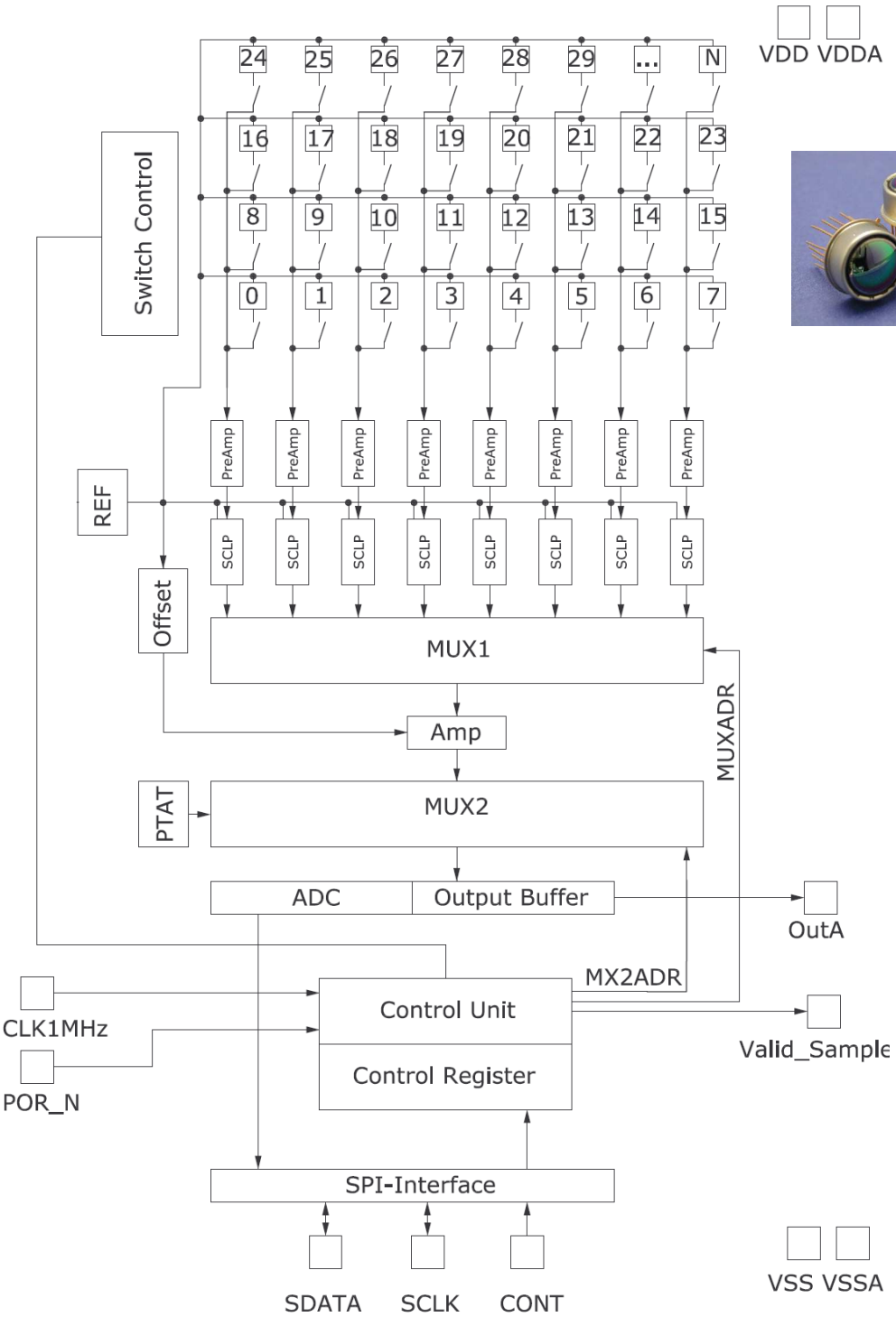
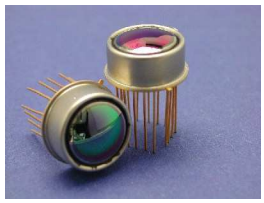
Specifications for Thermopilearrays
HTPA8x8, HTPA16x16, HTPA32x31, HTPA64x62

Rev.14: 2012.07.19 Fg

Principal Schematic for HTPA16x16:





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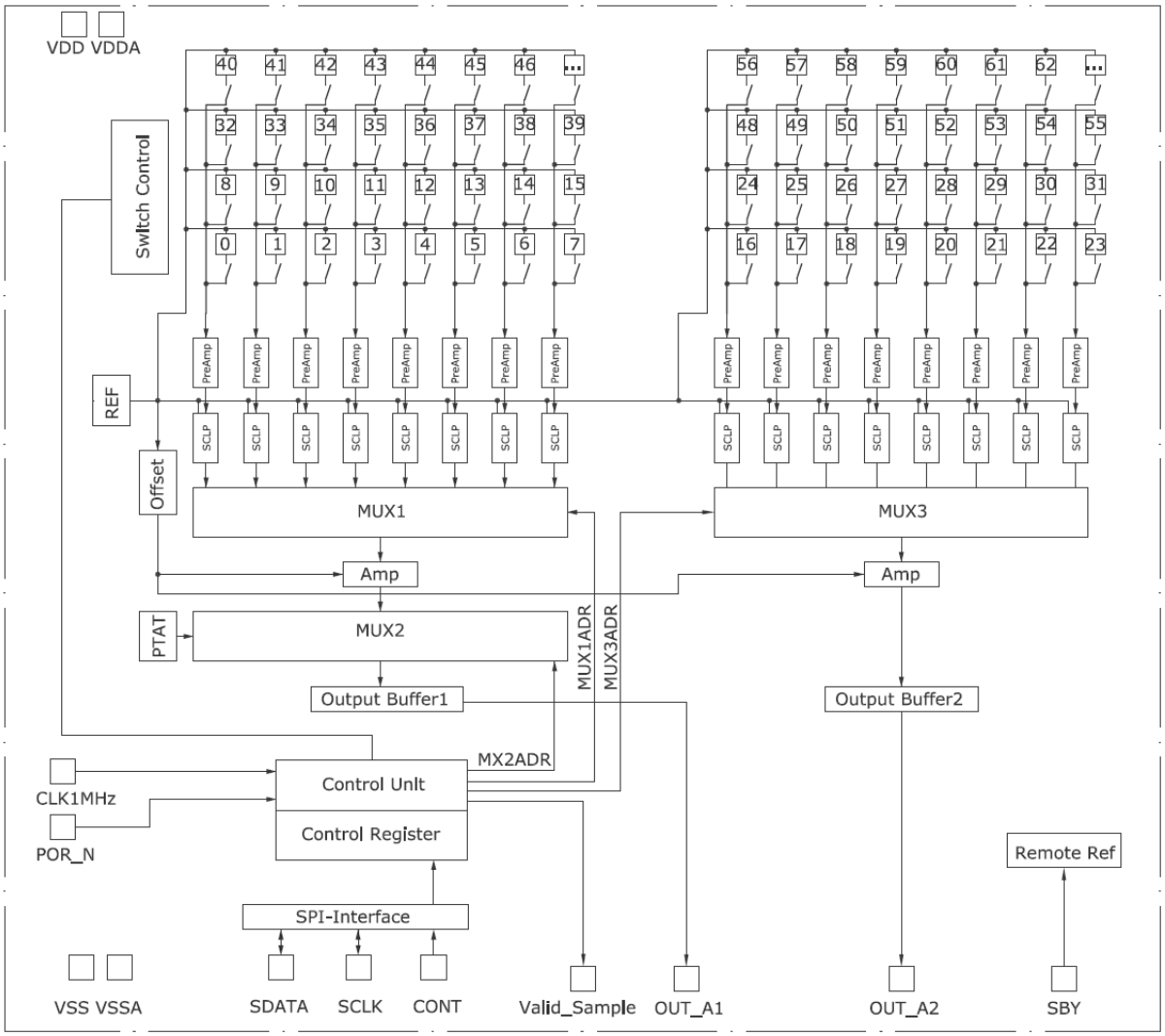
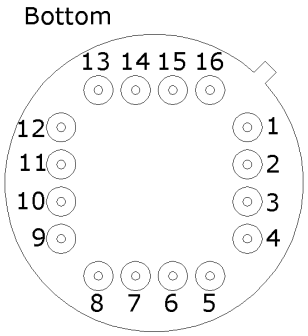
Principal Schematic for HTPA32x31 and HTPA64x62*:



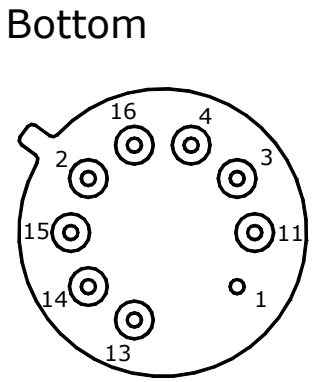
*Above shown is valid for 32x31. For HTPA64x62 the pixel numbers need to be changed.
Following pixel refer to OUT_A1: 0-31, 64-95, 128-159, …
Following pixel refer to OUT_A2: 32-63, 96-127, 160-191, …

Pin Assignment in TO8 for 8x8:



Connect all reference voltages via 100 nF capacitors to VSS.

Pin Assignment in TO39 for 8x8:



Connect all reference voltages via 100 nF capacitors to VSS.

Pin Assignment 8x8			
Pin	Name	Description	Type
1	VSS	Negative power supply voltage	Power
2	CONT	Control Pin for SPI	Digital Input
3	OUT_A	Analog Output	Analog Output
4	VCM_C	Common mode voltage	Reference Voltage*
5	VCM_OUT	Common mode voltage	Reference Voltage*
6	VREF_N	Negative reference voltage for ADC	Reference Voltage*
7	VREF_P	Positive reference voltage for ADC	Reference Voltage*
8	VREF_1225V	1.225V reference voltage	Reference Voltage*
9	AGND	Analog ground for ADC	Reference Voltage*
10	VDDA	Positive power supply voltage	Power
11	VDD	Positive power supply voltage	Power
12	POR_N	Power on reset, negatived	Digital Input
13	CLK_1MHZ	Master clock	Digital Input
14	VSAM	Valid sample	Digital Output
15	SCLK_IO	Clock input/output for SPI	Digital Input/Output
16	DATA_IO	Data input/output for SPI	Digital Input/Output

*) Connect via 100 nF to VSS

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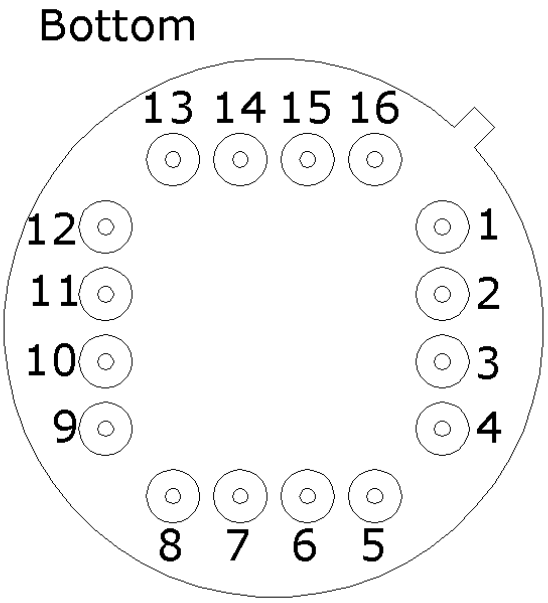
Pin Assignment in TO8 for 16x16:



Connect all reference voltages via 100 nF capacitors to VSS.

Pin Assignment 16x16			
Pin	Name	Description	Type
1	VREF_N	negative reference voltage for ADC	Reference Voltage*
2	VREF_P	positive reference voltage for ADC	Reference Voltage*
3	AGND	analog ground for ADC	Reference Voltage*
4	OUT_A	Analog Output	Analog Output
5	VCM_OUT	common mode voltage	Reference Voltage*
6	VCM_C	common mode voltage	Reference Voltage*
7	VREF_1225V	1.225V reference voltage	Reference Voltage*
8	VDD/VDDA	positive power supply voltage	Power
9	VSAM	valid sample	Digital Output
10	SCLK_IO	clock input/output for SPI	Digital Input/Output
11	CLK_1MHZ	master clock	Digital Input
12	POR_N	power on reset, negatived	Digital Input
13	SBY	Standby	Digital Input
14	VSS	negative power supply voltage	Power
15	DATA_IO	data input/output for SPI	Digital Input/Output
16	CONT	Control Pin for SPI	Digital Input

*) Connect via 100 nF to VSS

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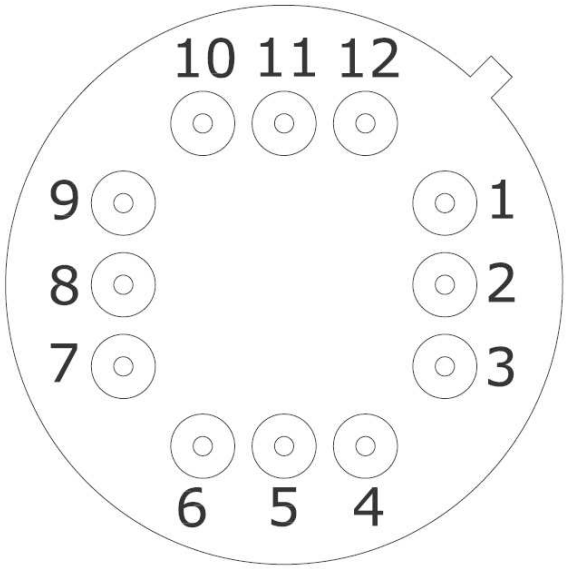
Pin Assignment in TO8 for 32x31 and 64x62:

Bottom



Connect all reference voltages via 100 nF capacitors to VSS.

Pin Assignment 32x31/64x62			
Pin	Name	Description	Type
1	CLK_1MHZ	master clock	Digital Input
2	SCLK_IO	clock input/output for SPI	Digital Input/Output **
3	SBY	Standby	Digital Input***
4	VSAM	valid sample	Digital Output
5	DATA_IO	data input/output for SPI	Digital Input/Output **
6	OUT_A2	Analog Output	Analog Output
7	VCM_C	common mode voltage	Reference Voltage*
8	VREF_1225V	1.225V reference voltage	Reference Voltage*
9	OUT_A1	Analog Output	Analog Output
10	VSS	negative power supply voltage	Power
11	VDD	positive power supply voltage	Power
12	CONT	Control Pin for SPI	Digital Input

*) Connect via 100 nF to VSS
**) The HTPA32x31 has no ADC, but the valid sample cycle number is delivered.
***) Connect to VSS or NC for internal reference voltages. Connect to VDD if VREF_1225V and VCM_C are applied from external. See “Application Note HTPA” for details.

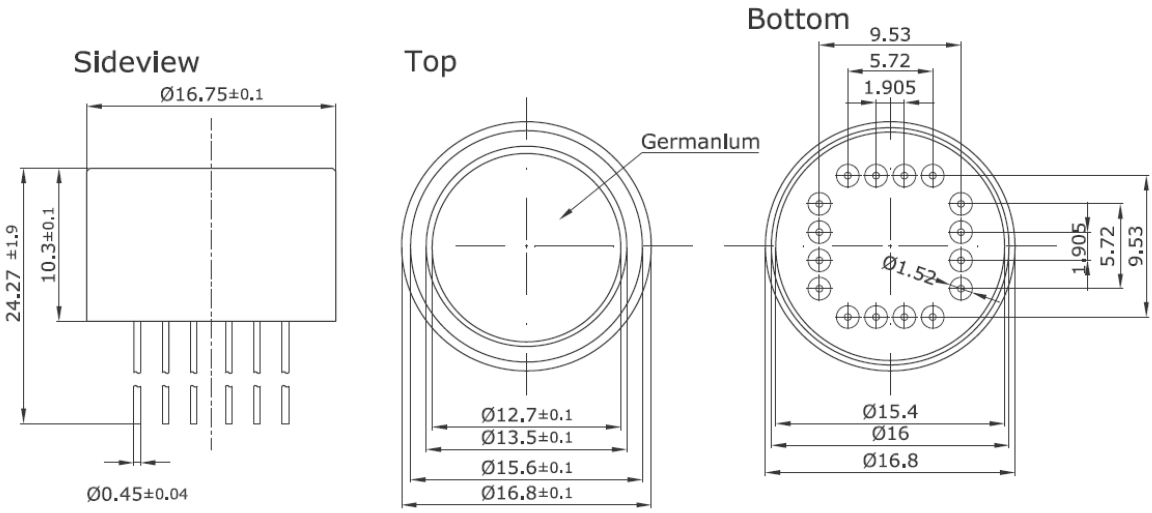
Possible Lens / Array type combinations:

Possible Combinations						
Lens	HTPA8x8 TO39	HTPA8x8 TO8	HTPA16x16	HTPA32x31	HTPA64x62	Remarks
L3	X	X	X	-	-	f/<1.0 Ge ARC
L3.6	X	X	X	-	-	f/<1.0 Si uncoated
L4.7	-	-	-	X	X	f/0.9 Dual Ge ARC
L5.5	X	-	-	-	-	f/1.0 Si uncoated
L7/1.2	X	-	-	-	-	f/1.2 Si ARC
L7.5	-	X	-	X	X	
L10/0.8	-	X	X	X	X	f/0.8 Dual Ge ARC
L10/1.0	-	X	X	X	X	f/1.0 Dual Ge ARC
L20/0.95	-	X	X	X	X	f/0.95 Dual Ge ARC

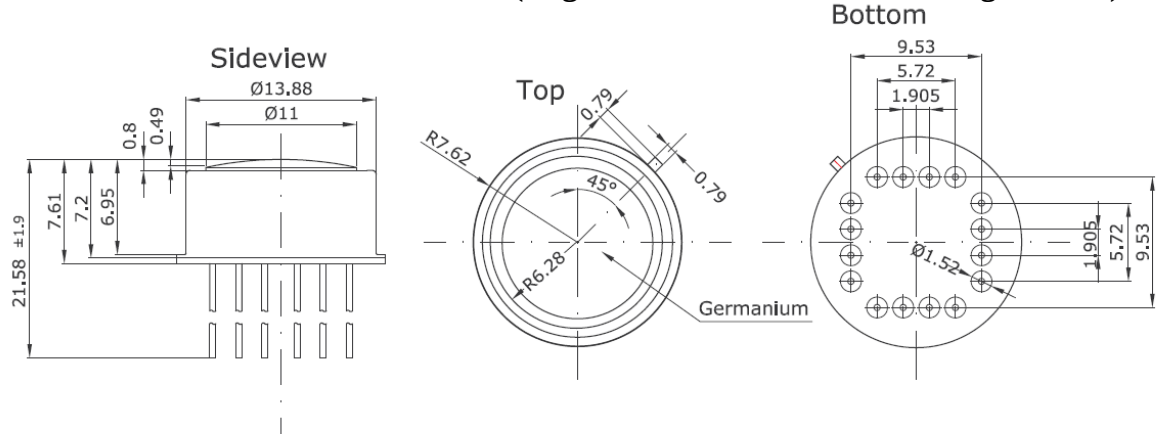
Grey marked columns:
8x8(TO8): Non-Standard product. Only for special purposes.^16x16: actual under redesign.

Outer Dimensions:

HTPA8x8L7 / HTPA16x16L7 in TO8 (single Germanium Lens, focal length 7 mm):



HTPA8x8L4 / HTPA16x16L4 in TO8 (single Germanium Lens, focal length 4 mm):



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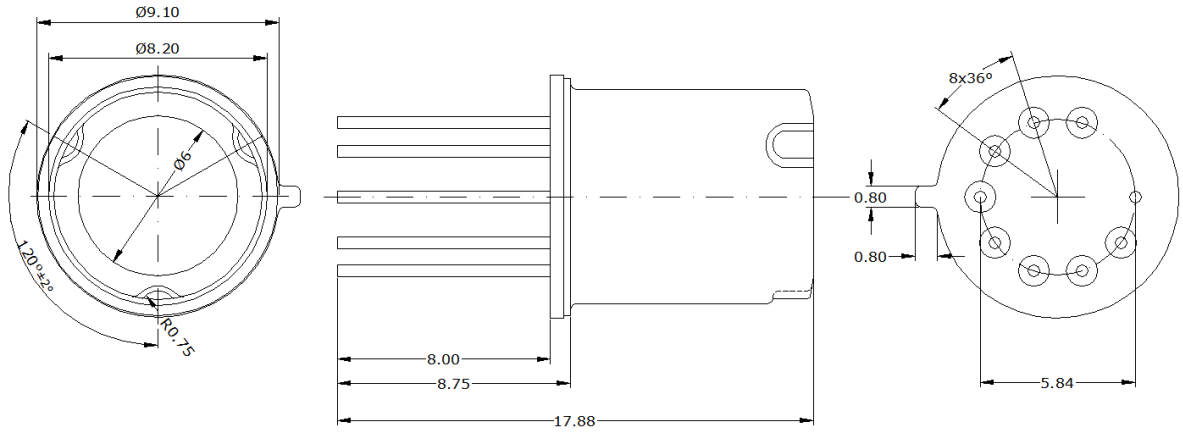
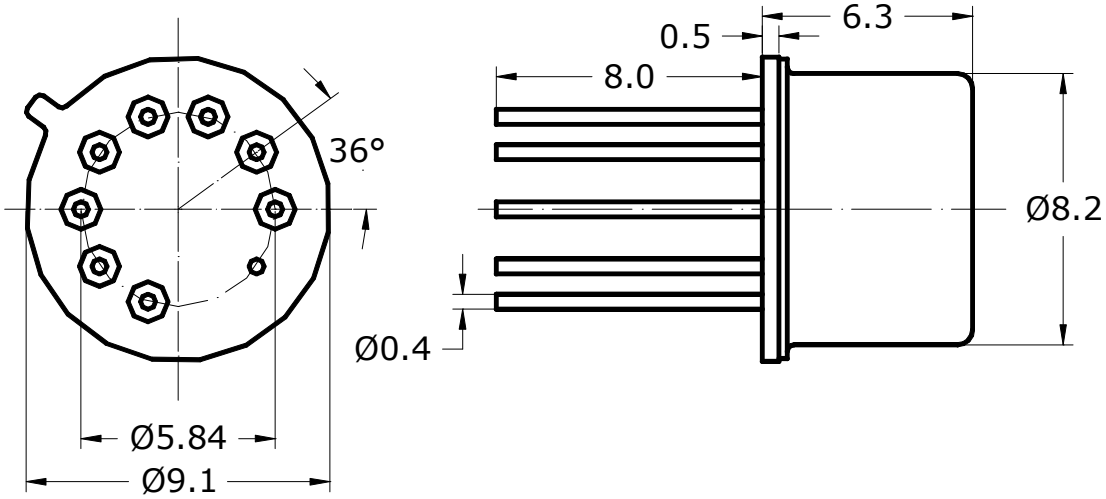
Outer Dimensions (continued):

HTPA8x8L7 in TO39 (single Germanium Lens, focal length 7 mm):

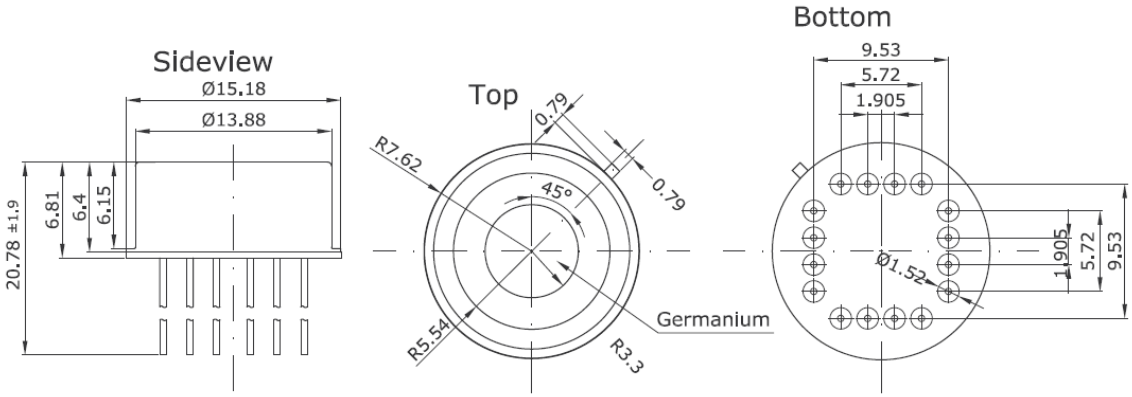


HTPA8x8L3 in TO39 (single Germanium Lens, focal length 3 mm), preliminary:

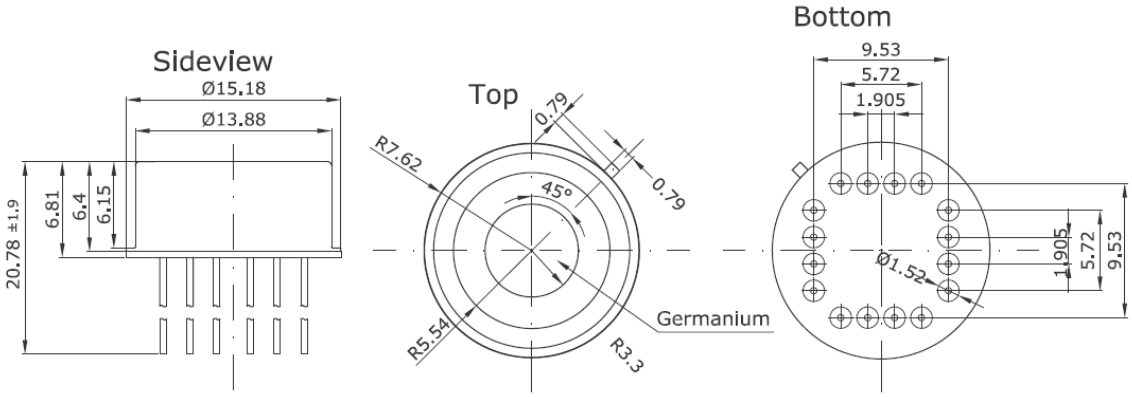


Outer Dimensions (continued):

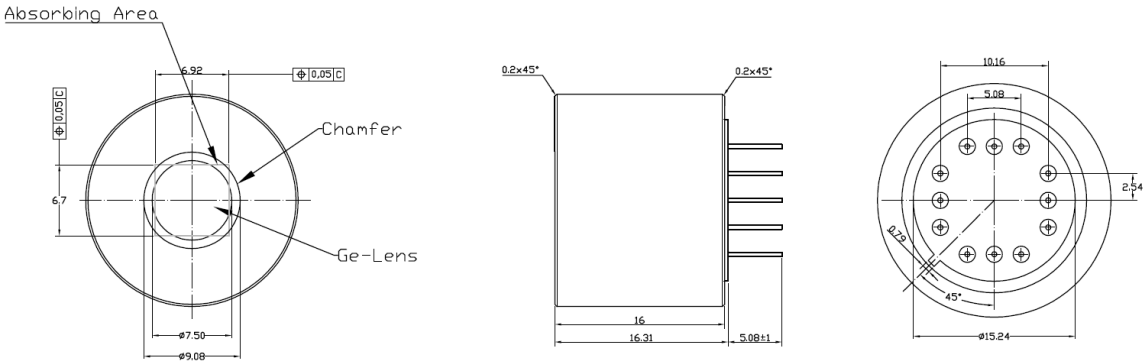
HTPA8x8L3 / HTPA16x16L3 in TO8 (single Germanium Lens, focal length 3 mm):



HTPA8x8L3 / HTPA16x16L3 in TO8 (single Germanium Lens, focal length 3 mm):

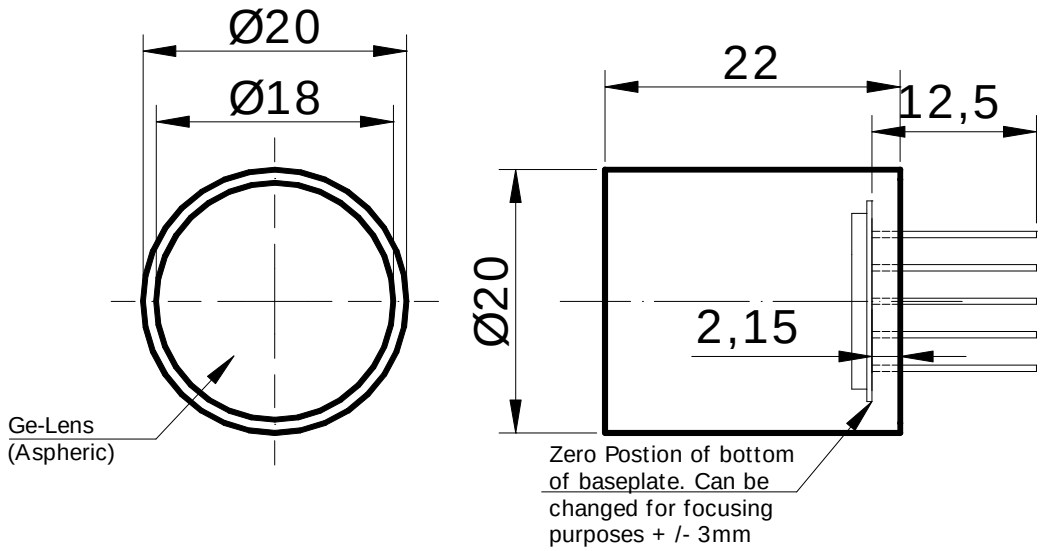


HTPA32x31L7.5 / HTPA16x16L3 in TO8 (dual Germanium Lens, focal length 7.5 mm):

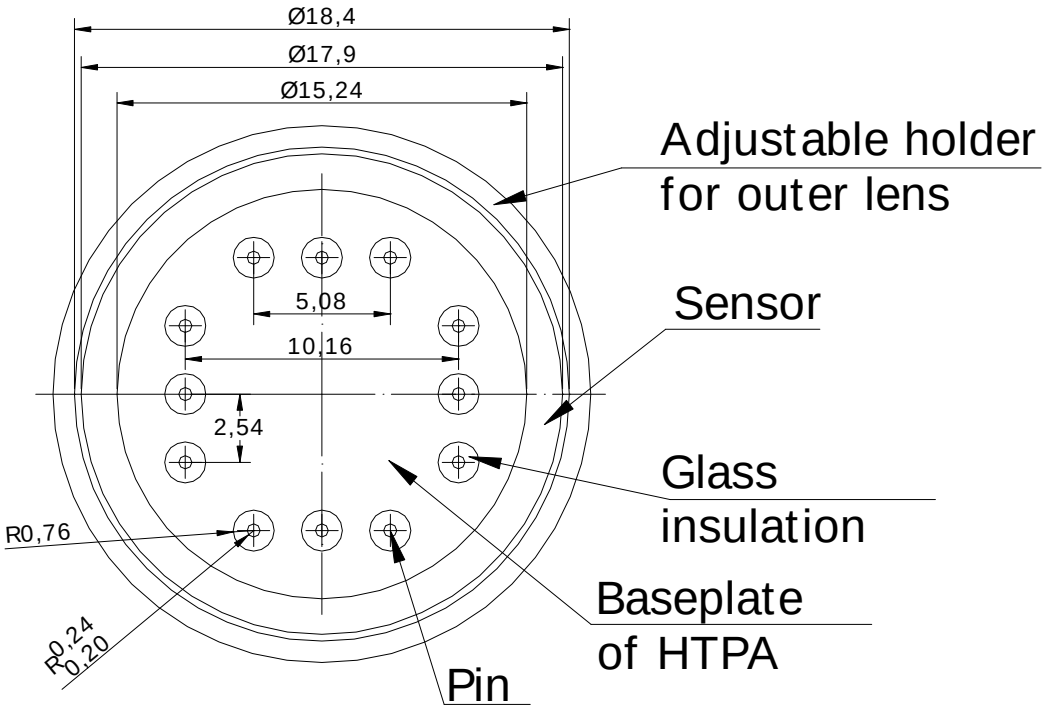


Outer Dimensions (continued):

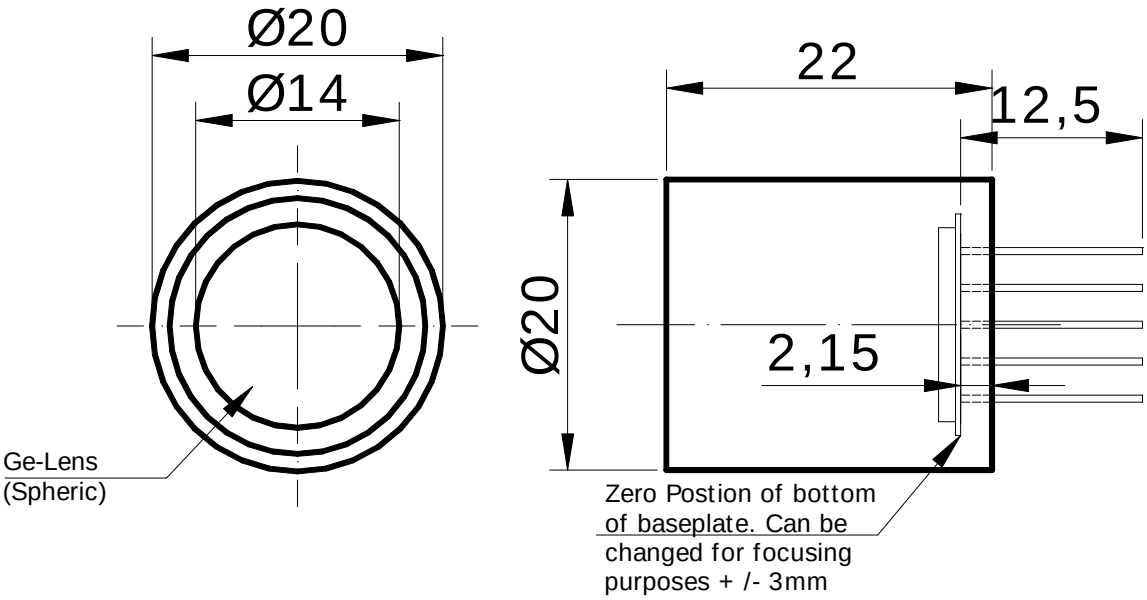
HTPA32x31L10/0.8 or HTPA64x62L10/0.8 (dual Germanium Aspherical/Spherical lens combination, focal length 10mm):



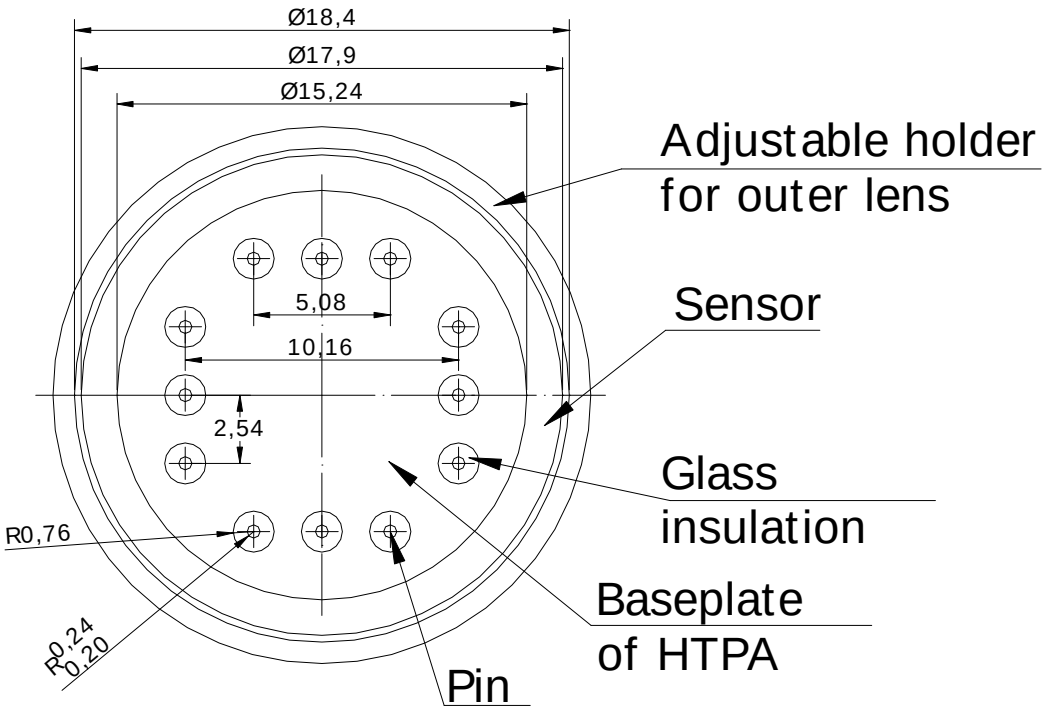
Bottom view:



HTPA32x31L10/1.0 (dual Germanium Spherical/Spherical lens combination, focal length 10mm):



Bottom view:



Internal Register Map 8x8 and 16x16:

Num	Name	Function	Default	Notes
0	R	Reset	0	In case of 1, the mux pixel counter is reset. ASIC stays in reset.
1	OPCTLL	Operating point control low	1	00: Analog operating point is at start of AD-range, only positive signals are convertible
				01: Analog operating point is in the middle of AD-range, positive and negative signals are convertible
				11: Analog operating point is at end of AD-range, only negative signals are convertible
2	OPCTLH	Operating point control high	0	10=01
3	MA0	Multiplexer address 0	0	-not used- write '0' to this location
4	MA1	Multiplexer address 1	0	-not used- write '0' to this location
5	MA2	Multiplexer address 2	0	-not used- write '0' to this location
6	MA3	Multiplexer address 3	0	-not used- write '0' to this location
7	MA4	Multiplexer address 4	0	-not used- write '0' to this location
8	MA5	Multiplexer address 5	0	-not used- write '0' to this location
9	MA6	Multiplexer address 6	0	-not used- write '0' to this location
10	AIM	Automatic increment mode	1	1 : auto increment mode
				0: manual mode (not used)
11	AMPL	Amplification high bit	0	0: low amplification
				1: high amplification
12		spare	0	-not used- write '0' to this location
13		spare	0	-not used- write '0' to this location
14		spare	0	-not used- write '0' to this location
15	BDUR	Break Duration	0	0: 64clks of MCLK
				1: 32clks of MCLK

Internal Register Map 32x31/64x62:

Num	Name	Function	Default	Notes
0	R	Reset	0	In case of 1, the mux pixel counter is reset. ASIC stays in reset.
1		spare	1	-not used- write '1' to this location
2		spare	0	-not used- write '0' to this location
3	MA0	Multiplexer address 0	0	-not used- write '0' to this location
4	MA1	Multiplexer address 1	0	-not used- write '0' to this location
5	MA2	Multiplexer address 2	0	-not used- write '0' to this location
6	MA3	Multiplexer address 3	0	-not used- write '0' to this location
7	MA4	Multiplexer address 4	0	-not used- write '0' to this location
8	MA5	Multiplexer address 5	0	-not used- write '0' to this location
9	MA6	Multiplexer address 6	0	-not used- write '0' to this location
10	AIM	Automatic increment mode	1	1 : auto increment mode
				0: manual mode (not used)
11	AMPL	Amplification high bit	0	0: low amplification
				1: high amplification
12		spare	0	-not used- write '0' to this location
13		spare	0	-not used- write '0' to this location
14		spare	0	-not used- write '0' to this location
15	BDUR	Break Duration	0	0: 64clks of MCLK
				1: 32clks of MCLK

Specifications for Thermopilearrays
HTPA8x8, HTPA16x16, HTPA32x31, HTPA64x62

Rev.14: 2012.07.19 Fg

Characteristics:

Common Specifications:

- Number of Thermocouples 80
- Technology n-poly/p-poly Si
- Element Resistance approx. 80 kOhms
- Sensitivity approx. 60 V/W without optics and filter
- Thermal Pixeltime constant <4 ms
- MUX preamplifier noise approx. 30 $nV/\sqrt{Hz}$
- Digital Interface SPI
- Analog Output Yes
- 2 point selectable Gains 2640x / 7920 x

Array-depending Specifications:

8x8 elements:

- Pitch 300 µm
- Absorber size 220 µm
- Max. Framerate 66,8 Hz (without Averaging)
- 4 internal Amps + MUX
- 64 sensitive elements
- Internal ADC 12 bit

FOV(L=3mm)= 44 deg
FOV(L=4mm)= 33 deg
FOV(L=7mm)= 20 deg

16x16 elements:

- Pitch 220 µm
- Absorber size 150 µm
- Max. Framerate 17,7 Hz (without Averaging)
- 8 internal Amps + MUX
- 256 sensitive elements
- Internal ADC 12 bit

FOV(L=3mm)= 61 deg
FOV(L=4mm)= 48 deg
FOV(L=7mm)= 28 deg

32x31 elements:

- Pitch 220 µm
- Absorber size 150 µm
- Max. Framerate 9,1 Hz * (without Averaging)
- 16 internal Amps + MUX
- 992 sensitive elements
- Internal ADC none

FOV(L=7.5mm)= 50 x 49 deg
FOV(L=10mm)= 39 x 38deg

64x62 elements:

- Pitch 110 µm
- Absorber size 57 µm
- Max. Framerate 4 Hz (without Averaging)
- 16 internal Amps + MUX
- 3968 sensitive elements
- Internal ADC none

FOV(L=10mm)= 39 x 38deg

L equals the focal length of the lens.
*) Framerates up to approx. 20 Hz are possible, but not approved yet.

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Electric Specifications:

Absolute Maximum Ratings:

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		-0.5		6	V
Voltage at All inputs and outputs	V_{IO}		-0.5		V_{CC}+0.5	V
Storage Temperature	T_{STG}		-30		125	Deg. C

Operating Conditions:

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.5		5.5	V
Operation Temperature	T_A		0		85	Deg. C
ESD-Protection		Human body model	1.5			kV
		100pF + 1k5Ohm				

Electrical Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Digital Input						
Frequency of MCLK	MCLK			1M	TBD	Hz
Input voltage high	V_{IH}		Vdd-1.2			V
Input voltage low	V_{IL}				1.2	V
Operating Frequency	f_{OP}	CLK_1MHz	500k	1M	TBD	Hz
PTAT						
Temperature range			0		85	Deg. C
PTAT value@ -20°C				TBD		V
PTAT value@100°C				TBD		V
Signal Processing						
First amplifier stage gain	G0		TBD	880	TBD	V/V
Second amplifier stage gain	G1	AMPL=0	TBD	3	TBD	V/V
Second amplifier stage gain	G1	AMPL=1	TBD	9	TBD	V/V
Analog path Output ripple	V_{PPSENS}		-	-	TBD	mV
Temp. coefficient Thermopile path output voltage	TCO_{OUTA}		TBD	-	TBD	mV/K
VoltageReference						
VREF_1225	V_{REF}	V_{CC}=5V, T_{amb}=25°C	1.2	1.225	1.25	V
Temp. coeff. of V_{REF}	TC_{REF}		TBD		TBD	ppm/K

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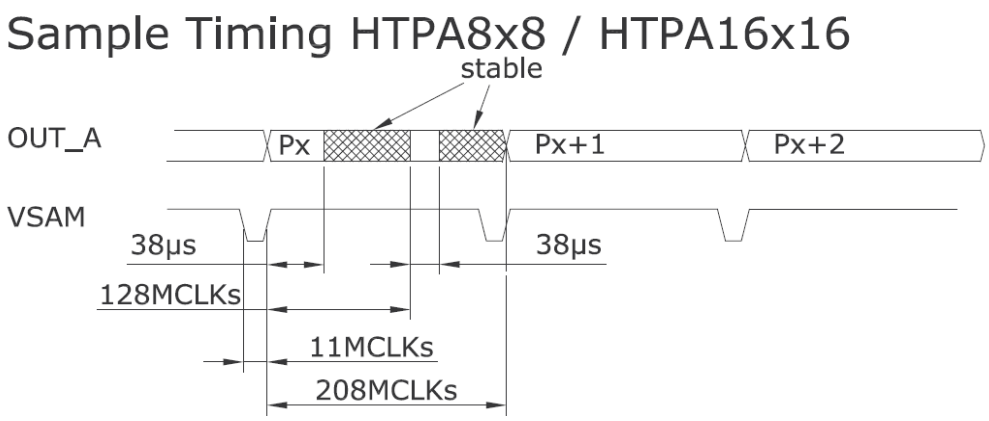
Electrical Characteristics (continued)

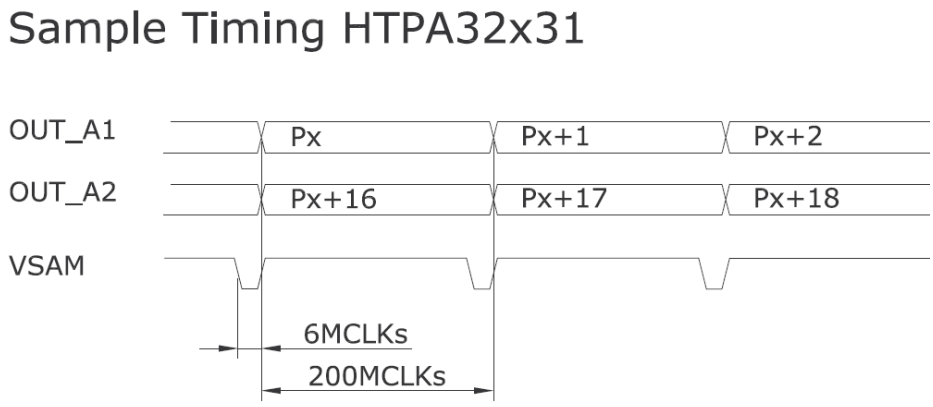
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Analog Output						
Output voltage swing	V_{OUTA}	load 10kOhm	0.5		V_{CC}-0.8	V
Power supply rejection ratio	P_{SRR}	AMPL=1	TBD			dB
Output current limit	I_{OUTA}	OUT_A	0.15			mA
General Parameters						
Overall current consumption	I_{DD}	CLK_1MHz=1MHz		7	TBD	mA
Start up time	T_{POR}	CLK_1MHz=1MHz Power On to first sample			TBD	mS

Timings HTPA8x8 and HTPA16x16:



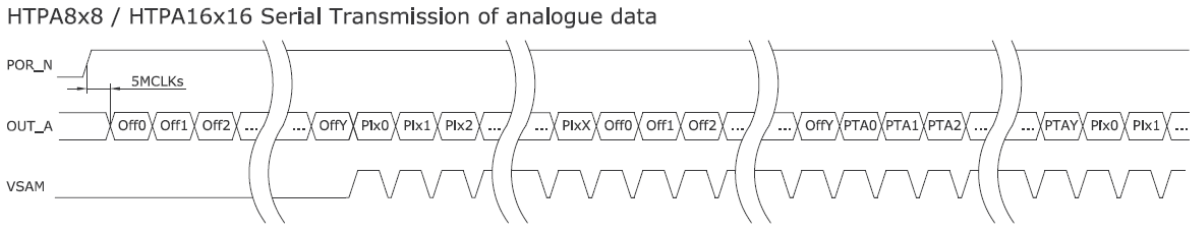
For the HTPA 8x8 and the HTPA 16x16 every analogous voltage has 2 stable domains, as shown above.

Timings HTPA32x31:



For the HTPA32x31 every analogous voltage is stable in the whole time domain.

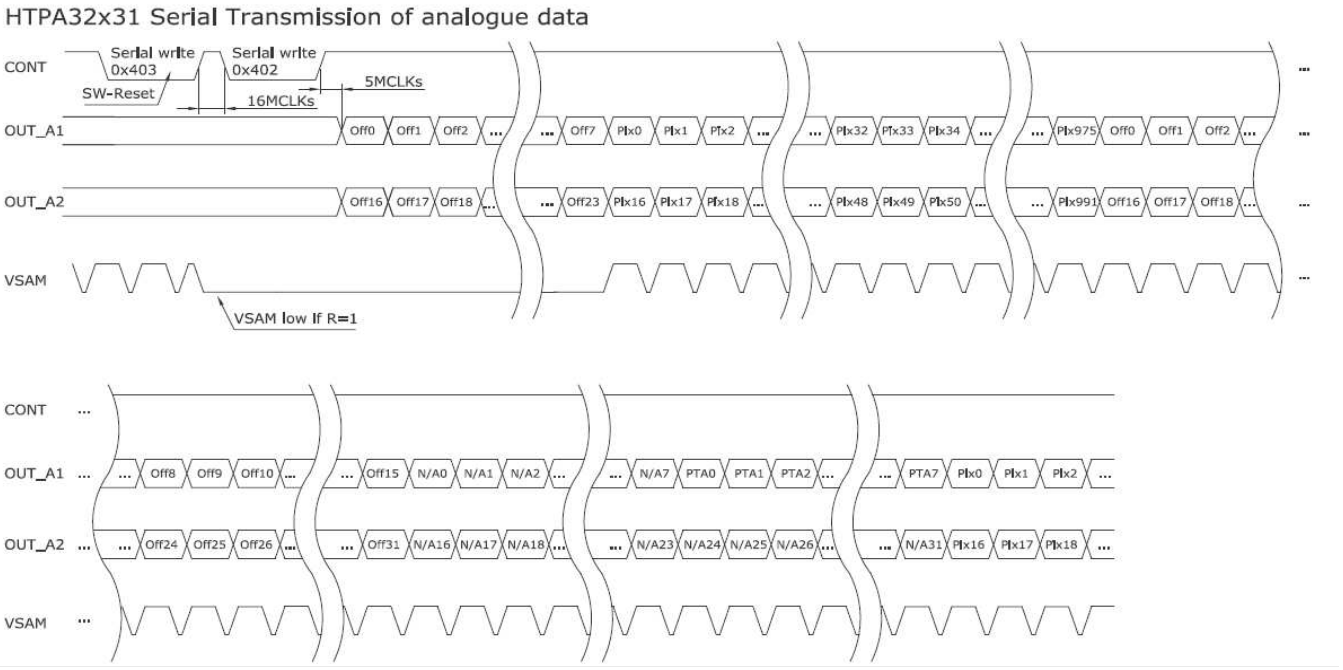
Serial Transmission:



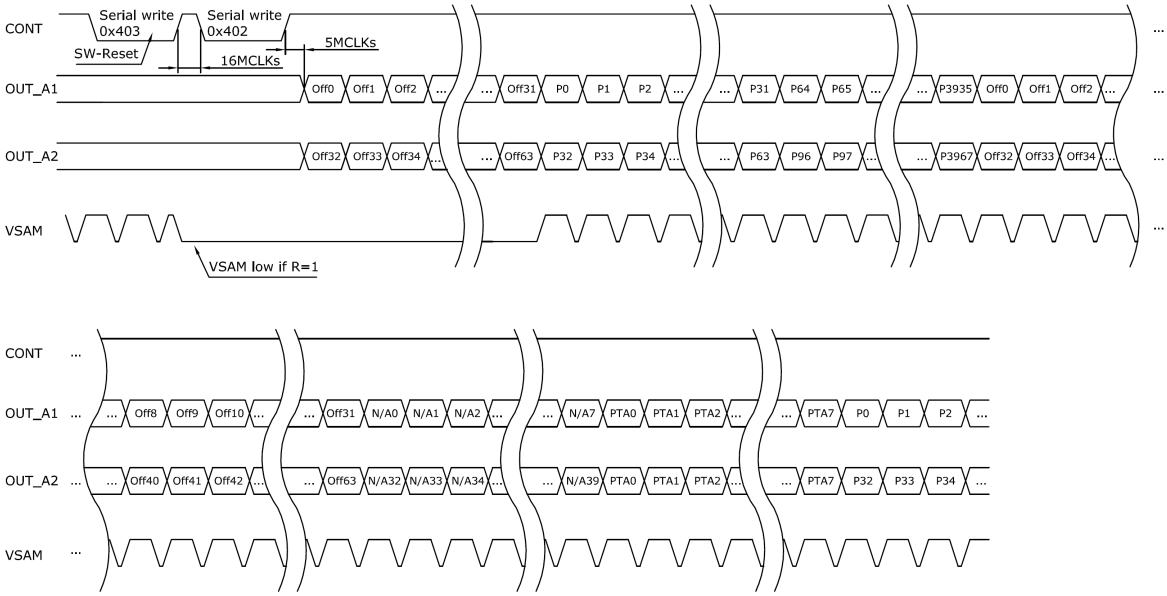
Off0…OffY	Electric offset of amplifier 0 to amplifier Y
Pix0…PixX	Amplified pixel voltage of Pixel0 to PixelX
PTA0…PTAY	PTAT-Signal ((Y+1)-times)

Constants for array types:

Type 8x8:	Type 16x16:
Y=3	Y=7
X=63	X=255



HTPA64x62 Serial Transmission of analogue data



The numeration of the pixels is in all cases line by line.

SPI Communication:

Data sampled at rising edge of SCLK, MSB first.
In case of ASIC as master device the frequency of the SCLK_IO is equal to the frequency of MCLK/2.

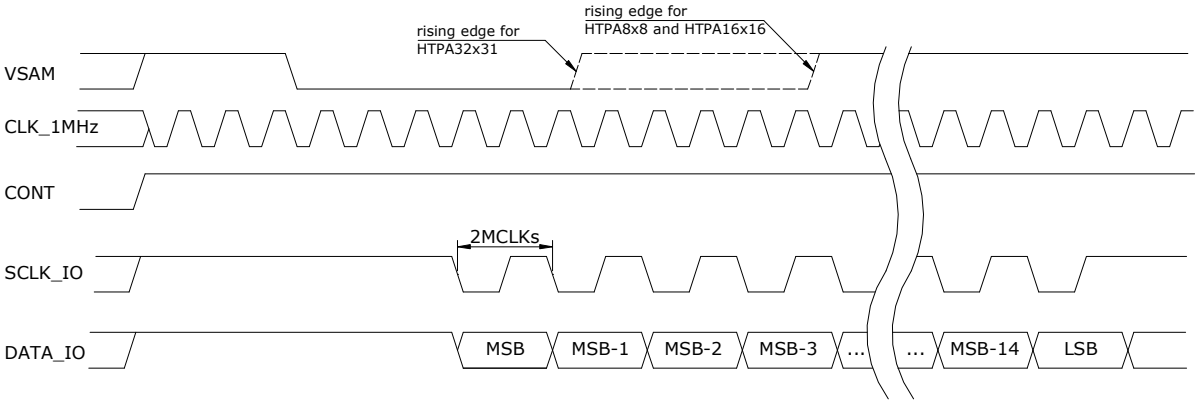
HTPA8x8 & HTPA16x16:
The four MSB's signify the row address of the current pixel, the other bits describe the ADC-result.

HTPA 32x31:
The valid sample cycle numbers are expensed in the least 10 bits. The value runs from 0 to 527.

HTPA 64x62:
The valid sample cycle numbers are expensed in the least 11 bits. The value runs from 0 to 2047.

The output drivers for SCLK_IO and DATA_IO are enabled by CONT.
If CONT is low the data can be written serially from external controller through DATA_IO. In that case the external controller has to wait a minimum delay time, until SCLK_IO and DATA_IO output drivers are disabled. After programming, the positive slope of CONT stores the contents, when the number of SCLK-pulses is equal 16. While the output driver of the ASIC is disabled a weak pull up ensures that the SCLK_IO pin is at high level. To execute a reset command, the µC has to write a logical "1" to the R-Bit in to configuration and afterwards a "0" into the R-bit, which requires two write cycles in this special case.

Serial Read from ASIC



Serial Write to ASIC