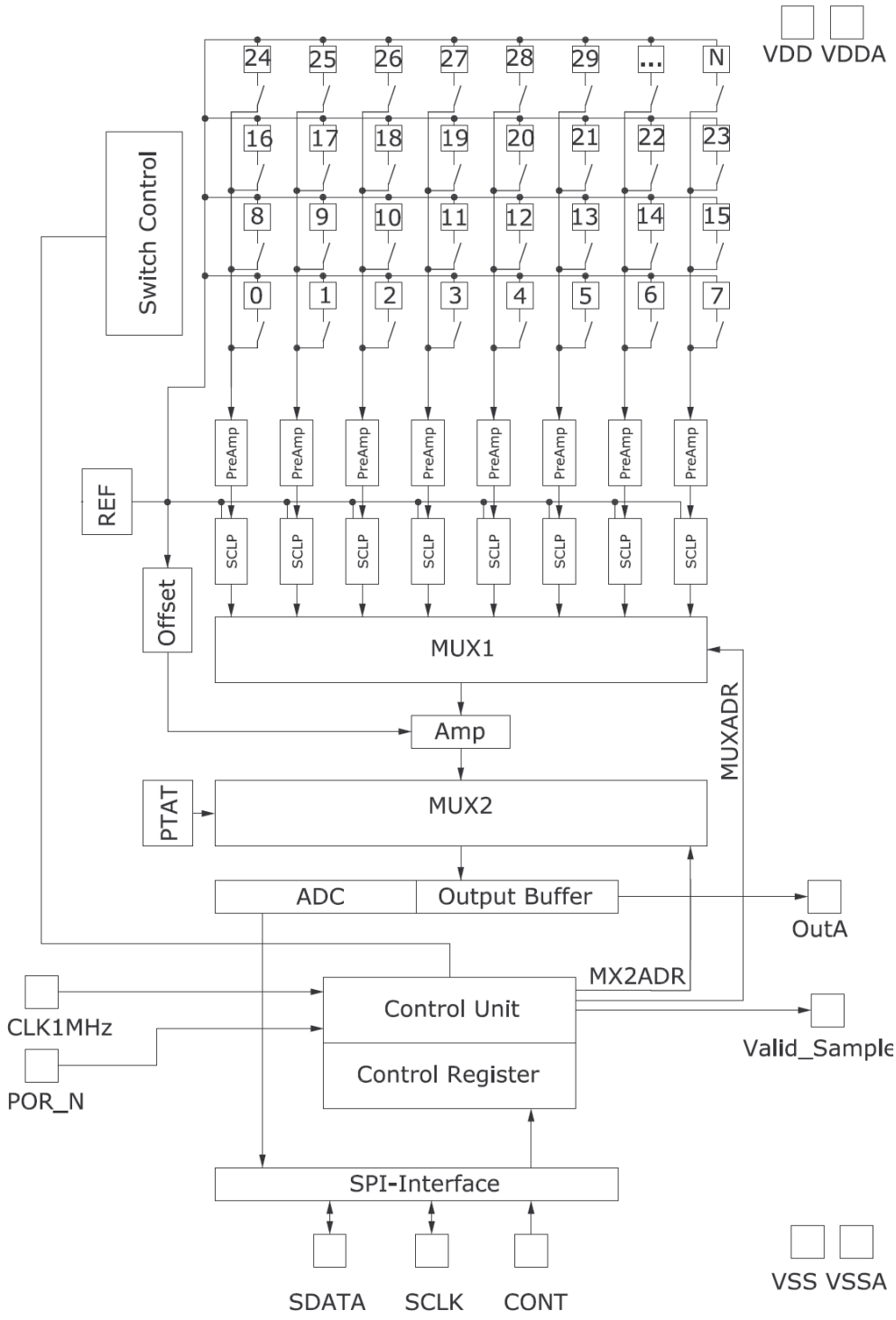
Principal Schematic for HTPA8x8:



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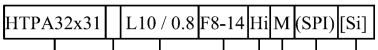
Order Code Example



Type:	
HTPA32x31	Please contact support for all available HTPA and module combinations.
Output:	
d	HTPA sensor with digital output
Not declared	HTPA sensor with analogous output
Optics:	
L	Focal length: In example L10 = 10.0 mm focal length
/	F-Number: In example /0.8
	For optics see also “HTPA standard optics”
Filter:	
F	Filter characteristics. In example F8-14 (µm, Bandpass)
Not declared	Broad band ARC
Sensitivity:	
Hi	Increased sensitivity
Not declared	Standard sensitivity
Version:	
A	Application set: comes with GUI, housing, power supply. Always UDP Interface.
C	Calibrated sensor (only digital). Carries calibration constants on internal EEPROM
M	Module: HTPA sensor soldered to PCB, calibrated stream
S	HTPA sensor only. Raw voltage output, not calibrated
Interface:	
SPI	SPI device; Three variants: HTPA82x62: 16bit ADC all other analogous HTPAs: 14bit ADC Digital HTPA: 12bit ADC
LC	SPI,Only Analogous HTPA, 12bit ADC low speed, external processing required
UDP	Ethernet, CAT5 cable connection
PoE	Power over Ethernet, CAT5 connection, UDP protocol
Lens Material:	
Si	Silicon
Not declared	Germanium

For modules, M(UART) and M(LC) are not recommended anymore. M(SPI) and M(UDP) offer a wider input voltage range, better ADC resolution and a wider measurement range.

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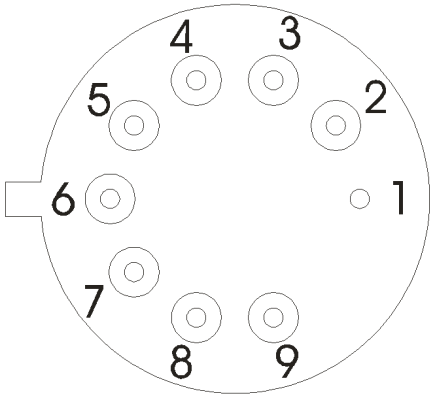
Pin Assignment in TO39 – Bottom View:



Connect all reference voltages via 100 nF capacitors to VSS.

Pin Assignment 8x8			
Pin	Name	Description	Type
1	VSS	Negative power supply voltage	Power
2	VDD	Positive power supply voltage	Power
3	OUT_A	Analog Output	Analog Output
4	VCM_C	Common mode voltage	Reference Voltage*
5	DATA_IO	Data input/output for SPI	Digital Input/Output
6	CONT	Control Pin for SPI	Digital Input
7	SCLK_IO	Clock input/output for SPI	Digital Input/Output
8	VSAM	Valid sample	Digital Output
9	CLK_1MHZ	Master clock	Digital Input

*) Connect via 100 nF to VSS

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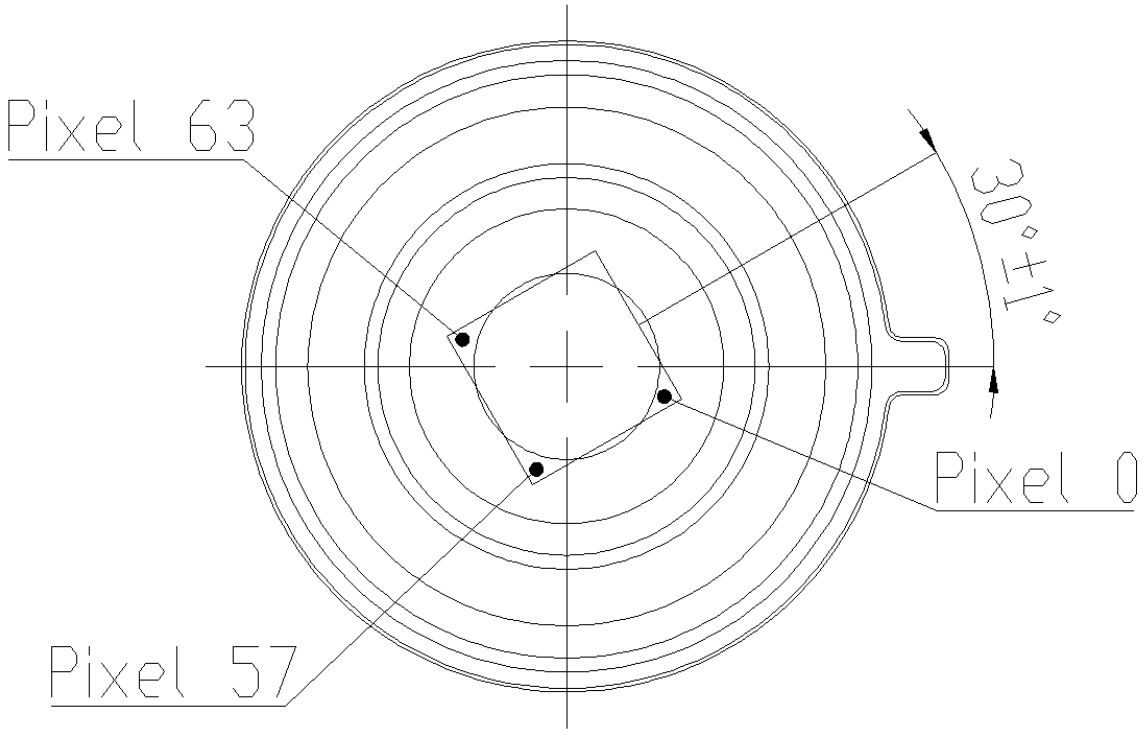
Optical Orientation of Pixels:



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Internal Register Map 8x8:

Num	Name	Function	Notes
0	R	Reset	1: Mux-Pixel-Counter on reset
'(2:1)	OPCTL(1:0)	Selection of operating point Reference choice at SCLP	00: VrefN 01: CM 10: VrefP
'(9:3)	MA(6:0)	Adress for static pixel selection	
10	AIM	Adress Increment Mode	0: adress = MA 1: auto adress inrement
11	AMP	Amplification	1: high amplification
14	SDL	SCLK Divider Low	different clock dividers for operating SCLK SCLK = MCLK / 2, 4, 8
15	SDH	SCLK Divider High	

Characteristics:

Common Specifications:

- Number of Thermocouples 80
- Technology n-poly/p-poly Si
- Element Resistance approx. 80 kOhms
- Sensitivity approx. 75 V/W without optics and filter
- Thermal Pixeltime constant <4 ms
- MUX preamplifier noise approx. 30 $nV/\sqrt{Hz}$
- Pixel + amplifier noise approx. 50 $nV/\sqrt{Hz}$
- Digital Interface SPI
- Analog Output Yes
- 2 point selectable Gains 2640x / 7920 x

- Pitch 300 µm
- Absorber size 220 µm
- Max. Framerate 100 Hz
  (without Averaging)
- 4 internal Amps + MUX
- 64 sensitive elements

Optical characteristics:

- Focal length: 2.1 mm (“L” equals the focal length of the lens)
- F-Number: 0.85
- Field of view: 70°
- lens coating: AR-Coating; average reflectance per surface
  < 3% for 8µm < λ < 11,5µm
  Environment acc. for MIL-C-48497

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Electric Specifications:

Absolute Maximum Ratings:

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{DD}		-0.5		6	V
Voltage at All inputs and outputs	V_{IO}		-0.5		V_{CC}+0.5	V
Storage Temperature	T_{STG}		-30		125	Deg. C

Operating Conditions:

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{DD}		4.5		5.5	V
Operation Temperature	T_A		0		85	Deg. C
ESD-Protection		Human body model 100pF + 1k5Ohm	1.5			kV

Electrical Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Digital Input						
Frequency of MCLK	MCLK		100k	1M	TBD	Hz
Input voltage high	V_{IH}		Vdd-1.2			V
Input voltage low	V_{IL}				1.2	V
Operating Frequency	f_{OP}	CLK_1MHz	100k	1M	TBD	Hz
PTAT						
Temperature range			0		85	Deg. C
PTAT value@ -20°C				TBD		V
PTAT value@100°C				TBD		V
Signal Processing						
First amplifier stage gain	G0		TBD	880	TBD	V/V
Second amplifier stage gain	G1	AMPL=0	TBD	3	TBD	V/V
Second amplifier stage gain	G1	AMPL=1	TBD	9	TBD	V/V
Analog path Output ripple	V_{PPSENS}	CLK_1MHz	65	91	120	mV
Temp. coefficient Thermopile path output voltage	TCO_{OUTA}		TBD	-	TBD	mV/K
VoltageReference						
VREF_1225	V_{REF}	V_{CC}=5V, T_{amb}=25°C	1.2	1.225	1.25	V
Temp. coeff. of V_{REF}	TC_{REF}		35	100	156	ppm/K

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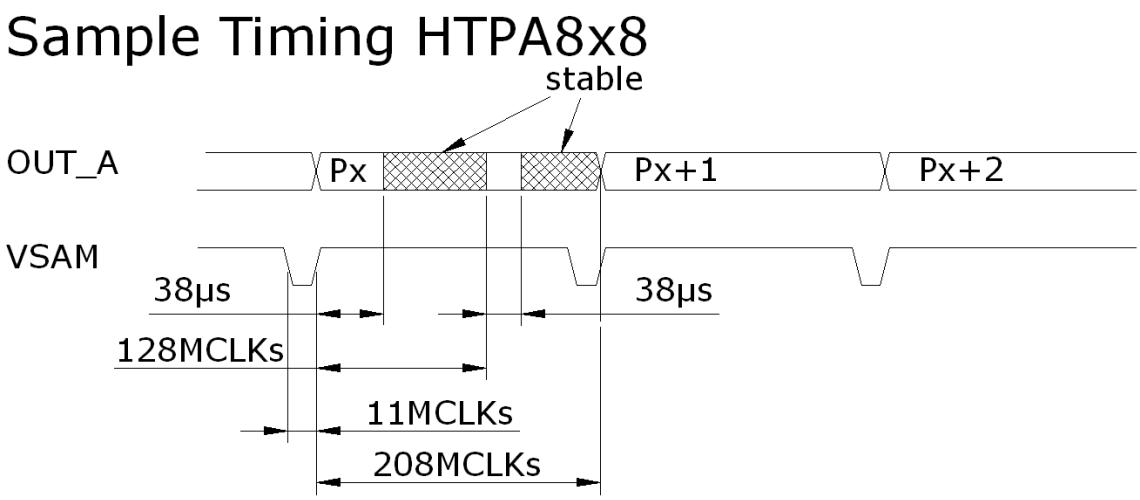
Electrical Characteristics (continued)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Analog Output						
Output voltage swing	V_{OUTA}	load 10kOhm	0.5		V_{CC}-0.8	V
Power supply rejection ratio	P_{SRR}	AMPL=0 VDD<5V	-16			dB
Output current limit	I_{OUTA}	OUT_A	0.15			mA
General Parameters						
Overall current consumption	I_{DD}	CLK_1MHz=1MHz 25° C	4.5	4.8	5.3	mA
Start up time	T_{POR}	Power On to first VSAM transition			805	cycles

Timings HTPA8x8:



For the HTPA 8x8 every analogous voltage has 2 stable domains, as shown above.

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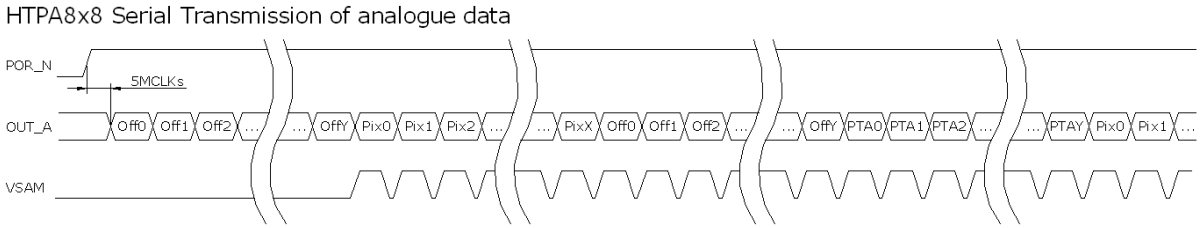
Serial Transmission:



Off0…OffY	Electric offset of amplifier 0 to amplifier Y
Pix0…PixX	Amplified pixel voltage of Pixel0 to PixelX
PTA0…PTAY	PTAT-Signal

Constants for array types:

Type 8x8:
Y=3
X=63

The numeration of the pixels is in all cases line by line.

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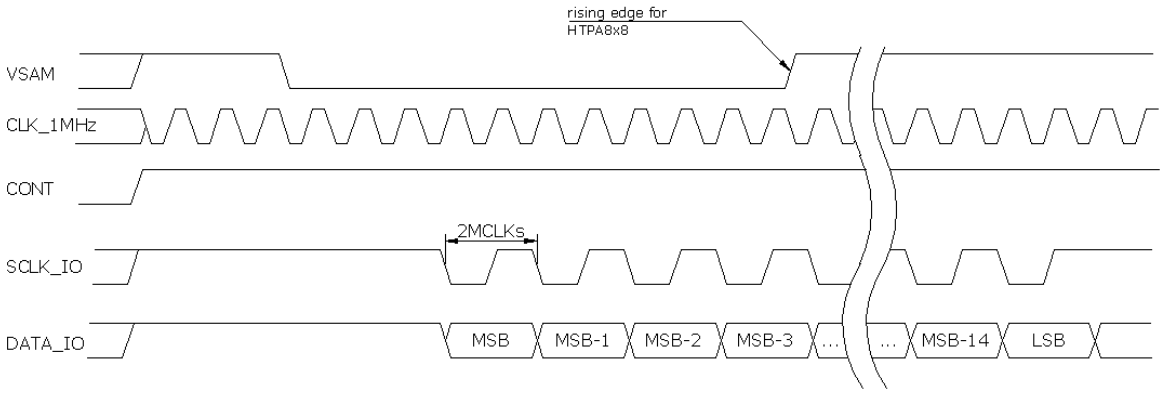
SPI Communication:

Data sampled at rising edge of SCLK, MSB first.
In case of ASIC as master device the frequency of the SCLK_IO is equal to the frequency of MCLK/2.

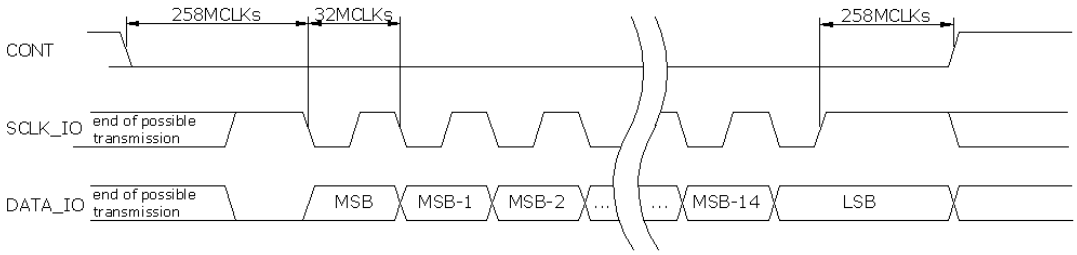
HTPA8x8:
The four MSB's signify the row address of the current pixel, the other bits describe the ADC-result. The ADC result has a large offset and therefore is not accurate. However, it might be used for movement detection or other applications, which not require absolute temperature measurements.

The output drivers for SCLK_IO and DATA_IO are enabled by CONT.
If CONT is low the data can be written serially from external controller through DATA_IO. In that case the external controller has to wait a minimum delay time, until SCLK_IO and DATA_IO output drivers are disabled. After programming, the positive slope of CONT stores the contents, when the number of SCLK-pulses is equal 16. While the output driver of the ASIC is disabled a weak pull up ensures that the SCLK_IO pin is at high level. To execute a reset command, the µC has to write a logical "1" to the R-Bit in to configuration and afterwards a "0" into the R-bit, which requires two write cycles in this special case.

Serial Read from ASIC



Serial Write to ASIC



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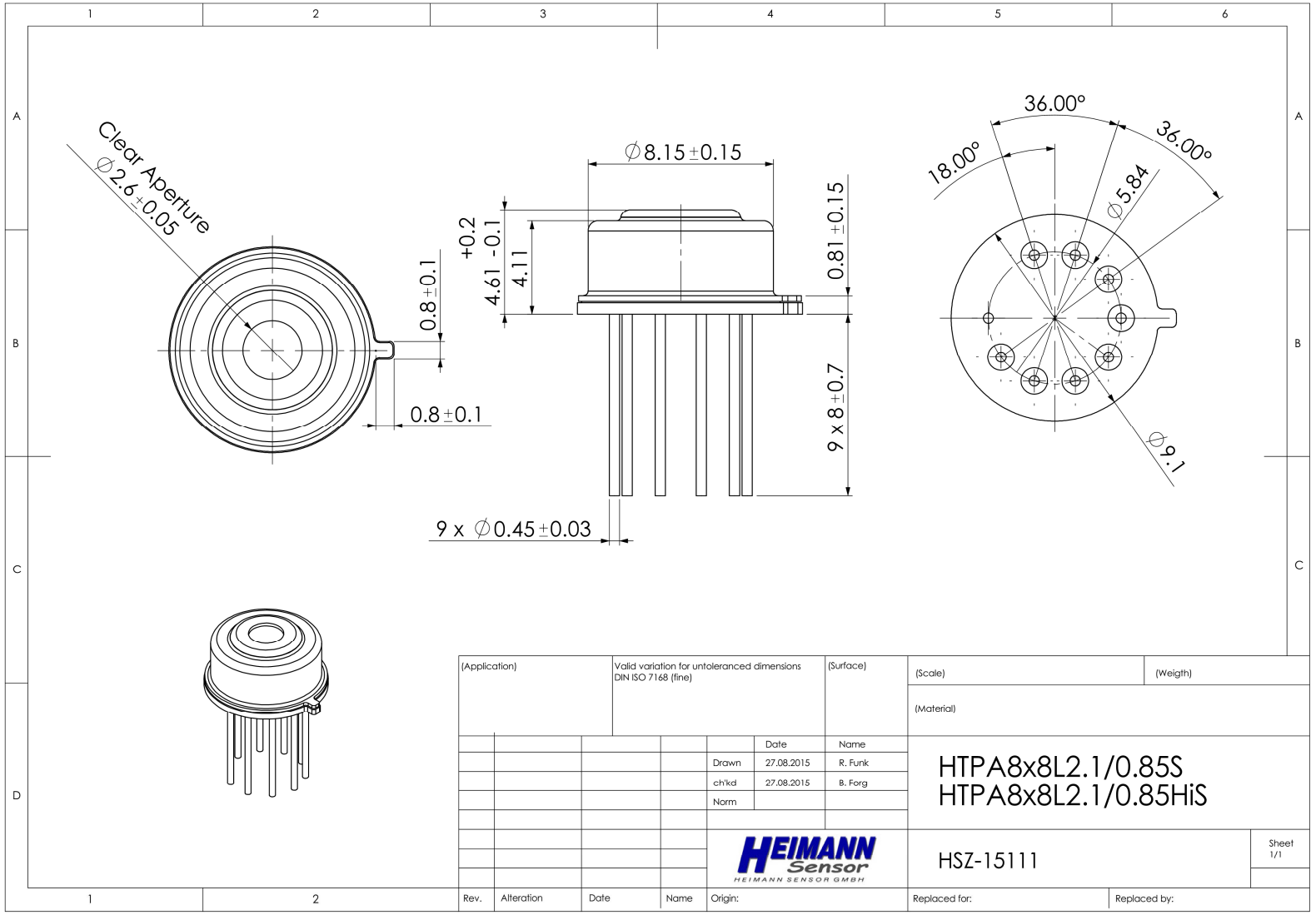
Thermopile Array With Lens Optics
Type HTPA 8x8 L5.5/1.0 Hi S
Type HTPA 8x8 L5.5/1.0 S

Dimensions:



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