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A CMOS-Based Thermopile Array Fabricated on a Single SiO_2 Membrane †

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Abstract: We present a novel thermopile-based infrared (IR) sensor array fabricated on a single CMOS dielectric membrane, comprising of poly-silicon p^+ and n^+ elements. Processing of the chip is simplified by fabricating the entire array on a single membrane and by using standard CMOS Al metal layers for thermopile cold junction heatsinking. On a chip area of 1.76 mm × 1.76 mm, with a membrane size of 1.2 mm × 1.2 mm, we fabricated IR sensor arrays with 8 × 8 to 100 × 100 pixels. The 8 × 8 pixel device has <2% thermal crosstalk, a responsivity of 36 V/W and enhanced optical absorption in the 8–14 μm waveband, making it particularly suitable for people presence sensing.

Keywords: MEMS; CMOS; infrared; thermopile array; IR image sensor; presence sensing

1. Introduction

Low-cost IR image sensors are increasingly used for a variety of applications, ranging from home appliances and security to automotive and IR cameras for smartphones [1]. These sensors typically consist of an array of thermopiles or bolometers, with the former being inherently insensitive to changes in ambient temperature [1] and being easier to manufacture using low-cost Complementary Metal–Oxide–Semiconductor (CMOS) fabrication processes [2,3], which makes the technology more attractive for commercialization. Thermopile sensors detect a temperature difference ΔT across each thermopile element and are composed of several thermocouples with their hot junctions thermally isolated, typically by a thin dielectric membrane [4,5]. When the membrane is heated by incident IR radiation, a voltage $V_T = N\alpha\Delta T$ is generated due to the Seebeck effect [5] which is proportional to the temperature difference across the thermocouple elements ΔT, the Seebeck coefficient α and the number of thermocouples N. The responsivity $\Re$ is defined as the change in voltage response due to incident optical power ($\Re = dV_T/dP$) and is highly dependent on the thermal resistance of the device [5]. Micromachining of the silicon substrate can be used to form a membrane with a high thermal resistance to enhance IR heating and thus responsivity [2,3]. A typical array consists of thermopile pixel elements, each fabricated on an isolated membrane, formed by bulk etching of the substrate [1,4]. However, this fabrication method requires critical process control to minimize substrate etching tolerances and undercut. IR thermopile arrays fabricated on a single membrane have been reported but employ non-standard structures above or below the membrane. Examples include bulk silicon layers [6] or additional gold layers [7] acting as heatsinks. Gold is not fully CMOS compatible, which results in non-standard processes and increased fabrication costs [3].

Here we present a CMOS based thermopile array fabricated on a single membrane, employing standard CMOS Al layers for heatsinking of thermopile cold junction elements; a design which simplifies chip processing.

2. Device Fabrication

Our thermopile arrays were fabricated using a commercial 0.35 µm CMOS process on 6 inch Si wafers. Four devices, having array sizes of 8 × 8, 24 × 24, 60 × 60 and 100 × 100 pixels, were fabricated as a proof of concept. The pixels are formed by highly doped p^+ and n^+ poly-Si layers with sheet resistances of 153 Ω/□ and 184 Ω/□ respectively. The interconnects between the poly-Si p^+ and n^+ elements, and the heatsinking tracks between the pixels are formed by three Al interconnect layers, with track widths of 20 µm and thicknesses of 0.4 µm, 0.4 µm and 0.8 µm, respectively (for the 8 × 8 pixel sensor). The SiO_2 based membrane has an area of 1200 µm × 1200 µm and is ~5 µm thick, see Figure 1. The layers were grown on a 375 µm thick Si substrate which was back-etched using Deep Reactive Ion Etching (DRIE) to form the membrane, with the first SiO_2 layer acting as an etch stop. The individual pixels consist of 36 thermocouples with their cold junctions placed adjacent to the surrounding heatsinking tracks, formed by the three Al layers.

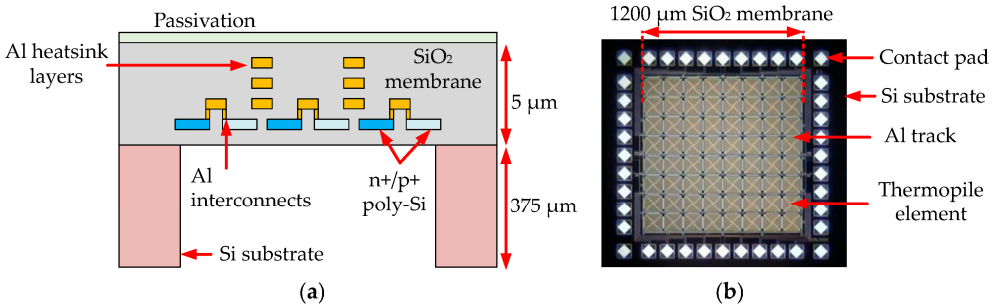

Figure 1. (**a**) Cross-sectional view showing the p^+/n^+ poly-Si and Al layers of the thermopile array; (**b**) Optical image of the thermopile array. Chip size = 1.76 mm × 1.76 mm.

3. Results and Discussions

For measurement purposes, we mounted the device in an open surface mount Quad-Flat No-leads (QFN) type package with the individual pixels electrically bonded. The active pixel elements were addressed using a multiplexer and amplified and digitized using an analogue-front-end integrated circuit (LMP93601), interfaced to an Arduino microcontroller board. The test setup is illustrated in Figure 2. For responsivity tests, the device was mounted at a distance of 50 mm from a blackbody source (Fluke 4180) which was held at a constant temperature of 100 °C.

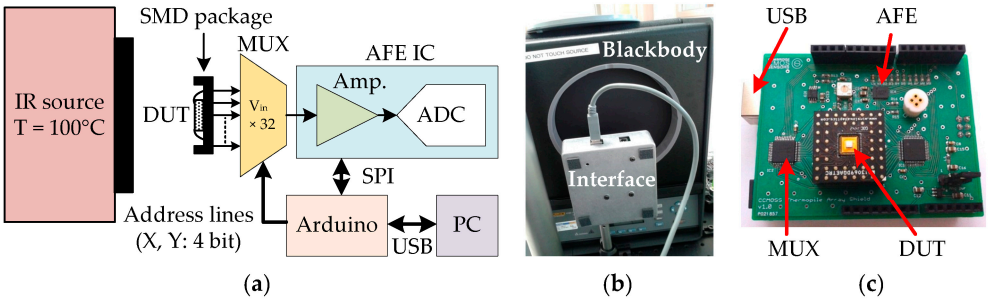

Figure 2. IR detector array: (**a**) Schematic; (**b**) Characterization setup; and (**c**) Circuit board interfacing.

The thermopile detector shows enhanced optical absorption in the 8–14 µm waveband (measured using a FTIR spectrometer) with an absorption peak of ~90% at 8.5 µm (see Figure 3a), making it suitable for people presence detection [8]. Optical absorption can be further enhanced by the addition of a high emissivity coating e.g., gold black layer, at the expense of an extra processing

step [2]. The uniformity of response to IR illumination per pixel for the 8 × 8 pixel array is shown in Figure 3b. Pixel elements in the center of the membrane show a maximum 15% drop in signal level due to the lower efficiency of the thermopile cold junction heatsinking. At the edge of the membrane, the substrate acts as a more efficient heatsink, maximizing ΔT between the hot and cold junctions, thereby creating a higher V_T. Responsivity non-uniformity could be compensated for by external gain compensation e.g. by using an Application-Specific Integrated Circuit (ASIC). The cross-sensitivity of the sensor (a measure of the crosstalk between the pixels) was measured by electrically heating an individual pixel using an embedded micro-heater and measuring V_T for both the heated and adjacent pixels. This is shown in Figure 3c for arrays with differing numbers of pixels. The 8 × 8 and 24 × 24 arrays show low thermal crosstalk (<2%); demonstrating the efficiency of the heatsinking between pixels. Arrays with smaller pixels show increased thermal crosstalk (>3.5%) due to increased thermal leakage, as the thermal path between pixels is reduced.

The 8 × 8 pixel array has a $\Re$ of 36 V/W and a specific detectivity $D^* = \sqrt{Af}/NEP$ of 9.5 × 10^6 cm Hz/W, where A is the membrane area, f the frequency bandwidth and $NEP = S_n/\Re$ the noise-equivalent power with S_n being the noise spectral density. Arrays with smaller pixel areas show a drop in $\Re$ due to the reduced conversion efficiency of each pixel, as shown in Figure 3d. $\Re$ could be further enhanced by vacuum packaging to minimize heat loss which would make higher resolution imaging possible [3].

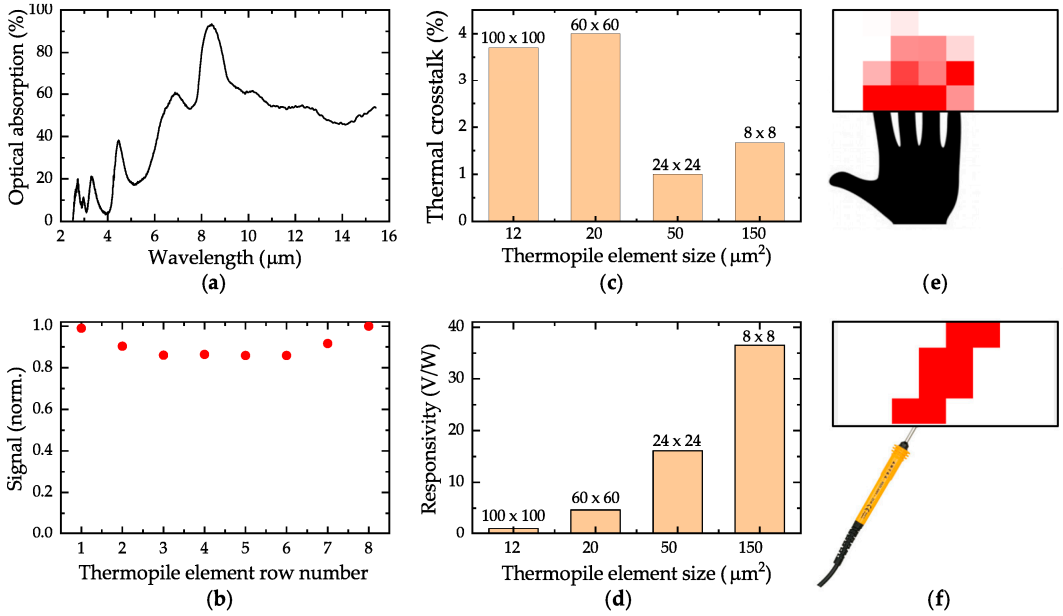

Figure 3. (**a**) Infrared absorption spectrum of the 8 × 8 pixel array measured using FTIR spectroscopy; (**b**) Uniformity of optical response; (**c**) Thermal crosstalk between pixels; (**d**) Responsivity values; (**e**) Hand and (**f**) soldering iron images taken using the 8 × 8 pixel array at 1 m distance (32 pixels addressed).

To demonstrate the application of our sensor, thermal images of objects were acquired using an Umicore IR lens [focal length = 6.8 mm, f-number = 1.4, and field of view (FOV) = 8°] and are shown in Figure 3e,f. People presence detection was possible at a distance of 2 m and there was good contrast between pixel elements. A fuller range of specifications for our sensor is presented in Table 1.

Table 1. Characteristics of the 8 × 8 pixel thermopile array.

Parameter	Value
Chip size	1.76 mm × 1.76 mm
Sensor elements	8 × 8 pixels
Thermopile material	n^+/p^+ Poly-Si
Membrane area	1200 μm × 1200 μm
Pixel area	150 × 150 μm
Membrane thickness	5.17 μm
Detector resistance	201 kΩ
$\Re$ (100 °C, 1 Hz)	36.5 V/W
D^* (100 °C, 1 Hz)	9.5×10^6 cm $\sqrt{\text{Hz}}$ /W
NEP	1.6 nW $\sqrt{\text{Hz}}$
S_n	58 nV/$\sqrt{\text{Hz}}$
Thermal crosstalk	<2%

4. Conclusions

A CMOS thermopile-based IR sensor array fabricated on a single SiO_2 dielectric membrane, comprising of poly-Si p^+ and n^+ elements has been demonstrated. Processing of the chip is simplified by the use of a single membrane and standard CMOS Al layers for thermopile cold junction heatsinking. The 8 × 8 pixel array with 20 μm wide heatsinking tracks shows low crosstalk (<2%), enhanced optical absorption in the 8–14 μm band and has a responsivity of 36 V/W, making it suitable for people presence and gesture detection, in low cost applications. Vacuum packaging and high emissivity coating could be used to further enhance responsivity.

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Conflicts of Interest: The authors declare no conflict of interest.

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