Content

HEIMANN Sensor GmbH
Maria-Reiche-Str. 1
D-01109 Dresden / Germany

Contact / Customer Support
Phone 49 (0) 6123 60 50 30
Fax 49 (0) 6123 60 50 39

Internet
www.heimannsensor.com
mail: info@heimannsensor.com

1 Principal Schematic for HTPA16x16d:

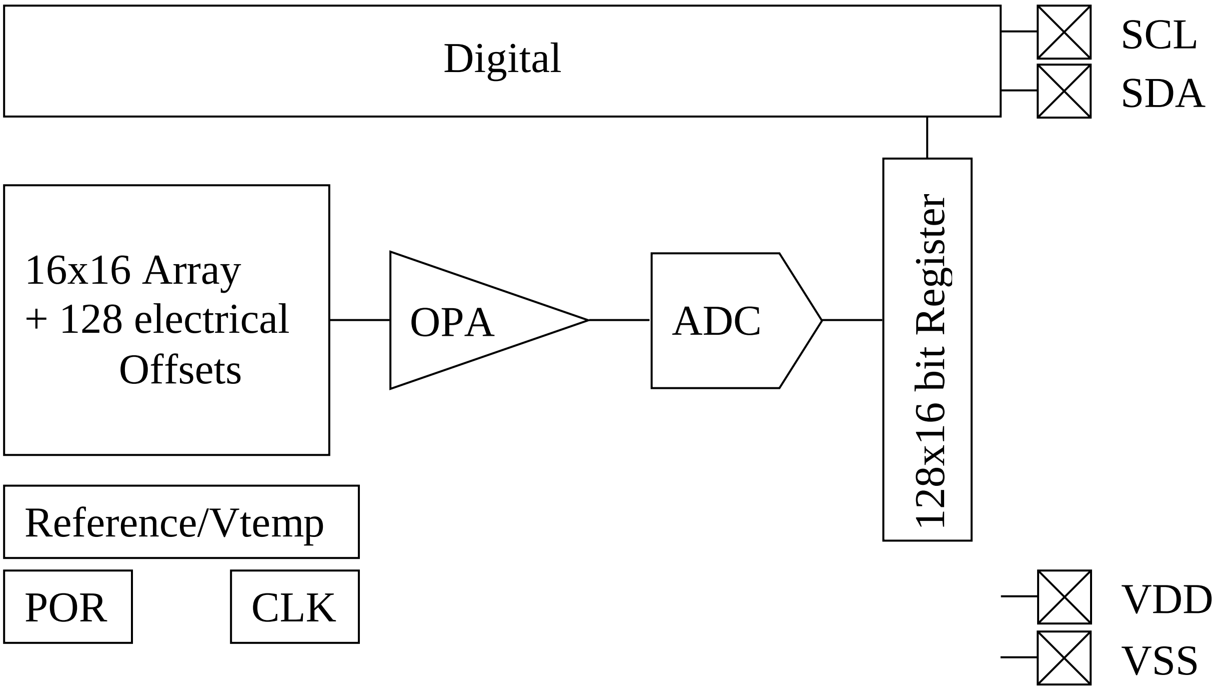

Figure 1: Schematic for HTPA16x16d

2 Pin Assignment– Bottom View:

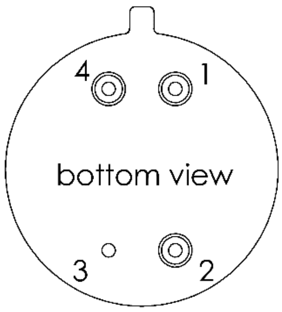

Figure 2: pin-allocation

Pin	Symbol	Description
1	SCL	Digital I/O, Open Drain, 100k PU, Serial Clock
2	VDD	Positive supply voltage
3	VSS	Negative supply voltage / Ground (0V) (connected to housing)
4	SDA	Digital I/O, Open Drain, 100k PU, Serial Data

HEIMANN Sensor GmbH
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D-01109 Dresden / Germany

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3 Optical Orientation

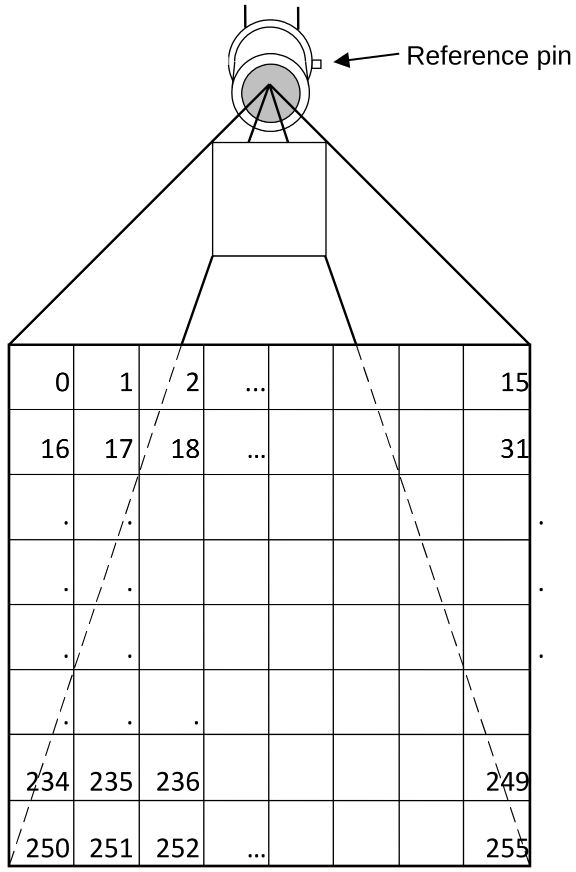

Figure 3: Optical orientation

HEIMANN Sensor GmbH
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D-01109 Dresden / Germany

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4 Order Code Example

HTPA32x32	S	d	R1	L10/0.95	F8-14	e	Hi	M	(SPI)	[Si]

Type:	
HTPA32x32	Please contact support for all available HTPA and module combinations.
Package:	
S	SMD variant
Not declared	TO can variant
Output:	
d	HTPA sensor with digital output
Not declared	HTPA sensor with analogous output
Revision:	
R1	Silicon revision 1
Optics:	
L	Focal length: In example L10 = 10.0 mm focal length
/	F-Number: In example /0.95
	For optics see also "HTPA standard optics"
Filter:	
F	Filter characteristics. In example F8-14 (µm, Bandpass)
Not declared	Broad band ARC
External aperture:	
Not declared	without external aperture
e	with external aperture
Sensitivity:	
UHi	Ultra high sensitivity
Hi	Increased sensitivity
Not declared	Standard sensitivity
Version:	
A	Application set: comes with GUI, housing, power supply. Always UDP Interface.
C	Calibrated sensor (only digital). Carries calibration constants on internal EEPROM
M	Module: HTPA sensor soldered to PCB, calibrated stream
S	HTPA sensor only. Raw voltage output, not calibrated
Interface:	
SPI	SPI device; Two variants: Analogous HTPAs: 14bit ADC Digital HTPA: 16bit ADC
UDP	Ethernet, CAT5 cable connection
PoE	Power over Ethernet, CAT5 connection, UDP protocol
Lens Material:	
Si	Silicon
Not declared	Germanium

Figure 4: Exemplary order code

5 Serial Order of Frame

The sensor is divided into two parts (top and bottom half) which are again separated into 2 blocks. The readout order is shown below for the different blocks.

Block 0 (top)
Block 1 (top)
Block 1 (bottom)
Block 0 (bottom)

Figure 5: Division of blocks

Whenever a conversion is started the Block x of the top and bottom half are measured at the same time. Each block consists of 64 Pixel that are sampled fully parallel. The readout order on the bottom half is mirrored compared to the top half so that the central lines are always read last.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255

readout order top

readout order bottom

Figure 6: 16x16d readout order for active pixel

The electrical offsets are sampled in parallel for the top and bottom half. The matching rows for the corresponding electrical offsets and active Pixel are marked with the same color. The conversion of the electrical offsets is started by sending the command for the BLIND bit during the start command, see 8.3.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127

Figure 7: 16x16d readout order for electrical offsets

HEIMANN Sensor GmbH
Maria-Reiche-Str. 1
D-01109 Dresden / Germany

Contact / Customer Support
Phone 49 (0) 6123 60 50 30
Fax 49 (0) 6123 60 50 39

Internet
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mail: info@heimannsensor.com

6 Characteristics:

6.1 Common Specifications:

Technology	n-poly/p-poly Si
Element Resistance	approx. 300 kOhms
Sensitivity	approx. 450 V/W without optics and filter
Thermal pixel time constant	<4 ms
Digital Interface	I²C
Analog Output	No
Selectable Clock	1 to 13 MHz
EEPROM size	1024x16 Bit

Pitch	90 µm
Absorber size	44 µm
Max. Framerate	120 Hz

(complete frame with maximum I²C and sensor clock speed and reduced ADC resolution)
256 sensitive elements

6.2 Optical characteristics:

Focal length:	2.1 mm ("L" equals the focal length of the lens)
F-Number:	0.8
Field of view:	45 x 45 deg
Lens coating:	LWP-Coating 5.0
	Cut On (Tr. 5%): 5.0 µm ± 0.3 µm

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6.3 Electric Specifications

Table 1: Absolute Maximum Ratings

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{DD}		-0.3		3.6	V
Voltage at All inputs and outputs	V_{IO}		-0.3		V_{DD}+0.3	V
Storage Temperature	T_{STG}		-40		85	Deg. C

Table 2: Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{DD}		3.3	3.35	3.6	V
Supply Current (sensor running)	I_{DD}		3	3.3	3.8	mA
Supply Current (sensor in idle state)	I_{DD}			TBD		mA
Standby Current (sensor in sleep state)	I_{SBY}			TBD		µA
Operation Temperature	T_A		-20		65	Deg. C
ESD-Protection		Human body model 100pF + 1k5Ohm	2.0			kV

Table 3: Electrical Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Digital Input						
Internal Clock frequency	F_{CLK}		1	5	13	MHz
Internal I²C Pull up	R_{PU}		1	100	100	kOhm
Bias current	I_{BIAS}		1	3	13	µA
BPA current	I_{BPA}		0.2	1.5	4.0	µA
Input voltage high	V_{IH}		0.7xV_{DD}			V
Input voltage low	V_{IL}				0.3xV_{DD}	V
PTAT						
Temperature range			TBD		TBD	Deg. C
PTAT gradient				TBD		K/V

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Table 4: Preamplifier / ADC

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Chopper frequency	F_{CHP}			20		kHz
Preamplifier Noise	N_{PA}	at 20 kHz		72		$nV/HZ^{1/2}$
Frame rate (Full Array)	FR1			18		Hz
Frame rate (Half Array)	FR4			36		HZ
ADC pos. Reference	V_{REFP}			1.6		V
ADC neg. Reference	V_{REFN}			0.9		V
ADC resolution	ADC_{LSB}	at 16 Bit		21		µV

7 I²C Timings HTPA16x16d:

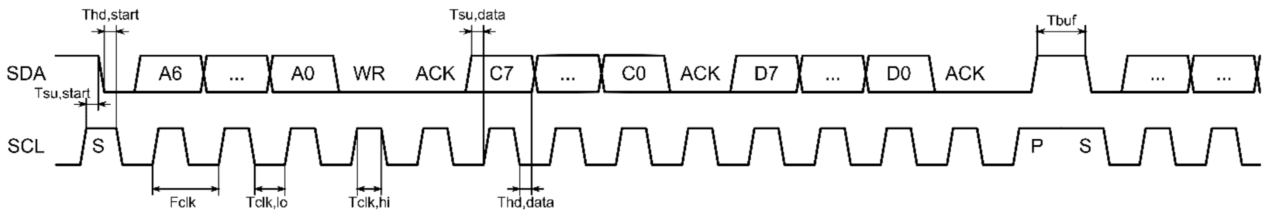

Figure 8: I²C Timings of HTPA16x16d

Table 5: I²C Timings

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
I²C clock frequency	F_{CLK}			400	1000	kHz
low pulse duration	$T_{CLK,lo}$		0.50			µs
high pulse duration	$T_{CLK,hi}$		0.26			µs
data set up time	$T_{SU,data}$		0.05			µs
data hold time	$T_{hd,data}$		0.00			µs
start setup time	$T_{SU,start}$		0.26			µs
start hold time	$T_{hd,start}$		0.26			µs
stop setup time	$T_{SU,stop}$		0.26			µs
stop hold time	$T_{hd,stop}$		0.26			µs
time between STOP / START	T_{buf}		0.50			µs

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8 I²C Communication:

The chip uses the **7-bit I²C address 0x1A** for configuration and **sensor** data and the **7-bit I²C address 0x1B** to access the internal **EEPROM**. The address byte is followed by a W/R bit and an 8-bit command.

8.1 Write Command:

In case of a write access to an internal register the command is followed by the data byte. The chip acknowledges each byte with a low active ACK bit.

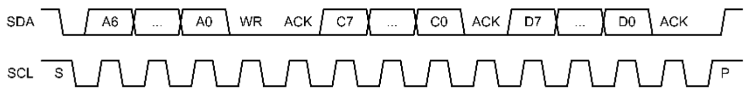

Figure 9: Write command

8.2 Read Command:

To read data from the chip first the address and command must be sent. After the last ACK a new start-bit (repeated start) and the address with a set read-flag initiates the read sequence. There can be bytes read as many as required. The last byte must be denoted by a not-acknowledge. The shown example below can be used e.g. to get the status register.

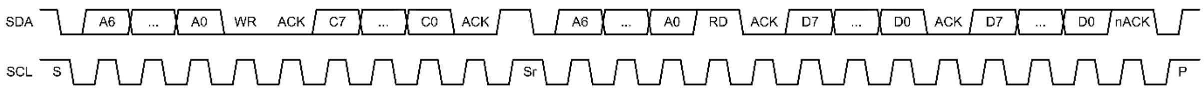

Figure 10: Read command

8.3 Sensor Commands:

The sensor has several registers that can be written and read, they are listed below.

Table 6: Configuration register (write only)

Addr / CMD	0x1A (7 Bit!) / 0x01							
Config Reg	7	6	5	4	3	2	1	0
Name	RFU		BLOCK		START	VDD_MEAS	BLIND	WAKEUP
Default	0	0	0	0	0	0	0	0

The WAKEUP bit is used to switch on / off the chip and must be set prior all other operations. After the START bit is set the chip starts a conversion of the array or blind elements and enters the idle state (not sleep!) when finished. The BLOCK selects one of the four multiplexed array blocks.
If the BLIND bit is set the electrical offsets are sampled instead of the active pixel and the setting of the BLOCK is ignored.
If VDD_MEAS bit is set the VDD voltage is measured instead of the PTAT value.
RFU means reserved for future use and can be subject to change.

HEIMANN Sensor GmbH
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D-01109 Dresden / Germany

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Fax 49 (0) 6123 60 50 39

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Table 7: Status Register (read only)

Addr / CMD	0x1A (7 Bit!) / 0x02							
Status Reg	7	6	5	4	3	2	1	0
Name	RFU				BLOCK		VDD_MEAS	EOC
Default	0	0	0	0	0	0	0	0

If the EOC flag is set a previous started conversion has been finished.

Table 8: Trim Register 1 (write only)

Addr / CMD	0x1A (7 Bit!) / 0x03							
Trim Reg 1	7	6	5	4	3	2	1	0
Name	RFU				MBIT TRIM			
Default	0	0	0	0	1	1	0	0

MBIT_TRIM: m = 4 to 12 ⇒ (m+4) bit as ADC resolution (Default: m=12)

Table 9: Trim Register 2 (write only)

Addr / CMD	0x1A (7 Bit!) / 0x04							
Trim Reg 2	7	6	5	4	3	2	1	0
Name	RFU			BIAS TRIM TOP				
Default	0	0	0	0	1	1	0	0

BIAS_TRIM_TOP: 0 to 31 ⇒ 1µA to 13µA (Default: 5µA)
This setting is used to adjust the bias current of the ADC. A faster clock frequency requires a higher bias current setting.

Table 10: Trim Register 3 (write only)

Addr / CMD	0x1A (7 Bit!) / 0x05							
Trim Reg 3	7	6	5	4	3	2	1	0
Name	RFU			BIAS TRIM BOT				
Default	0	0	0	0	1	1	0	0

BIAS_TRIM_BOT: 0 to 31 ⇒ 1µA to 13µA (Default: 5µA)
This setting is used to adjust the bias current of the ADC. A faster clock frequency requires a higher bias current setting.

Table 11: Trim Register 4 (write only)

Addr / CMD	0x1A (7 Bit!) / 0x06							
Trim Reg 4	7	6	5	4	3	2	1	0
Name	RFU		CLK TRIM					
Default	0	0	0	1	0	1	0	1

CLK_TRIM: 0 to 63 ⇒ 1MHz to 13MHz (Default: 5MHz)
NOTE: The measure time depends on the clock frequency settings. One quarter frame takes about:

$$t_{FR4} = \frac{32 \cdot \left(2^{MBIT} + 4\right)}{F_{CLK}} \approx 27ms@5MHz$$

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Table 12: Trim Register 5 (write only)

Addr / CMD	0x1A (7 Bit!) / 0x07							
Trim Reg 5	7	6	5	4	3	2	1	0
Name	RFU			BPA TRIM TOP				
Default	0	0	0	0	1	1	0	0

BPA_TRIM_TOP: 0 to 31 ⇒ 0.2µA to 4.0µA (Default: 1.5µA)
This setting is used to adjust the common mode voltage of the preamplifier.

Table 13: Trim Register 6 (write only)

Addr / CMD	0x1A (7 Bit!) / 0x08							
Trim Reg 6	7	6	5	4	3	2	1	0
Name	RFU			BPA TRIM BOT				
Default	0	0	0	0	1	1	0	0

BPA_TRIM_BOT: 0 to 31 ⇒ 0.2µA to 4.0µA (Default: 1.5µA)
This setting is used to adjust the common mode voltage of the preamplifier.

Table 14: Trim Register 7 (write only)

Addr / CMD	0x1A (7 Bit!) / 0x09							
Trim Reg 7	7	6	5	4	3	2	1	0
Name	PU SDA TRIM				PU SCL TRIM			
Default	1	0	0	0	1	0	0	0

PU_SDA_TRIM: select internal pull up resistor on SDA (Default: 100kOhm)
PU_SCL_TRIM: select internal pull up resistor on SCL (Default: 100kOhm)
"1000" = 100 kOhm; "0100" = 50 kOhm; "0010" = 10 kOhm; "0001" = 1 kOhm

Table 15: Read Data 1 Command (Top Half of Array)

Addr / CMD	0x1A (7 Bit!) / 0x0A							
Read Data	7	6	5	4	3	2	1	0
1. Byte / 2. Byte	PTAT 1 MSB / LSB							
3. Byte / 4. Byte	Pixel (0+BLOCK*64) MSB / LSB							
5. Byte / 6. Byte	Pixel (1+BLOCK*64) MSB / LSB							
…	…							
129. Byte / 130. Byte	Pixel (63+BLOCK*64) MSB / LSB							

Table 16: Read Data 2 Command (Bottom Half of Array)

Addr / CMD	0x1A (7 Bit!) / 0x0B							
Read Data	7	6	5	4	3	2	1	0
1. Byte / 2. Byte	PTAT 2 MSB / LSB							
3. Byte / 4. Byte	Pixel (240-BLOCK*64) MSB / LSB							
5. Byte / 6. Byte	Pixel (241-BLOCK*64) MSB / LSB							
…								
33. Byte / 34. Byte	Pixel (255-BLOCK*64) MSB / LSB							
35. Byte / 36. Byte	Pixel (224-BLOCK*64) MSB / LSB							
37. Byte / 38. Byte	Pixel (225-BLOCK*64) MSB / LSB							
…								

65. Byte / 66. Byte	Pixel (239-BLOCK*64) MSB / LSB
67. Byte / 68. Byte	Pixel (192-BLOCK*64) MSB / LSB
…	
129. Byte / 130. Byte	Pixel (207-BLOCK*64) MSB / LSB

The complete sensor data must be read at once. If the communication fails somewhere in between, all successive data will be corrupted. The readout can be stopped anywhere by pausing the clock. A new initialized readout proceeds at this stopped byte by continuing the clock, but the index is reset when a new conversion has been started.
If the bit for the electrical offsets (Bit 1 in Config 0x01) is set the electrical offsets are sampled and can be read similar to the active pixel:

Table 17: Read Data electrical offsets (Top Half of Array)

Addr / CMD	0x1A (7 Bit!) / 0x0A							
Read Data	7	6	5	4	3	2	1	0
1. Byte / 2. Byte	PTAT 1 MSB / LSB or VDD 1 MSB / LSB							
3. Byte / 4. Byte	electrical offset (0) MSB / LSB							
5. Byte / 6. Byte	electrical offset (1) MSB / LSB							
…	…							
129. Byte / 130. Byte	electrical offset (63) MSB / LSB							

Table 18: Read Data electrical offsets (Bottom Half of Array)

Addr / CMD	0x1A (7 Bit!) / 0x0B							
Read Data	7	6	5	4	3	2	1	0
1. Byte / 2. Byte	PTAT 2 MSB / LSB or VDD 2 MSB / LSB							
3. Byte / 4. Byte	electrical offset (112) MSB / LSB							
5. Byte / 6. Byte	electrical offset (113) MSB / LSB							
…	…							
33. Byte / 34. Byte	electrical offset (127) MSB / LSB							
35. Byte / 36. Byte	electrical offset (96) MSB / LSB							
…	…							
129. Byte / 130. Byte	electrical offset (79) MSB / LSB							

The complete sensor data must be read at once. If the communication fails somewhere in between, all successive data will be corrupted. The readout can be stopped anywhere by pausing the clock. A new initialized readout proceeds at this stopped byte by continuing the clock, but the index is reset when a new conversion has been started.

8.4 EEPROM communication

To read/write data from/to the internal EEPROM the I2C address 0x1B is used.

Table 19: EEPROM Commands

Name	CMD	Read / Write	Comment
Standby	0x00	W	
Active	0x01	W	releases all signals to default state wait for 15µs when wake up from standby
Normal Erase	0x02	W	program pulse width 5ms
Normal Write	0x03	W	program pulse width 5ms

Block Erase	0x04	W	program pulse width 5ms
Block Write	0x05	W	program pulse width 5ms
Normal Read	0x06	W	
Set Data	0x0A	W	16 bit data, MSB first
Get Data	0x0B	R	16 bit data, MSB first

Note: The EEPROM must be activated (wake up from standby) prior being used. The active command also initializes the EEPROM to its default state.
Note: Each word must be erased before it can be written, a write command stores only a “1” to the EEPROM cell.
Note: The commands “SET_DATA” / “GET_DATA” will increment the address pointer, except for the first execution after “SET_ADDR”.

8.5 I²C Example Sequences – EEPROM Wakeup / Standby

	ADDR	W/R	EEPROM_ACTIVE	
S	0x1B	0	0x01	P

	ADDR	W/R	EEPROM_STANDBY	
S	0x1B	0	0x01	P

Figure 11: EEPROM Wakeup / Standby

8.6 I²C Example Sequences – EEPROM Block Erase / Block Write

	ADDR	W/R	BLOCK_ERASE	
S	0x1B	0	0x04	P

wait 5ms

	ADDR	W/R	EEPROM_ACTIVE	
S	0x1B	0	0x01	P

	ADDR	W/R	SET_DATA	DATA_MSB	DATA_LSB	
S	0x1B	0	0x0A	DATA	DATA	P

	ADDR	W/R	BLOCK_WRITE	
S	0x1B	0	0x05	P

wait 5ms

	ADDR	W/R	EEPROM_ACTIVE	
S	0x1B	0	0x01	P

Figure 12: EEPROM Block Erase / Block Write

HEIMANN Sensor GmbH
Maria-Reiche-Str. 1
D-01109 Dresden / Germany

Contact / Customer Support
Phone 49 (0) 6123 60 50 30
Fax 49 (0) 6123 60 50 39

Internet
www.heimannsensor.com
mail: info@heimannsensor.com

8.7 I²C Example Sequences – EEPROM Sequential Erase / Write

	ADDR	W/R	SET_ADDR	EEP_ADDR	
S	0x1B	0	0x09	ADDR	P

	ADDR	W/R	NORMAL_ERASE	
S	0x1B	0	0x02	P

wait 5ms

	ADDR	W/R	SET_DATA	DATA_MSB	DATA_LSB	
S	0x1B	0	0x0A	DATA	DATA	P

	ADDR	W/R	NORMAL_WRITE	
S	0x1B	0	0x03	P

wait 5ms

	ADDR	W/R	SET_ADDR	EEP_ADDR	
S	0x1B	0	0x09	ADDR	P

	ADDR	W/R	NORMAL_ERASE	
S	0x1B	0	0x02	P

wait 5ms

	ADDR	W/R	SET_DATA	DATA_MSB	DATA_LSB	
S	0x1B	0	0x0A	DATA	DATA	P

	ADDR	W/R	NORMAL_WRITE	
S	0x1B	0	0x03	P

wait 5ms

	ADDR	W/R	SET_ADDR	EEP_ADDR	
S	0x1B	0	0x09	ADDR	P

	ADDR	W/R	NORMAL_ERASE	
S	0x1B	0	0x02	P

wait 5ms

	ADDR	W/R	SET_DATA	DATA_MSB	DATA_LSB	
S	0x1B	0	0x0A	DATA	DATA	P

	ADDR	W/R	NORMAL_WRITE	
S	0x1B	0	0x03	P

wait 5ms

	ADDR	W/R	SET_ADDR	EEP_ADDR	
S	0x1B	0	0x09	ADDR	P

	ADDR	W/R	NORMAL_ERASE	
S	0x1B	0	0x02	P

wait 5ms

	ADDR	W/R	EEPROM_ACTIVE	
S	0x1B	0	0x01	P

Figure 13: EEPROM Sequential Erase / Write

HEIMANN Sensor GmbH
Maria-Reiche-Str. 1
D-01109 Dresden / Germany

Contact / Customer Support
Phone 49 (0) 6123 60 50 30
Fax 49 (0) 6123 60 50 39

Internet
www.heimannsensor.com
mail: info@heimannsensor.com

8.8 I2C Example Sequence – EEPROM Continuous Erase

	ADDR	W/R	SET_ADDR	EEP_ADDR	
S	0x1B	0	0x09	ADDR	P

	ADDR	W/R	NORMAL_ERASE	
S	0x1B	0	0x02	P

wait 5ms

	ADDR	W/R	SET_ADDR	EEP_ADDR	
S	0x1B	0	0x09	ADDR	P

	ADDR	W/R	NORMAL_ERASE	
S	0x1B	0	0x02	P

wait 5ms

	ADDR	W/R	EEPROM_ACTIVE	
S	0x1B	0	0x01	P

Figure 14: EEPROM Continuous Erase

8.9 I2C Example Sequence – EEPROM Continuous Write

	ADDR	W/R	SET_ADDR	EEP_ADDR	
S	0x1B	0	0x09	ADDR	P

	ADDR	W/R	SET_DATA	DATA_MSB	DATA_LSB	
S	0x1B	0	0x0A	DATA	DATA	P

	ADDR	W/R	NORMAL_WRITE	
S	0x1B	0	0x03	P

wait 5ms

	ADDR	W/R	SET_DATA	DATA_MSB	DATA_LSB	
S	0x1B	0	0x0A	DATA	DATA	P

	ADDR	W/R	NORMAL_WRITE	
S	0x1B	0	0x03	P

wait 5ms

	ADDR	W/R	EEPROM_ACTIVE	
S	0x1B	0	0x01	P

Figure 15: EEPROM Continuous Write

8.10 I2C Example Sequence – EEPROM Sequential Read

	ADDR	W/R	SET_ADDR	EEP_ADDR	
S	0x1B	0	0x09	ADDR	P

	ADDR	W/R	NORMAL_READ	
S	0x1B	0	0x06	P

	ADDR	W/R	GET_DATA		ADDR	W/R	DATA_MSB	DATA_LSB	
S	0x1B	0	0x0B	Sr	0x1B	1	??	??	P

	ADDR	W/R	SET_ADDR	EEP_ADDR	
S	0x1B	0	0x09	ADDR	P

	ADDR	W/R	NORMAL_READ	
S	0x1B	0	0x06	P

	ADDR	W/R	GET_DATA		ADDR	W/R	DATA_MSB	DATA_LSB	
S	0x1B	0	0x0B	Sr	0x1B	1	??	??	P

	ADDR	W/R	EEPROM_ACTIVE	
S	0x1B	0	0x01	P

Figure 16: EEPROM Sequential Read

8.11 I2C Example Sequence – EEPROM Continuous Read

	ADDR	W/R	SET_ADDR	EEP_ADDR	
S	0x1B	0	0x09	ADDR	P

	ADDR	W/R	NORMAL_READ	
S	0x1B	0	0x06	P

	ADDR	W/R	GET_DATA		ADDR	W/R	DATA_MSB	DATA_LSB	
S	0x1B	0	0x0B	Sr	0x1B	1	??	??	P

	ADDR	W/R	GET_DATA		ADDR	W/R	DATA_MSB	DATA_LSB	
S	0x1B	0	0x0B	Sr	0x1B	1	??	??	P

	ADDR	W/R	GET_DATA		ADDR	W/R	DATA_MSB	DATA_LSB	
S	0x1B	0	0x0B	Sr	0x1B	1	??	??	P

	ADDR	W/R	GET_DATA		ADDR	W/R	DATA_MSB	DATA_LSB	
S	0x1B	0	0x0B	Sr	0x1B	1	??	??	P

	ADDR	W/R	EEPROM_ACTIVE	
S	0x1B	0	0x01	P

Figure 17: EEPROM Continuous Read

HEIMANN Sensor GmbH
Maria-Reiche-Str. 1
D-01109 Dresden / Germany

Contact / Customer Support
Phone 49 (0) 6123 60 50 30
Fax 49 (0) 6123 60 50 39

Internet
www.heimannsensor.com
mail: info@heimannsensor.com

8.12 I²C Example Sequences – Init and Read Thermopile Array

(There should be a delay of at least 5 ms between the write of each Configuration Register)

	ADDR	W/R	CONFIG_REG	WAKEUP	
S	0x1A	0	0x01	0x01	P

	ADDR	W/R	TRIM_REG1	MBIT_TRIM	
S	0x1A	0	0x03	0x0C	P

	ADDR	W/R	TRIM_REG2	BIAS_TRIML	
S	0x1A	0	0x04	0x0C	P

	ADDR	W/R	TRIM_REG3	BIAS_TRIMR	
S	0x1A	0	0x05	0x0C	P

	ADDR	W/R	TRIM_REG4	CLK_TRIM	
S	0x1A	0	0x06	0x14	P

	ADDR	W/R	TRIM_REG5	BPA_TRIML	
S	0x1A	0	0x07	0x0C	P

	ADDR	W/R	TRIM_REG6	BPA_TRIMR	
S	0x1A	0	0x08	0x0C	P

	ADDR	W/R	TRIM_REG7	PU_TRIM	
S	0x1A	0	0x09	0x88	P

	ADDR	W/R	CONFIG_REG	START|WAKEUP	
S	0x1A	0	0x01	0x09	P

	ADDR	W/R	STATUS_REG		ADDR	W/R	STATUS	
S	0x1A	0	0x02	Sr	0x34	1	??	P

Wait 30 ms (Poll EOC bit)

	ADDR	W/R	STATUS_REG		ADDR	W/R	STATUS	
S	0x1A	0	0x02	Sr	0x34	1	??	P

	ADDR	W/R	READ_DATA 1		ADDR	W/R	PTAT1 MSB	PTAT1 LSB	P0,0 MSB	P0,0 LSB	…	Px,y MSB	Px,y LSB	
S	0x1A	0	0x0A	Sr	0x34	1	??	??	??	??	…	??	??	P

	ADDR	W/R	READ_DATA 2		ADDR	W/R	PTAT2 MSB	PTAT2 LSB	P0,0 MSB	P0,0 LSB	…	Px,y MSB	Px,y LSB	
S	0x1A	0	0x0B	Sr	0x34	1	??	??	??	??	…	??	??	P

	ADDR	W/R	CONFIG_REG	SLEEP	
S	0x1A	0	0x01	0x00	P

Figure 18: Init and Read Thermopile Array

HEIMANN Sensor GmbH
Maria-Reiche-Str. 1
D-01109 Dresden / Germany

Contact / Customer Support
Phone 49 (0) 6123 60 50 30
Fax 49 (0) 6123 60 50 39

Internet
www.heimannsensor.com
mail: info@heimannsensor.com

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9 Temperature calculation

The object and ambient temperature can be calculated from the sensor output and the stored calibration data. The table below is showing an overview of the EEPROM.

16x16d	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
0	PixCmin [float]		PixCmax [float]						gradScale	GlobalGain			TN	epsilon		
10											MBIT(calib)	BIAS(calib)	CLK(calib)	BPA(calib)	PU(calib)	
20	MBIT(user)	BIAS(user)	CLK(user)	BPA(user)	PU(user)	VDDTh1	VDDTh2						PTATTh1	PTATTh2		
30					PTAT-gradient (float)		PTAT-offset (float)				Device ID				VddScGrad	VddScOff
40 … 90	VddCompGrad stored as 12 bit sigend values															
A0 … F0	VddCompOff stored as 12 bit sigend values															
100 … 1F0	$Th1_{ij}$ / $Grad_{ij}$ stored as 16 bit signed values															
200 … 2F0	$Th2_{ij}$ /$Offset_{ij}$ stored as 16 bit signed values															
300 … 3F0	P_{ij} stored as 16 bit unsigned values															

Figure 19: EEPROM overview 16x16d

All values are stored as unsigned 16 bit values in the little endian format unless they are specified otherwise. Grey marked areas are used during calibration or for future use and are Heimann Sensor reserved.
MBIT(calib), BIAS(calib), CLK(calib), BPA(calib) and PU(calib) are the settings for the registers that have been used during calibration (see chapter 8.3 on how to set them).
MBIT(user), BIAS(user), CLK(user), BPA(user) and PU(user) are free to be set by the user. The temperature calculation is only valid if the same settings are used that have been set during calibration!
TN is the tablenumber and has to match the given tablenumber in the sample code.
GlobalGain, VDDTh1, VDDTh2, PTATTh1 and PTATTh2 are stored as 16 bit unsigned values.
VDDTH1 and VDDTH2 is the used supply voltage during calibration measured by the sensor itself and stored in Digits.
The corresponding order of $ThGrad_{ij}$, $ThOffset_{ij}$ and P_{ij} to the Pixelnumber is given by the following overview:

16x16d

ThGrad$_{0,0}$ → Pixel 0	ThGrad$_{0,1}$ → Pixel 1	…	ThGrad$_{0,15}$ → Pixel 15
ThGrad$_{1,0}$ → Pixel 16	ThGrad$_{1,1}$ → Pixel 17	…	ThGrad$_{1,15}$ → Pixel 31
.			
.			
.			
ThGrad$_{7,0}$ → Pixel 112	ThGrad$_{7,1}$ → Pixel 113	…	ThGrad$_{7,15}$ → Pixel 127
ThGrad$_{8,0}$ → Pixel 240	ThGrad$_{8,1}$ → Pixel 241	…	ThGrad$_{8,15}$ → Pixel 255
ThGrad$_{9,0}$ → Pixel 224	ThGrad$_{9,1}$ → Pixel 225	…	ThGrad$_{9,15}$ → Pixel 239
.			
.			
.			
ThGrad15$_{,0}$ → Pixel 128	ThGrad$_{31,1}$ → Pixel 129	…	ThGrad$_{31,31}$ → Pixel 143

Figure 20: Readout order 16x16d

HEIMANN Sensor GmbH
Maria-Reiche-Str. 1
D-01109 Dresden / Germany

Contact / Customer Support
Phone 49 (0) 6123 60 50 30
Fax 49 (0) 6123 60 50 39

Internet
www.heimannsensor.com
mail: info@heimannsensor.com

The order of $VddCompGrad_{ij}$ and $VddCompOff_{ij}$ is similar to the electrical Offsets and have to be used block by block. $VddCompGrad_{ij}$ and $VddCompOff_{ij}$ are stored as 12 bit signed values. Please check the sample code for a more detailed readout of the 12 bit values.

16x16d

VddCompGrad$_{0,0}$ → Pixel 0	VddCompGrad$_{0,1}$ → Pixel 1	…	VddCompGrad$_{0,15}$ → Pixel 15	top half
VddCompGrad$_{1,0}$ → Pixel 15	VddCompGrad$_{1,1}$ → Pixel 16	…	VddCompGrad$_{1,15}$ → Pixel 31	
VddCompGrad$_{2,0}$ → Pixel 32	VddCompGrad$_{2,1}$ → Pixel 33	…	VddCompGrad$_{2,15}$ → Pixel 47	
VddCompGrad$_{3,0}$ → Pixel 48	VddCompGrad$_{3,1}$ → Pixel 49	…	VddCompGrad$_{3,15}$ → Pixel 63	
VddCompGrad$_{0,0}$ → Pixel 64	VddCompGrad$_{0,1}$ → Pixel 65	…	VddCompGrad$_{0,15}$ → Pixel 79	
.				
.				
.				
VddCompGrad$_{3,0}$ → Pixel 112	VddCompGrad$_{3,1}$ → Pixel 113	…	VddCompGrad$_{3,15}$ → Pixel 127	
VddCompGrad$_{4,0}$ → Pixel 240	VddCompGrad$_{4,1}$ → Pixel 241	…	VddCompGrad$_{4,15}$ → Pixel 255	bottom half
VddCompGrad$_{5,0}$ → Pixel 224	VddCompGrad$_{5,1}$ → Pixel 225	…	VddCompGrad$_{5,15}$ → Pixel 239	
VddCompGrad$_{6,0}$ → Pixel 208	VddCompGrad$_{6,1}$ → Pixel 209	…	VddCompGrad$_{6,15}$ → Pixel 223	
VddCompGrad$_{7,0}$ → Pixel 192	VddCompGrad$_{7,1}$ → Pixel 193	…	VddCompGrad$_{7,15}$ → Pixel 207	
VddCompGrad$_{4,0}$ → Pixel 176	VddCompGrad$_{4,1}$ → Pixel 177	…	VddCompGrad$_{4,15}$ → Pixel 191	
.				
.				
.				
VddCompGrad$_{7,0}$ → Pixel 128	VddCompGrad$_{7,1}$ → Pixel 129	…	VddCompGrad$_{7,15}$ → Pixel 143	

Figure 21: Readout of VDDCompGrad 16x16d

9.1 Ambient Temperature:

The ambient temperature (Ta) is calculated from the average measured PTAT value, the $PTAT_{gradient}$ and the $PTAT_{offset}$.

$$Ta = PTAT_{av} \cdot PTAT_{gradient} + PTAT_{offset}$$

(Value is given back in dK)

Where:

$PTAT_{gradient}$	is the gradient of the PTAT stored in the EEPROM as a float value
$PTAT_{offset}$	is the offset of the PTAT stored in the EEPROM as a float value
$PTAT_{av} = \frac{\sum_{i=0}^{3} PTAT_i}{4}$	is the average measured PTAT value

9.2 Thermal Offset:

The thermal offset of the sensor needs to be substracted for each pixel to compensate for any thermal drifts.

$$V_{ij\_Comp} = V_{ij} - \frac{ThGrad_{ij} \cdot PTAT_{av}}{2^{gradScale}} - ThOffset_{ij}$$

Where:

ij	represents the row (i) and column (j) of the pixel
V_{ij_Comp}	is the thermal offset compensated voltage

V_{ij}	is the raw pixel data (digital), readout from the RAM
$ThGrad_{ij}$	is the thermal gradient, stored in the EEPROM from 0x100 to 0x1FF
$ThOffset_{ij}$	is the thermal offset, stored in the EEPROM from 0x200 to 0x2FF
$gradScale$	is the scaling coefficient for the thermal gradient stored in the EEPROM

9.3 Electrical Offset

The electrical offset is used to compensate changes in the supply voltage. This compensation is only a subtraction, so it can be done before or after the thermal offset compensation (here done afterwards).
The compensation for the top half is done by using the following formula:

$$V_{ij\_Comp}* = V_{ij\_Comp} - elOffset[(j + i \cdot 16)\%64]$$

and the bottom half analogue with this formula:

$$V_{ij\_Comp}* = V_{ij\_Comp} - elOffset[(j + i \cdot 16)\%64 + 64]$$

where:

ij	represents the row (i) and column (j) of the pixel and electrical offset
$V_{ij\_Comp}*$	is the thermal and electrical offset compensated voltage
V_{ij_Comp}	is the thermal offset compensated voltage
$elOffset[ij]$	is the electrical offset belonging to Pixel ij
$i\%128$	is the rest of the integer division of i by 128 (e.g. 130:128=2) ("modulo")

Please see chapter 5 for the serial order.

9.4 Vdd Compensation

A supply voltage compensation called VddComp is used to take care of supply voltage changes. In order to use this compensation the supply voltage of the sensor (Vdd) has to be measured by the sensor from time to time by setting the configuration register and the average of Vdd 1 and Vdd 2 is resulting in Vdd (similar like $PTAT_{av}$).
The compensation for the top half is done by using the following formula:

$$VDD_{av} = \frac{\sum_{i=0}^{3} VDD_i}{4}$$

$$V_{ij\_VDDComp} = V_{ij\_Comp}* - \frac{\left(\frac{VddCompGrad[(j + i \cdot 16)\%64] \cdot PTAT_{av}}{2^{VddScGrad}} + VddCompOff[(j + i \cdot 16)\%64]\right)}{2^{VddScOff}} \cdot \left(VDD_{av} - VDD_{TH1} - \left(\frac{VDD_{TH2} - VDD_{TH1}}{PTAT_{TH2} - PTAT_{TH1}}\right) \cdot (PTAT_{av} - PTAT_{TH1})\right)$$

And the bottom half analogue with this formula:

$$V_{ij\_VDDComp} = V_{ij\_Comp}* - \frac{\left(\frac{VddCompGrad[(j+i\cdot 16)\%64+128]\cdot PTAT_{av}}{2^{VddScGrad}} + VddCompOff[(j+i\cdot 16)\%64+64]\right)}{2^{VddScOff}} \cdot \left(VDD_{av} - VDD_{TH1} - \left(\frac{VDD_{TH2}-VDD_{TH1}}{PTAT_{TH2}-PTAT_{TH1}}\right)\cdot (PTAT_{av} - PTAT_{TH1})\right)$$

Where:

ij	represents the row (i) and column (j) of the pixel
$V_{ij\_VDDComp}$	is the Vdd compensated voltage
$V_{ij\_Comp}*$	is the thermal and electrical offset compensated voltage
$VddCompGrad[ij]$	is the VddComp gradient belonging to Pixel ij
$VddCompOff[ij]$	is the VddComp offset belonging to Pixel ij
$i\%128$	is the rest of the integer division of i by 128 (e.g. 130:128=2) (“modulo”)
VDD_{av}	is the average measured supply voltage of the sensor in Digits
$VddScGrad$	is a scaling coefficient and stored in the EEPROM 0x3E
$VddScOff$	is a scaling coefficient and stored in the EEPROM 0x3F
VDD_{TH1}	is the supply voltage during calibration point 1 stored in the EEPROM 0x25
VDD_{TH2}	is the supply voltage during calibration point 2 stored in the EEPROM 0x26
$PTAT_{TH1}$	is the PTAT value of calibration point 1 stored in the EEPROM 0x2C
$PTAT_{TH2}$	is the PTAT value of calibration point 2 stored in the EEPROM 0x2D

9.5 Object Temperature:

The calculation of the object temperature is done by using a look-up table and doing a bi-linear interpolation, the matching table is given by the tablenumber (TN). The table is supplied in a separate file named “Table.c”. If you do not have the file, please ask Heimann Sensor for support.

The sensitivity coefficients ($PixC_{ij}$) are calculated in the following way:

$$PixC_{ij} = \left(\frac{P_{ij}\cdot(PixC_{\max} - PixC_{\min})}{65535} + PixC_{\min}\right)\cdot\frac{epsilon}{100}\cdot\frac{GlobalGain}{10000}$$

Where:

$PixC_{ij}$	is the sensitivity coefficient for each pixel
P_{ij}	is the stored sensitivity coefficient scaled to 16 bit
$PixC_{\min}$	is the minimum sensitivity coefficient, used for scaling
$PixC_{\max}$	is the maximum sensitivity coefficient, used for scaling
$epsilon$	is the emissivity factor
$GlobalGain$	is a factor for fine tuning of the sensitivity for all Pixel

Leading to a compensation of the pixel voltage

$$V_{ij\_PixC} = \frac{V_{ij\_VDDComp} \cdot \mathrm{PCSCALEVAL}}{PixC_{ij}}$$

Where:

V_{ij_PixC}	is the sensitivity compensated IR voltage
PCSCALEVAL	is a defined scaling coefficient, typically set to $1 \cdot 10^8$

HEIMANN Sensor GmbH
Maria-Reiche-Str. 1
D-01109 Dresden / Germany

Contact / Customer Support
Phone 49 (0) 6123 60 50 30
Fax 49 (0) 6123 60 50 39

Internet
www.heimannsensor.com
mail: info@heimannsensor.com

9.6 Example calculation:

Example values:

$$PTAT_{av} = \frac{\sum_{i=0}^{3} PTAT_i}{4} = 38152\ Digits$$

$$PTAT_{gradient} = 0.0211\ dK / Digit$$

$$PTAT_{offset} = 2195.0\ dK$$

$$V_{00} = 34435\ Digits$$

$$elOffset[0] = 34240$$

$$gradScale = 24$$

$$ThGrad_{00} = 11137 \xrightarrow[sign\,check]{} 11137$$

$$ThOffset_{00} = 65506 \xrightarrow[sign\,check]{} -30$$

$$VDD_{av} = 35000$$

$$VDD_{TH1} = 33942$$

$$VDD_{TH2} = 36942$$

$$PTAT_{TH1} = 30000$$

$$PTAT_{TH2} = 42000$$

$$VddCalib = 33942$$

$$VddCompGrad[0] = 10356 \xrightarrow[sign\,check]{} 10356$$

$$VddCompOff[0] = 51390 \xrightarrow[sign\,check]{} -14146$$

$$VddScGrad = 16$$

$$VddScOff = 23$$

$$PixC_{00} = 1.087 \cdot 10^8$$

$$\mathrm{PCSCALEVAL} = 1 \cdot 10^8$$

Compensation of electrical offset:

$$V_{00\_Comp}* = V_{00\_Comp} - elOffset[0] = 34439 - 34240 = 199$$

Compensation of supply voltage:

$$V_{ij\_VDDComp} = V_{ij\_Comp}* - \frac{\left(\frac{VddCompGrad[0] \cdot PTAT_{av}}{2^{VddScGrad}} + VddCompOff[0]\right)}{2^{VddScOff}} \cdot \left(VDD_{av} - VDD_{TH1} - \left(\frac{VDD_{TH2} - VDD_{TH1}}{PTAT_{TH2} - PTAT_{TH1}}\right) \cdot (PTAT_{av} - PTAT_{TH1}) \right)$$

$$= 199 - \frac{\left(\frac{10356 \cdot 38152}{2^{16}} - 14146\right) \cdot (35000 - 33942 - 2038)}{2^{23}} = 199 - (1) = 198$$

Table 20: Example look-up table

TA[dK]/dig	2882	3032	3182	3332
-64	1494	2128	2491	2775
-32	2466	2692	2898	3091
0	2882	3032	3182	3332
32	3170	3285	3406	3530
64	3396	3491	3592	3699
96	3584	3665	3754	3848
128	3746	3818	3897	3981
160	3890	3954	4025	4102
192	4019	4078	4143	4214
224	4137	4191	4251	4317
256	4246	4296	4351	4413
288	4347	4393	4445	4503
320	4441	4485	4534	4588

$$V_{00\_PixC} = \frac{198 \cdot 1 \cdot 10^8}{1.087 \cdot 10^8} = 182$$

Ta was calculated before to 3000 dK.
The matching region in the look-up table is already marked yellow, the bi-linear interpolation is leading to an object temperature of 3941 dK = 120.9 °C.
A global Offset (GlobalOff) is used for fine tuning of the measured object temperature and has to be added to the object temperature. This value is stored in the EEPROM.

HEIMANN Sensor GmbH
Maria-Reiche-Str. 1
D-01109 Dresden / Germany

Contact / Customer Support
Phone 49 (0) 6123 60 50 30
Fax 49 (0) 6123 60 50 39

Internet
www.heimannsensor.com
mail: info@heimannsensor.com

HTPA16x16dR1L2.1/0.8F5.0HiC[Si]

Thermopile Array With Lens Optics

Rev.1: 2017.10.16 Lupp/Schnorr

Look-up Table

The matching look-up table has to be taken from the Table.c file. Here is just shown an exemplary data for one optics.

To in dK

dig \ Ta[dK]	2782	2882	2982	3082	3182	3282	3382
-512				1295	1742	2005	2202
-448				1848	2094	2284	2442
-384				2156	2340	2496	2634
-320				2381	2534	2671	2797
-256	2042	2244	2414	2562	2697	2822	2938
-192	2287	2445	2587	2717	2839	2954	3065
-128	2481	2612	2735	2852	2964	3073	3180
-64	2642	2755	2865	2972	3078	3182	3285
0	2782	2882	2982	3082	3182	3282	3382
64	2906	2996	3089	3183	3278	3375	3473
128	3019	3101	3187	3276	3368	3462	3558
192	3121	3197	3278	3363	3452	3544	3638
256	3216	3286	3363	3445	3531	3621	3715
320	3305	3370	3443	3522	3606	3695	3787
384	3387	3449	3519	3595	3677	3764	3856
448	3465	3524	3590	3664	3745	3831	3922
512	3539	3595	3659	3731	3810	3895	3986
576	3609	3662	3724	3794	3872	3957	4047
640	3676	3727	3787	3855	3932	4016	4106
704	3740	3788	3847	3914	3990	4073	4163
768	3802	3848	3904	3971	4046	4128	4218
832	3861	3905	3960	4025	4100	4182	4271
896	3918	3960	4014	4078	4152	4233	4322
960	3973	4014	4066	4129	4202	4284	4372
1024	4026	4065	4117	4179	4251	4332	4421
1088	4077	4115	4166	4227	4299	4380	4469
1152	4127	4164	4213	4274	4345	4426	4515
1216	4175	4211	4260	4320	4391	4471	4560
1280	4222	4257	4305	4364	4435	4515	4604
1344	4268	4302	4349	4408	4478	4558	4647
1408	4312	4345	4391	4450	4520	4600	4689
1472	4355	4388	4433	4491	4561	4641	4730
1536	4398	4429	4474	4532	4601	4681	4770
1600	4439	4470	4514	4571	4640	4720	4809
1664	4480	4509	4553	4610	4679	4758	4848
1728	4519	4548	4591	4648	4716	4796	4885
1792	4558	4586	4629	4685	4753	4833	4922
1856	4595	4623	4666	4721	4790	4869	4959
1920	4633	4660	4702	4757	4825	4905	4995
1984	4669	4696	4737	4792	4860	4940	5030
2048	4705	4731	4772	4826	4894	4974	5064
2112	4740	4765	4806	4860	4928	5008	5098
2176	4774	4799	4839	4894	4961	5041	5131
2240	4808	4832	4872	4926	4994	5074	5164
2304	4841	4865	4904	4958	5026	5106	5197
2368	4873	4897	4936	4990	5058	5137	5228
2432	4906	4929	4968	5021	5089	5169	5260
2496	4937	4960	4998	5052	5119	5199	5291
2560	4968	4991	5029	5082	5149	5230	5321
2624	4999	5021	5059	5112	5179	5259	5351
2688	5029	5050	5088	5141	5208	5289	5381
2752	5059	5080	5117	5170	5237	5318	5410
2816	5088	5109	5146	5199	5266	5346	5439
2880	5117	5137	5174	5227	5294	5375	5467
2944	5145	5165	5202	5255	5322	5402	5495
3008	5173	5193	5230	5282	5349	5430	5523
3072	5201	5220	5257	5309	5376	5457	5550
3136	5228	5247	5284	5336	5403	5484	5577
3200	5255	5274	5310	5362	5429	5510	5604
3264	5282	5300	5336	5388	5455	5537	5630
3328	5308	5326	5362	5414	5481	5563	5656
3392	5334	5352	5388	5439	5507	5588	5682
3456	5360	5377	5413	5465	5532	5613	5708
3520	5385	5403	5438	5489	5557	5638	5733
3584	5410	5427	5462	5514	5581	5663	5758
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4160	5623	5639	5673	5724	5792	5875	5971
4224	5646	5661	5695	5746	5814	5897	5994
4288	5668	5683	5717	5768	5836	5919	6016
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4416	5712	5727	5760	5811	5879	5963	6060
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13632	7757	7761	7791	7846	7925	8025	8145
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13888	7797	7801	7831	7886	7965	8066	8187
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14016	7817	7821	7851	7906	7985	8086	8207
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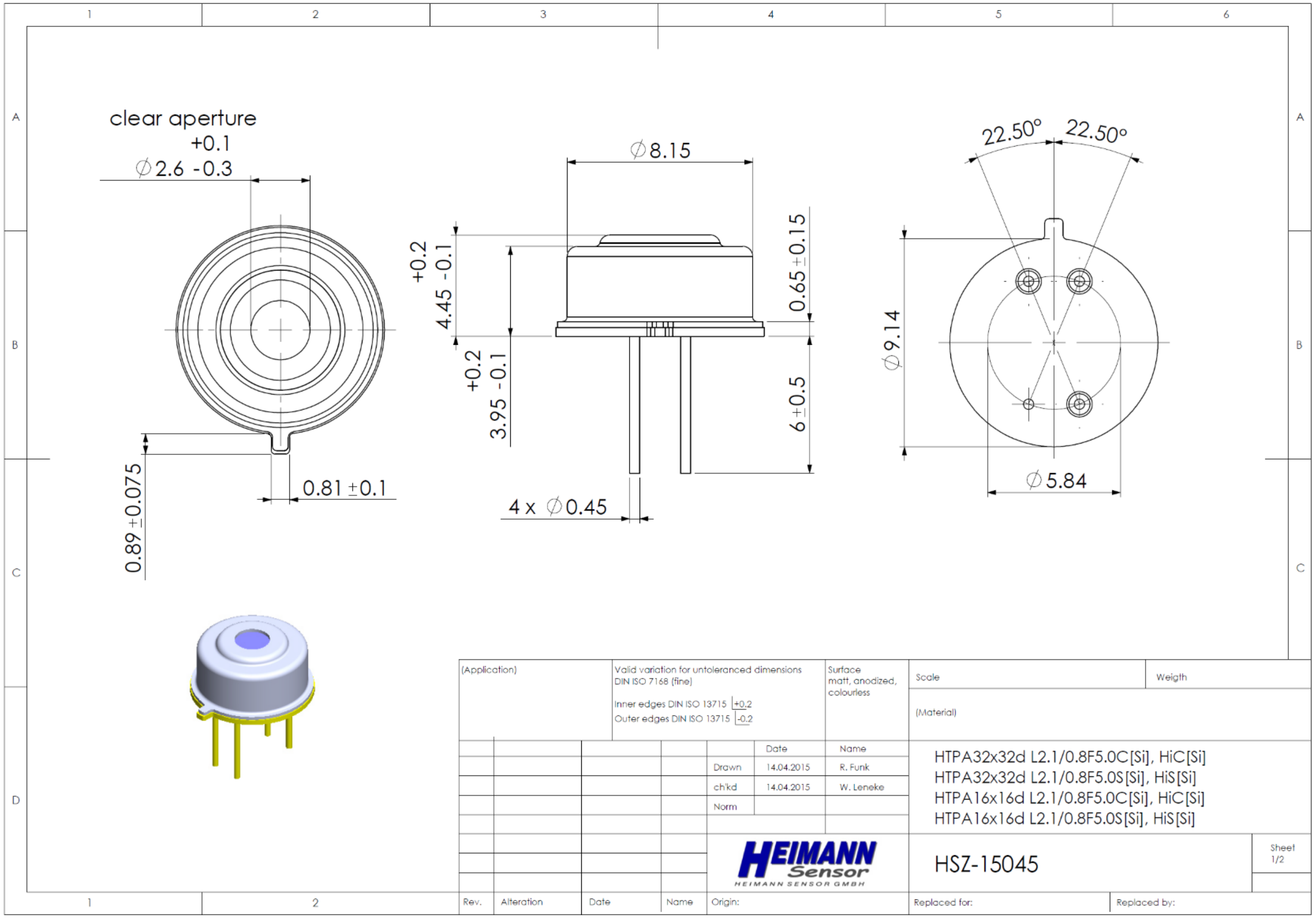
14144	7836	7841	7871	7926	8005	8106	8228
14208	7846	7851	7881	7936	8015	8116	8238

HEIMANN Sensor GmbH
Maria-Reiche-Str. 1
D-01109 Dresden / Germany

Contact / Customer Support
Phone 49 (0) 6123 60 50 30
Fax 49 (0) 6123 60 50 39

Internet
www.heimannsensor.com
mail: info@heimannsensor.com

10 Outer Dimensions:



HEIMANN Sensor GmbH
Maria-Reiche-Str. 1
D-01109 Dresden / Germany

Contact / Customer Support
Phone 49 (0) 6123 60 50 30
Fax 49 (0) 6123 60 50 39

Internet
www.heimannsensor.com
mail: info@heimannsensor.com