LAB. 4 - LED Light Control Circuit

【Purpose】

Design an LED light control circuit.

I. Understand the working principle of IC-CD4094.
II. Understand the serial transmission principle.
III. Design the control circuit of IC-CD4094.

【Experiment background】

Verilog design experience, state machine concept.

【Experimental Materials】

Please count the experimental materials carefully when borrowing and returning them.

I. FPGA Altera DE2-board
II. IC-CD4094BC x2
III. LED light x16
IV. 100 ohm resistor x1

Each group should bring their own solder sucker, soldering iron, and multimeter.

【Explain The Principle】

1. Principle of CD4094 Operation

CD4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel outputs. A combination of bit tristate gates is illustrated in Figure 1. Every positive edge trigger causes data to be serially inputted into the shift register (lower part of Figure 3). The output terminal of the final stage (Qs) can be used for cascading other devices. The Qs data is transmitted to another output terminal Q's upon a negative edge trigger, as depicted in Figure 2.

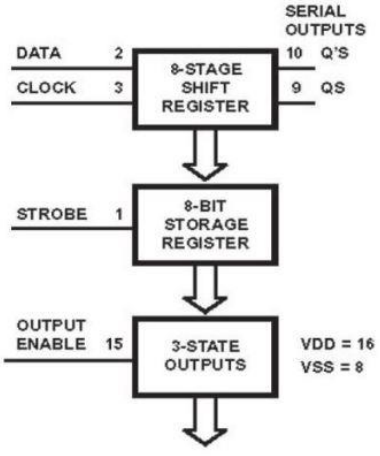


Figure 1. Schematic

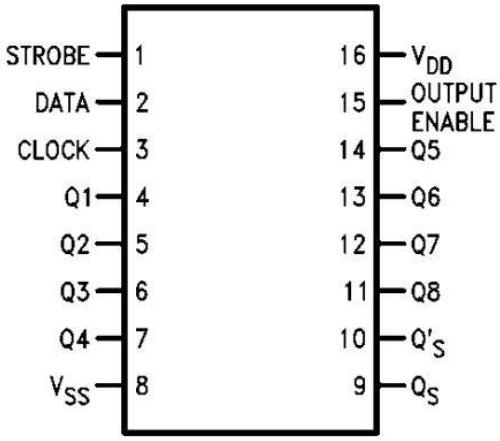


Figure 2. IC- CD4094BC Pinout

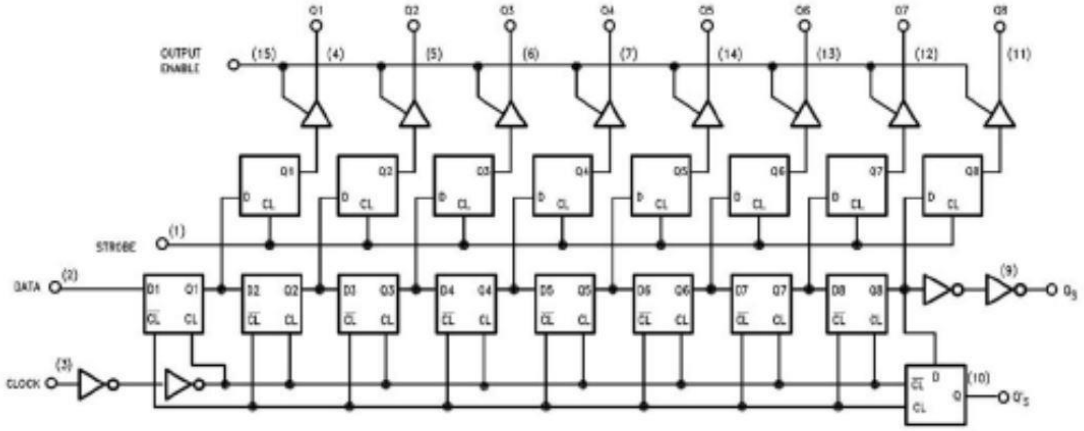


Figure 3. Schematic

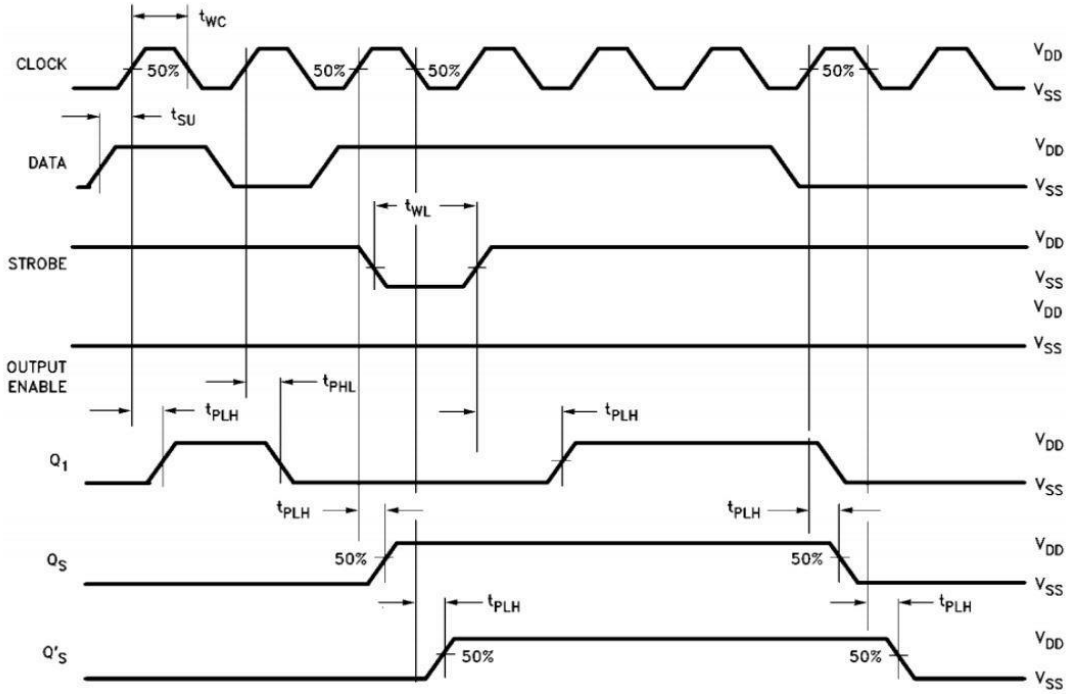
2. CD4094 Truth Table

Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q_N	Q_S (Note 1)	Q'_Σ
⌐	0	X	X	Hi-Z	Hi-Z	Q7	No Change
¬	0	X	X	Hi-Z	Hi-Z	No Change	Q7
⌐	1	0	X	No Change	No Change	Q7	No Change
⌐	1	1	0	0	Q_N–1	Q7	No Change
⌐	1	1	1	1	Q_N–1	Q7	No Change
¬	1	1	1	No Change	No Change	No Change	Q7

X = Don't Care
¬ = HIGH-to-LOW
⌐ = LOW-to-HIGH

Note 1: At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q_S.

3. Timing diagram



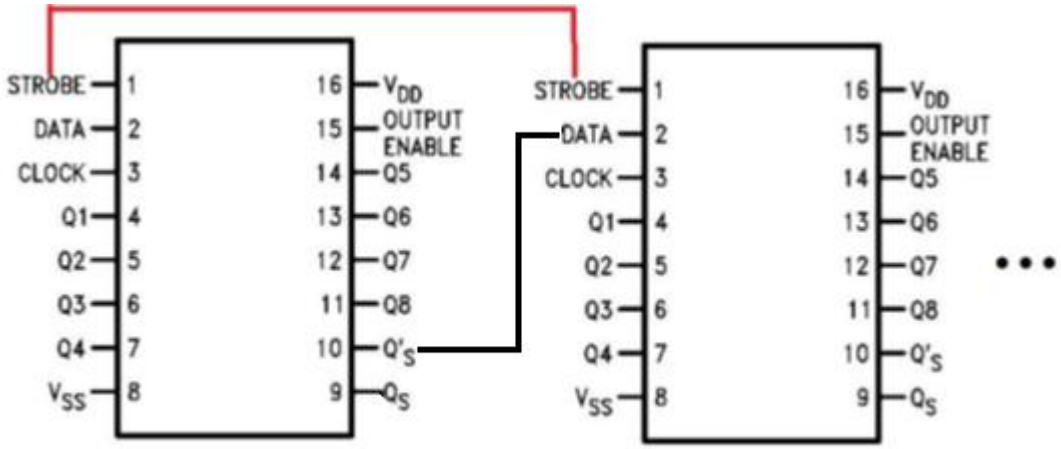
At each stage of the shift register, the output terminal corresponds to an individual storage element. When the input strobe transitions to 0, the storage element does not lock the data. When the strobe is set to 1, the storage element latches the data from input D and outputs it to the tristate buffer. When the output enable is set to 1, the tristate gates allow parallel data output.

4. Serial Transmission

The IC-4094 reads the value at the data input terminal (D) on the positive edge of the clock signal (CP) at its input terminal, and performs a shift operation, allowing for serial input data to be entered. Using the strobe signal (str), parallel data can be converted into serial output, thus enabling the conservation of a substantial number of transmission ports.

5. IC Controller Design

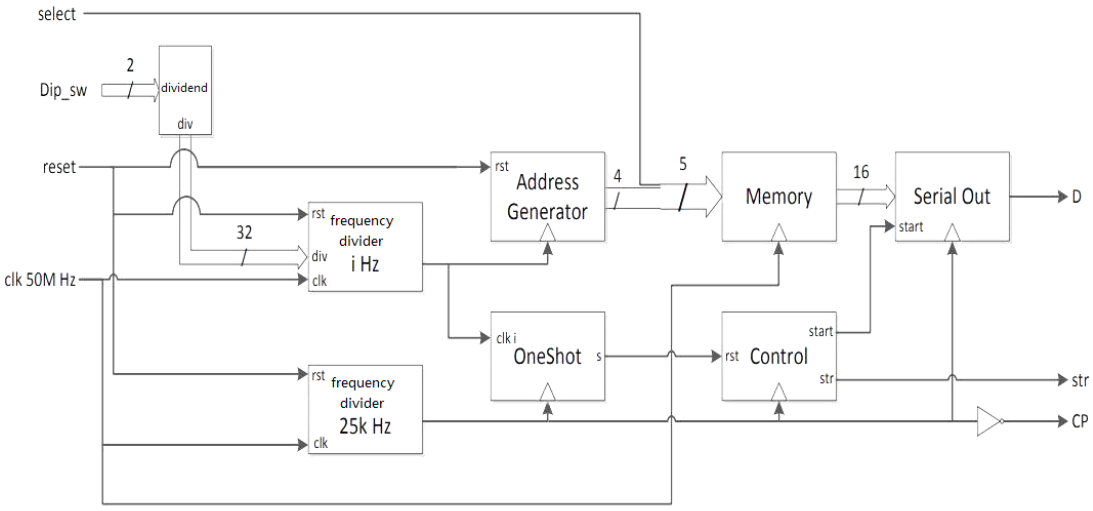
If the output terminal Qs of the previous stage is connected to the data input terminal (D) of the next stage and n IC-4094 chips are cascaded (where $n \geq 1$), it is possible to process serial input data of 8n bits. With a rapid clock (25kHz), the 8n bits of serialized values can be sequentially written, and at the 8*n-th clock cycle, the data at each stage can be locked into the storage registers. This allows the serialized output values to be formed and output at each stage



【Implementation】

Create an LED control circuit and utilize the cascade connection of two control circuits. By cascading two IC-4094 chips, achieve the control of 16 LEDs using a single data transmission port. This circuit enables the presentation of results wherein a user-defined 16-bit memory-stored value is sequentially displayed by the LEDs.

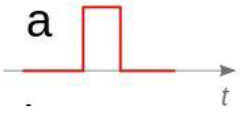
1. Schematic Diagram



2. Design Principles

According to the user's desired variation in timing difference (clki), utilizing the clock (CP) provided for the IC, serially output 16 values. To ensure that the IC captures the correct D, an inverted signal is applied to CP, delaying its positive edge update trigger by half a period compared to D's update trigger. After outputting 16 values, the "str" signal generates a pulse of one period length, causing data to pass through the storage registers and getting locked in place. This ensures that the data passes through the storage registers and becomes latched after the pulse is generated by "str".

Note: A pulse signal refers to a signal that briefly deviates from a reference value to a higher or lower level, and then rapidly returns to the reference value. For instance, the square wave pulse waveform depicted in the diagram on the right.



3. Architecture

Input Pins: clk_50MHz, Dip_sw[1:0], select, reset

- The Dip_sw can modify the speed of LED pattern switching.
- Sel_light can change the different lighting patterns of LEDs.

Output Pins: str, CP, D

- Control the latch enable, input clock, and data for each IC separately

Two Frequency Dividers:

1. Frequency Divider 50M/divHz(iHz): Converts the 50 MHz signal on the board into 2 Hz, 4 Hz, 6 Hz, and 8 Hz signals to control the speed of switching the stored patterns in memory.
2. Frequency Divider 25KHz: Converts the 50 MHz signal on the board into a 25 kHz signal for the IC's use in generating CP (Clock Pulse).

Address Generator：Generates the 4-bit address values required for memory. When the "rst" signal is raised, the address is reset to zero, allowing the memory to start outputting data from the beginning. (Hint: Utilize the concept of an asynchronous counter.)

Select: Switches the LED lighting pattern.

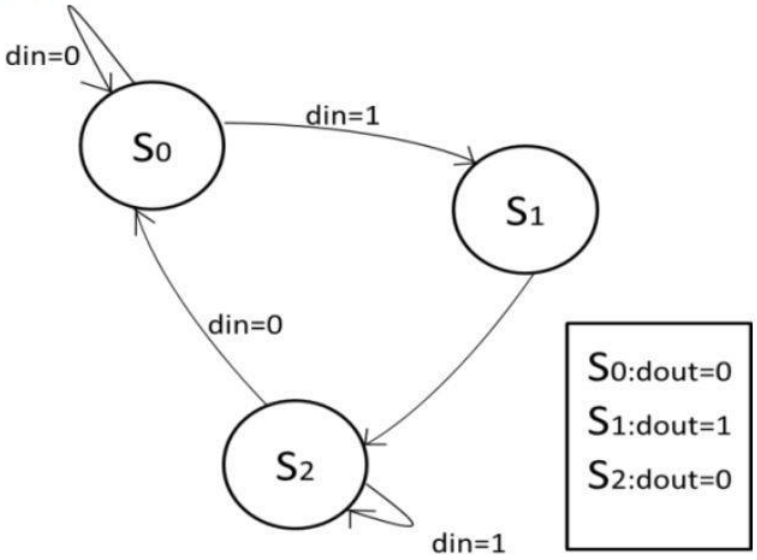
Memory: Megafunction-generated memory module (16 bits * 32 words) that stores two different LED patterns, as provided in the attached MIF file.

Serial Out: When "start" is set to 1, the input 16-bit value is stored in the register. After "start" becomes 0, on each positive edge of the clock, the highest bit of the register is sequentially sent out to D.

CP: Provides the clock signal to the IC. As Serial Out uses a positive-edge trigger, an inverter is applied to the IC's CLOCK (CP) signal to make it negative-edge triggered. This ensures that data is written to the IC when it's ready, synchronized with the negative edge trigger.

Oneshot: Designed using a state machine, it generates a pulse signal of length 1 clock cycle (25 kHz) after a longer input signal's positive edge trigger.

State for Reference



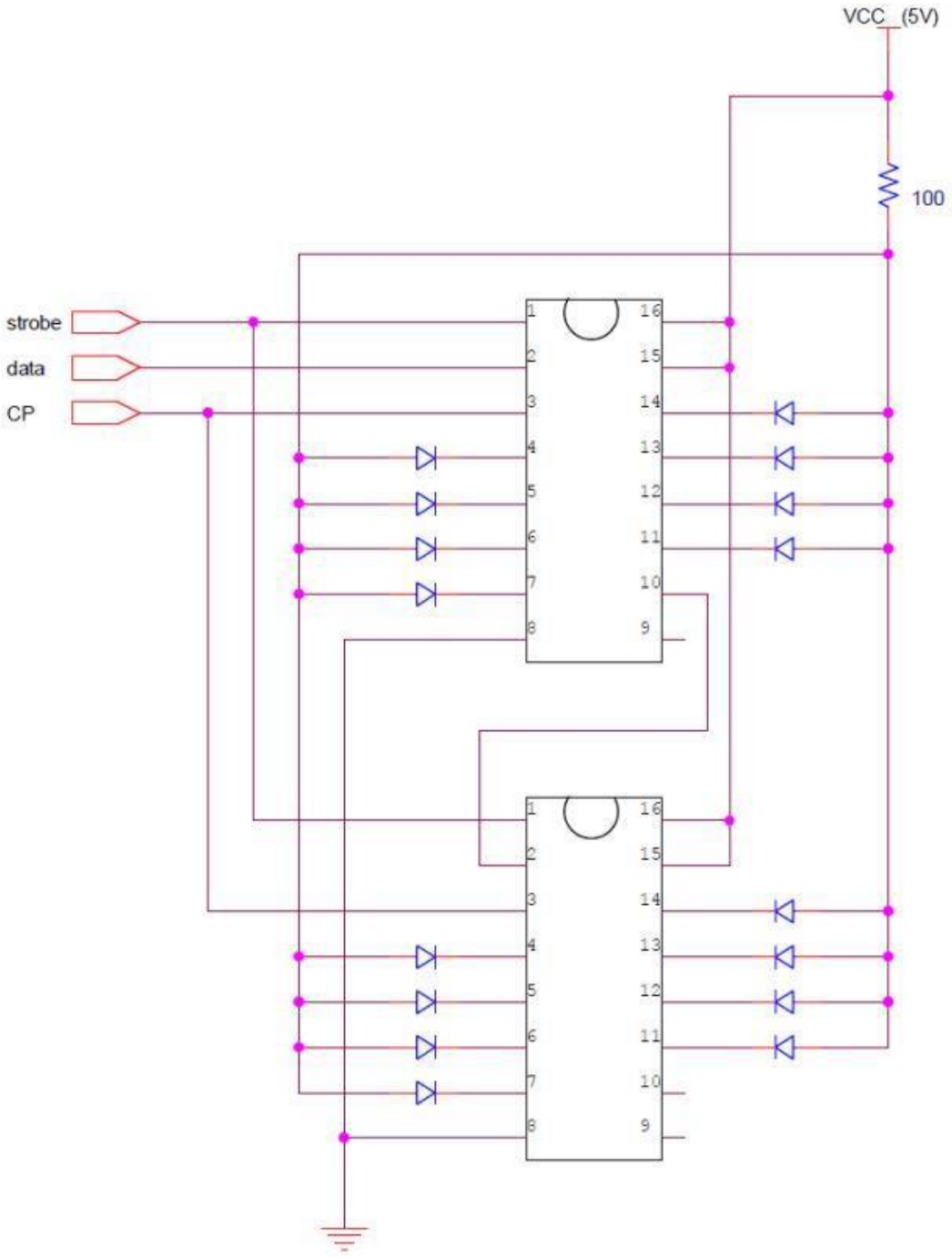
Control: Based on the OneShot output (s), generate two signals:

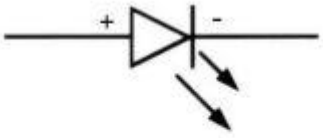
- **Serial out control signal "start"**
- **IC control signal "str"**

When "s" is raised, output a "start" signal of one clock cycle length. After the "start" signal ends, output a "str" signal of one clock cycle length on the 16th clock cycle.

(Hint: You can use a counter or state machine design.)

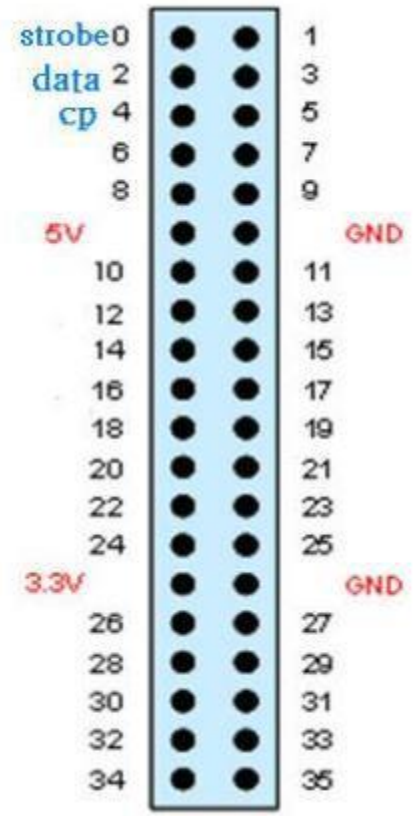
4. Circuit Diagram:





LED symbol

5. GPIO Pinout Diagram (GPIO 1):



Unified Output Pin:

DEII:	str: PIN_K25	D: PIN_M22	CP : PIN_M19
DE1-SOC:	str:PIN_AB17	D :PIN_AB21	CP:PIN_AD24

Additional Information: The VCC (5V) and ground connections of the circuit board are supplied by the FPGA board.

6. Implementation Content

1. Complete the module design based on the schematic diagram using the Verilog language.
2. Solder IC-CD4094 and LEDs onto the PCB board.
3. Implement the module using an FPGA and customize the content of the memory to create the LED marquee.
4. Explain the functionality and principles to the teaching assistant.

7. Bonus: Implement any creative or additional features.

For example:

1. Add a music box feature to synchronize flashing with the rhythm.
2. Incorporate an analog-to-digital circuit that adjusts the flashing speed based on a light-dependent resistor's input.

8. Experiment Report: The report should include

- Overall schematic diagram.
- Waveform simulations with annotations.
- Verilog code for each module with comments (excluding memory module).
- Introduction of creative features (if implemented).
- Reflections on the experiment.