ELECTRICAL ENGINEERING 5 －
Analog-to-Digital Converter Control Circuit

【Purpose】

Designing the control circuit for analog-to-digital converter.

i. Understand the Operating of IC-ADC0809.
ii. Design control circuit for ADC0809.
iii. Using a thermistor to experience the results of analog-to-digital conversion.

【Experiment Background】

Verilog design experience.

【Experiment Material】

FPGA Altera DE2-board	x1	OR	FPGA tarsic DE1-SOC	x1
IC-ADC0809	x1		Pin header	x14
10K thermistor	x1		2k, 10k, 150k, resistor	x1
0.1uF capacitor	x1		IC socket	x1
General-Purpose Printed Circuit Board	x1			

Each group should have your own solder sucker, soldering iron, and multimeter.

【Principle and Description】

1. Principle of IC-ADC0809

The ADC0809 is an 8-bit analog-to-digital conversion IC. It operates with an input range of 0V to 5V. The digital conversion value is represented by 8 bits. This IC is equipped with 8 analog input channels, which can be selected by providing a 3-bit input to specify the analog channel for conversion.

Figure 1 at next page shows the pinout diagram of the ADC0809. Table 1 provides the mapping between analog channel selection and addresses.

Here are the meanings of the pins:

Vcc/Gnd	：5v/0v		
VRef(+/-)	：5v/0v		
Input：		**Output** ：	
ALE	：Analog Enable	EOC	：End of Convert
Start	：Start Convert	$2^{-1} \sim 2^{-8}$	：Digital Output
IN0/IN1	：Analog Input		
Add A, B, C	：Switch Channel		
OE	：Output Enable		

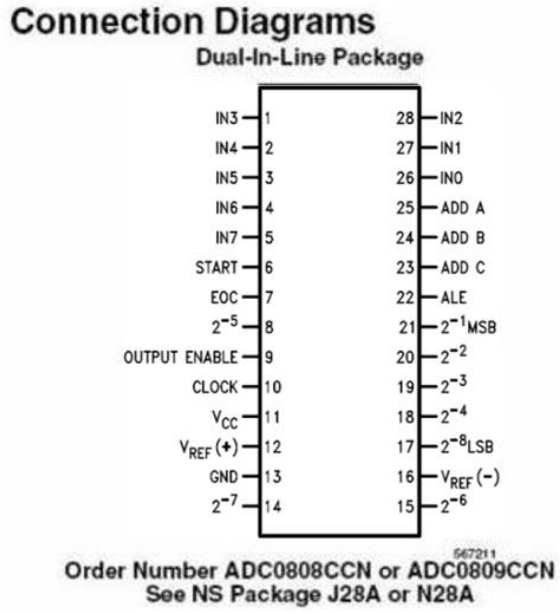


Figure 1.

TABLE 1. Analog Channel Selection

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

Table 1.

In the connection diagram, IN0~IN7 represent analog input channels. There are eight input channels. Selecting which input channel is like an 8-to-1 multiplexer, determined by 3 bits of address lines (ADD A, ADD B, ADD C). The conversion result is output on 2^{-1} (which means MSB) to 2^{-8} (which means LSB). These 8 pins' signals can be displayed by an FPGA and two seven-segment displays.

The conversion process of this IC is illustrated in the timing diagram shown in Figure 2.

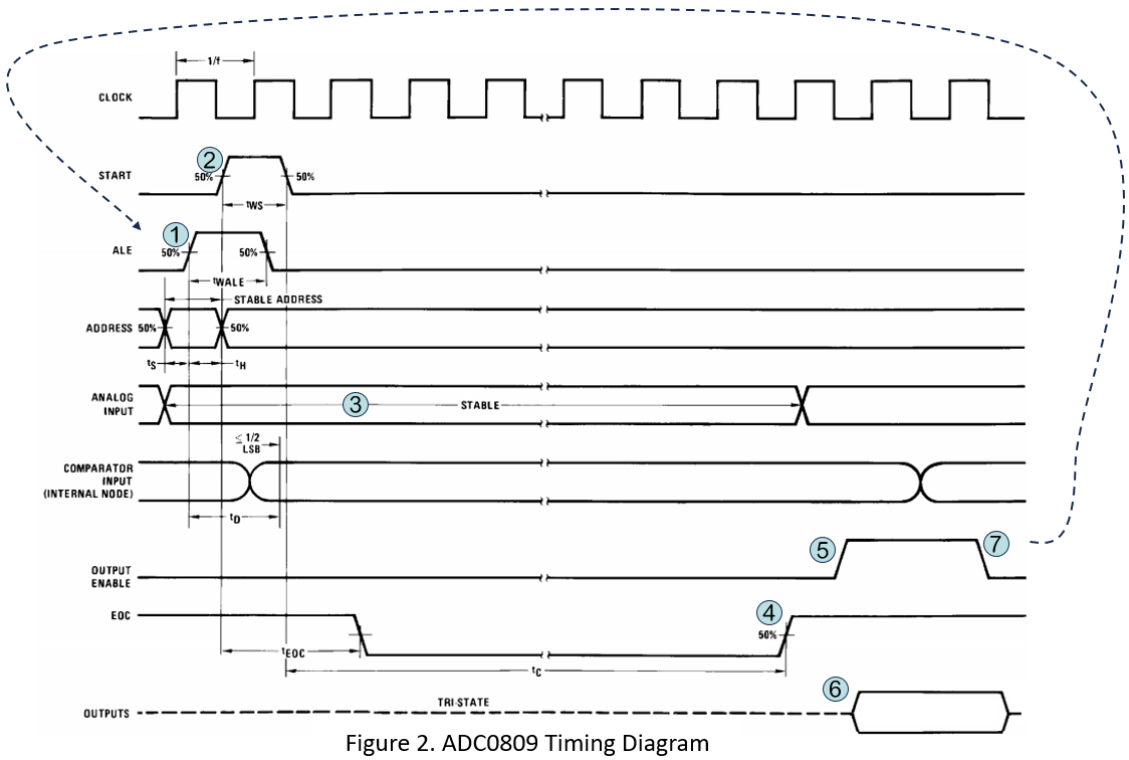


Figure 2. ADC0809 Timing Diagram

To use this IC for analog signal conversion, the process begins by setting the analog channel (Address) to be converted. Then, the ALE (Analog Enable) signal is sent to indicate that the analog signal is ready. Finally, the Start signal is sent to instruct the ADC0809 to convert the value of the selected analog channel.

Upon completion of the conversion, the ADC0809 sets EOC (End of Conversion) to 1. At this point, once the OE (Output Enable) is set to 1, the ADC0809 will release the converted digital value. The analog-to-digital conversion process is then complete.

Due to the nature of electronic characteristics, there are specific timing constraints between signals. These specifications are provided in Appendix 1 at the end of this handout.

2. Design of the ADC0809 Controller and Display Circuit

i. Operation of the AD Controller:

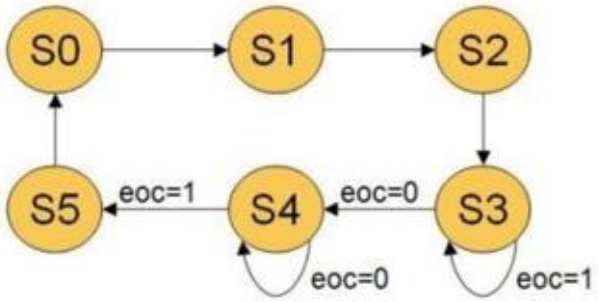
The AD controller is like a state machine, as shown in Figure 3. In the S0, the analog signal channel (Address) must be specified. In this experiment, only the cross-voltage value of the thermistor is being read. Therefore, pins 23, 24, and 25 of the ADC0809 are directly grounded (Address = 000), designating the analog input as IN0.

In S1, the ALE signal is set to 1. Following by S2 where the START signal is set to 1. Transitioning to S3, The EOC condition is checked. If it's 0, it signifies that the conversion has started and the controller proceeds to S4. The conversion process completes when EOC becomes 1.

We connect EOC and Output Enable, meaning that when EOC=1, requests for value retrieval can be issued during this period. At S5, a request for value retrieval (signal line is g_d) is send, then the system returns to S0.

ii. Read Data at Backend and Display the Data:

After the value retrieval request (g_d) is sent, the backends' Dff need to receive the value transmitted by the ADC0809. Once received, the cross-voltage value of the thermistor is displayed on the seven-segment display.

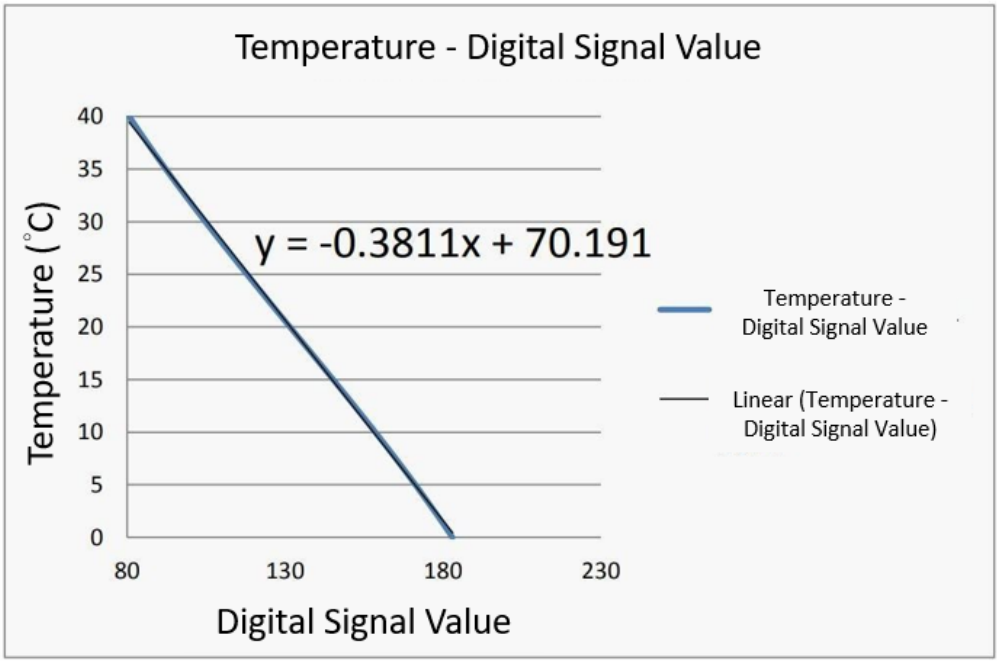


State	Output
S0	ale=0,start=0,g_d=0
S1	ale=1,start=0,g_d=0
S2	ale=0,start=1,g_d=0
S3	ale=0,start=0,g_d=0
S4	ale=0,start=0,g_d=0
S5	ale=0,start=0,g_d=1

Figure 3. AD Control State Diagram

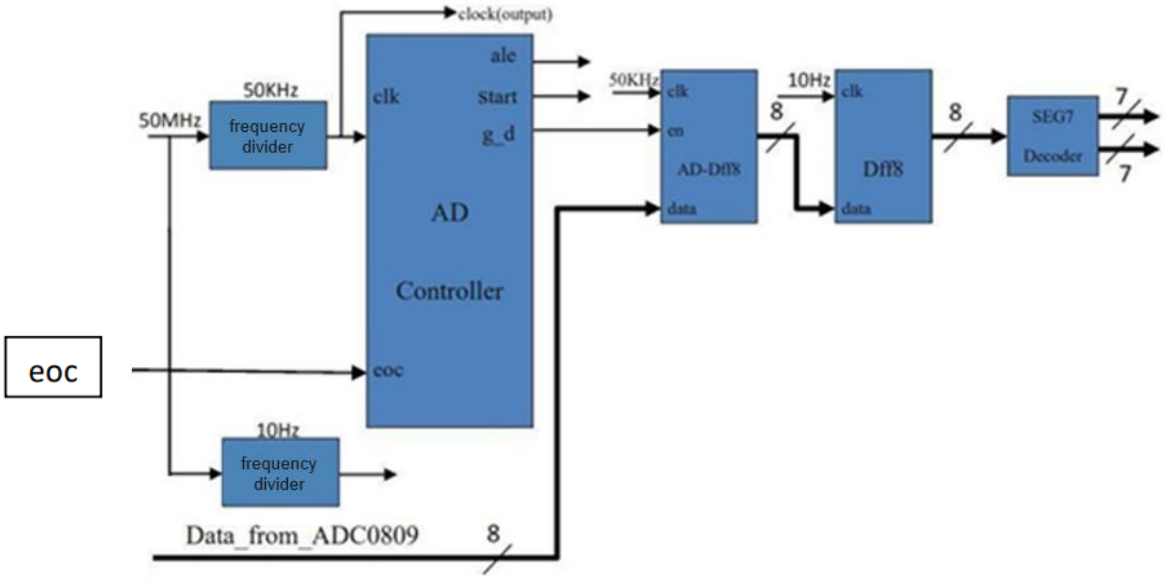
3. Circuit Design Principle of Thermistor

As temperature and the reciprocal of the thermistor's resistance are inversely proportional, so we connect thermistors in parallel. By doing this, the voltage divider values can approximate a linear relationship with temperature. This approximation allows deriving a linear conversion formula relating temperature to the voltage divider value.



Temp(℃)	Value	Temp(℃)	Value	Temp(℃)	Value
0	183	14	148	28	110
1	181	15	145	29	107
2	178	16	143	30	105
3	176	17	140	31	102
4	174	18	137	32	100
5	171	19	134	33	97
6	169	20	132	34	95
7	166	21	129	35	92
8	164	22	126	36	90
9	161	23	123	37	88
10	159	24	121	38	85
11	156	25	118	39	83
12	153	26	115	40	81
13	151	27	113		

【Implement】



1. Circuit Architecture Analysis

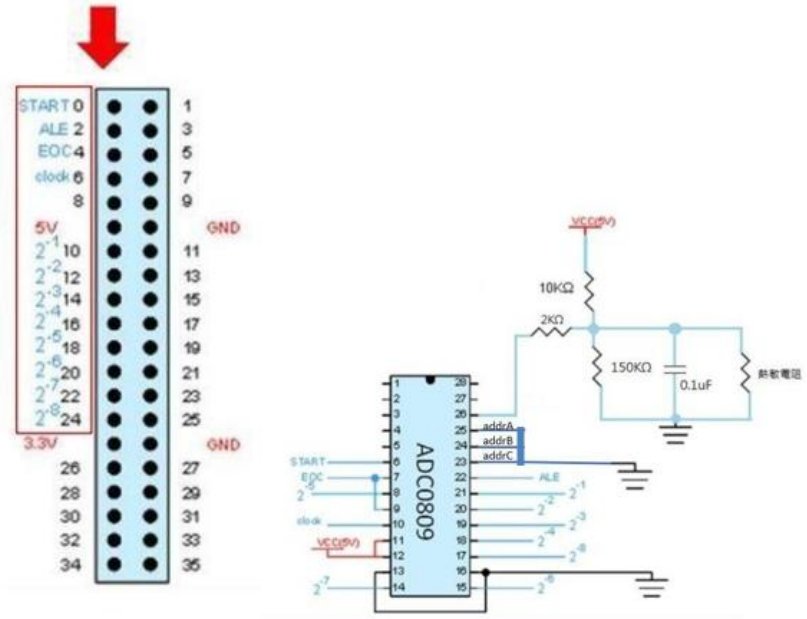
Design the ADC0809 Controller to generate control signals and data sampling signals for the ADC0809. Utilize the control signals to convert the analog signal from the thermistor into digital form through the ADC0809. The display circuit should use the sampling signal to decode the digital signal and display the digital value of the thermistor voltage divider on the seven-segment display on the board.

This configuration is illustrated in the diagram above, which includes:

- **i.** Input pin : clk_50MHz, eoc, Data_from_ADC0809[7:0].
- **ii.** Output pin : clk_50KHz, ale, start, 7-seg output.
- **iii.** Two frequency dividers :
  a. Change clk_50MHz from FPGA board to clk_50KHz(clock range for ADC0808 is from 10K to 1280K).
  b. Change clk_50MHz from FPGA board to 10Hz for seven-segment display output.
- **iv.** AD Controller :
  Control the conversion process of the ADC0809 and send sampling signals to the display circuit. (Refer to Principle 2).
- **v.** AD-Dff8 : Latch the data signal sent from the ADC0809
- **vi.** Dff8 : Latch the data from AD-Dff88

2. Pinout Diagram of the Circuit Board (GPIO 0)

The sequence for soldering pins is as follows:



Notice:

The sequence of soldering the male header pins in this experiment must match exactly with the direction indicated by the arrow in the diagram.

In-class implementation content:

i. Complete the module design based on the architecture diagram above and write the Verilog code for each module.

ii. Implement the design on the circuit board according to the pinout diagram.
Additional Information:

a. The 5V supply on the circuit board is provided by the FPGA development board.
b. Connect the ground of the FPGA with the ground of all components on the circuit board.
c. Display the hexadecimal value on the 7-segment display.

Bonus Points:

Implement any creative or additional functionalities. For example: Displaying the accurate temperature value.

Experiment Report:

The report should include Overall architecture diagram, waveform simulations of each module (explaining how functionality was verified), Verilog code for each module with comments (excluding memory module), creative ideas implemented (if applicable), and personal reflections on the experiment.

Electrical Characteristics – Timing Specifications

Timing Specifications $V_{CC}=V_{REF(+)}=5V$, $V_{REF(-)}=GND$, $t_r=t_f=20$ ns and $T_A=25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	(*Figure 5*)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	(*Figure 5*)		100	200	ns
t_s	Minimum Address Set-Up Time	(*Figure 5*)		25	50	ns
t_H	Minimum Address Hold Time	(*Figure 5*)		25	50	ns
t_D	Analog MUX Delay Time From ALE	$R_S=0\Omega$ (*Figure 5*)		1	2.5	µs
t_{H1}, t_{H0}	OE Control to Q Logic State	$C_L=50$ pF, $R_L=10k$ (*Figure 8*)		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	$C_L=1p$ pF, $R_L=10k$ (*Figure 8*)		125	250	ns
t_c	Conversion Time	$f_c=640$ kHz, (*Figure 5*) (Note 7)	90	100	116	µs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	(*Figure 5*)	0		8 + 2 µS	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs		10	15	pF

Appendix 1 : ADC0809 timing specifications