Analog Lab 3:

Experiment6:

Phase Lock Loop

Date: 2023/11/30

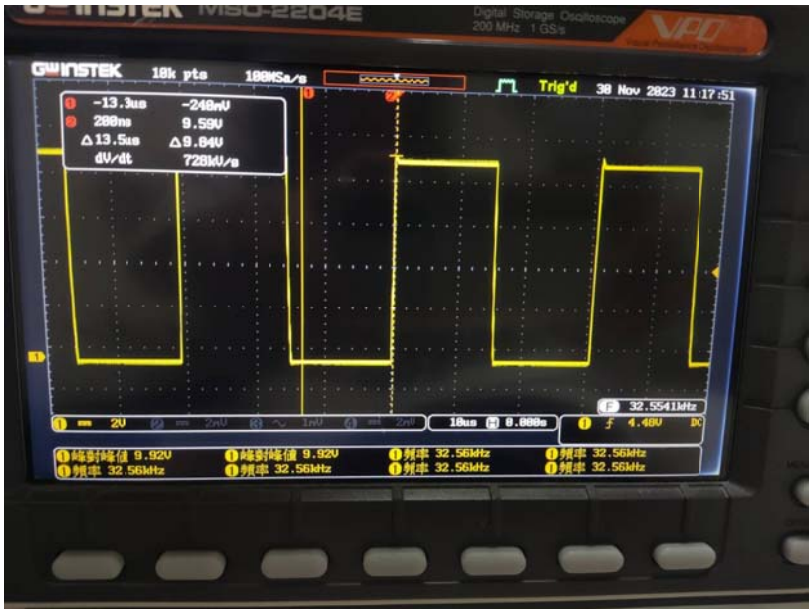
Class: 電機三全英班

Group: Group 11

Name: B103105006 胡庭翊

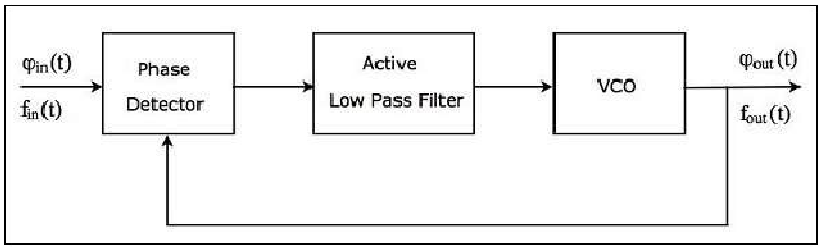
Working Project #1 Free Running Frequency

I. Measurement Data



The free running frequency $f_0 = 32.56Hz$

II. Observation and Discussion



PLL is consisted of a voltage controlled oscillator, phase detector, and a lowpass filter, and the bandwidth of the lowpass filter is decided by the C_7 of the 7^{th} pin.

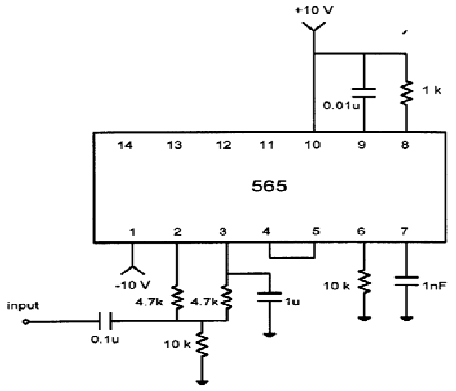


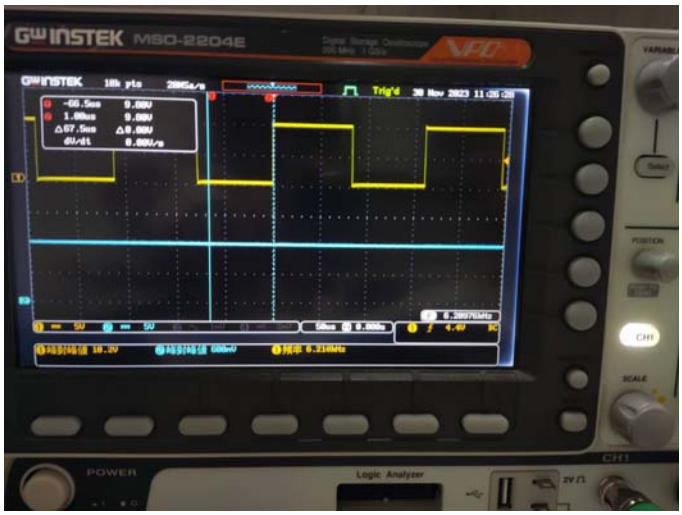
圖 4.2

We know that $f_0 \approx 0.3/R_8C_9$, when choosing $R_8 = 1k\Omega$, $C_9 = 0.01\mu F$, f_0

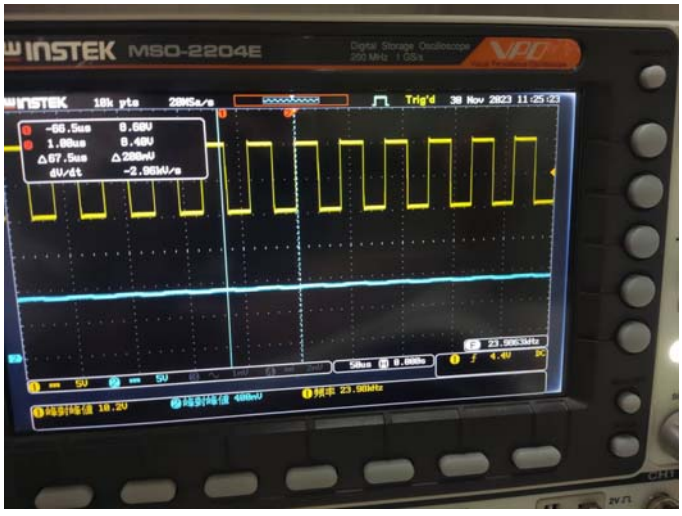
should be 30kHz in ideal. We connect the 4th pin to the oscillator and observe a square wave result, our measurement data is close to the ideal number.

Working Project #2 Characteristic of VCO

I. Measurement Data

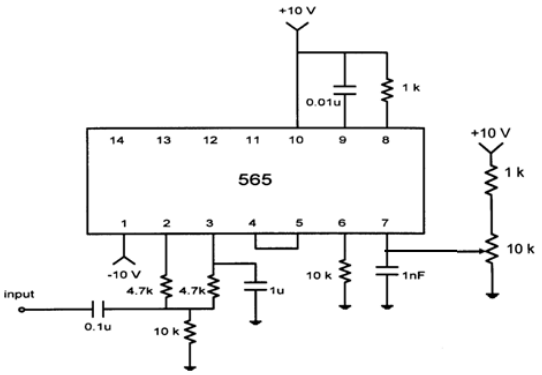


The VCO input voltage (pin7): 9.88V
The frequency output (pin4): 6.210 kHz



The VCO input voltage (pin7): 8.48V
The frequency output (pin4): 23.98 kHz

II. Observation and Discussion



Connecting a 10k changeable register to pin7, which is, the input pin of the voltage controlled oscillator, we can simply modify the input voltage to the VCO inside the IC.

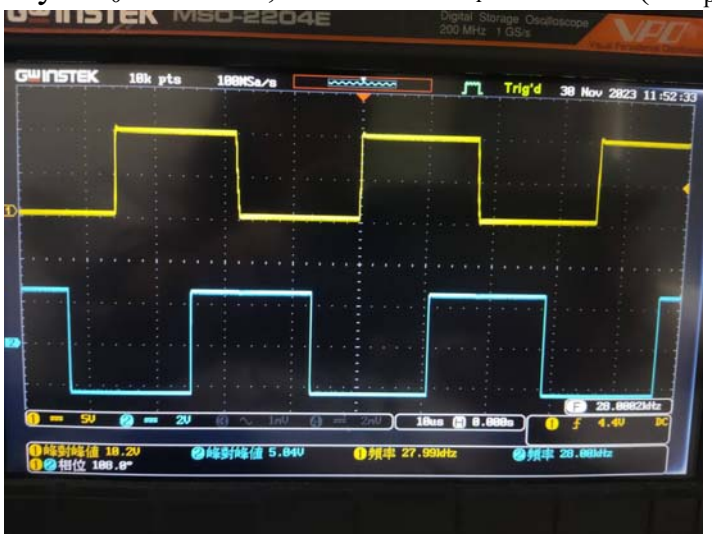
From the result, we can tell that when the changeable register converts, the output frequency f_0 will also change.

Working Project #3 Feed an Input to PLL

I. Measurement Result

Set the function generator to output a square wave to PLL input:

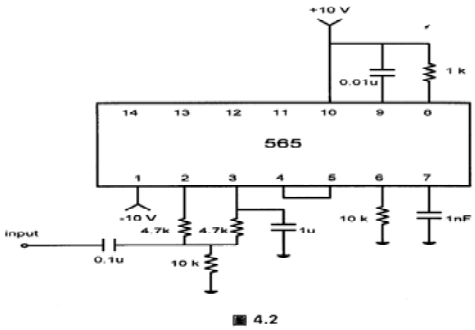
Say if $f_0 = 30$ kHz, here we set $f_i = 28$ kHz (5 $V_{p\text{-}p}$)



$f_o = f_i = 28.00$ kHz

The PLL can really lock the input signal.

II. Observation and Discussion



4.2

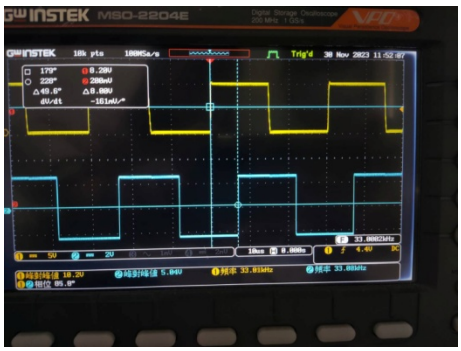
Before connecting the signal to the PLL input, we can found that it is impossible to observe f_0 and f_i in the same time since they have different frequency.

However, after connecting f_i to the input of the circuit, the PLL will lock the input signal, $f_0 = f_i$ at last.

Working Project #4 Observe the Phase Difference

I. Measurement Result

Set the function generator to output a square wave at measured frequency f_0. Apply it to PLL input:



Phase difference = 85.8°

II. Observation and Discussion

When phase locking f_i to f_0, the phase difference of the two signal = 90°, which is 1/4 of the period.

Working Project #5 Lock Range

I. Measurement Result

frequency	15k	16k	17k	18k	19k	20k	21k	22k	23k	24k
voltage	8.33	9.01	8.92	8.84	8.76	8.69	8.6	8.53	8.46	8.38
phase	X	178.9	170.2	165.1	159.2	154.5	146.1	141.4	136.4	131.0

frequency	25k	26k	27k	28k	29k	30k	31k	32k	33k	34k
voltage	8.30	8.23	8.16	8.08	8.0	7.93	7.85	7.78	7.72	7.68
phase	126.1	121.2	116.2	110.7	105.4	100.7	97.9	98.1	89.5	86.2

frequency	35k	36k	37k	38k	39k	40k	41k	42k	43k	44k
voltage	7.63	7.54	7.44	7.39	7.34	7.3	7.85	7.78	6.94	6.85
phase	83.4	77.2	70.1	68.2	63.8	54.0	44.2	39.4	33.1	28.9

frequency	45k	46k	47k	48k	49k
voltage	6.78	6.68	6.61	6.52	7.0
phase	23.3	15.9	11.9	6.2	X

II. Observation and Discussion

First we find the frequency where the phase difference of f_i and f_0 is 90➔at 33k Hz, the phase difference is 89.5°.

Then we find the frequency of the highest and lowest phase difference.

The range of the highest and lowest lock frequency is called the Lock Range. It is the biggest range of the frequency that a PLL can lock.

Working Project #6 Capture Range

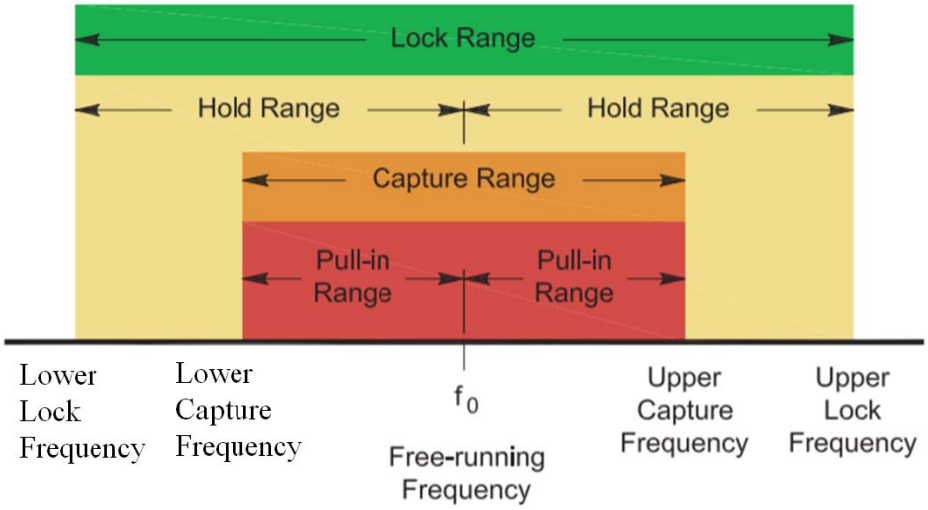
I. Measurement Result

Capacitance of C_7	1uF	10uF
f_o	34 kHz	35 kHz
Lock range	29 kHz ~ 39 kHz	34 kHz ~ 36 kHz
Capture range	32 kHz ~ 36 kHz	34 kHz ~ 36 kHz

II. Observation and Discussion

Capture range: the range of the input frequencies around the VCO center frequency in which the loop can lock the input when starting form unlocked condition.

Lock range: the range of input frequencies over which the loop can remain in the lock condition once it has captured the input signal.



Feedback

This communication experiment marked our inaugural foray into the realm of phase-locked loops (PLL). The lab focused on measuring Free Running Mode, Capture Range, and Lock Range, essential parameters in PLL analysis. As a culminating project for the semester, I found the hands-on implementation of PLL to be both challenging and insightful.

However, I must admit that documenting experimental data for each frequency felt somewhat laborious. Despite the meticulous nature of the task, the experience provided a practical understanding of the intricacies involved in working with phase-locked loops. Overall, the experiment served as a valuable introduction to communication systems and the practical application of PLL concepts.