PDSD

HW2
Synopsys Design Vision EDA Tool

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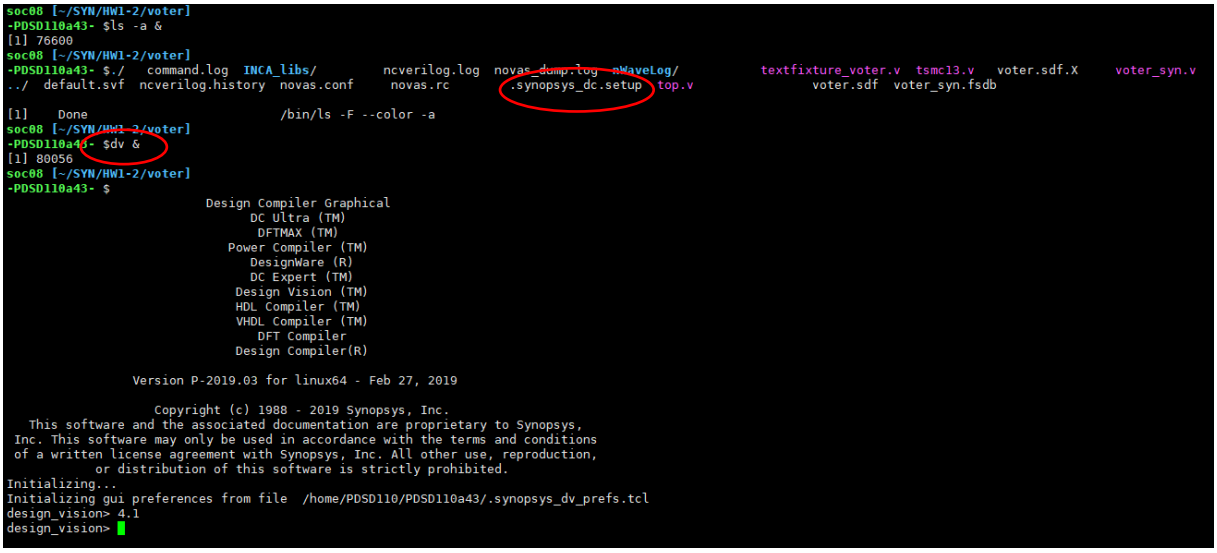
壹、合成流程

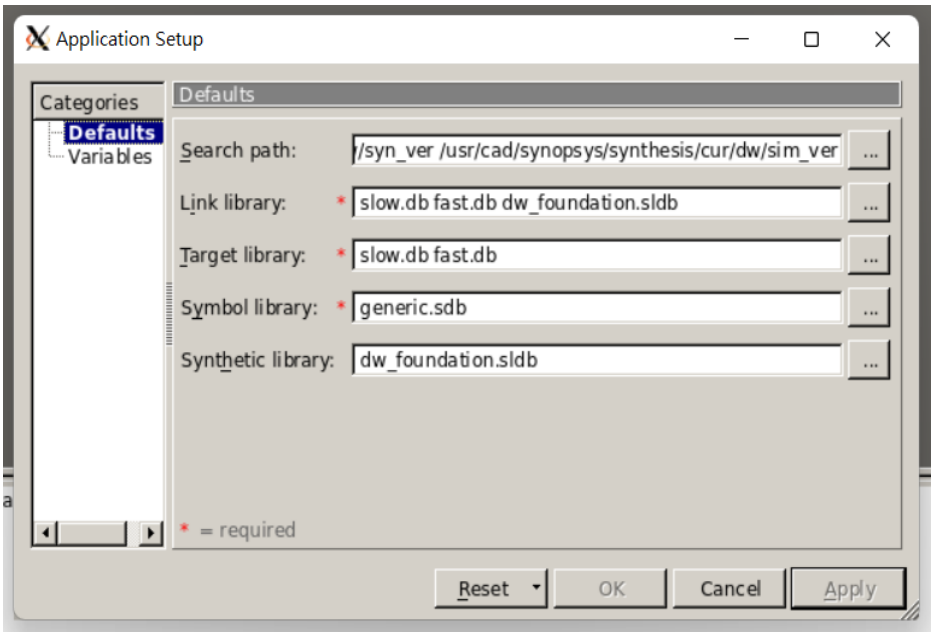
此次需進行邏輯合成的有 RCA、CLA、voter 及 median，而此報告的合成流程將以 voter 為例，其餘 Verilog code 的合成流程也與 voter 相同，若中途的設置有作調整的話，將額外進行解說。

一、啟動 Design Compiler

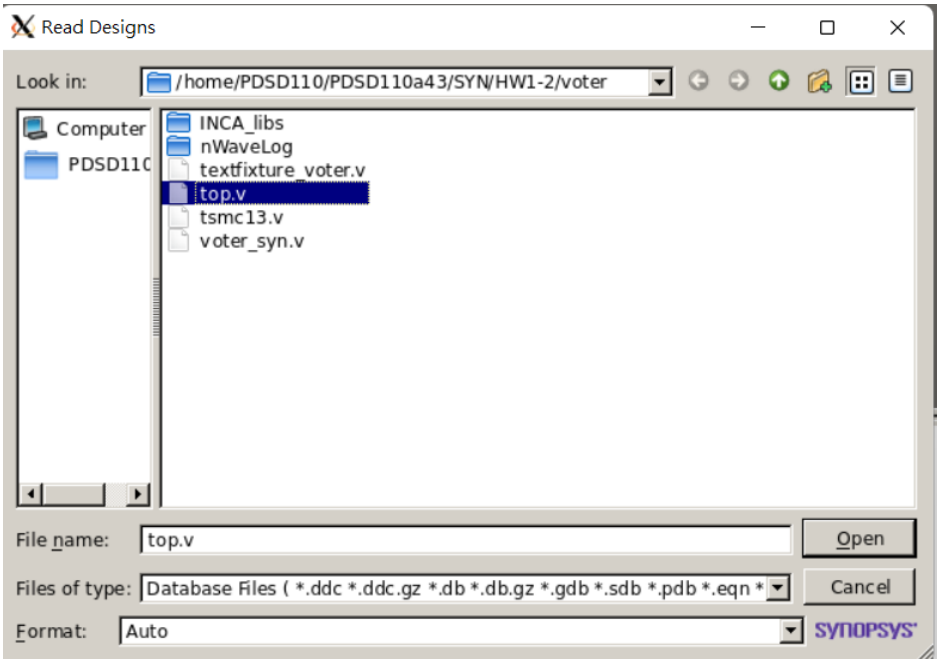


先在工作站中打開要邏輯合成的資料夾，並在資料夾中確認是否有 setup 檔，確認後輸入 dv 啟動 Design Vision。

二、確認 Library 是否載入

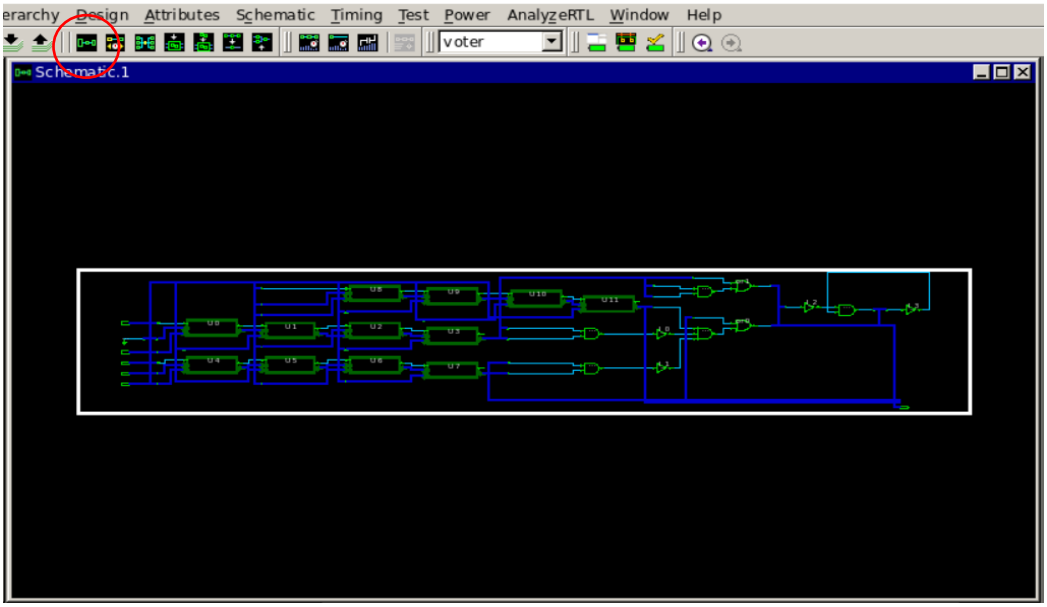


三、讀檔並確認是否有 error 或 warning 出現



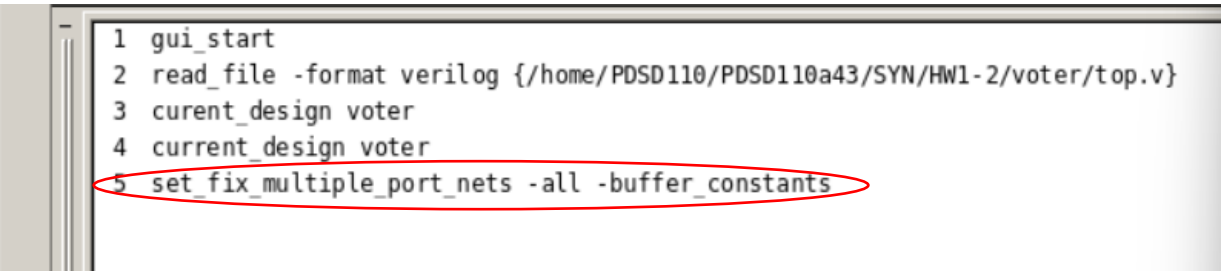
若讀檔正確且 Verilog code 沒有錯誤的話將會顯示上圖紅色圈內的提示且 Design Vision 會標示當前的 design module。

四、查看電路架構圖



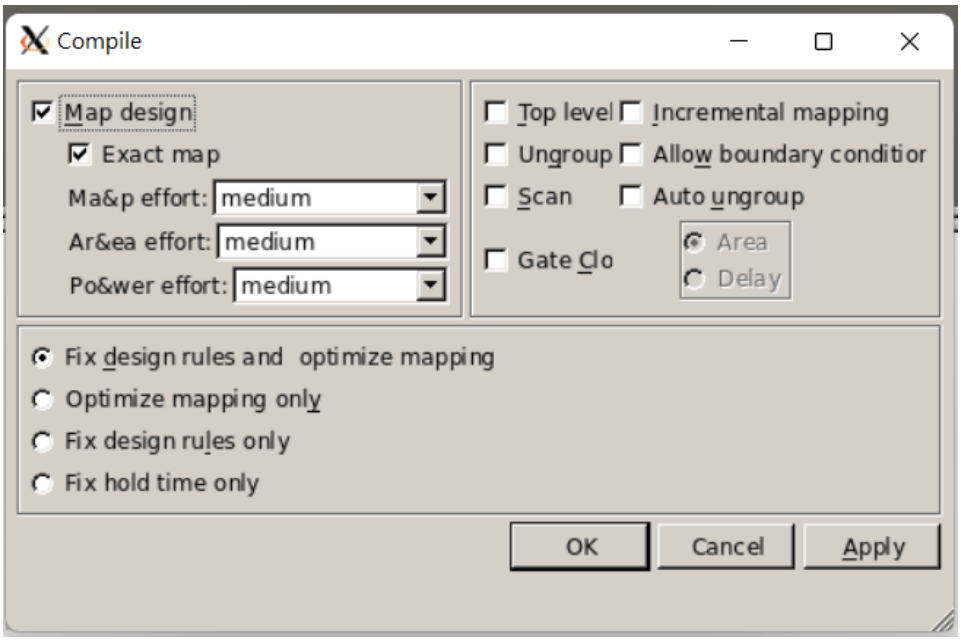
選擇 logic hierarchy 的 module 後，點一下上圖紅圈的圖示就可查看電路架構圖。

五、預防可能的 Assign Statement Problem

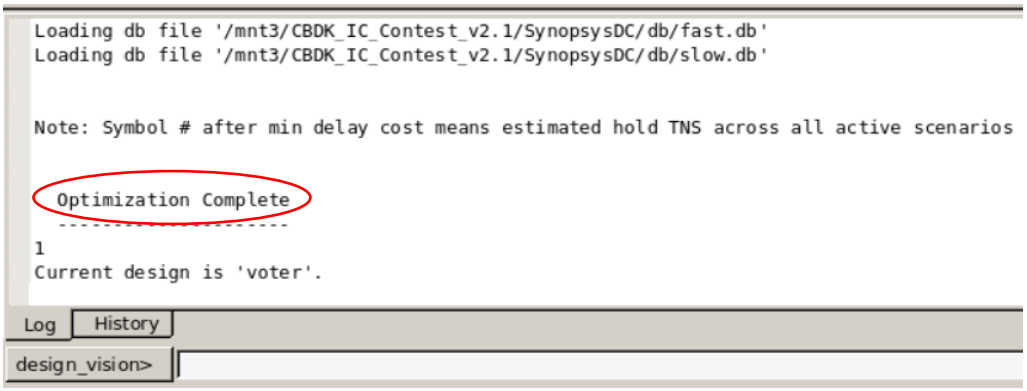


在 command line 輸入第五點的指令避免有 assign statement 的問題產生。

六、進行 Compile Design



選定好 module 後，在工具列上的 Design 點 Compile Design，而 Compile Design 的設置如上圖所示。

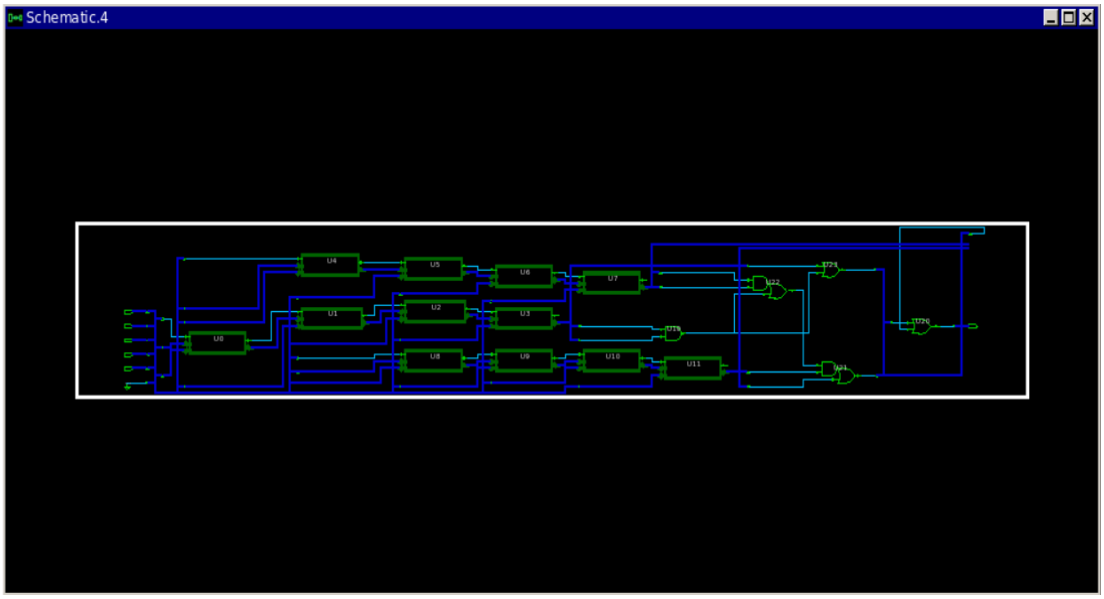


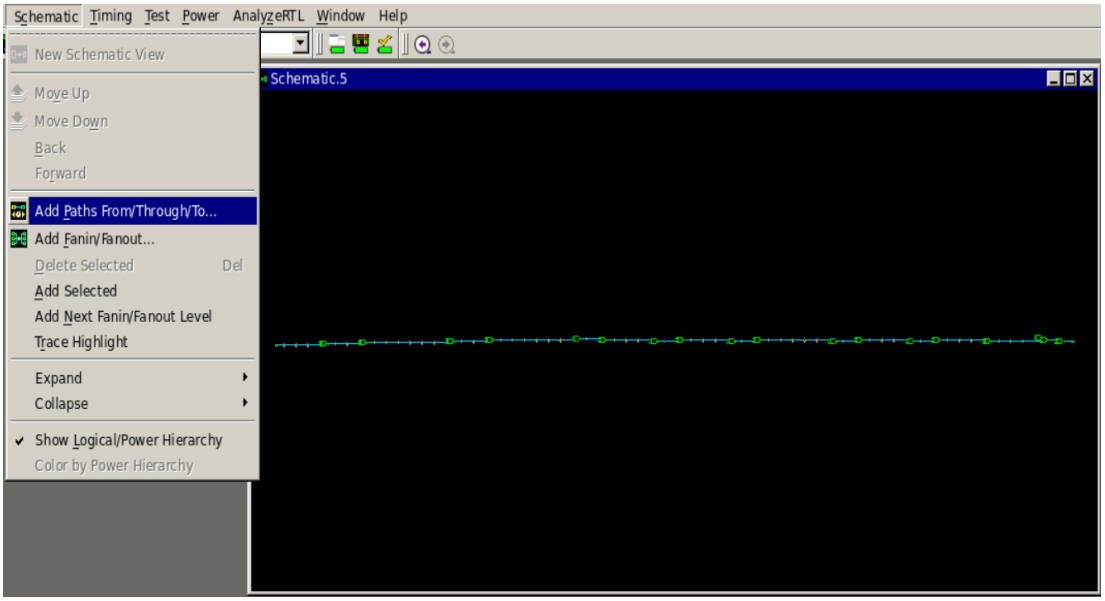
若 Compile Design 成功，則會出現上圖紅圈的提示。

```
1  gui_start
2  read_file -format verilog {/home/PDSD110/PDSD110a43/SYN/HW1-2/voter/top.v}
3  curent_design voter
4  current_design voter
5  set_fix_multiple_port_nets -all -buffer_constants
6  compile -exact_map
7  change_names -hierarchy -rule verilog
8  write -hierarchy -format verilog -output /home/PDSD110/PDSD110a43/SYN/HW1-2/voter/voter_syn.v
```

Compile Design 完成後輸入上圖第七點的指令來讓電路不會再出現 assign，接著將此檔案儲存成 syn 的.v 檔，如上圖第八點所示。

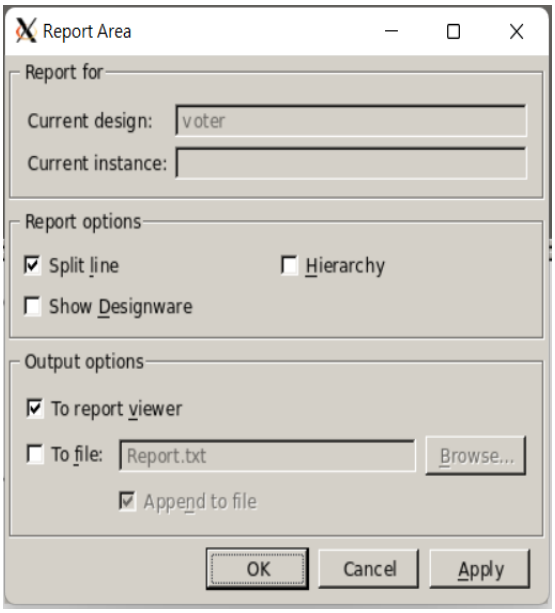
七、查看合成完的電路架構圖及 Critical Path





同先前步驟即可查看合成完後最佳化的電路架構圖，若要查看 Critical Path，則照著上圖的動作，及可得到電路的 Critical Path。

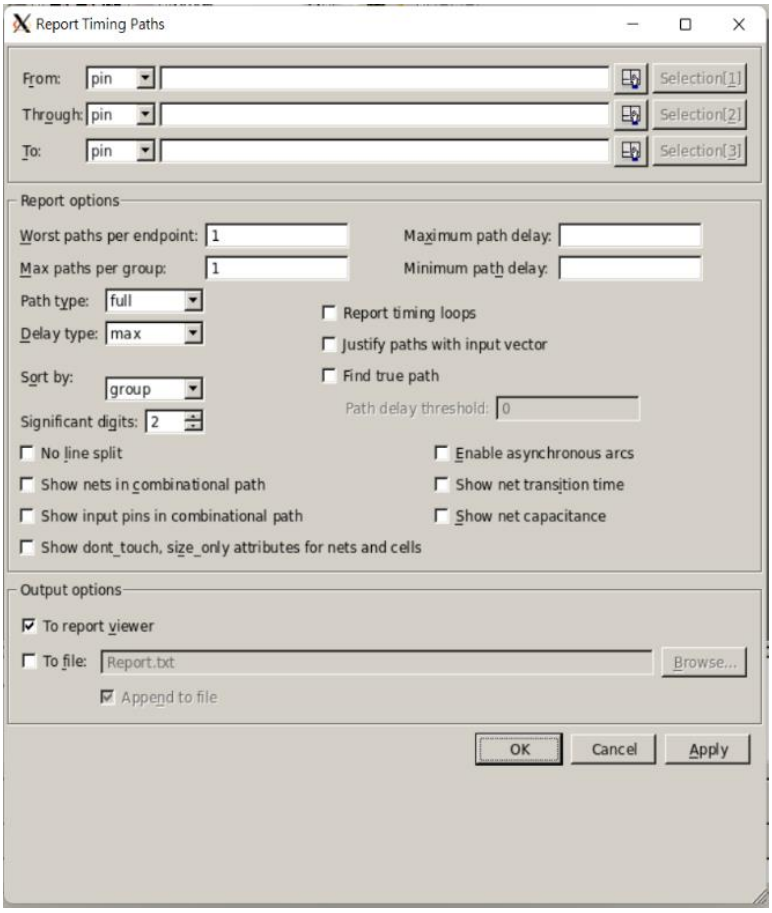
八、Area Report




```
****************************************
Report : area
Design : voter
Version: P-2019.03
Date   : Tue Apr 19 02:15:18 2022
****************************************

Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          618
Number of nets:                           796
Number of cells:                          306
Number of combinational cells:            185
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                      17

Combinational area:               1624.411767
Buf/Inv area:                        0.000000
Noncombinational area:               0.000000
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  1624.411767
Total area:                 undefined

***** End Of Report *****
```

若要查看電路面積的資訊則先選擇要查看的 module，接著在工具列上的 Design 點 Report Area 則可得到電路面積相關數據，而 Report Area 的設置如上左圖所示。

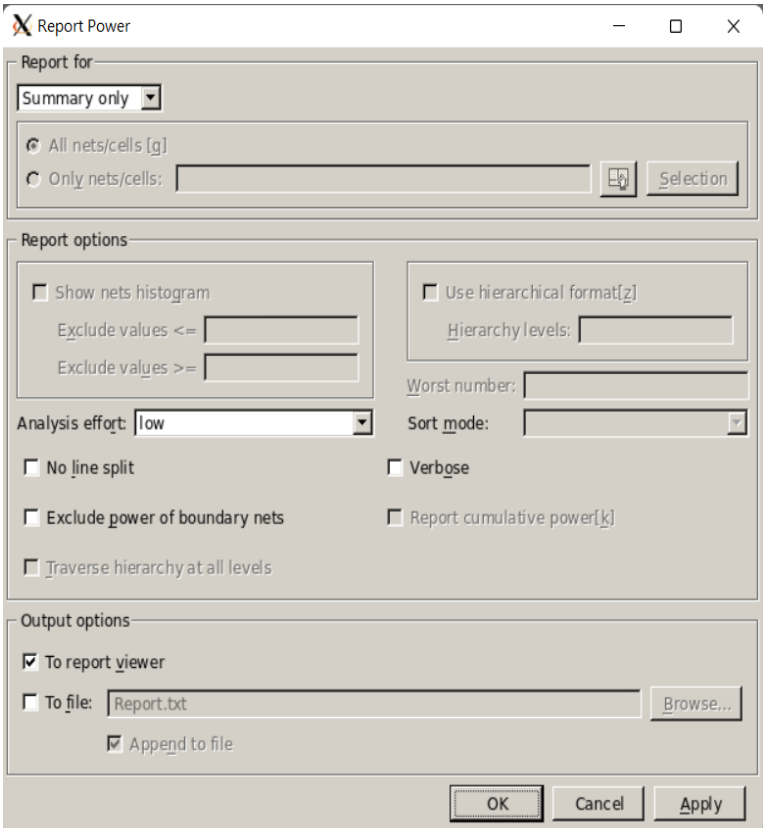
九、Timing Report



```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : voter
Version: P-2019.03
Date   : Tue Apr 19 02:15:43 2022
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: In_1[2] (input port)
  Endpoint: Out[1] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  In_1[2] (in)                             0.00       0.00 r
  U8/A[0] (adder_3_4)                      0.00       0.00 r
  U8/U0/A (full_adder_12)                  0.00       0.00 r
  U8/U0/U0/A (half_adder_24)               0.00       0.00 r
  U8/U0/U0/U1/Y (XOR2X1)                   0.14       0.14 r
  U8/U0/U0/S (half_adder_24)               0.00       0.14 r
  U8/U0/U1/A (half_adder_23)               0.00       0.14 r
  U8/U0/U1/U1/Y (XOR2X1)                   0.19       0.33 r
  U8/U0/U1/S (half_adder_23)               0.00       0.33 r
  U8/U0/Sum (full_adder_12)                0.00       0.33 r
  U8/Sum[0] (adder_3_4)                    0.00       0.33 r
  U9/A[0] (adder_3_3)                      0.00       0.33 r
  U9/U0/A (full_adder_9)                   0.00       0.33 r
  U9/U0/U0/A (half_adder_18)               0.00       0.33 r
  U9/U0/U0/U1/Y (XOR2X1)                   0.19       0.53 f
  U9/U0/U0/S (half_adder_18)               0.00       0.53 f
  U9/U0/U1/A (half_adder_17)               0.00       0.53 f
  U9/U0/U1/U1/Y (XOR2X1)                   0.18       0.71 f
  U9/U0/U1/S (half_adder_17)               0.00       0.71 f
  U9/U0/Sum (full_adder_9)                 0.00       0.71 f
  U10/U1/U1/B (half_adder_9)               0.00       1.13 f
  U10/U1/U1/U2/Y (AND2X1)                  0.17       1.30 f
  U10/U1/U1/C (half_adder_9)               0.00       1.30 f
  U10/U1/U2/Y (OR2X1)                      0.25       1.55 f
  U10/U1/C_out (full_adder_5)              0.00       1.55 f
  U10/U2/C_in (full_adder_4)               0.00       1.55 f
  U10/U2/U1/B (half_adder_7)               0.00       1.55 f
  U10/U2/U1/U2/Y (AND2X1)                  0.17       1.72 f
  U10/U2/U1/C (half_adder_7)               0.00       1.72 f
  U10/U2/U2/Y (OR2X1)                      0.25       1.97 f
  U10/U2/C_out (full_adder_4)              0.00       1.97 f
  U10/C_out (adder_3_2)                    0.00       1.97 f
  U11/C_in (adder_3_1)                     0.00       1.97 f
  U11/U0/C_in (full_adder_3)               0.00       1.97 f
  U11/U0/U1/B (half_adder_5)               0.00       1.97 f
  U11/U0/U1/U2/Y (AND2X1)                  0.17       2.14 f
  U11/U0/U1/C (half_adder_5)               0.00       2.14 f
  U11/U0/U2/Y (OR2X1)                      0.25       2.39 f
  U11/U0/C_out (full_adder_3)              0.00       2.39 f
  U11/U1/C_in (full_adder_2)               0.00       2.39 f
  U11/U1/U1/B (half_adder_3)               0.00       2.39 f
  U11/U1/U1/U2/Y (AND2X1)                  0.17       2.56 f
  U11/U1/U1/C (half_adder_3)               0.00       2.56 f
  U11/U1/U2/Y (OR2X1)                      0.25       2.81 f
  U11/U1/C_out (full_adder_2)              0.00       2.81 f
  U11/U2/C_in (full_adder_1)               0.00       2.81 f
  U11/U2/U1/B (half_adder_1)               0.00       2.81 f
  U11/U2/U1/U1/Y (XOR2X1)                  0.14       2.95 f
  U11/U2/U1/S (half_adder_1)               0.00       2.95 f
  U11/U2/Sum (full_adder_1)                0.00       2.95 f
  U11/Sum[2] (adder_3_1)                   0.00       2.95 f
  U21/Y (AO21X1)                           0.26       3.21 f
  U20/Y (NOR2X1)                           0.06       3.26 r
  Out[1] (out)                             0.00       3.26 r
  data arrival time                                   3.26
  -----------------------------------------------------------
  (Path is unconstrained)


***** End Of Report *****
```

若要查看電路延遲的資訊則先選擇要查看的 module，接著在工具列上的 Timing 點 Report Timing Path，則可得到電路延遲的相關數據，而 Timing Report 的設置如上圖所示。

十、Power Report



```
Report : power
        -analysis_effort low
Design : voter
Version: P-2019.03
Date   : Tue Apr 19 02:17:19 2022
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 112.9891 uW   (76%)
  Net Switching Power  =  35.0757 uW   (24%)
                         ---------
Total Dynamic Power    = 148.0648 uW  (100%)

Cell Leakage Power     =   2.1860 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register           0.0000           0.0000            0.0000             0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational      0.1130        3.5076e-02        2.1860e+06             0.1503  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total              0.1130 mW     3.5076e-02 mW     2.1860e+06 pW          0.1503 mW

***** End Of Report *****
```

若要查看電路功率的資訊則先選擇要查看的 module，接著在工具列上的 Design 點 Report Power，則可得到電路功率的相關數據，而 Power Report 的設置如上圖所示。

十一、Report Qor

```
design_vision> report_qor

****************************************
Report : qor
Design : voter
Version: P-2019.03
Date   : Tue Apr 19 02:18:24 2022
****************************************


  Timing Path Group (none)
  -----------------------------------
  Levels of Logic:               17.00
  Critical Path Length:           3.26
  Critical Path Slack:          uninit
  Critical Path Clk Period:        n/a
  Total Negative Slack:           0.00
  No. of Violating Paths:         0.00
  Worst Hold Violation:           0.00
  Total Hold Violation:           0.00
  No. of Hold Violations:         0.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:         120
  Hierarchical Port Count:         600
  Leaf Cell Count:                 185
  Buf/Inv Cell Count:                0
  Buf Cell Count:                    0
  Inv Cell Count:                    0
  CT Buf/Inv Cell Count:             0
  Combinational Cell Count:        185
```

```
Area
-----------------------------------
Combinational Area:     1624.411767
Noncombinational Area:     0.000000
Buf/Inv Area:              0.000000
Total Buffer Area:             0.00
Total Inverter Area:           0.00
Macro/Black Box Area:      0.000000
Net Area:                  0.000000
-----------------------------------
Cell Area:              1624.411767
Design Area:            1624.411767


Design Rules
-----------------------------------
Total Number of Nets:           201
Nets With Violations:             0
Max Trans Violations:             0
Max Cap Violations:               0
-----------------------------------


Hostname: soc08

Compile CPU Statistics
---------------------------------------
Resource Sharing:                  0.00
Logic Optimization:                0.33
Mapping Optimization:              0.31
---------------------------------------
Overall Compile Time:              3.03
Overall Compile Wall Clock Time:   3.62
```

若想要快速取得邏輯合成電路的相關資訊，則可輸入上圖紅圈內的指令，結果如上圖所示(功率需使用 Power Report)。

十二、儲存電路及 Timing 檔

```
gui_start
read_file -format verilog {/home/PDSD110/PDSD110a43/SYN/HW1-2/voter/top.v}
curent_design voter
current_design voter
set_fix_multiple_port_nets -all -buffer_constants
compile -exact_map
change_names -hierarchy -rule verilog
write -hierarchy -format verilog -output /home/PDSD110/PDSD110a43/SYN/HW1-2/voter/voter_syn.v
uplevel #0 { report_area }
uplevel #0 { report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by group }
uplevel #0 { report_power -analysis_effort low }
report_qor
write_sdf -version 1.0 -context verilog voter.sdf
```

若要儲存邏輯合成電路的 sdf 檔，則需輸入上圖紅圈內的指令，儲存完後即可存檔並在指令欄輸入 exit 關閉邏輯合成軟體。

十三、重新模擬 Testbench

```
`timescale  10ns/100ps

`include    "./voter_syn.v"
`include    "./tsmc13.v"


module textfixture_voter;

reg     [2:0]       In_1,In_2,In_3,In_4,In_5;

wire    [2:0]       Out;

voter U0(In_1,In_2,In_3,In_4,In_5,Out);
```

```
initial begin

$sdf_annotate("voter.sdf",U0);

end

initial begin

$fsdbDumpfile("voter_syn.fsdb");
$fsdbDumpvars;

end
```

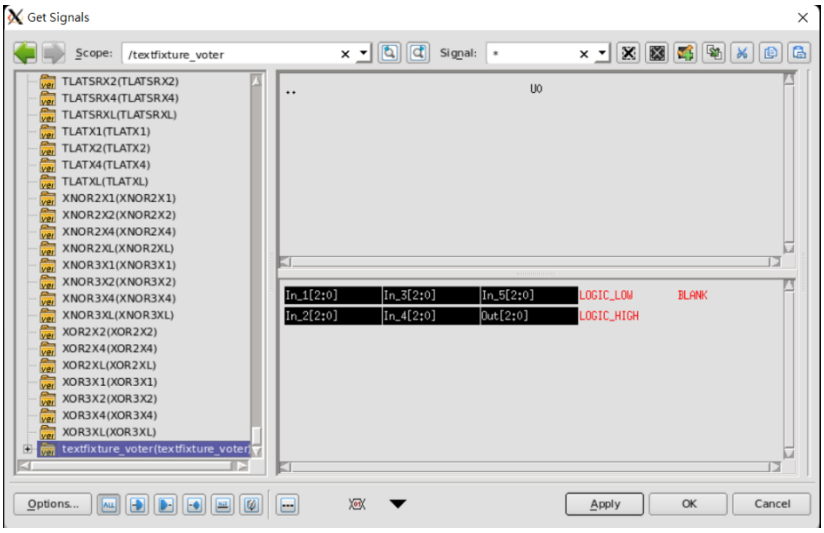
在模擬前要在 testbench 加上 timescale、引入要模擬的.v 檔、台積電.13 製程檔、sdf 檔及波形檔。

```
#####################################################
#        32BIT is the default mode                  #
#    If you want to run 64BIT mode,                 #
#    please set the LD_LIBRARY_PATH and SHLIB_PATH   #
#    to path of 64BIT by yourself.                  #
#####################################################
soc08 [~]
-PDSD110a43- $cd
2022_univ_cell/          EX2/                icc test/           nWaveLog/           SYN/                    test2/
command.log              Example/            novas.conf          Practice/           synopsys_cache_P-2019.03/ verilog PDSD/
default.svf              filenames.log       novas.rc            RTL/                test/
soc08 [~]
-PDSD110a43- $cd SYN/
soc08 [~/SYN]
-PDSD110a43- $cd HW1-2/
soc08 [~/SYN/HW1-2]
-PDSD110a43- $cd voter/
soc08 [~/SYN/HW1-2/voter]
-PDSD110a43- $ncverilog textfixture_voter.v +access+r
```

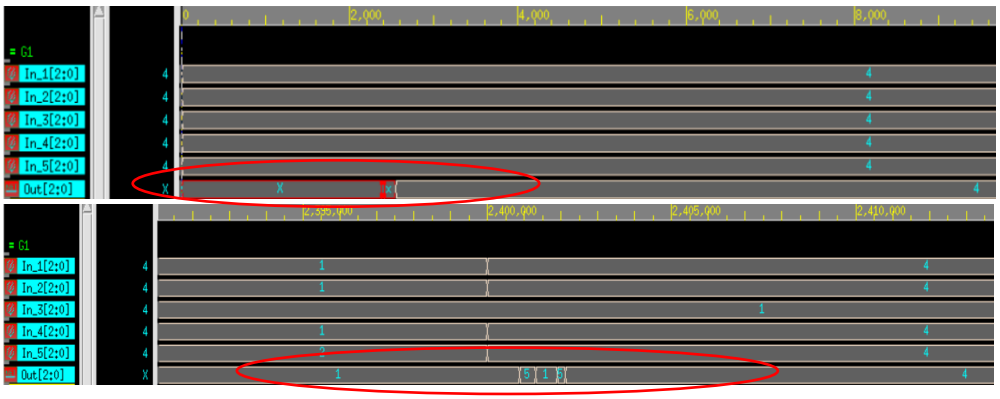
打開工作站使用 ncverilog 模擬 testbench。

```
        Reading SDF file from location "voter.sdf"
        Annotating SDF timing data:
                Compiled SDF file:      voter.sdf.X
                Log file:
                Backannotation scope:   textfixture_voter.U0
                Configuration file:
                MTM control:
                Scale factors:
                Scale type:
        Annotation completed successfully...
```

確認在模擬過程中有在終端機出現上圖紅色方框內的訊息



在工作站開啟 nWave 後，找到電路的 fsdb 檔並找到 testbench module name，然後選取所要觀察的訊號。

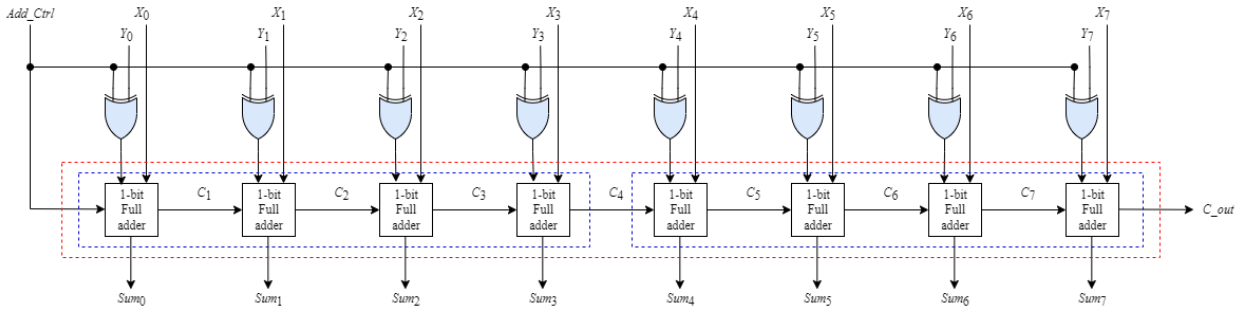


在觀察波形時需能觀察到初始的 output 為 unknown 以及在數值變化時輸出會有 delay 的效應。

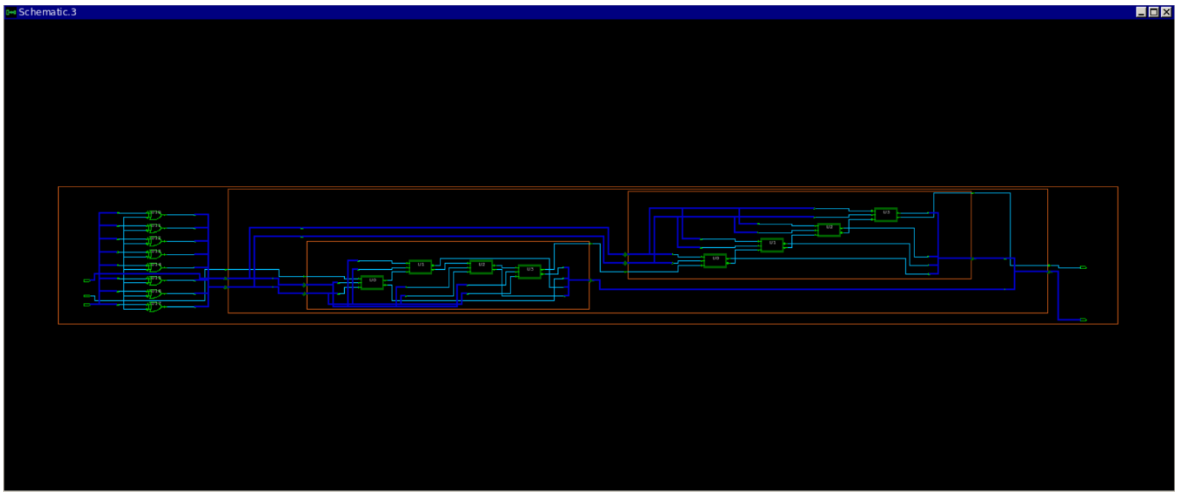
貳、電路分析

一、RCA

i. 電路架構



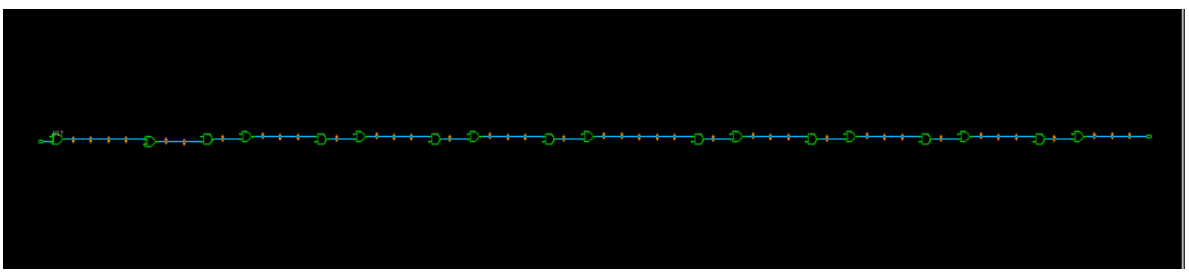
(合成前)



(合成後)

※比較:電路在合成前與合成後架構相同，兩者皆是以八個 full adder 及 XOR 閘所組成。

ii. 最長路徑



iii. 面積

```
****************************************
Report : area
Design : adder
Version: P-2019.03
Date   : Tue Apr 19 01:04:26 2022
****************************************

Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          184
Number of nets:                           223
Number of cells:                           75
Number of combinational cells:             48
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       2

Combinational area:               448.113590
Buf/Inv area:                       0.000000
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  448.113590
Total area:                 undefined

***** End Of Report *****
```

```
design_vision> report_qor

****************************************
Report : qor
Design : adder
Version: P-2019.03
Date   : Tue Apr 19 01:18:40 2022
****************************************


  Timing Path Group (none)
  -----------------------------------
  Levels of Logic:              18.00
  Critical Path Length:          3.70
  Critical Path Slack:         uninit
  Critical Path Clk Period:       n/a
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:          0.00
  Total Hold Violation:          0.00
  No. of Hold Violations:        0.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:         27
  Hierarchical Port Count:        158
  Leaf Cell Count:                 48
  Buf/Inv Cell Count:               0
  Buf Cell Count:                   0
  Inv Cell Count:                   0
  CT Buf/Inv Cell Count:            0
  Combinational Cell Count:        48
```

電路面積: 448.113590(um^2)

根據.13 製程約使用了 448.113590÷5≒90 個 NAND2 gates

Combinational Cell Count: 48 個邏輯閘

最長路徑邏輯閘層數: 18 層

iv. 延遲

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
         -sort_by group
Design : adder
Version: P-2019.03
Date   : Tue Apr 19 01:06:01 2022
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: Add_ctrl (input port)
  Endpoint: C_out (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  Add_ctrl (in)                            0.00       0.00 r
  U17/Y (XOR2X1)                           0.14       0.14 r
  U8/B[0] (adder_8)                        0.00       0.14 r
  U8/U0/B[0] (adder_4_0)                   0.00       0.14 r
  U8/U0/U0/B (full_adder_0)                0.00       0.14 r
  U8/U0/U0/U0/B (half_adder_0)             0.00       0.14 r
  U8/U0/U0/U0/U1/Y (XOR2X1)                0.20       0.34 f
  U8/U0/U0/U0/S (half_adder_0)             0.00       0.34 f
  U8/U0/U0/U1/A (half_adder_15)            0.00       0.34 f
  U8/U0/U0/U1/U2/Y (AND2X1)                0.20       0.54 f
  U8/U0/U0/U1/C (half_adder_15)            0.00       0.54 f
  U8/U0/U0/U2/Y (OR2X1)                    0.25       0.79 f
  U8/U0/U0/C_out (full_adder_0)            0.00       0.79 f
  U8/U0/U1/C_in (full_adder_7)             0.00       0.79 f
  U8/U0/U1/U1/B (half_adder_13)            0.00       0.79 f
  U8/U0/U1/U1/U2/Y (AND2X1)                0.17       0.96 f
  U8/U0/U1/U1/C (half_adder_13)            0.00       0.96 f
  U8/U0/U1/U2/Y (OR2X1)                    0.25       1.21 f
  U8/U0/U1/C_out (full_adder_7)            0.00       1.21 f
  U8/U0/U2/C_in (full_adder_6)             0.00       1.21 f
```

```
  U8/U0/U2/U2/Y (OR2X1)                    0.25       1.64 f
  U8/U0/U2/C_out (full_adder_6)            0.00       1.64 f
  U8/U0/U3/C_in (full_adder_5)             0.00       1.64 f
  U8/U0/U3/U1/B (half_adder_9)             0.00       1.64 f
  U8/U0/U3/U1/U2/Y (AND2X1)                0.17       1.81 f
  U8/U0/U3/U1/C (half_adder_9)             0.00       1.81 f
  U8/U0/U3/U2/Y (OR2X1)                    0.25       2.06 f
  U8/U0/U3/C_out (full_adder_5)            0.00       2.06 f
  U8/U0/C_out (adder_4_0)                  0.00       2.06 f
  U8/U1/C_in (adder_4_1)                   0.00       2.06 f
  U8/U1/U0/C_in (full_adder_4)             0.00       2.06 f
  U8/U1/U0/U1/B (half_adder_7)             0.00       2.06 f
  U8/U1/U0/U1/U2/Y (AND2X1)                0.17       2.23 f
  U8/U1/U0/U1/C (half_adder_7)             0.00       2.23 f
  U8/U1/U0/U2/Y (OR2X1)                    0.25       2.48 f
  U8/U1/U0/C_out (full_adder_4)            0.00       2.48 f
  U8/U1/U1/C_in (full_adder_3)             0.00       2.48 f
  U8/U1/U1/U1/B (half_adder_5)             0.00       2.48 f
  U8/U1/U1/U1/U2/Y (AND2X1)                0.17       2.65 f
  U8/U1/U1/U1/C (half_adder_5)             0.00       2.65 f
  U8/U1/U1/U2/Y (OR2X1)                    0.25       2.90 f
  U8/U1/U1/C_out (full_adder_3)            0.00       2.90 f
  U8/U1/U2/C_in (full_adder_2)             0.00       2.90 f
  U8/U1/U2/U1/B (half_adder_3)             0.00       2.90 f
  U8/U1/U2/U1/U2/Y (AND2X1)                0.17       3.07 f
  U8/U1/U2/U1/C (half_adder_3)             0.00       3.07 f
  U8/U1/U2/U2/Y (OR2X1)                    0.25       3.32 f
  U8/U1/U2/C_out (full_adder_2)            0.00       3.32 f
  U8/U1/U3/C_in (full_adder_1)             0.00       3.32 f
  U8/U1/U3/U1/B (half_adder_1)             0.00       3.32 f
  U8/U1/U3/U1/U2/Y (AND2X1)                0.17       3.49 f
  U8/U1/U3/U1/C (half_adder_1)             0.00       3.49 f
  U8/U1/U3/U2/Y (OR2X1)                    0.21       3.70 f
  U8/U1/U3/C_out (full_adder_1)            0.00       3.70 f
  U8/U1/C_out (adder_4_1)                  0.00       3.70 f
  U8/C_out (adder_8)                       0.00       3.70 f
  C_out (out)                              0.00       3.70 f
  data arrival time                                   3.70
  -----------------------------------------------------------
  (Path is unconstrained)
```

電路延遲時間:3.70(ns)

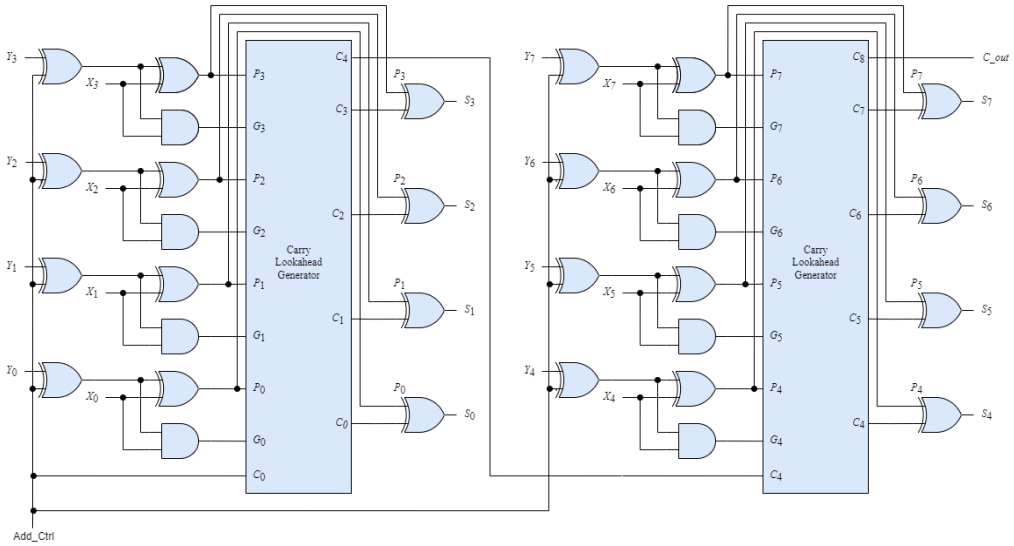
v. 功率

```
****************************************
Report : power
        -analysis_effort low
Design : adder
Version: P-2019.03
Date   : Tue Apr 19 01:10:07 2022
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  60.6764 uW   (80%)
  Net Switching Power  =  15.2832 uW   (20%)
                         ---------
Total Dynamic Power    =  75.9596 uW  (100%)

Cell Leakage Power     = 614.1201 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register           0.0000           0.0000            0.0000             0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational  6.0676e-02       1.5283e-02        6.1412e+05         7.6574e-02  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total          6.0676e-02 mW     1.5283e-02 mW     6.1412e+05 pW      7.6574e-02 mW

***** End Of Report *****
```

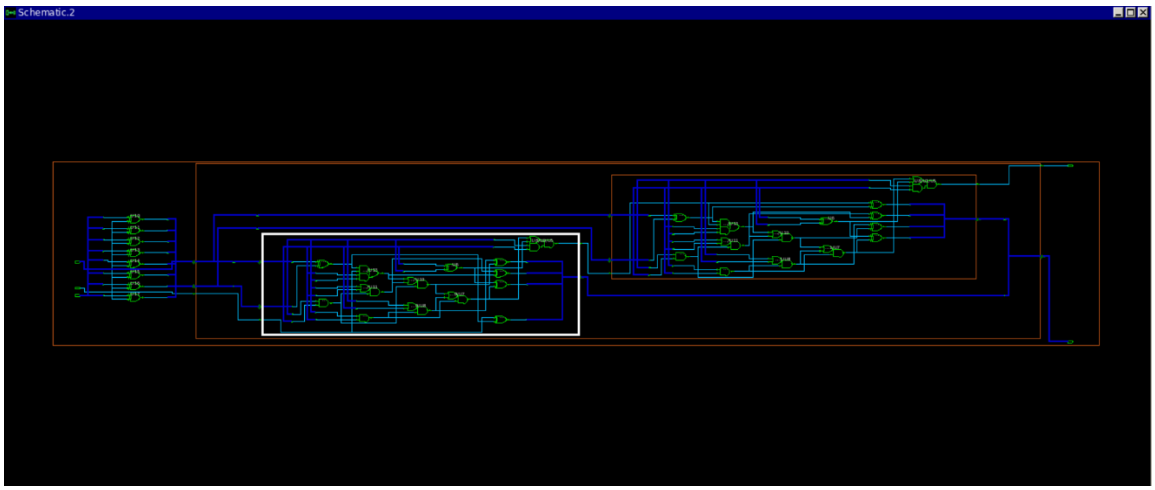
電路總功耗：7.6574×10^{-2}(mW)

二、CLA

i. 電路架構



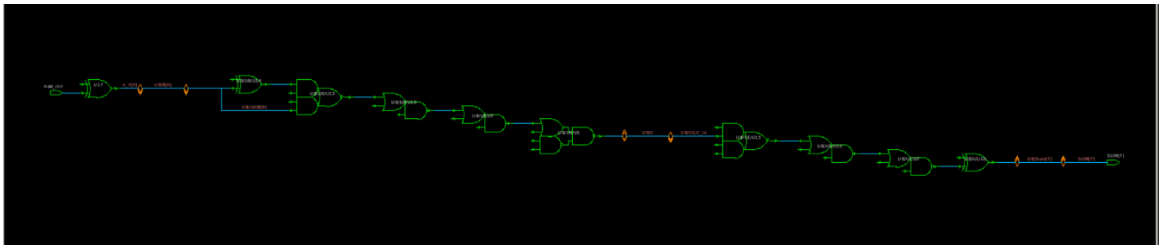
(合成前)



(合成後)

※比較:電路在合成前與合成後在 carry-lookahead generator 的架構上有所不同，合成前經過的邏輯閘層數較少，但使用邏輯閘數量較多；合成後的邏輯閘層數較多，但使用的邏輯閘數量較少。

ii. 最長路徑



iii. 面積

```
****************************************
Report : area
Design : adder
Version: P-2019.03
Date   : Tue Apr 19 01:53:15 2022
****************************************

Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                           80
Number of nets:                           107
Number of cells:                           39
Number of combinational cells:             36
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       2

Combinational area:               359.848793
Buf/Inv area:                       0.000000
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  359.848793
Total area:                 undefined

***** End Of Report *****
```

```
design_vision> report_qor

****************************************
Report : qor
Design : adder
Version: P-2019.03
Date   : Tue Apr 19 01:57:15 2022
****************************************

  Timing Path Group (none)
  -----------------------------------
  Levels of Logic:               10.00
  Critical Path Length:           2.21
  Critical Path Slack:          uninit
  Critical Path Clk Period:        n/a
  Total Negative Slack:           0.00
  No. of Violating Paths:         0.00
  Worst Hold Violation:           0.00
  Total Hold Violation:           0.00
  No. of Hold Violations:         0.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:           3
  Hierarchical Port Count:          54
  Leaf Cell Count:                  36
  Buf/Inv Cell Count:                0
  Buf Cell Count:                    0
  Inv Cell Count:                    0
  CT Buf/Inv Cell Count:             0
```

電路面積: 359.848793(um^2)

根據.13 製程約使用了 359.848793÷5≒72 個 NAND2 gates

Combinational Cell Count: 36 個邏輯閘

最長路徑邏輯閘層數: 10 層

※比較:合成前的 Combinational Cell Count 有 60 個邏輯閘；最長路徑層數為 7 層

iv. 延遲

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : adder
Version: P-2019.03
Date   : Tue Apr 19 01:53:45 2022
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: Add_ctrl (input port)
  Endpoint: SUM[7] (output port)
  Path Group: (none)
  Path Type: max

  Point                                                   Incr       Path
  -----------------------------------------------------------------------
  input external delay                                    0.00       0.00 r
  Add_ctrl (in)                                           0.00       0.00 r
  U17/Y (XOR2X1)                                          0.15       0.15 r
  U8/B[0] (carry_lookahead_adder_8)                       0.00       0.15 r
  U8/U0/B[0] (carry_lookahead_adder_4_0)                  0.00       0.15 r
  U8/U0/U14/Y (XOR2X1)                                    0.22       0.37 r
  U8/U0/U13/Y (AOI22X1)                                   0.11       0.48 f
  U8/U0/U10/Y (OA21XL)                                    0.29       0.78 f
  U8/U0/U7/Y (OA21XL)                                     0.30       1.07 f
  U8/U0/U5/Y (OAI2BB2XL)                                  0.27       1.35 r
  U8/U0/C_out (carry_lookahead_adder_4_0)                 0.00       1.35 r
  U8/U1/C_in (carry_lookahead_adder_4_1)                  0.00       1.35 r
  U8/U1/U13/Y (AOI22X1)                                   0.12       1.47 f
  U8/U1/U10/Y (OA21XL)                                    0.29       1.76 f
  U8/U1/U7/Y (OA21XL)                                     0.30       2.06 f
  U8/U1/U1/Y (XOR2X1)                                     0.15       2.21 f
  U8/U1/Sum[3] (carry_lookahead_adder_4_1)                0.00       2.21 f
  U8/Sum[7] (carry_lookahead_adder_8)                     0.00       2.21 f
  SUM[7] (out)                                            0.00       2.21 f
  data arrival time                                                  2.21
  -----------------------------------------------------------------------
  (Path is unconstrained)


***** End Of Report *****
```

電路延遲時間:2.21(ns)

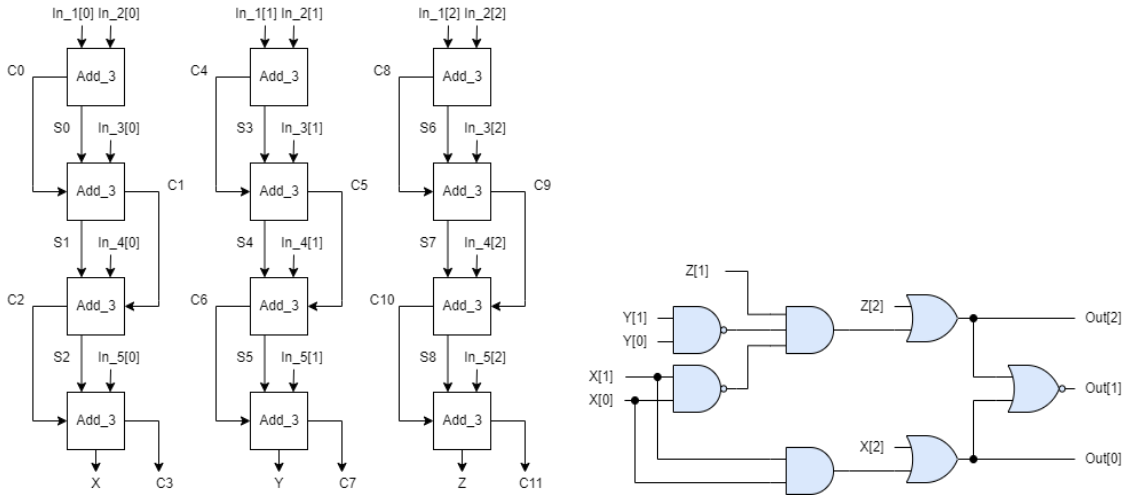
v. 功率

```
---------------------------------------
Report : power
        -analysis_effort low
Design : adder
Version: P-2019.03
Date   : Tue Apr 19 01:56:12 2022
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  46.2857 uW   (75%)
  Net Switching Power  =  15.3256 uW   (25%)
                          ---------
Total Dynamic Power    =  61.6114 uW  (100%)

Cell Leakage Power     = 409.3030 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register           0.0000           0.0000            0.0000             0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational  4.6286e-02       1.5326e-02        4.0930e+05         6.2021e-02  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total          4.6286e-02 mW     1.5326e-02 mW     4.0930e+05 pW      6.2021e-02 mW

***** End Of Report *****
```

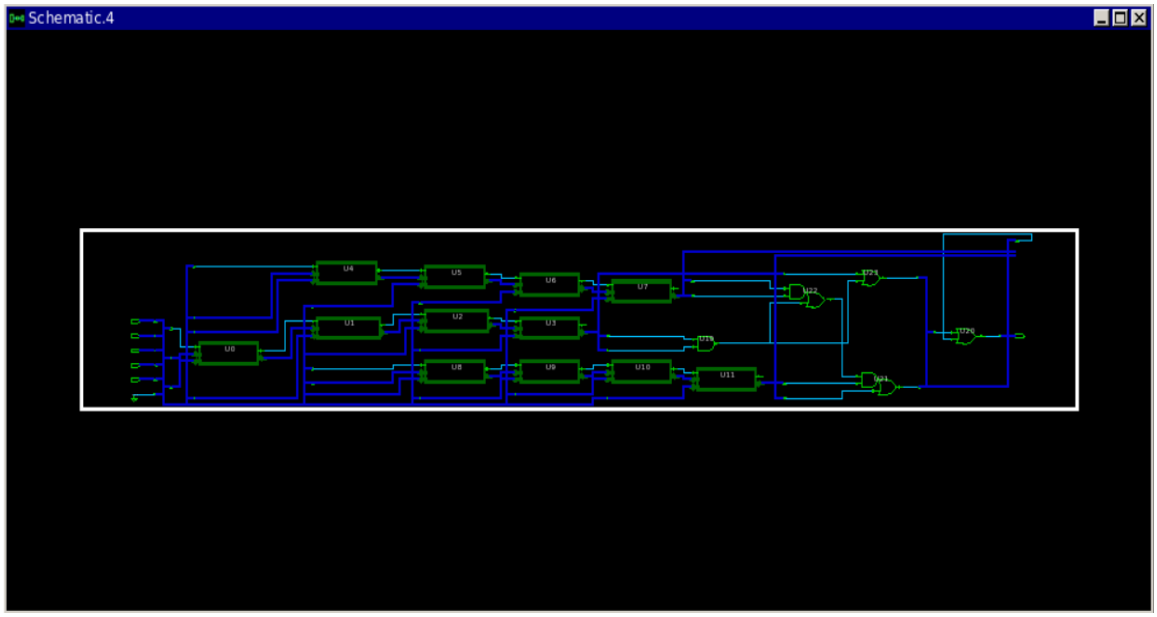
電路總功耗: 6.2021×10^{-2}(mW)

三、voter

i. 電路架構



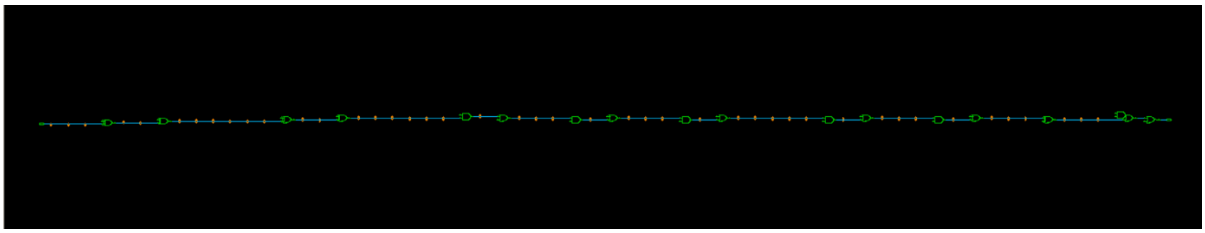
（合成前）



（合成後）

※比較:合成前與合成後架構幾乎相同，皆為 12 個 add_3 和比較用的邏輯閘所組成，但合成後的電路的比較邏輯閘數量較少且最長路徑邏輯閘層數較低。

ii. 最長路徑



iii. 面積

```
****************************************
Report : area
Design : voter
Version: P-2019.03
Date   : Tue Apr 19 02:15:18 2022
****************************************

Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          618
Number of nets:                           796
Number of cells:                          306
Number of combinational cells:            185
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                      17

Combinational area:               1624.411767
Buf/Inv area:                        0.000000
Noncombinational area:               0.000000
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  1624.411767
Total area:                 undefined

***** End Of Report *****
```

```
design_vision> report_qor

****************************************
Report : qor
Design : voter
Version: P-2019.03
Date   : Tue Apr 19 02:18:24 2022
****************************************


  Timing Path Group (none)
  -----------------------------------
  Levels of Logic:               17.00
  Critical Path Length:           3.26
  Critical Path Slack:          uninit
  Critical Path Clk Period:        n/a
  Total Negative Slack:           0.00
  No. of Violating Paths:         0.00
  Worst Hold Violation:           0.00
  Total Hold Violation:           0.00
  No. of Hold Violations:         0.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:         120
  Hierarchical Port Count:         600
  Leaf Cell Count:                 185
  Buf/Inv Cell Count:                0
  Buf Cell Count:                    0
  Inv Cell Count:                    0
  CT Buf/Inv Cell Count:             0
  Combinational Cell Count:        185
```

電路面積: 1624.411767(um^2)

根據.13 製程約使用了 1624.411767÷5≒325 個 NAND2 gates

Combinational Cell Count: 185 個邏輯閘

最長路徑邏輯閘層數: 17 層

※比較: 合成前的 Combinational Cell Count 有 187 個邏輯閘；最長路徑層數為 32 層

iv. 延遲

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : voter
Version: P-2019.03
Date   : Tue Apr 19 02:15:43 2022
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: In_1[2] (input port)
  Endpoint: Out[1] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  In_1[2] (in)                             0.00       0.00 r
  U8/A[0] (adder_3_4)                      0.00       0.00 r
  U8/U0/A (full_adder_12)                  0.00       0.00 r
  U8/U0/U0/A (half_adder_24)               0.00       0.00 r
  U8/U0/U0/U1/Y (XOR2X1)                   0.14       0.14 r
  U8/U0/U0/S (half_adder_24)               0.00       0.14 r
  U8/U0/U1/A (half_adder_23)               0.00       0.14 r
  U8/U0/U1/U1/Y (XOR2X1)                   0.19       0.33 r
  U8/U0/U1/S (half_adder_23)               0.00       0.33 r
  U8/U0/Sum (full_adder_12)                0.00       0.33 r
  U8/Sum[0] (adder_3_4)                    0.00       0.33 r
  U9/A[0] (adder_3_3)                      0.00       0.33 r
  U9/U0/A (full_adder_9)                   0.00       0.33 r
  U9/U0/U0/A (half_adder_18)               0.00       0.33 r
  U9/U0/U0/U1/Y (XOR2X1)                   0.19       0.53 f
  U9/U0/U0/S (half_adder_18)               0.00       0.53 f
  U9/U0/U1/A (half_adder_17)               0.00       0.53 f
  U9/U0/U1/U1/Y (XOR2X1)                   0.18       0.71 f
  U9/U0/U1/S (half_adder_17)               0.00       0.71 f
  U9/U0/Sum (full_adder_9)                 0.00       0.71 f
  U10/U1/U1/B (half_adder_9)               0.00       1.13 f
  U10/U1/U1/U2/Y (AND2X1)                  0.17       1.30 f
  U10/U1/U1/C (half_adder_9)               0.00       1.30 f
  U10/U1/U2/Y (OR2X1)                      0.25       1.55 f
  U10/U1/C_out (full_adder_5)              0.00       1.55 f
  U10/U2/C_in (full_adder_4)               0.00       1.55 f
  U10/U2/U1/B (half_adder_7)               0.00       1.55 f
  U10/U2/U1/U2/Y (AND2X1)                  0.17       1.72 f
  U10/U2/U1/C (half_adder_7)               0.00       1.72 f
  U10/U2/U2/Y (OR2X1)                      0.25       1.97 f
  U10/U2/C_out (full_adder_4)              0.00       1.97 f
  U10/C_out (adder_3_2)                    0.00       1.97 f
  U11/C_in (adder_3_1)                     0.00       1.97 f
  U11/U0/C_in (full_adder_3)               0.00       1.97 f
  U11/U0/U1/B (half_adder_5)               0.00       1.97 f
  U11/U0/U1/U2/Y (AND2X1)                  0.17       2.14 f
  U11/U0/U1/C (half_adder_5)               0.00       2.14 f
  U11/U0/U2/Y (OR2X1)                      0.25       2.39 f
  U11/U0/C_out (full_adder_3)              0.00       2.39 f
  U11/U1/C_in (full_adder_2)               0.00       2.39 f
  U11/U1/U1/B (half_adder_3)               0.00       2.39 f
  U11/U1/U1/U2/Y (AND2X1)                  0.17       2.56 f
  U11/U1/U1/C (half_adder_3)               0.00       2.56 f
  U11/U1/U2/Y (OR2X1)                      0.25       2.81 f
  U11/U1/C_out (full_adder_2)              0.00       2.81 f
  U11/U2/C_in (full_adder_1)               0.00       2.81 f
  U11/U2/U1/B (half_adder_1)               0.00       2.81 f
  U11/U2/U1/U1/Y (XOR2X1)                  0.14       2.95 f
  U11/U2/U1/S (half_adder_1)               0.00       2.95 f
  U11/U2/Sum (full_adder_1)                0.00       2.95 f
  U11/Sum[2] (adder_3_1)                   0.00       2.95 f
  U21/Y (AO21X1)                           0.26       3.21 f
  U20/Y (NOR2X1)                           0.06       3.26 r
  Out[1] (out)                             0.00       3.26 r
  data arrival time                                   3.26
  -----------------------------------------------------------
  (Path is unconstrained)


***** End Of Report *****
```

電路延遲時間:3.26(ns)

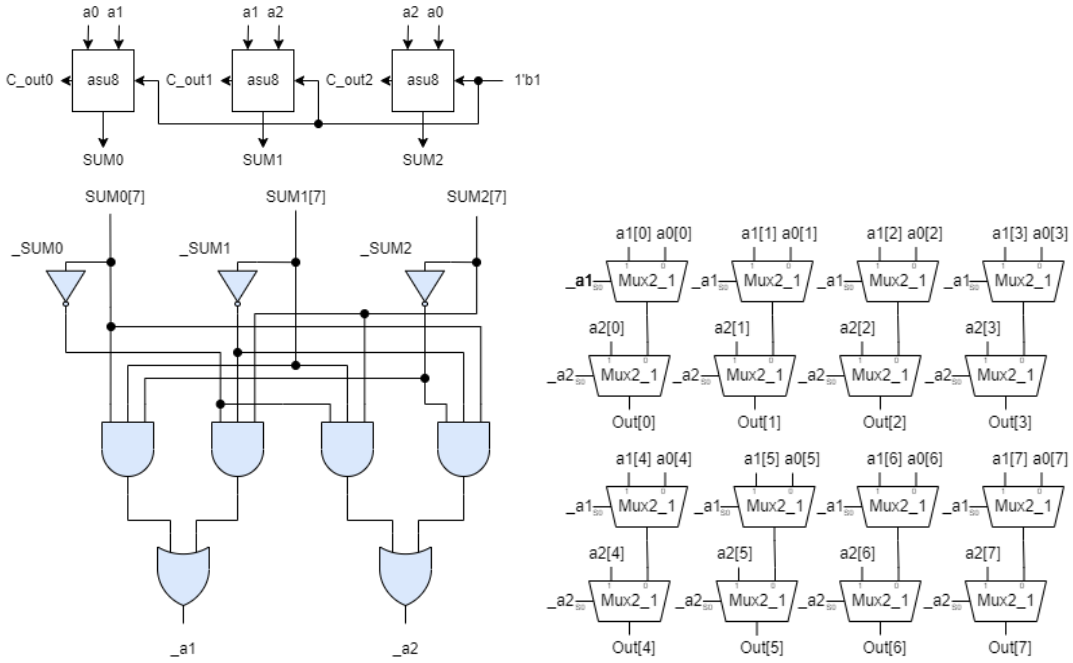
v. 功率

```
Report : power
        -analysis_effort low
Design : voter
Version: P-2019.03
Date   : Tue Apr 19 02:17:19 2022
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 112.9891 uW   (76%)
  Net Switching Power  =  35.0757 uW   (24%)
                         ---------
Total Dynamic Power    = 148.0648 uW  (100%)

Cell Leakage Power     =   2.1860 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad           0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory           0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box        0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network    0.0000           0.0000              0.0000             0.0000  (   0.00%)
register         0.0000           0.0000              0.0000             0.0000  (   0.00%)
sequential       0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational    0.1130        3.5076e-02          2.1860e+06            0.1503  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total            0.1130 mW     3.5076e-02 mW     2.1860e+06 pW         0.1503 mW

***** End Of Report *****
```

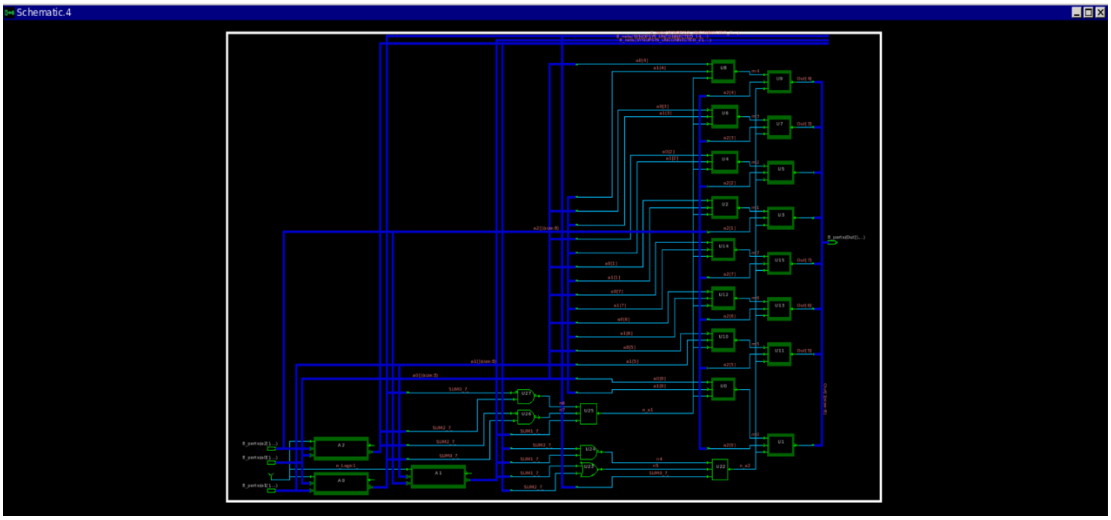
電路總功耗:0.1503(mW)

四、median

i. 電路架構



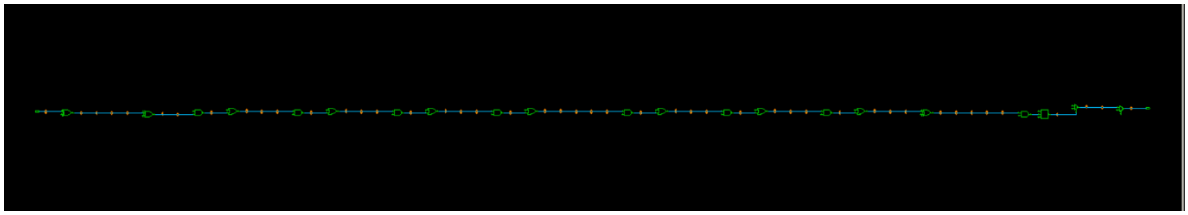
(合成前)



(合成後)

※比較:合成前與合成後的電路架構幾乎相同，皆為 asu8、決定 select bit 的邏輯電路和 2-to-1MUX 所組成，但由於製程的關係，合成後電路的 MUX 所使用到的邏輯閘數目較少，最長路徑層數也就跟著降低。

ii. 最長路徑



iii. 面積

```
****************************************
Report : area
Design : median
Version: P-2019.03
Date   : Tue Apr 19 02:29:08 2022
****************************************

Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          648
Number of nets:                           783
Number of cells:                          267
Number of combinational cells:            166
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                      23

Combinational area:               1610.832566
Buf/Inv area:                        0.000000
Noncombinational area:               0.000000
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  1610.832566
Total area:                 undefined

***** End Of Report *****
```

```
design_vision> report_qor

****************************************
Report : qor
Design : median
Version: P-2019.03
Date   : Tue Apr 19 02:32:06 2022
****************************************


  Timing Path Group (none)
  -----------------------------------
  Levels of Logic:              21.00
  Critical Path Length:          4.69
  Critical Path Slack:         uninit
  Critical Path Clk Period:       n/a
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:          0.00
  Total Hold Violation:          0.00
  No. of Hold Violations:        0.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:        100
  Hierarchical Port Count:        616
  Leaf Cell Count:                166
  Buf/Inv Cell Count:               0
  Buf Cell Count:                   0
  Inv Cell Count:                   0
  CT Buf/Inv Cell Count:            0
  Combinational Cell Count:       166
```

電路面積: 1610.832566(um^2)

根據.13 製程約使用了 1610.832566÷5≒322 個 NAND2 gates

Combinational Cell Count: 166 個邏輯閘

最長路徑邏輯閘層數: 21 層

※比較:合成前的 Combinational Cell Count 有 217 個邏輯閘；最長路徑層數為 24 層

iv. 延遲

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : median
Version: P-2019.03
Date   : Tue Apr 19 02:29:40 2022
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: a0[0] (input port)
  Endpoint: Out[7] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  a0[0] (in)                               0.00       0.00 f
  A2/Y[0] (asu8_1)                         0.00       0.00 f
  A2/U9/Y (XOR2X1)                         0.09       0.09 r
  A2/U8/B[0] (adder_8_1)                   0.00       0.09 r
  A2/U8/U0/B[0] (adder_4_2)                0.00       0.09 r
  A2/U8/U0/U0/B (full_adder_8)             0.00       0.09 r
  A2/U8/U0/U0/U0/B (half_adder_16)         0.00       0.09 r
  A2/U8/U0/U0/U0/U1/Y (XOR2X1)             0.18       0.27 f
  A2/U8/U0/U0/U0/S (half_adder_16)         0.00       0.27 f
  A2/U8/U0/U0/U1/A (half_adder_15)         0.00       0.27 f
  A2/U8/U0/U0/U1/U2/Y (AND2X1)             0.20       0.47 f
  A2/U8/U0/U0/U1/C (half_adder_15)         0.00       0.47 f
  A2/U8/U0/U0/U2/Y (OR2X1)                 0.25       0.73 f
  A2/U8/U0/U0/C_out (full_adder_8)         0.00       0.73 f
  A2/U8/U0/U1/C_in (full_adder_7)          0.00       0.73 f
  A2/U8/U0/U1/U1/B (half_adder_13)         0.00       0.73 f
  A2/U8/U0/U1/U1/U2/Y (AND2X1)             0.17       0.90 f
  A2/U8/U0/U1/U1/C (half_adder_13)         0.00       0.90 f
  A2/U8/U0/U1/U2/Y (OR2X1)                 0.25       1.15 f
  A2/U8/U0/U1/C_out (full_adder_7)         0.00       1.15 f
  A2/U8/U1/U0/U1/B (half_adder_7)          0.00       1.99 f
  A2/U8/U1/U0/U1/U2/Y (AND2X1)             0.17       2.16 f
  A2/U8/U1/U0/U1/C (half_adder_7)          0.00       2.16 f
  A2/U8/U1/U0/U2/Y (OR2X1)                 0.25       2.41 f
  A2/U8/U1/U0/C_out (full_adder_4)         0.00       2.41 f
  A2/U8/U1/U1/C_in (full_adder_3)          0.00       2.41 f
  A2/U8/U1/U1/U1/B (half_adder_5)          0.00       2.41 f
  A2/U8/U1/U1/U1/U2/Y (AND2X1)             0.17       2.58 f
  A2/U8/U1/U1/U1/C (half_adder_5)          0.00       2.58 f
  A2/U8/U1/U1/U2/Y (OR2X1)                 0.25       2.83 f
  A2/U8/U1/U1/C_out (full_adder_3)         0.00       2.83 f
  A2/U8/U1/U2/C_in (full_adder_2)          0.00       2.83 f
  A2/U8/U1/U2/U1/B (half_adder_3)          0.00       2.83 f
  A2/U8/U1/U2/U1/U2/Y (AND2X1)             0.17       3.00 f
  A2/U8/U1/U2/U1/C (half_adder_3)          0.00       3.00 f
  A2/U8/U1/U2/U2/Y (OR2X1)                 0.25       3.26 f
  A2/U8/U1/U2/C_out (full_adder_2)         0.00       3.26 f
  A2/U8/U1/U3/C_in (full_adder_1)          0.00       3.26 f
  A2/U8/U1/U3/U1/B (half_adder_1)          0.00       3.26 f
  A2/U8/U1/U3/U1/U1/Y (XOR2X1)             0.17       3.43 f
  A2/U8/U1/U3/U1/S (half_adder_1)          0.00       3.43 f
  A2/U8/U1/U3/Sum (full_adder_1)           0.00       3.43 f
  A2/U8/U1/Sum[3] (adder_4_1)              0.00       3.43 f
  A2/U8/Sum[7] (adder_8_1)                 0.00       3.43 f
  A2/SUM[7] (asu8_1)                       0.00       3.43 f
  U26/Y (NAND2BX1)                         0.19       3.62 f
  U25/Y (MXI2X1)                           0.50       4.13 r
  U14/Sel (MUX2_1_2)                       0.00       4.13 r
  U14/U1/Y (CLKMX2X2)                      0.42       4.55 r
  U14/Out (MUX2_1_2)                       0.00       4.55 r
  U15/A (MUX2_1_1)                         0.00       4.55 r
  U15/U1/Y (CLKMX2X2)                      0.14       4.69 r
  U15/Out (MUX2_1_1)                       0.00       4.69 r
  Out[7] (out)                             0.00       4.69 r
  data arrival time                                   4.69
  -----------------------------------------------------------
  (Path is unconstrained)


***** End Of Report *****
```

電路延遲時間:4.69(ns)

v. 功率

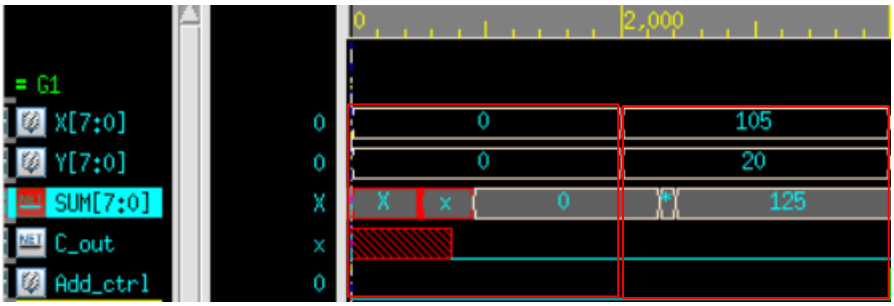
```
----------------------------------------
Report : power
        -analysis_effort low
Design : median
Version: P-2019.03
Date   : Tue Apr 19 02:30:44 2022
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 184.9509 uW   (77%)
  Net Switching Power  =  55.7209 uW   (23%)
                         ---------
Total Dynamic Power    = 240.6718 uW  (100%)

Cell Leakage Power     =   2.2425 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad           0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory           0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box        0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network    0.0000           0.0000              0.0000             0.0000  (   0.00%)
register         0.0000           0.0000              0.0000             0.0000  (   0.00%)
sequential       0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational    0.1850       5.5721e-02          2.2425e+06             0.2429  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total            0.1850 mW    5.5721e-02 mW     2.2425e+06 pW          0.2429 mW

***** End Of Report *****
```

電路總功耗:0.2429(mW)

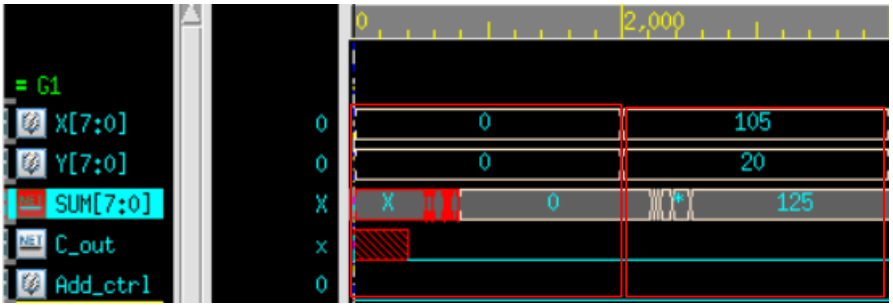
參、Testbench 驗證

一、RCA(1) & CLA(2)

(一)、正數加法



…(1)



…(2)

〈分析一〉

X=0, Y=0, Add_ctrl=0(加法運算), C_out=0(無進位),SUM=0

〈結論一〉

0+0=0，且在[-127,127]範圍內，無溢出和進位。計算結果正確

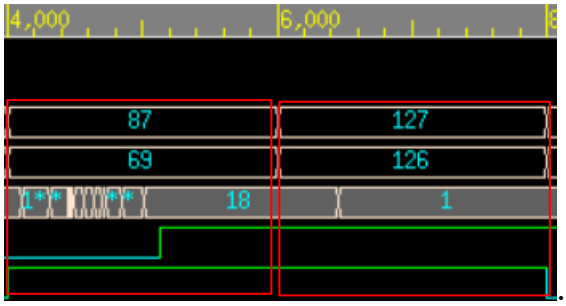
〈分析二〉

X=105, Y=20, Add_ctrl=0(加法運算), C_out=0(無進位),SUM=125

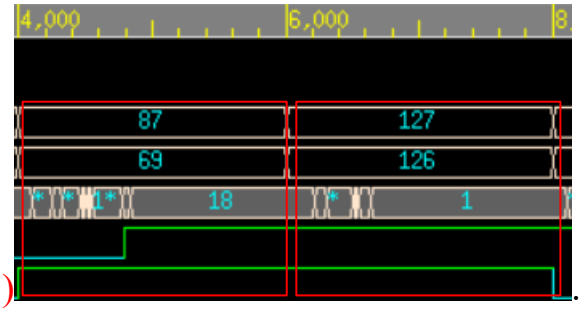
〈結論二〉

105+20=125，且在[-127,127]範圍內，無溢出和進位。計算結果正確

(二)、正數減法



..(1)



..(2)

〈分析一〉

X=87, Y=69, Add_ctrl=1(減法運算), C_out=1(有進位),SUM=18

〈結論一〉

87-69=18，且在[-127,127]範圍內，無溢出，有進位。計算結果正確

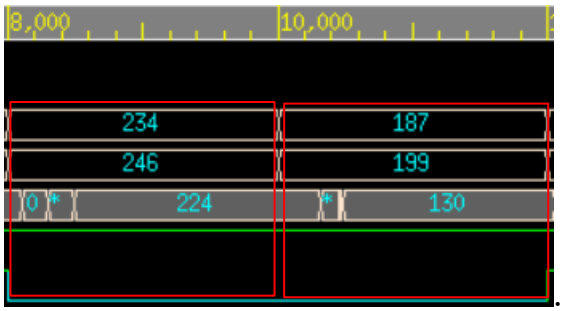
〈分析二〉

X=127, Y=126, Add_ctrl=1(減法運算), C_out=1(有進位),SUM=1

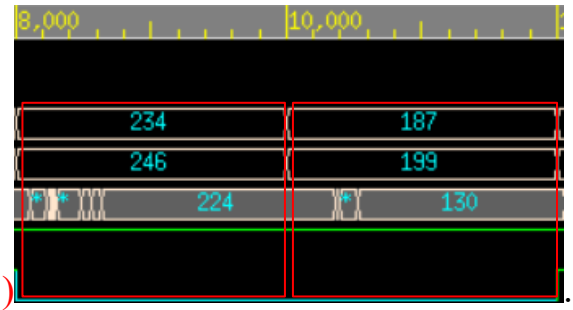
〈結論二〉

127-126=1，且在[-127,127]範圍內，無溢出，有進位。計算結果正確

(三)、負數加法



..(1)



..(2)

〈分析一〉

X=234, Y=246, Add_ctrl=0(加法運算), C_out=1(有進位),SUM=224

X=234，不在[-127,127]範圍內，以負數補數表示→X=234-256=-22

Y=246，不在[-127,127]範圍內，以負數補數表示→Y=246-256=-10

SUM=224，不在[-127,127]範圍內，以負數補數表示→SUM=224-256=-32

〈結論一〉

(-22)+(-10)=-32，且-32 的補數為 256+(-32)=224。計算結果正確

〈分析二〉

X=187, Y=199, Add_ctrl=0(加法運算), C_out=1(有進位),SUM=130

X=187，不在[-127,127]範圍內，以負數補數表示→X=187-256=-69

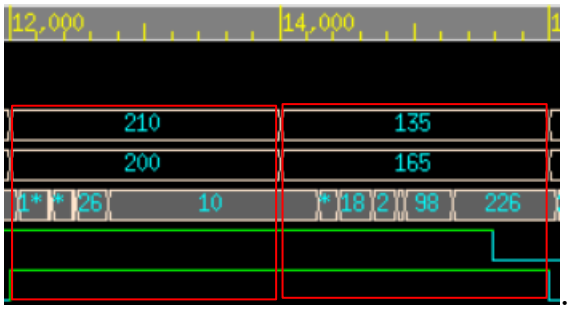
Y=199，不在[-127,127]範圍內，以負數補數表示→Y=199-256=-57

SUM=130，不在[-127,127]範圍內，以負數補數表示→SUM=130-256 = -126

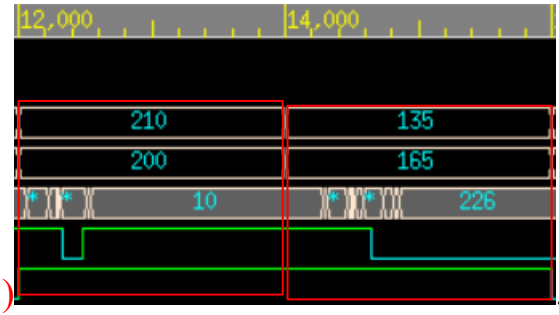
〈結論二〉

(-69)+(-57)=-126，且-126 的補數為 256+(-126)=130。計算結果正確

(四)、負數減法



..(1)



..(2)

〈分析一〉

X=210, Y=200, Add_ctrl=1(減法運算), C_out=1(有進位),SUM=10

X=210，不在[-127,127]範圍內，以負數補數表示→X=210-256=-46

Y=200，不在[-127,127]範圍內，以負數補數表示→Y=200-256=-56

SUM=10，在[-127,127]範圍內

〈結論一〉

(-46)-(-56)=10，無溢出。計算結果正確

〈分析二〉

X=135, Y=165, Add_ctrl=1(減法運算), C_out=1(有進位),SUM=226

X=135，不在[-127,127]範圍內，以負數補數表示→X=135-256=-121

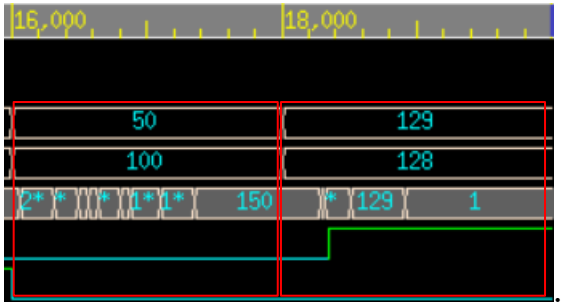
Y=165，不在[-127,127]範圍內，以負數補數表示→Y=165-256=-91

SUM=226，不在[-127,127]範圍內，以負數補數表示→SUM=226-256=-30

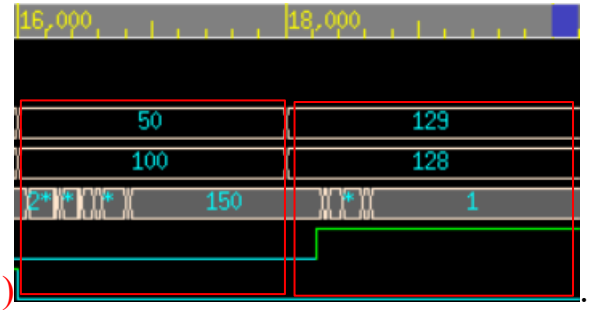
〈結論二〉

(-121)-(-91)=-30，且-30 的補數為 256+(-30)=226。計算結果正確

(五)、溢位



..(1)



..(2)

溢位的情形有兩種，第一種為兩正數相加，其結果超過 127；第二種為兩負數相加，其結果小於-127。當有溢出時，兩正數相加會視為無符號數相加無進位元，而兩負數相加則結果為正補數表示。

〈分析一〉

X=50, Y=100, Add_ctrl=0(加法運算), C_out=0(無進位),SUM=150

X=50，Y=100，在[-127,127]範圍內

SUM=150，不在[-127,127]範圍內，為相加超過 127 的例子

〈結論一〉

50+100=150，不在[-127,127]範圍內，有溢出，視為無符號數相加無進位元。

計算結果正確

〈分析二〉

X=129, Y=128, Add_ctrl=0(加法運算), C_out=1(有進位),SUM=1

X=129，不在[-127,127]範圍內，以負數補數表示→X=129-256=-127

Y=128，不在[-127,127]範圍內，以負數補數表示→Y=128-256=-128

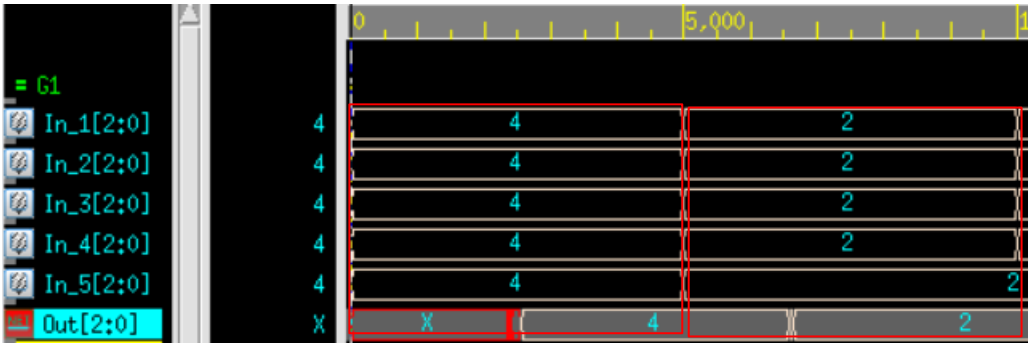
SUM=1，在[-127,127]範圍內，為減超過-127 的例子

〈結論二〉

(-127)+(-128)=-255，不在[-127,127]範圍內，有溢出，結果為正補數表示，-255+256=1。計算結果正確

二、voter

(一) 輸入皆相同



〈分析一〉

In_1=100，In_2=100，In_3=100，In_4=100，In_5=100，Out=100

〈結論一〉

全部輸入皆為 100，輸出結果為 100。計算結果正確

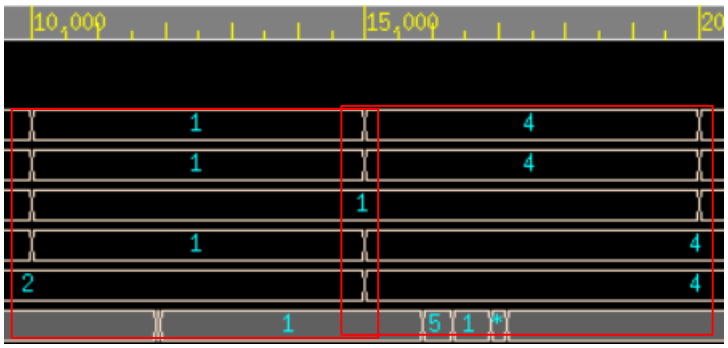
〈分析二〉

In_1=010，In_2=010，In_3=010，In_4=010，In_5=010，Out=010

〈結論二〉

全部輸入皆為 010，輸出結果為 010。計算結果正確

(二)、輸入四同一不同



〈分析一〉

In_1=001，In_2=001，In_3=000，In_4=000，In_5=010，Out=001

〈結論一〉

有四個輸入為 001，數量佔多數，輸出結果為 001。計算結果正確

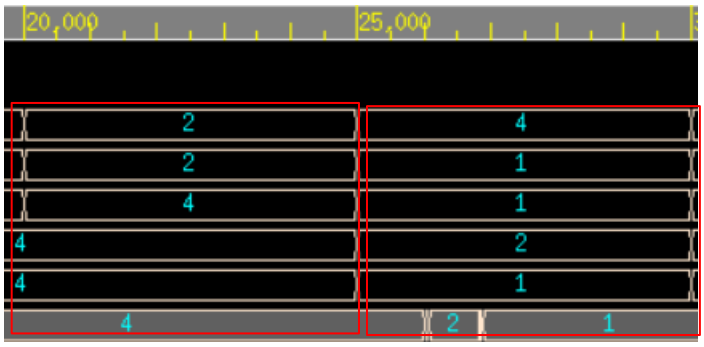
〈分析二〉

In_1=100，In_2=100，In_3=001，In_4=100，In_5=100，Out=100

〈結論二〉

有四個輸入為 100，數量佔多數，輸出結果為 100。計算結果正確

(三)、輸入三個相同



〈分析一〉

In_1=010，In_2=010，In_3=100，In_4=100，In_5=100，Out=100

〈結論一〉

有三個輸入為 100，數量佔多數，輸出結果為 100。計算結果正確

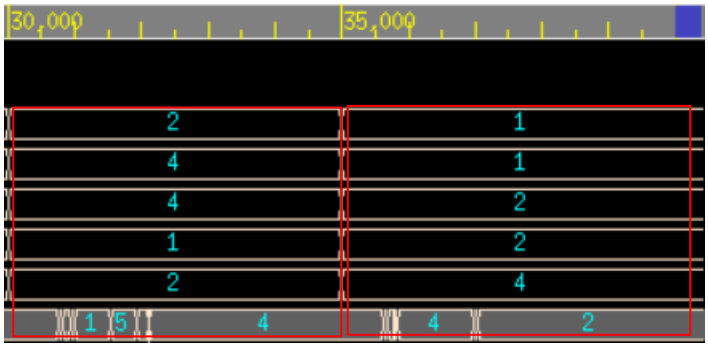
〈分析二〉

In_1=100，In_2=001，In_3=001，In_4=010，In_5=001，Out=001

〈結論二〉

有三個輸入為 001，數量佔多數，輸出結果為 001。計算結果正確

(四)、輸入兩組相同平手



〈分析一〉

In_1=010，In_2=100，In_3=100，In_4=001，In_5=010，Out=100

〈結論一〉

輸入為 100 和 010 的數量相同，100 數值較大，輸出結果為 100。計算結果正確

〈分析二〉

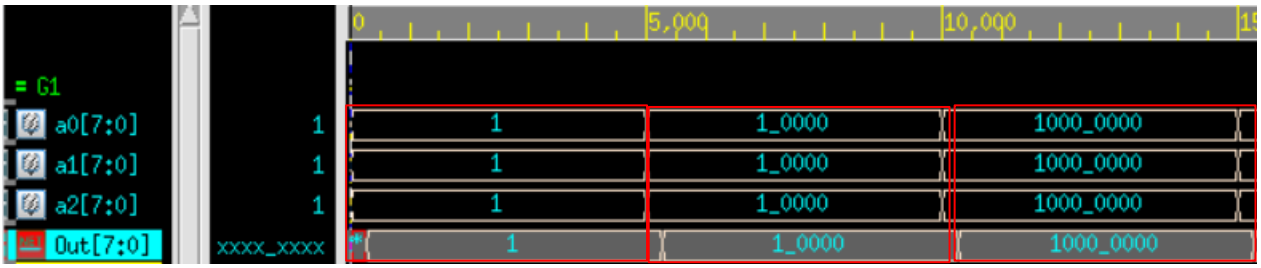
In_1=001，In_2=001，In_3=010，In_4=010，In_5=100，Out=010

〈結論二〉

輸入為 001 和 010 的數量相同，010 數值較大，輸出結果為 010。計算結果正確

三、median

(一)、輸入皆相同



〈分析一〉

a0=00000001，a1=00000001，a2=00000001，Out=00000001

〈結論一〉

輸入皆為 00000001，輸出結果為 00000001。計算結果正確

〈分析二〉

a0=00010000，a1=00010000，a2=00010000，Out=00010000

〈結論二〉

輸入皆為 00010000，輸出結果為 00010000。計算結果正確

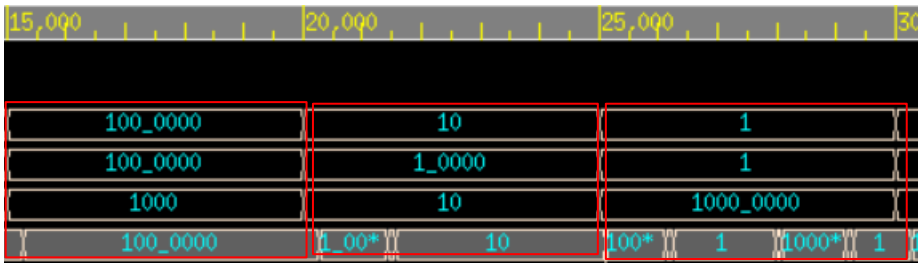
〈分析三〉

a0=10000000，a1=10000000，a2=10000000，Out=10000000

〈結論三〉

輸入皆為 10000000，輸出結果為 10000000。計算結果正確

(二)、輸入兩同一不同



〈分析一〉

a0=01000000，a1=01000000，a2=00001000，Out=01000000

〈結論一〉

有兩個輸入為 01000000，因此中位數為輸入數值相同者，輸出結果為 01000000。計算結果正確

〈分析二〉

a0=00000010，a1=00010000，a2=00000010，Out=00000010

〈結論二〉

有兩個輸入為 00000010，因此中位數為輸入數值相同者，輸出結果為 00000010。計算結果正確

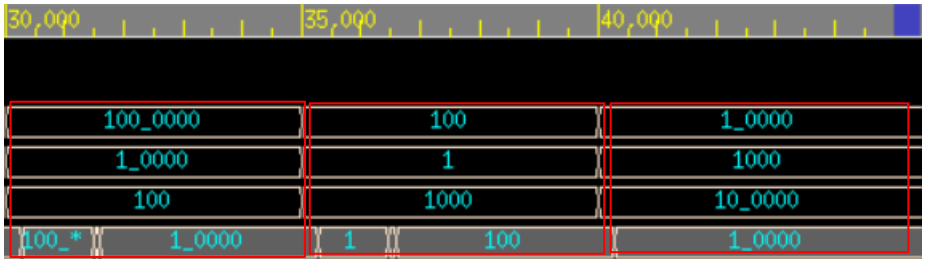
〈分析三〉

a0=00000001，a1=00000001，a2=10000000，Out=00000001

〈結論三〉

有兩個輸入為 00000001，因此中位數為輸入數值相同者，輸出結果為 00000001。計算結果正確

(三)、輸入皆不同



〈分析一〉

a0=01000000，a1=00010000，a2=00000100，Out=00010000

〈結論一〉

中位數為 00010000，輸出結果為 00010000。計算結果正確

〈分析二〉

a0=00000100，a1=00000001，a2=00001000，Out=00000100

〈結論二〉

中位數為 00000100，輸出結果為 00000100。計算結果正確

〈分析三〉

a0=00010000，a1=00001000，a2=00100000，Out=00010000

〈結論三〉

中位數為 00010000，輸出結果為 00010000。計算結果正確

Delay effect

產生 delay effect 的原因在於訊號抵達 output port 的 delay 時間不同所導致，也就是說在最長路徑的訊號計算完成抵達 output port 前，其餘不同路徑的訊號就會先抵達 output port，造成 output 的數值一直產生變動。

肆、問題討論與反思

在這次的邏輯合成實作中最大的困難大概就是要熟悉邏輯合成軟體的操作介面以及流程，起初常常忘記打在 compile design 前後要打的指令，導致必須重新讀檔，不過後來跑過一次流程把所有需要打的指令存成一個腳本檔後，整個邏輯合成的過程就順暢了許多。另外由於前幾次作業需要自己在邏輯閘加上延遲，但卻不能確切知道整個電路在合成過後實際上的延遲，所以在 testbench 設定的 cycle 都比較大，結果合成後的電路再觀察波形時就難以觀察到 delay effect 的現象，因此必須重新設定 testbench 的 cycle 來解決這個問題，不過邏輯合成軟體會自動忽略掉原先設置的邏輯閘延遲，因此往後在做 testbench 模擬時，就可以參照電路最長路徑的延遲時間來設定 testbench 就好，節省了需要在邏輯閘加上延遲的功夫。至於在電路架構的部分，最讓我感到意外的就是 CLA 在邏輯合成後它的面積和延遲都比 RCA 還小，跟之前學到的面積較大，延遲較小的特性不一樣，或許是製程的關係導致，不然在同樣設置及先前的邏輯電路架構下，CLA 的變化應該不會那麼大，這個新發現讓我知道了原先的電路架構在經過邏輯合成的最佳化以及先進製程的加成下，其電路的效能能夠有相當幅度的提升，不過要再有更進一步的提升，仍必須靠我們自己去設計更好的架構和演算法才能達成，這也是將來自己必須去學習和突破的部分。