Digital Lab 2:

Practice of Logic Gate ICs

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Class: 電機二全英班

Group: Group 8

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Lab 2: Practice of Logic Gate ICs

I. Objective

To understand TTL (Transistor-Transistor Logic) digital IC and use of the basic logic gates.

- Basic logic gate : NOT, AND, OR
- Universal logic gate : NOR, NAND
- Bit comparison logic : X-OR, X-NOR

II. Material List

1. IC: 7404, 7408, 7432, 7400, 7402, 7486 (one of each)
2. 330Ω resistor
3. Bread board
4. Single-core cable
5. LED
6. +5V power supply
7. Digital multi-meter

III. Function of Experiment Circuits

According to the truth tables of logic gates, observe the output and input. If the output is logic-1, it is high potential and the LED will be on; if the output is logic-0, it is low potential and the LED will be off.

Please note:

When you use the digital multi-meter to measure voltage, a parallel connection needs to be made with the circuit under test. As for the measurement of current, a series connection must be made.

IV. Electrical Diagram and Illustration

A. Classification of Digital IC

<table>
<tr><td rowspan="10">Digital IC</td><td rowspan="8">Bipolar</td><td rowspan="6">Saturated</td><td rowspan="3">RTL</td><td>DCTL (Direct-Coupled Transistor Logic)</td></tr>
<tr><td>RTL (Resistor-Transistor Logic)</td></tr>
<tr><td>RCTL (Resistor-Capacitor-Transistor Logic)</td></tr>
<tr><td rowspan="2">DTL</td><td>DTL (Diode-Transistor Logic)</td></tr>
<tr><td>HTL (High-Threshold Logic)</td></tr>
<tr><td colspan="2">TTL (Transistor-Transistor Logic)</td></tr>
<tr><td rowspan="2">Unsaturated</td><td colspan="2">ECL (Emitter-coupled Logic)</td></tr>
<tr><td colspan="2">CTL (Complementary Transistor Logic)</td></tr>
<tr><td rowspan="2">Unipolar</td><td colspan="3">MOS (Metal-Oxide-Semiconductor FET)</td></tr>
<tr><td colspan="3">CMOS (Complementary MOS)</td></tr>
</table>

B. Characteristic of TTL IC

- The power supply used in TTL series is DC 5V.
- The voltages of the input and output states "0" and "1" are shown in the table below.

Logic State	Input Voltage	Output Voltage
0	Below 0.8V	Below 0.4V
1	Above 2.0V	Above 2.4V

- SN54 series are guaranteed to work in the temperature range of -55 ℃ ~ 125 ℃
- SN74 series are guaranteed to work in the temperature range of 0 ℃~70 ℃.

C. Identification of Resistor Color Code

1. Number

Black	Brown	Red	Orange	Yellow	Green	Blue	Violet	Grey	White
0	1	2	3	4	5	6	7	8	9

2. Multiplier

Black	Brown	Red	Orange	Yellow	Green	Blue	Violet	Grey	Gold
1	10	100	1K	10K	100K	1M	10M	0.1	0.01

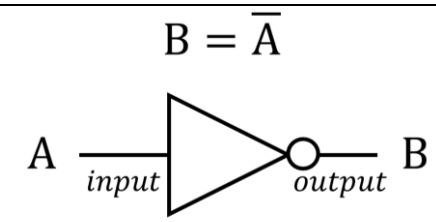
3. Tolerance

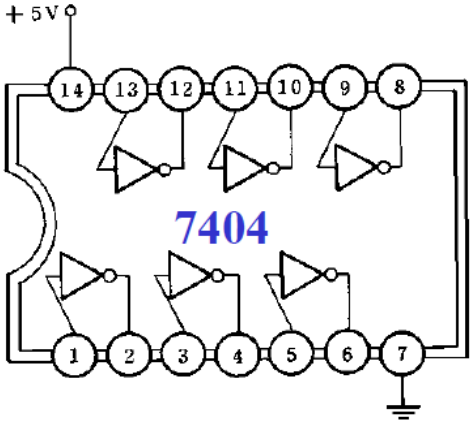
Black	Brown	Red	Green	Violet	Gold
1	10	100	100K	10M	0.01

D. Experiment Procedure

1. NOT Gate

Input A	Output B	Output Voltage Level
0		
1		

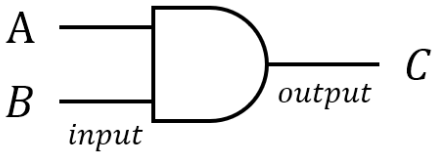


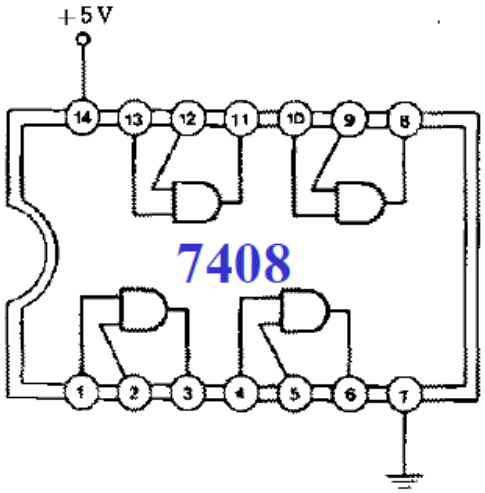


2. AND Gate

Input A	Input B	Output C	Output Voltage Level
0	0		
0	1		
1	0		
1	1		

$$C = A \cdot B$$

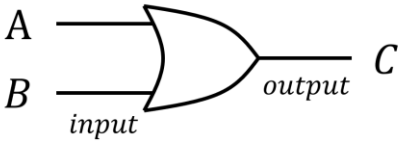


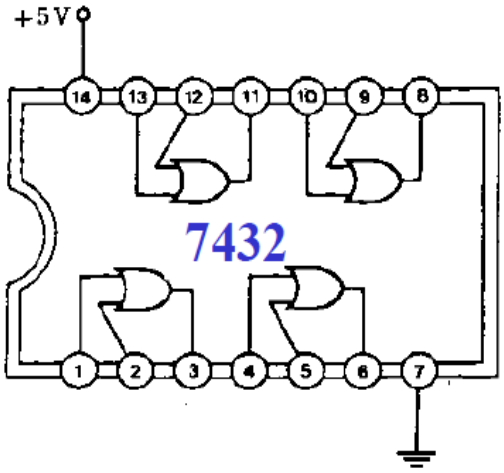


3. OR Gate

Input A	Input B	Output C	Output Voltage Level
0	0		
0	1		
1	0		
1	1		

$$C = A + B$$

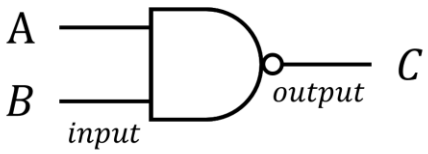


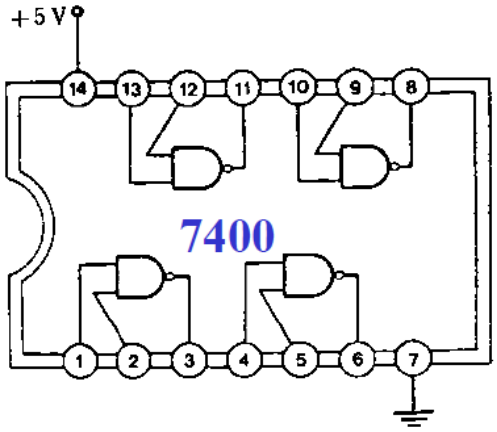


4. NAND Gate

Input A	Input B	Output C	Output Voltage Level
0	0		
0	1		
1	0		
1	1		

$$C = \overline{A \cdot B}$$

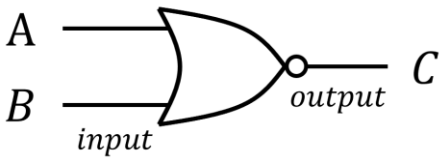


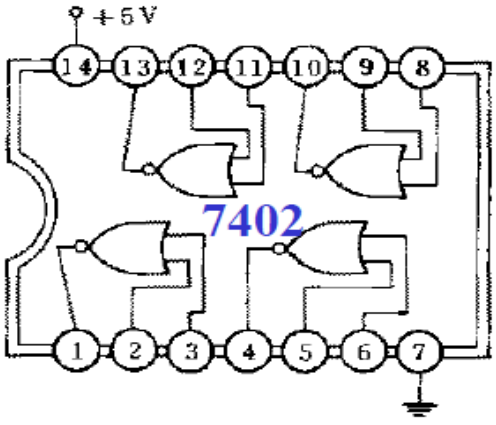


5. NOR Gate

Input A	Input B	Output C	Output Voltage Level
0	0		
0	1		
1	0		
1	1		

$$C = \overline{A + B}$$

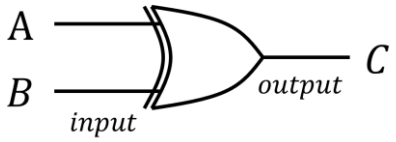


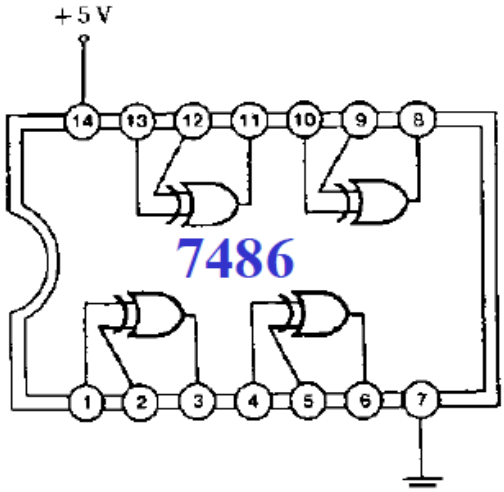


6. XOR Gate

Input A	Input B	Output C	Output Voltage Level
0	0		
0	1		
1	0		
1	1		

$$C = \mathrm{A} \oplus \mathrm{B} = \overline{A} \cdot \mathrm{B} + A \cdot \overline{B}$$



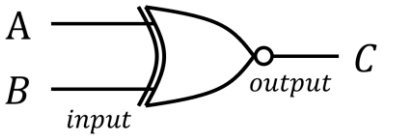


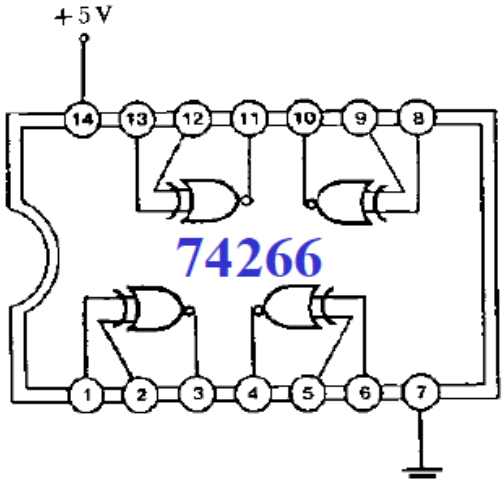
7. XNOR Gate

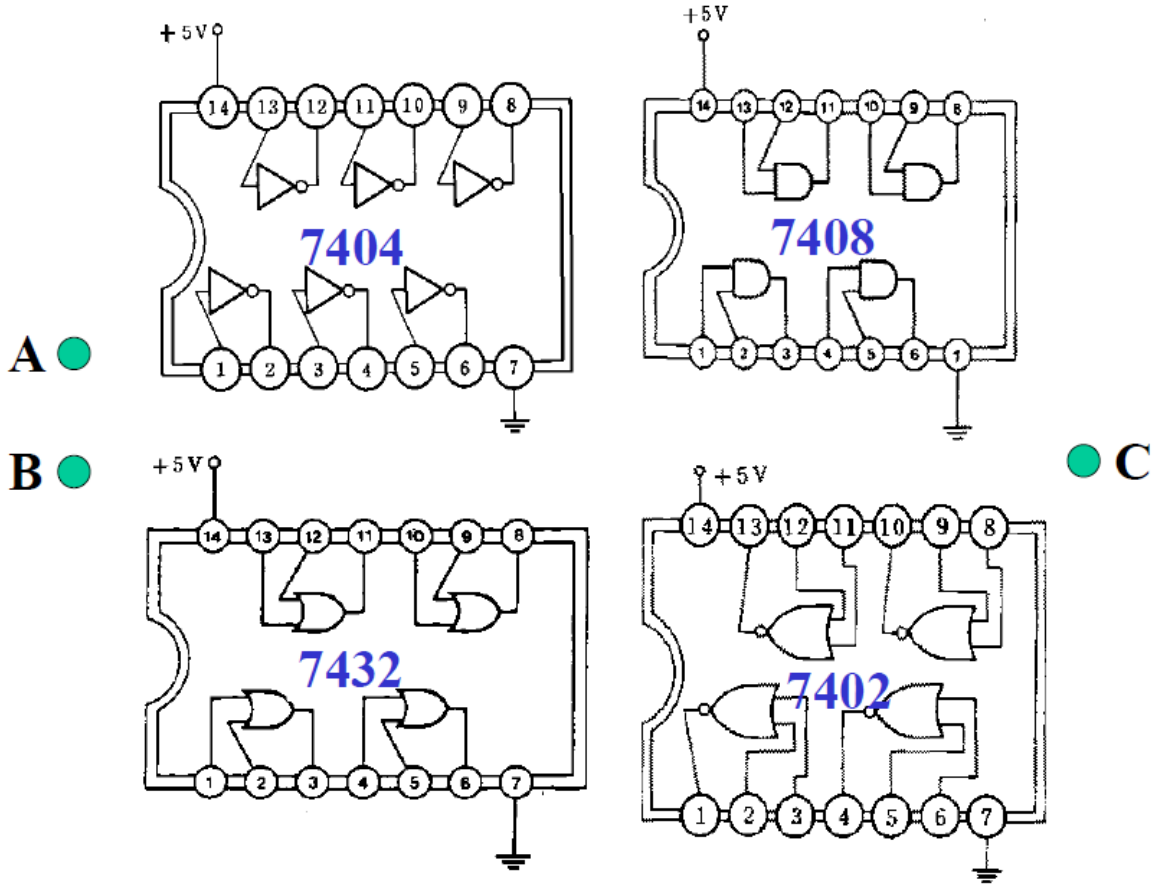
- Please connect a 330Ω resistor and an LED light in series to the output part.
- The 74266 IC is not prepared for this experiment. Please use other ICs such as 7402, 7404, 7408 or 7432 to implement the same function as the XNOR gate (74266) and draw your wiring diagram (note: not all ICs may be used).

Input A	Input B	Output C	Output Voltage Level
0	0		
0	1		
1	0		
1	1		

$$C = \overline{\mathrm{A} \oplus \mathrm{B}} = \overline{\overline{A} \cdot \mathrm{B} + A \cdot \overline{B}}$$







8. Use NOR gates to implement basic logic gates.

- Please connect a 330Ω resistor and an LED light in series to the output part.

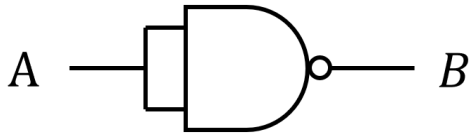
(1) Please use the NOR gate(s) to implement the same function as the NOT gate. Draw your wiring diagram and record the experimental results based on the truth table.

(2) Please use the NOR gate(s) to implement the same function as the AND gate. Draw your wiring diagram and record the experimental results based on the truth table.

(3) Please use the NOR gate(s) to implement the same function as the OR gate. Draw your wiring diagram and record the experimental results based on the truth table.

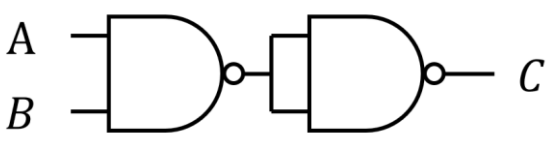
V. Reference:

- Using the NAND gate to implement the same function as the NOT gate.



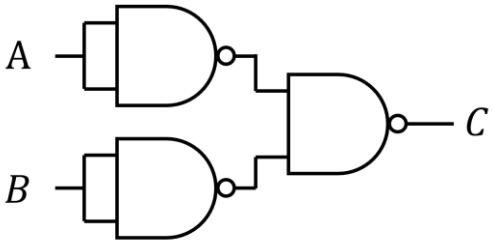
$$B = \overline{A \cdot A} = \overline{A}$$

- Using the NAND gate to implement the same function as the AND gate.



$$C = \overline{\overline{A \cdot B} \cdot \overline{A \cdot B}} = \overline{\overline{A \cdot B}} = A \cdot B$$

- Using the NAND gate to implement the same function as the OR gate.



$$C = \overline{\overline{A \cdot A} \cdot \overline{B \cdot B}}$$
$$= \overline{\overline{A} \cdot \overline{B}} = A + B$$

VI. Checking Items:

A. Each team member must implement the circuits and make measurement. Those teams who have completed the experiments must ask a TA to check, and the TA will ask one of the team members to repeat the experiments and verify the results.

B. After completing the experiments, all the components must be sorted (placed in the material box), the wires should be returned, and the **instrument should be turned off**. Clean up the seat and turn off the extension cord switch. **After completion, you must ask a TA to check if you can leave.**

VII. Precautions:

A. The IC is placed with the notch facing left, corresponding to the IC pin diagram, and each IC must be biased (VCC is connected to +5V, GND is connected to ground).

B. When measuring voltage or current, start from the large scale, and then turn it down gradually to avoid damage to the meter.

C. If you have any questions during the experiment, please feel free to raise your hand and ask TAs at any time.

D. Everyone needs to submit the report of this experiment.

VIII. Test Result

1. NOT Gate (7404)

Input A	Output B	Output Voltage Level
0	1	4.444V
1	0	0.066V

2. AND Gate (7408)

Input A	Input B	Output C	Output Voltage Level
0	0	0	0.039V
0	1	0	0.039V
1	0	0	0.039V
1	1	1	4.437V

3. OR Gate (7432)

Input A	Input B	Output C	Output Voltage Level
0	0	0	0.050V
0	1	1	4.438V
1	0	1	4.434V
1	1	1	4.437V

4. NAND Gate (7400)

Input A	Input B	Output C	Output Voltage Level
0	0	1	4.452V
0	1	1	4.453V
1	0	1	4.457V
1	1	0	0.037V

5. NOR Gate (7402)

Input A	Input B	Output C	Output Voltage Level
0	0	1	4.447V
0	1	0	0.040V
1	0	0	0.040V
1	1	0	0.036V

6. XOR Gate (7486)

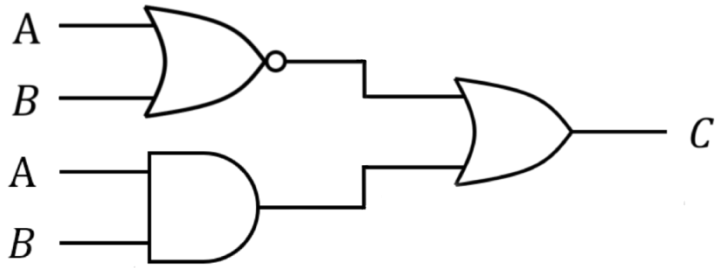
Input A	Input B	Output C	Output Voltage Level
0	0	0	0.041V
0	1	1	4.421V
1	0	1	4.418V
1	1	0	0.046V

7. XNOR Gate

$$C = \overline{A \oplus B} = \overline{\overline{A} \cdot B + A \cdot \overline{B}}$$

$$= (A + \overline{B}) \cdot (\overline{A} + B) = A \cdot \overline{A} + \overline{B} \cdot \overline{A} + A \cdot B + \overline{B} \cdot B$$

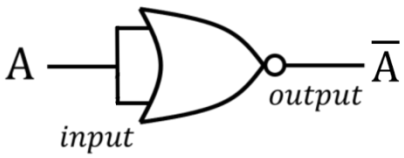
$$= \overline{B} \cdot \overline{A} + A \cdot B = \overline{A + B} + A \cdot B \text{ (NOR) (OR) (AND)}$$



Input A	Input B	Output C	Output Voltage Level
0	0	1	4.431V
0	1	0	0.051V
1	0	0	0.051V
1	1	1	4.432V

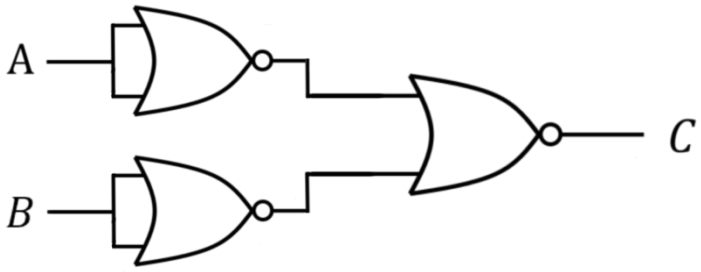
8.

(1) $\overline{A + A} = \overline{A}$



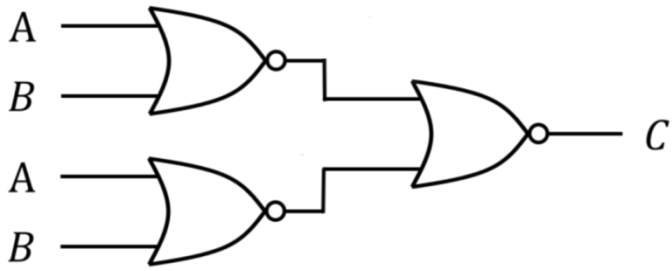
Input A	Output B	Output Voltage Level
0	1	4.402V
1	0	0.036V

(2) $\overline{\overline{A+A}+\overline{B+B}} = \overline{\overline{A}+\overline{B}} = A \cdot B$



Input A	Input B	Output C	Output Voltage Level
0	0	0	0.035V
0	1	0	0.040V
1	0	0	0.040V
1	1	1	3.388V

(3) $\overline{\overline{A+B}+\overline{A+B}} = \overline{\overline{A+B}} = A + B$



Input A	Input B	Output C	Output Voltage Level
0	0	0	0.035V
0	1	1	3.389V
1	0	1	3.389V
1	1	1	3.389V

IX. Problem discussion

We encountered problem when we conduct the experiment of NOR Gate (7402): the output is not the same as we expected. We were confused at first and checked our circuit connection several times, but in no vain. After we asked for TA's help, we found that the only problem is that the pins of 7402 are set in opposite direction compare to other ICs. We have to be much more careful when connecting circuits of NOR Gate.

Nevertheless, we forgot to bring the probe of our multimeters, instead, we used clips to measure the voltage. Although clips can also be used to measure,

the statistics are not as accurate as probes did. At the end, to get more proper statistics, we borrow probes from TA.

X. Review of the experiment

During the logic gate experiment, my group-mate and I gained a deeper understanding of digital electronics and their applications in computing . We were able to construct several different types of logic gates, including AND, OR, NOT, NAND, and NOR gates, and observe how they functioned when presented with different input combinations.

We also had the opportunity to work with integrated circuits (ICs), which made it much easier to construct more complex circuits. Using ICs, we could simply connect the inputs and outputs of the ICs instead of having to build each individual gate from scratch.

In addition to using ICs, we utilized Karnaugh maps (K-maps) to simplify the logic circuits. K-maps are graphical tools used to minimize Boolean expressions and reduce the number of gates required in a circuit. By identifying groups of adjacent 1s in the truth table, we were able to simplify the Boolean expression and reduce the number of gates required to implement the circuit.

Throughout the experiment, we faced challenges in troubleshooting issues with the circuits when they didn't produce the expected output. This required a combination of analytical thinking and hands-on experimentation to identify where the problem was occurring and make the necessary adjustments.

In conclusion, the logic gate experiment was a valuable learning experience that deepened our understanding of digital electronics and their practical applications. We would like to thank our group members and the teaching assistants for their support throughout the experiment.