National Sun Yat-sen University
Department of Electrical Engineering

112-1 Practical Digital System Design

HW4 Traffic Light Controller

Name: 胡庭翊

Student ID: B103015006

I. Algorithm

1. Sync Counter

a. How to Design

To make a counter, I need to be assured that it can be controlled not only by the clock but also inputs of reset and enable.
The states needed to be changed with the clock, so that the waiting time for each state would depend on the frequency of the clock itself.
Also, it should have the function of car detection to control whether the converting process conduct or not, lastly, it should have a function of reset so as it can be used to be manually controlled.

b. Features

A counter in this circuit can help user notice current state, and it will also be easier for user to modify the operation time for each states: i.e. if user wishes to have a shorter or longer time of state-convert.

c. Operation Method

The input should be reset, enable, and clock for 1 bit of each, and the output should be the current state after convert, so as it can be used in the latter module. The size of state should be 3 bits since we have 8 temporary states: ST0, ST1, ST2, ST3, ST4, ST5, ST6, ST7.

Triggered at every positive edge of clock, if there is car on the farm road being detected, then the convert process will be started, current state=ST0, and the state will +1 in every positive edge clock. However, if reset=1, than current state will be set to ST0 no matter enable is 1 or not.
Last but not last, when enable=0, the convert process will be stopped.

2. Traffic Light Controller

a. How to Design

To make a traffic light controller, I need to make sure that it can be controlled by a counter, and then output the states of traffic light on highway and farm road.
The states of traffic lights are red light, yellow light, and green light, which means, to operate a traffic light control circuit, we should have 6 different types of outputs.
Also, it should be known that red light, yellow light, and green light cannot happen at both side of the roads, otherwise, it may caused car accidents.

b. Features

By controlling 2 sides of traffic light together, we can avoid nonsense situation from happens, which is, two same lights happens at the same time. Moreover, we can easily control both traffic light system and force them to be controlled at the same time, there won't be any chances that two traffic light system operate under different clocks.

c. Operation Method

When there are cars on farm road, an ideal state convert of me is:

High way: green light; Farm road: red light.
(If there are cars on farm road:)
High way: green light; Farm road: red light.
High way: yellow light; Farm road: red light.
High way: red light; Farm road: yellow light.
High way: red light; Farm road: green light.

(Wait for 5 clocks for car to pass.)
(Then convert back to highway again.)

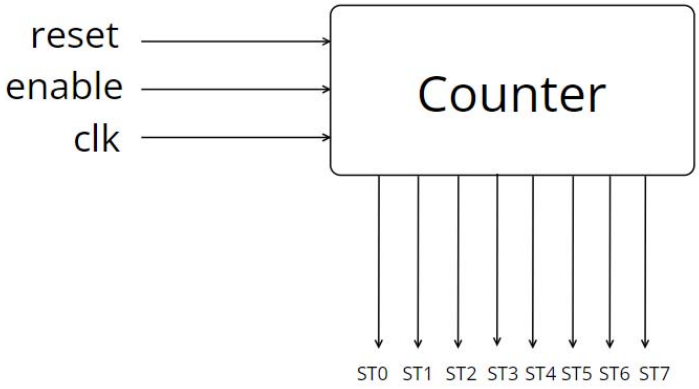
High way: red light; Farm road: yellow light.
High way: yellow light; Farm road: red light.

High way: green light; Farm road: red light.

(Wait for 5 clocks for car to pass.)
(Detect if there is any car on farm road again)
(If yes, then transfer the traffic light states again.)
(If no, high way traffic light will remain green while farm road remain red.)

II. Circuit Architecure

1. Sync Counter

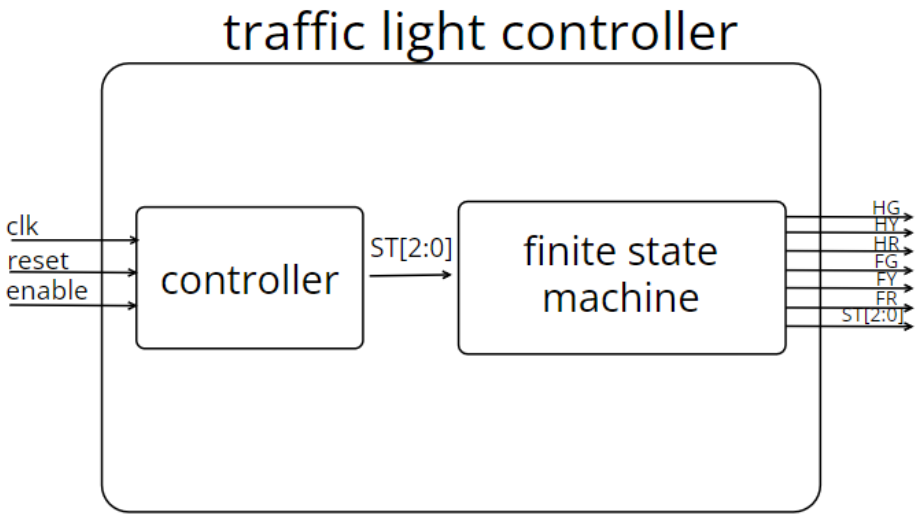


The counter will count+1 at every cycle of clock, and will be reset if reset=1, start counting when enable=1.

When counter count to 0, it outputs ST0;
when counter count to 1, it outputs ST1;
when counter count to 2, it outputs ST2;
when counter count to 3, it outputs ST3;
when counter count from 4~8, it outputs ST4;
when counter count to 9, it outputs ST5;
when counter count to 10, it outputs ST6;
when counter count to 11~15, it outputs ST7.

After a cycle, the counter will count to 0 again.

2. Communication



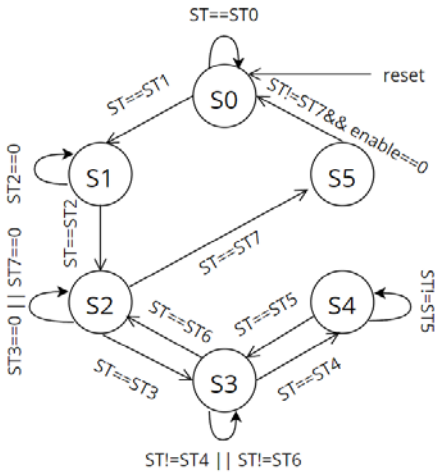
Here, the meaning of the output state of counter is:

ST0: State of S0 in finite state machine;
ST1: State of S1 in finite state machine;
ST2: State of S2 in finite state machine;
ST3: State of S3 in finite state machine;
ST4: State of S4 in finite state machine;
ST5: State of S3 in finite state machine;
ST6: State of S2 in finite state machine;
ST7: State of S5 in finite state machine.

The reason why here we have multiple assignments to the same output state is that, although we have a total number of 8 states, some of them are actually repeated. In order to simplify and smaller our area, here we assign and tidy them up together.

3. Traffic Light Controller

The traffic light controller is composed of a counter and a finite state machine.
The state diagram of the finite state machine is as follow:



The meaning of each state in finite state machine is:

S0: Highway green light; Farm road: red light.
(This is the initial state when there is no car on farm road.)

S1: Highway green light; Farm road: red light.
(There is car on farm road, the counter starts to count.)

S2: Highway yellow light; Farm road: red light.

S3: Highway red light; Farm road: yellow light.

S4: Highway red light; Farm road: green light.

S5: Highway green light; Farm road: red light.

Where HR means highway red light, HY means highway yellow light, HG means highway green light; FR means farm road red light, FY means farm road yellow light, FG means farm road green light.

III. Synthesis Process

1. Check Setup File

First open XShell and cd to our target folder, check the folder in which the design compiler is to be executed contains the .synopsys_dc.setup file by typing 'ls –a'.

```
soc08 [~/HW4_B103015006]
-PDSD112a20- $ls -a
./                              ncverilog.history    traffic_light.sdf
../                             ncverilog.log        traffic_light.sdf.X
command.log                     novas_dump.log       traffic_light_syn.v
default.svf                     .synopsys_dc.setup   traffic_light.v
filenames_80820_D20231209.log   tb_traffic_light.v   tsmc13.v
INCA_libs/                      traffic_light.fsdb
```

2. Invoke Design Compiler

Type 'dv' to invoke the design compiler.

```
soc08 [~/HW4_B103015006]
-PDSD112a20- $dv

                          Design Compiler Graphical
                                DC Ultra (TM)
                                 DFTMAX (TM)
                             Power Compiler (TM)
                                DesignWare (R)
                                DC Expert (TM)
                              Design Vision (TM)
                              HDL Compiler (TM)
                              VHDL Compiler (TM)
                                 DFT Compiler
                              Design Compiler(R)

                Version P-2019.03 for linux64 - Feb 27, 2019

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s
 of a written license agreement with Synopsys, Inc. All other use, reproduction
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            or distribution of this software is strictly prohibited.
Initializing...
Initializing gui preferences from file  /home/PDSD112/PDSD112a20/.synopsys_dv_p
refs.tcl
design_vision> 4.1
design_vision>
```
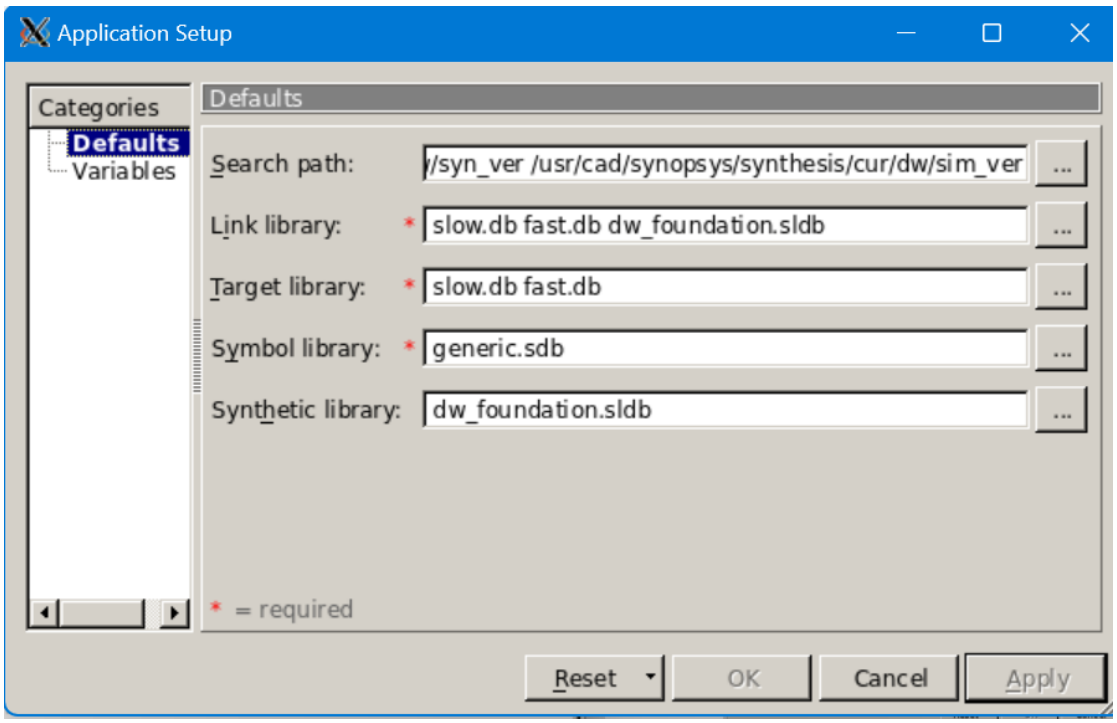
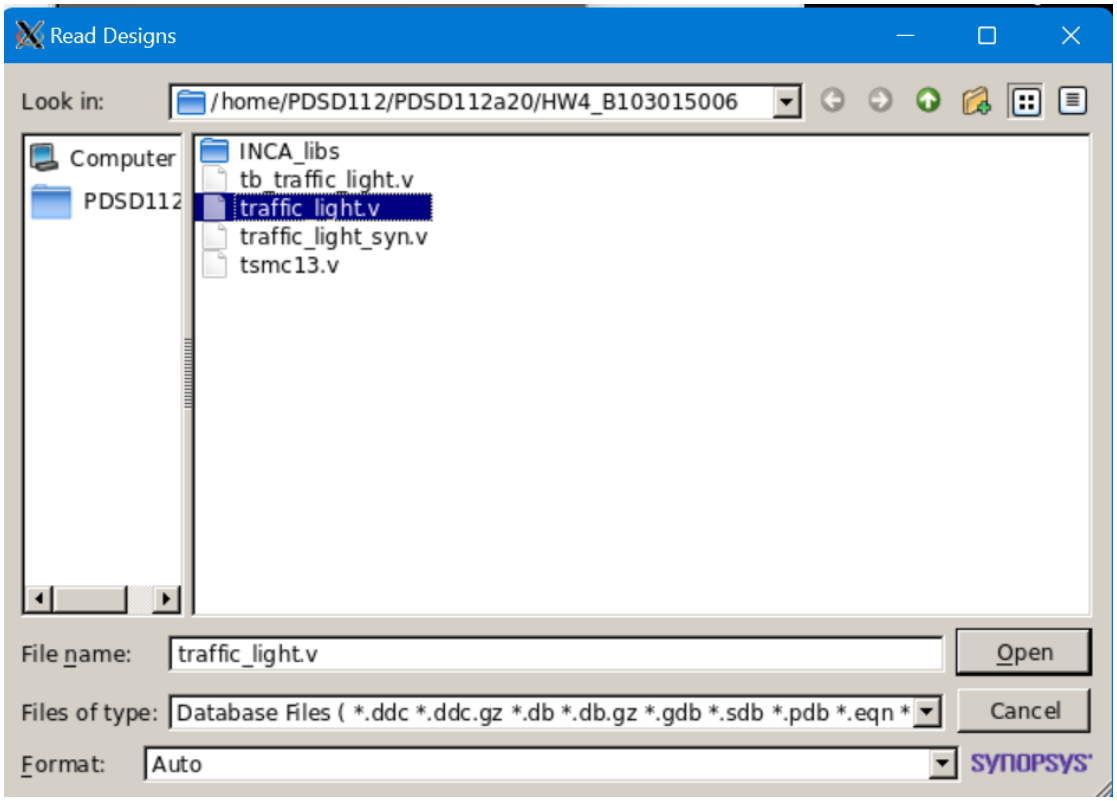

3. Check if library is correctly loaded



The library is correctly loaded.

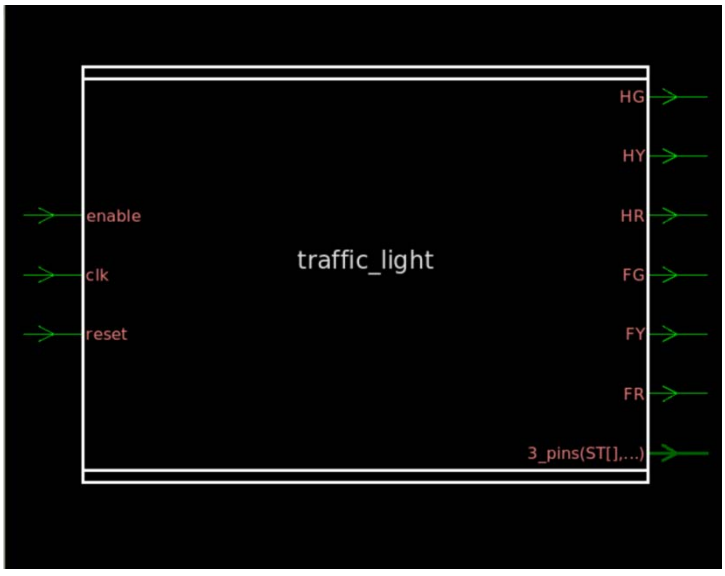
4. Read file



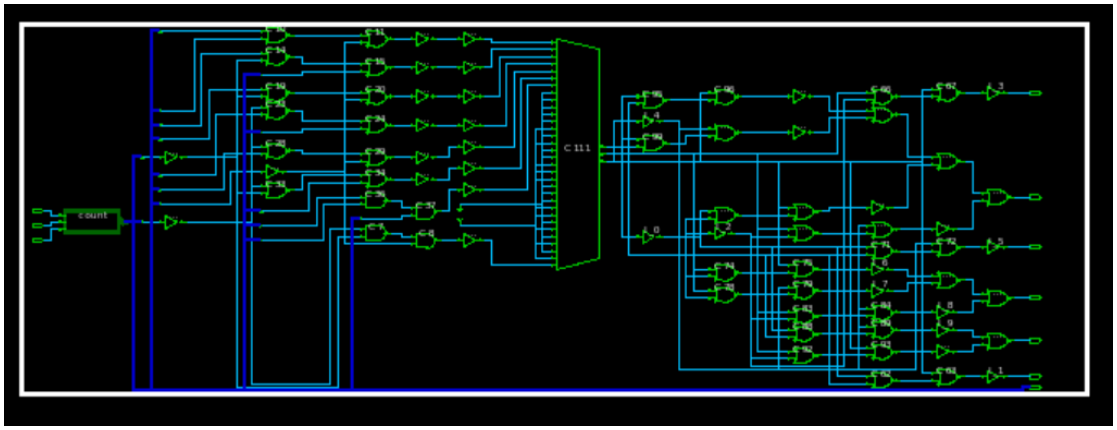
Check if any errors or warnings appear.
The design is correctly read without latches.

```
Statistics for case statements in always block at line 14 in file
        '/home/PDSD112/PDSD112a20/HW4_B103015006/traffic_light.v'
===============================================
|           Line           |  full/ parallel  |
===============================================
|            15            |    auto/auto     |
===============================================

Statistics for case statements in always block at line 59 in file
        '/home/PDSD112/PDSD112a20/HW4_B103015006/traffic_light.v'
===============================================
|           Line           |  full/ parallel  |
===============================================
|            60            |    auto/auto     |
===============================================

Inferred memory devices in process
        in routine counter line 46 in file
                '/home/PDSD112/PDSD112a20/HW4_B103015006/traffic_light.v'.
=============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
=============================================================================
|      count_reg      | Flip-flop |   5   |  Y  | N  | N  | N  | N  | N  | N  |
=============================================================================
Presto compilation completed successfully.
Current design is now '/home/PDSD112/PDSD112a20/HW4_B103015006/traffic_light.db:traffic_li
Loaded 2 designs.
Current design is 'traffic_light'.
design_vision>
Current design is 'traffic_light'.
```

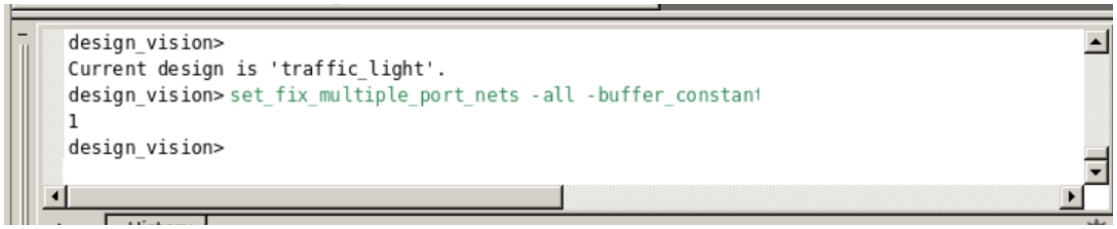
5. Symbol View



6. Schematic View

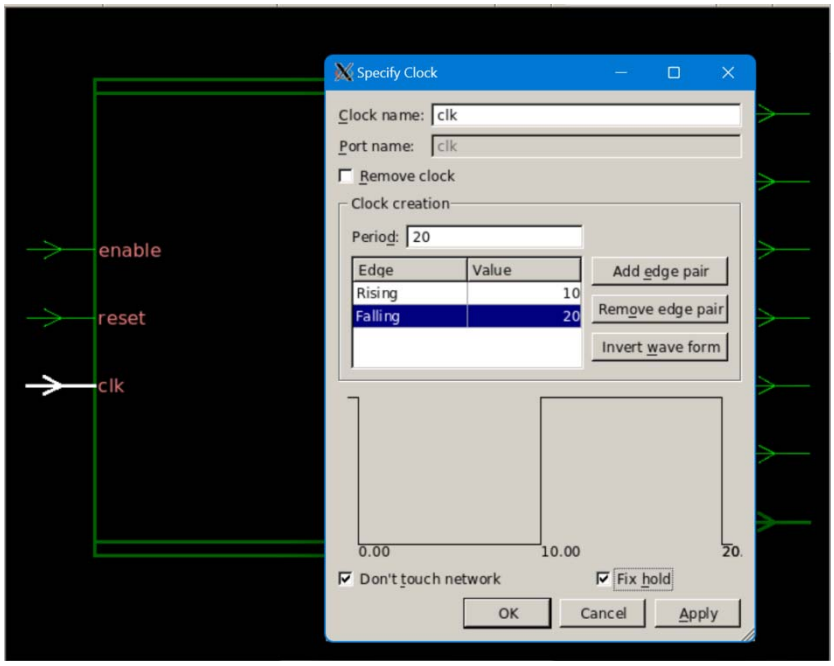


7. Prevent Possible Assign Statement Problem



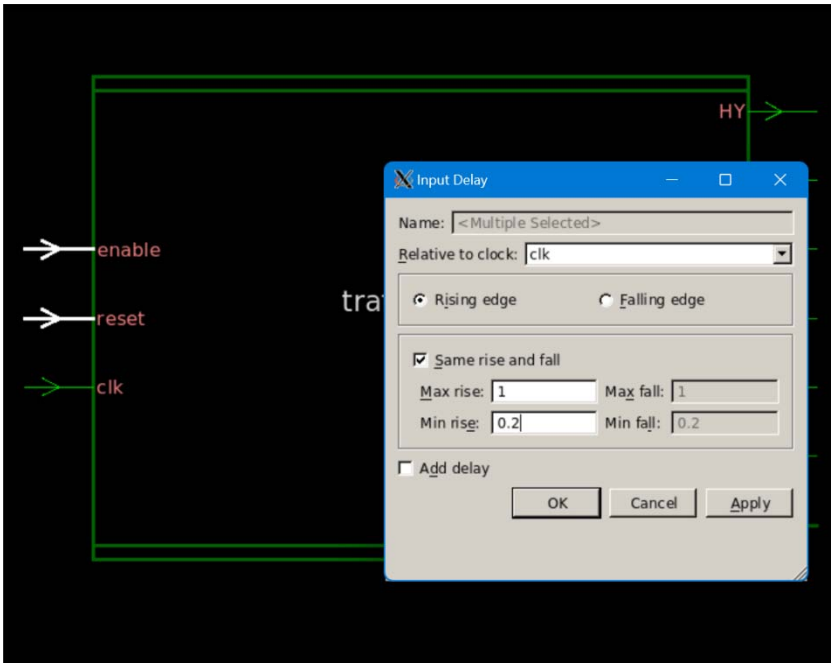
Type ‘set_fix_multiple_port_nets -all -buffer_constants’ in the command line.

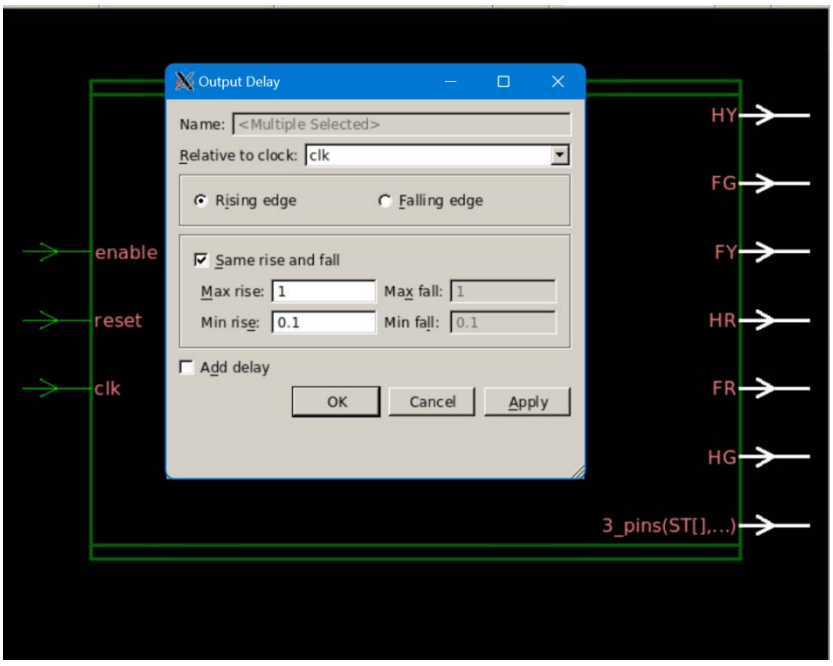
8. Specify Clock



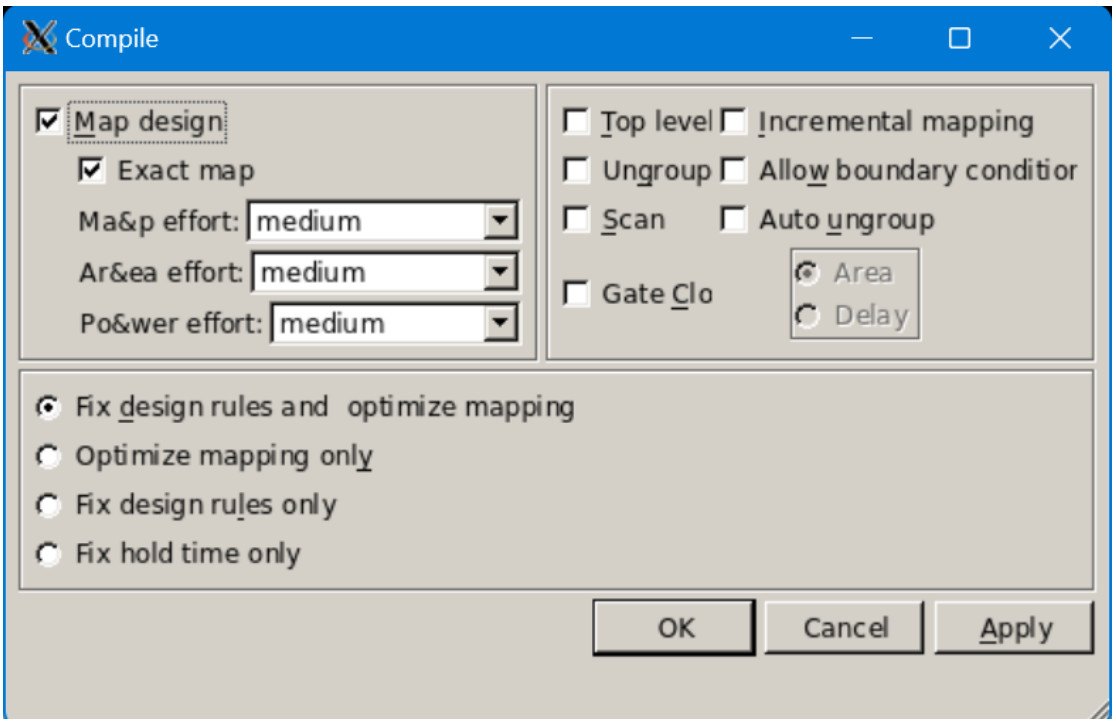
9. Set Input/Output Delay

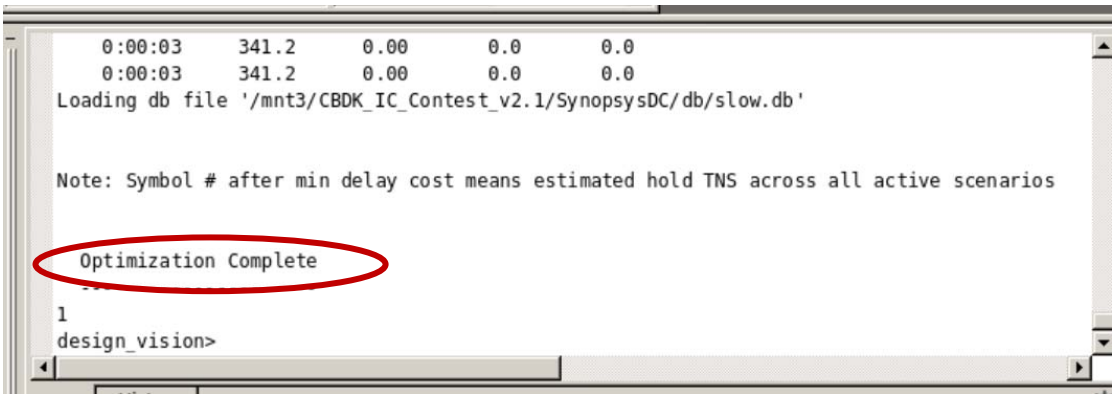
Attribute→Operating Environment
Select the input and output pins respectively and set the min and max rise time.





10. Compile Design

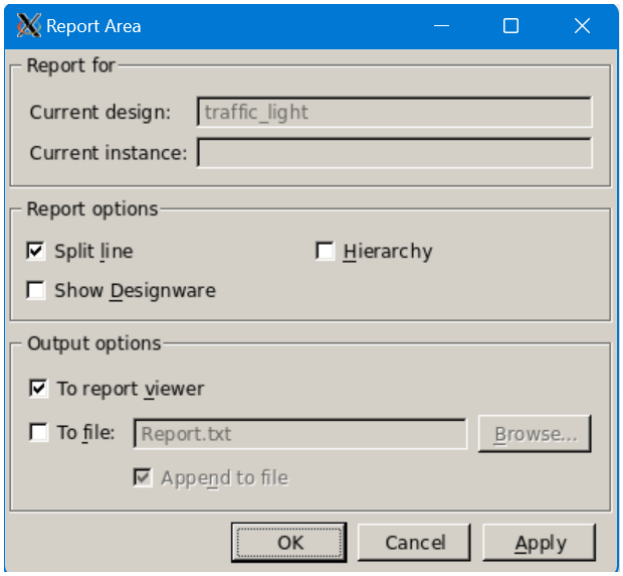




The compile process completed successfully.
Enter ‘change_names -hierarchy -rule verilog’ in the command line in order to remove assign in the circuit.

11. Area Report

Design→Report Area



The output result of the area report will be shown as below.

```
****************************************
Report : area
Design : traffic_light
Version: P-2019.03
Date   : Sun Dec 10 02:22:39 2023
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                           18
Number of nets:                            43
Number of cells:                           30
Number of combinational cells:             24
Number of sequential cells:                 5
Number of macros/black boxes:               0
Number of buf/inv:                          3
Number of references:                       8

Combinational area:               196.898402
Buf/Inv area:                      10.184400
Noncombinational area:            144.279003
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  341.177405
Total area:                 undefined

***** End Of Report *****
```

Unit: um × um

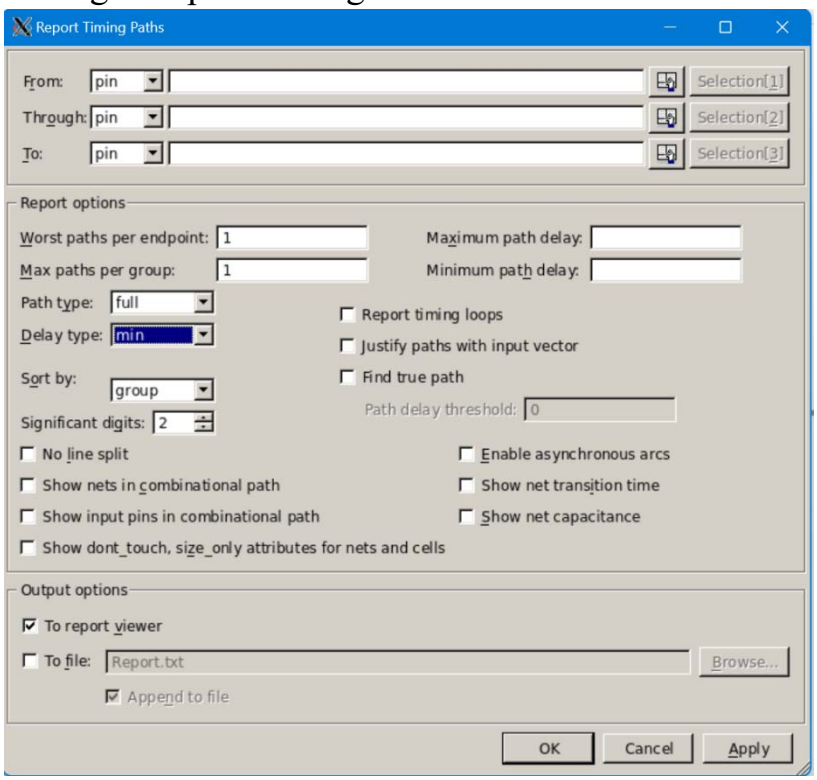
Gate count = reported area/ area of a NAND2 gate

Area of a NAND2 gate is approximately:

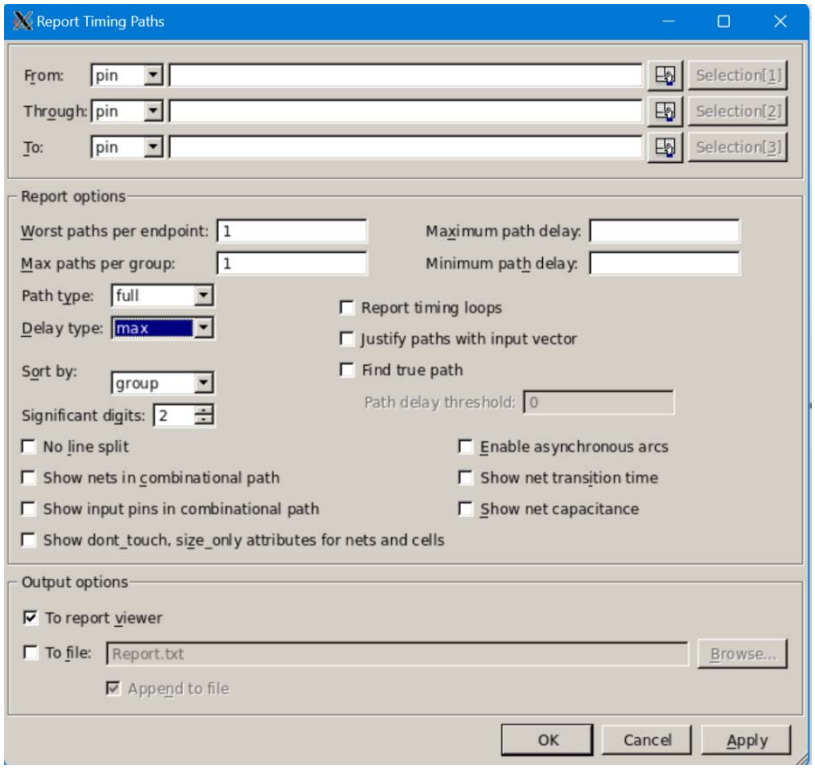
- 5 um × um for a 0.13um technology
- 10 um × um for a 0.18um technology

12. Timing Report

Timing→Report Timing Path



Set delay time to max to see the information of setup time.



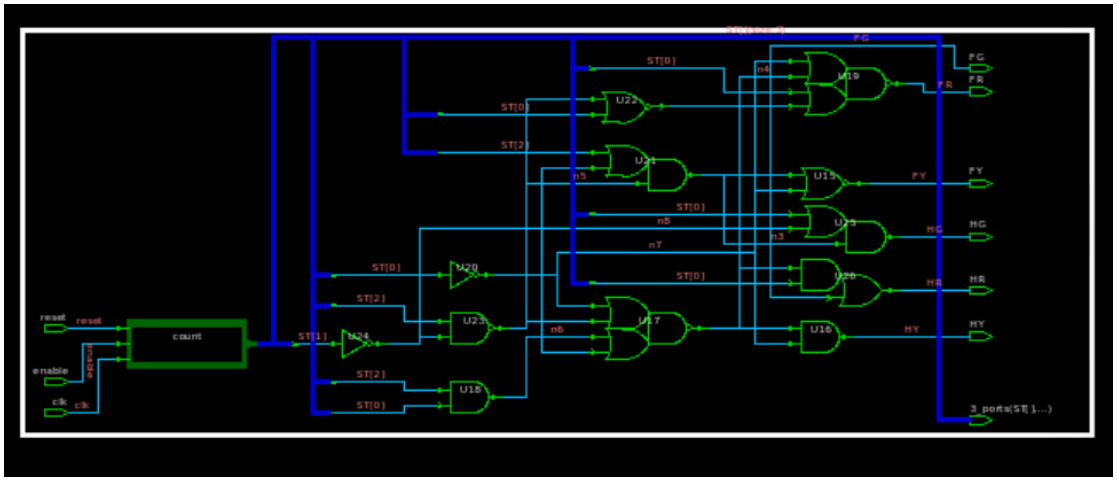
Set delay time to min to see the information of hold time.

The output result of the timing report will be shown as below.

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
         -sort_by group
Design : traffic_light
Version: P-2019.03
Date   : Sun Dec 10 02:29:54 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: count/count_reg_2_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: HR (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  count/count_reg_2_/CK (DFFTRX1)          0.00      10.00 r
  count/count_reg_2_/Q (DFFTRX1)           0.52      10.52 f
  count/U8/Y (NAND2X1)                     0.12      10.64 r
  count/U3/Y (AOI21X1)                     0.14      10.78 f
  count/ST[0] (counter)                    0.00      10.78 f
  U18/Y (AND2X2)                           0.19      10.97 f
  U17/Y (OAI22XL)                          0.30      11.27 r
  U26/Y (AO21X1)                           0.20      11.47 r
  HR (out)                                 0.00      11.47 r
  data arrival time                                  11.47

  clock clk (rise edge)                   30.00      30.00
  clock network delay (ideal)              0.00      30.00
  output external delay                   -1.00      29.00
  data required time                                 29.00
  -----------------------------------------------------------
  data required time                                 29.00
  data arrival time                                 -11.47
  -----------------------------------------------------------
  slack (MET)                                        17.53


***** End Of Report *****
```

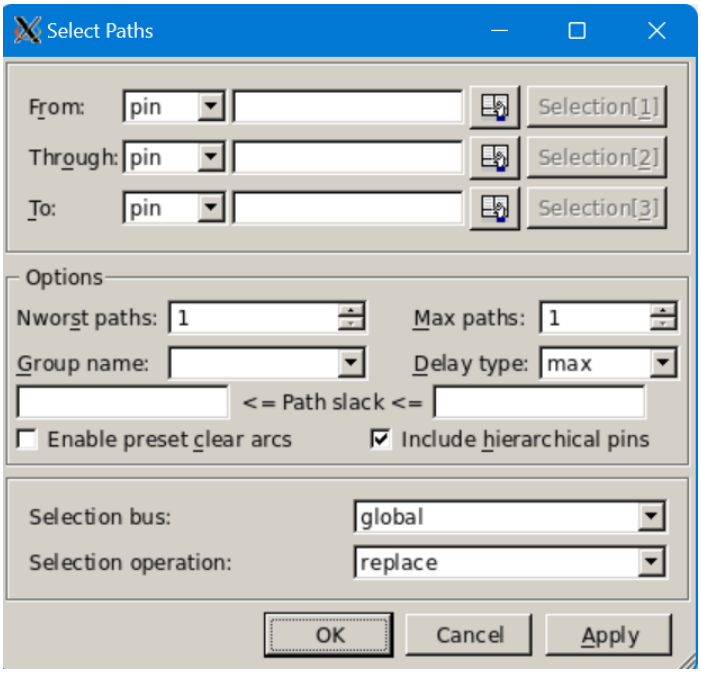
13. Critical Path Highlight

Following is the circuit after compiled:

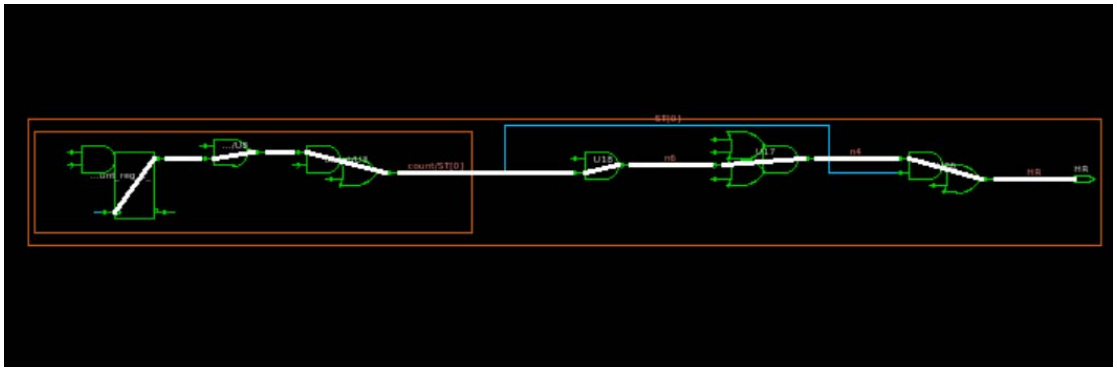


One of the methods is: Select->Paths From/Through/to

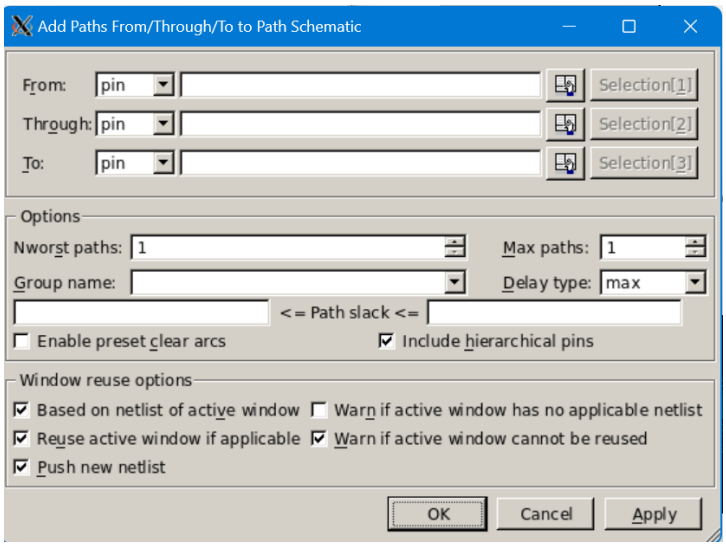
We set the delay type to max.



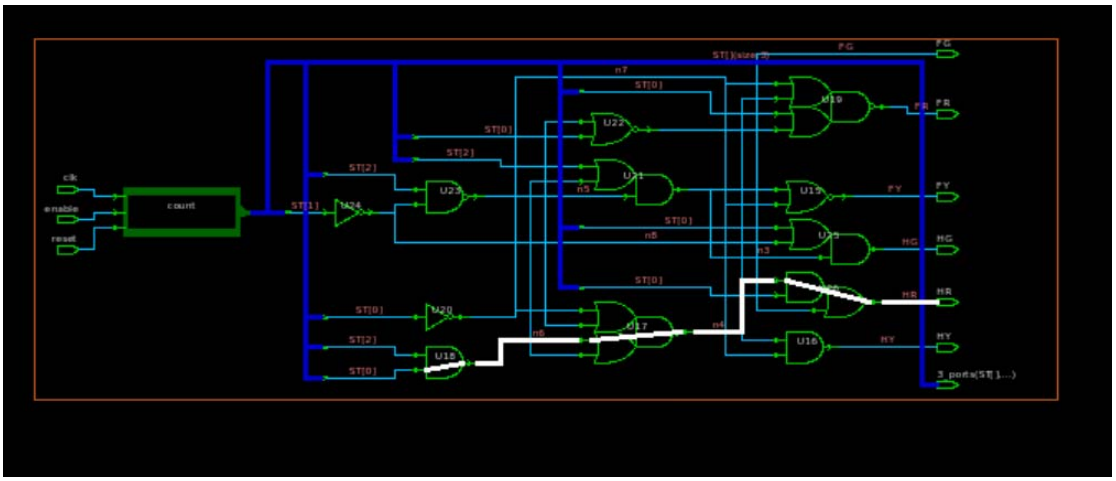
The critical path will be highlighted on the schematic window using a white line.



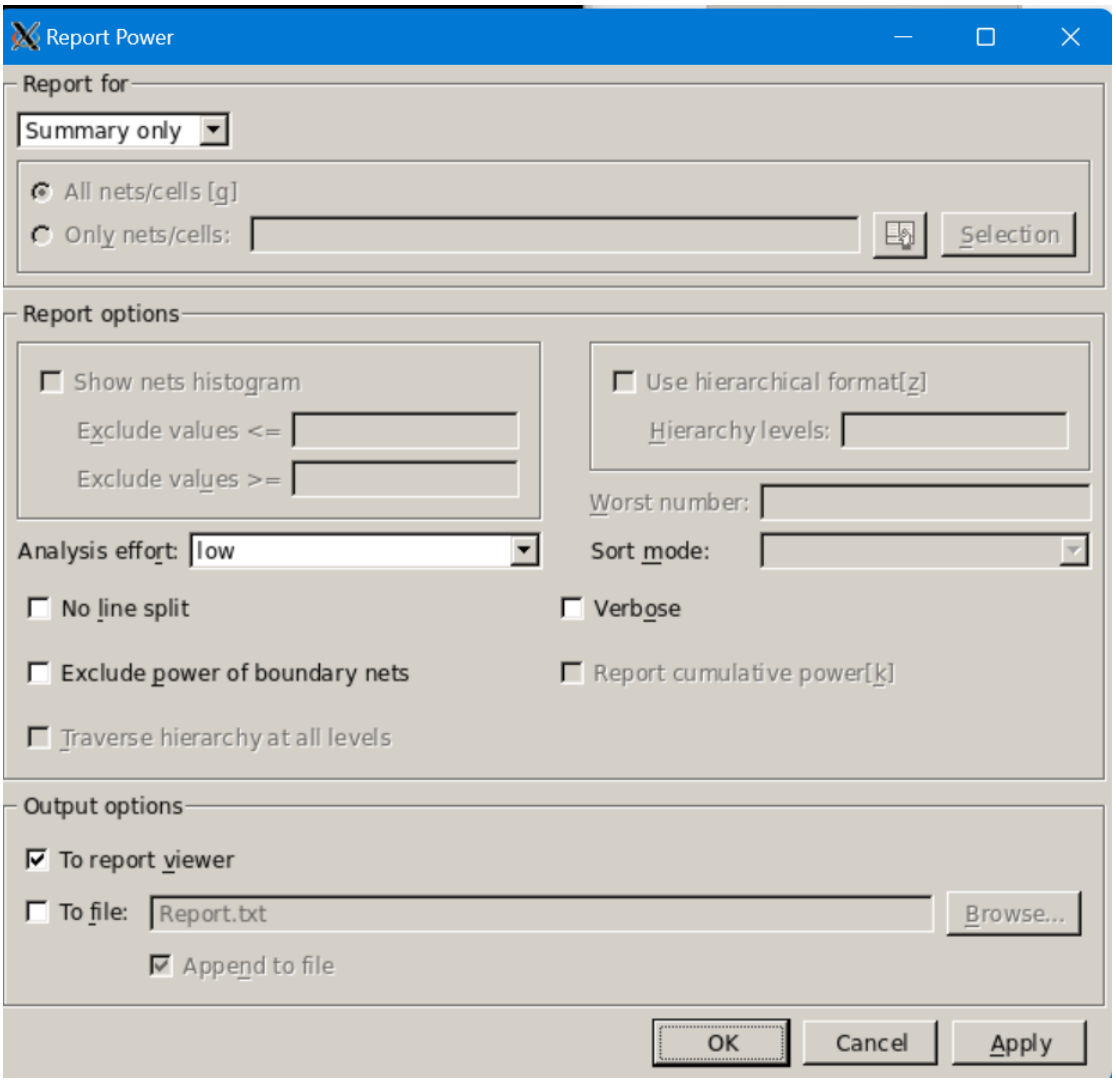
The other method is: Schematic->Paths From/Through/to
Set the delay type to max.



Set the delay type to max.
A new window will open up showing the entire critical path.



14. Power Report



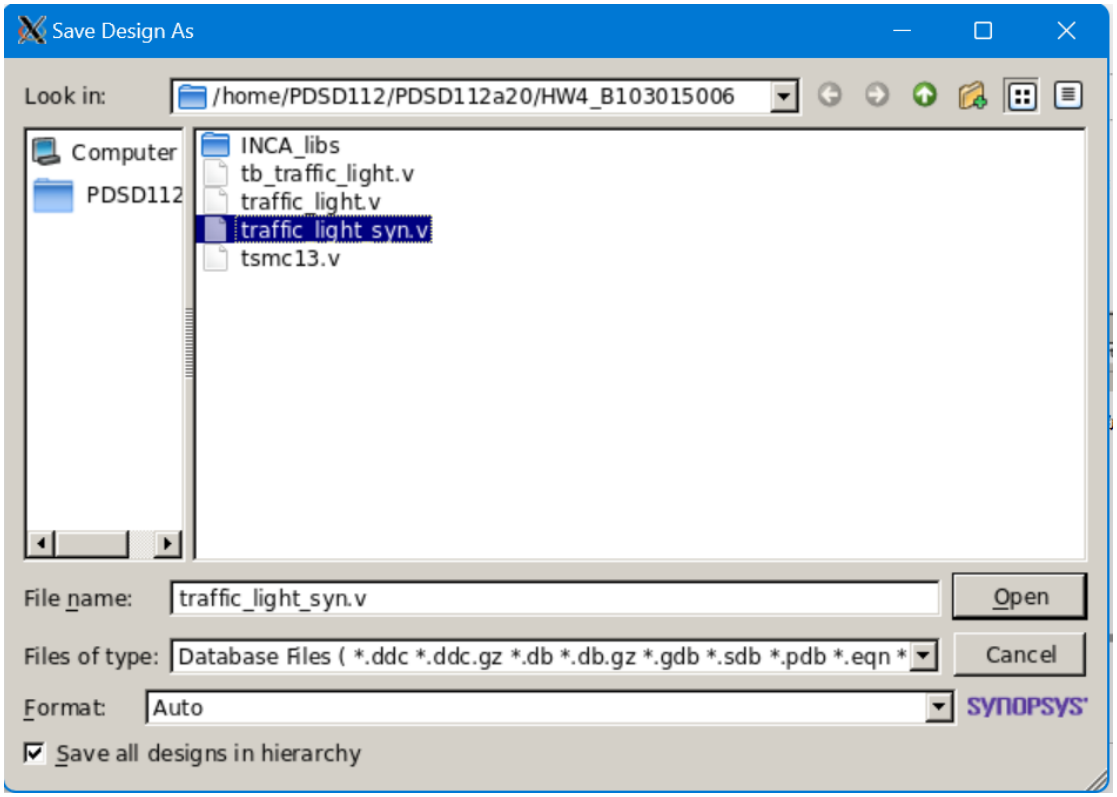
```
****************************************
Report : power
        -analysis_effort low

Design : traffic_light
Version: P-2019.03
Date   : Sun Dec 10 02:56:48 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   5.9761 uW   (94%)
  Net Switching Power  = 361.9794 nW    (6%)
                         ---------
Total Dynamic Power    =   6.3380 uW  (100%)

Cell Leakage Power     = 308.4187 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register       5.6367e-03       1.0591e-04        1.4527e+05         5.8878e-03  (  88.59%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational  3.3941e-04       2.5607e-04        1.6315e+05         7.5863e-04  (  11.41%)
--------------------------------------------------------------------------------------------------
Total          5.9761e-03 mW     3.6198e-04 mW     3.0842e+05 pW      6.6465e-03 mW

***** End Of Report *****
```

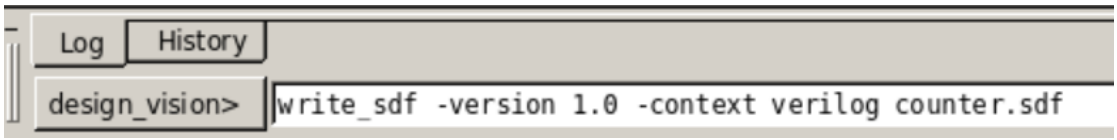
15. Report Qor

If we want to fast access the information of the synthesized circuit, then we can enter ‘report_qor’ in the command line.

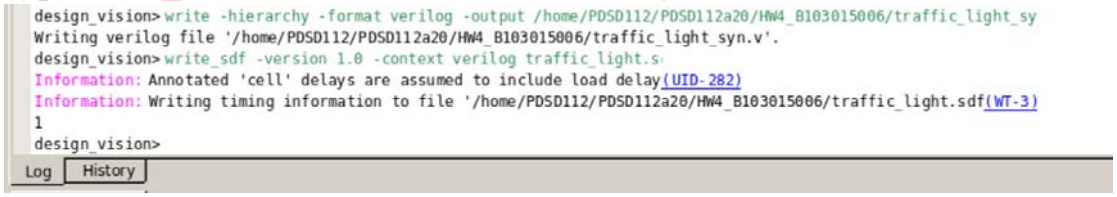
```
design_vision> report_qor

****************************************
Report : qor
Design : traffic_light
Version: P-2019.03
Date   : Sun Dec 10 03:00:57 2023
****************************************


  Timing Path Group 'clk'
  -----------------------------------
  Levels of Logic:               5.00
  Critical Path Length:          1.47
  Critical Path Slack:          17.53
  Critical Path Clk Period:     20.00
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:          0.00
  Total Hold Violation:          0.00
  No. of Hold Violations:        0.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:           1
  Hierarchical Port Count:           6
  Leaf Cell Count:                  29
  Buf/Inv Cell Count:                3
  Buf Cell Count:                    0
  Inv Cell Count:                    3
  CT Buf/Inv Cell Count:             0
  Combinational Cell Count:         24
  Sequential Cell Count:             5
  Macro Count:                       0
  -----------------------------------


  Area
  -----------------------------------
  Combinational Area:      196.898402
  Noncombinational Area:   144.279003
  Buf/Inv Area:             10.184400
  Total Buffer Area:             0.00
  Total Inverter Area:          10.18
  Macro/Black Box Area:      0.000000
  Net Area:                  0.000000
  -----------------------------------
  Cell Area:               341.177405
  Design Area:             341.177405


  Design Rules
  -----------------------------------
  Total Number of Nets:             37
  Nets With Violations:              0
  Max Trans Violations:              0
  Max Cap Violations:                0
  -----------------------------------


  Hostname: soc08

  Compile CPU Statistics
  ---------------------------------------
  Resource Sharing:                  0.06
  Logic Optimization:                0.72
  Mapping Optimization:              0.16
  ---------------------------------------
  Overall Compile Time:              2.80
  Overall Compile Wall Clock Time:   3.54

  --------------------------------------------------------------------

  Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0


  Design (Hold)  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0

  --------------------------------------------------------------------


1
design_vision>
```

16. Save Design Circuit and Timing Files





Type ‘wrie_sdf –version 1.0 –context verilog (filename).sdf’.



17. Rerun Verilog Simulation

Modify the testbench:

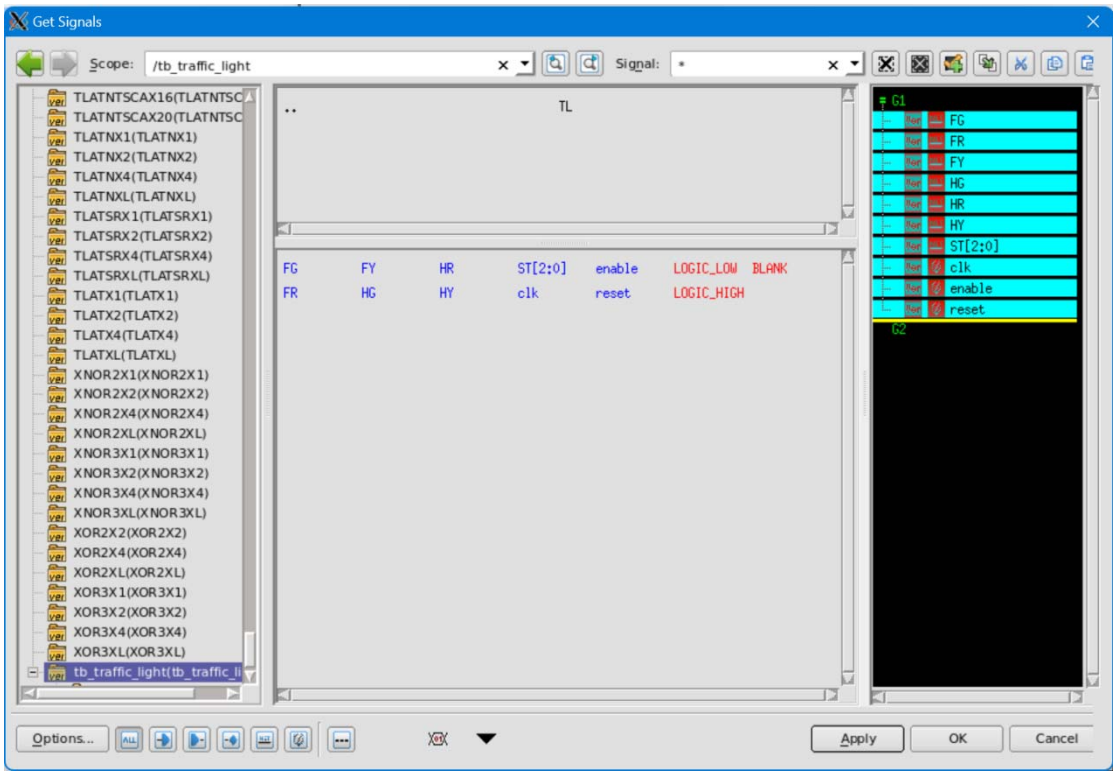
```
`timescale 1ns/10ps

`include "./traffic_light_syn.v"
`include "./tsmc13.v"

initial begin
$sdf_annotate("traffic_light.sdf", TL);
end
```

```
initial begin
    $fsdbDumpfile ("traffic_light.fsdb");
    $fsdbDumpvars;
    $fsdbDumpMDA;
end
```

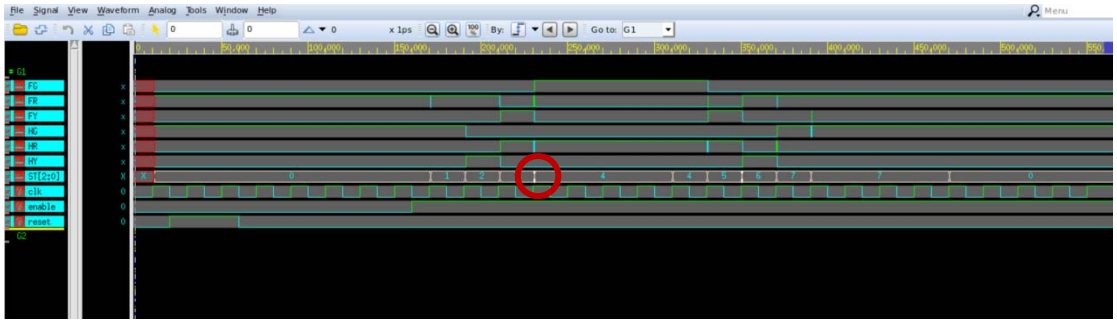
Enter ‘ncverilog tb.v +access+r’ in the workstation command line to initiate the simulation.

```
soc08 [~/HW4_B103015006]
-PDSD112a20- $ncverilog tb_traffic_light.v +access+r
ncverilog: 15.20-s039: (c) Copyright 1995-2017 Cadence Design Systems, Inc.
file: tb_traffic_light.v
        module worklib.counter:v
                errors: 0, warnings: 0
        module worklib.traffic_light:v
                errors: 0, warnings: 0
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
  DFFTRX1 count_reg_4_ ( .D(N29), .RN(n7), .CK(clk), .Q(count[4]) );
                       |
ncelab: *W,CUVWSP (./traffic_light_syn.v,15|21): 1 output port was not connecte
d:
ncelab: (./tsmc13.v,19387): QN

  DFFTRX1 count_reg_1_ ( .D(N26), .RN(n7), .CK(clk), .Q(count[1]) );
                       |
ncelab: *W,CUVWSP (./traffic_light_syn.v,17|21): 1 output port was not connecte
d:
ncelab: (./tsmc13.v,19387): QN

  DFFTRX1 count_reg_3_ ( .D(N28), .RN(n7), .CK(clk), .Q(count[3]) );
                       |
ncelab: *W,CUVWSP (./traffic_light_syn.v,19|21): 1 output port was not connecte
d:
ncelab: (./tsmc13.v,19387): QN

        Reading SDF file from location "traffic_light.sdf"
        Compiled SDF file "traffic_light.sdf.X" older than source SDF file "tra
ffic_light.sdf".
        Recompiling.
        Writing compiled SDF file to "traffic_light.sdf.X".
        Annotating SDF timing data:
                Compiled SDF file:     traffic_light.sdf.X
                Log file:
                Backannotation scope:  tb_traffic_light.TL
                Configuration file:
                MTM control:
                Scale factors:
                Scale type:
        Annotation completed successfully...
        SDF statistics: No. of PathDelays = 2957  Annotated = 2.67% -- No. of T
checks = 1230  Annotated = 2.44%
                                      Total      Annotated      Percentage
                  Path Delays          2957             79            2.67
                        $hold            64              0            0.00
                       $width           378             10            2.65
```

Make sure ‘Annotation completed successfully’ is in terminal. Open nWave and find testbench module name.



Select signals to be observed.

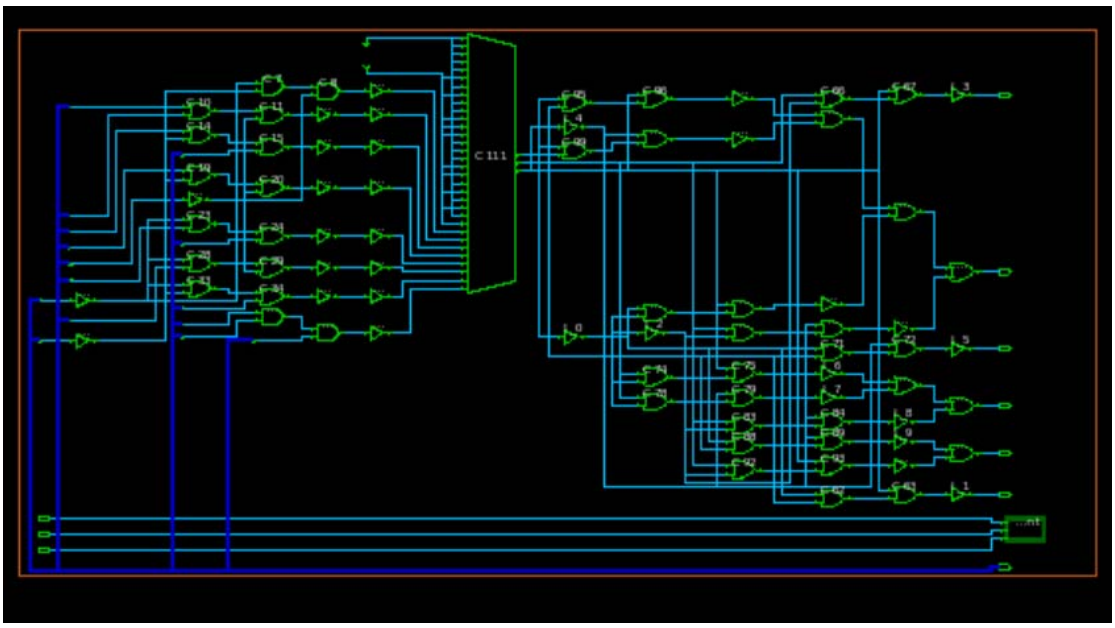


Delay effect can be observed.

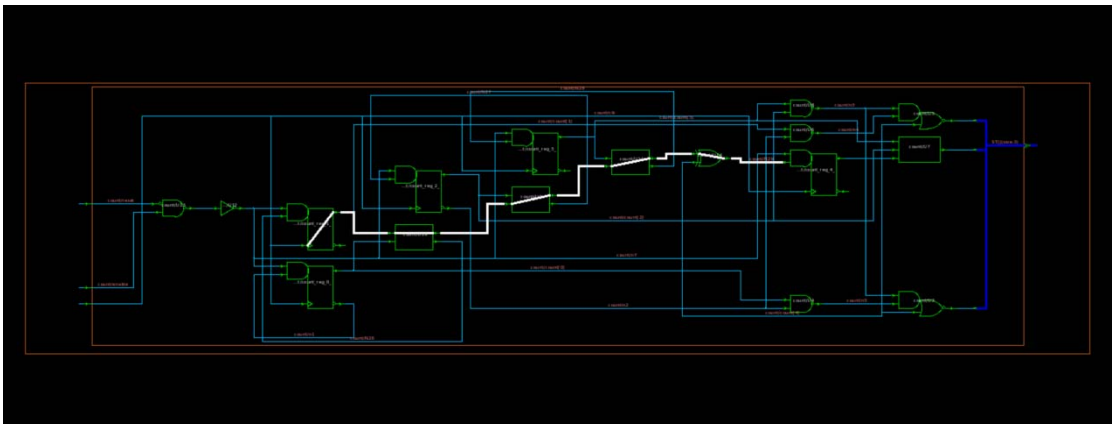
IV. Circuit Analysis

1. Critical Path

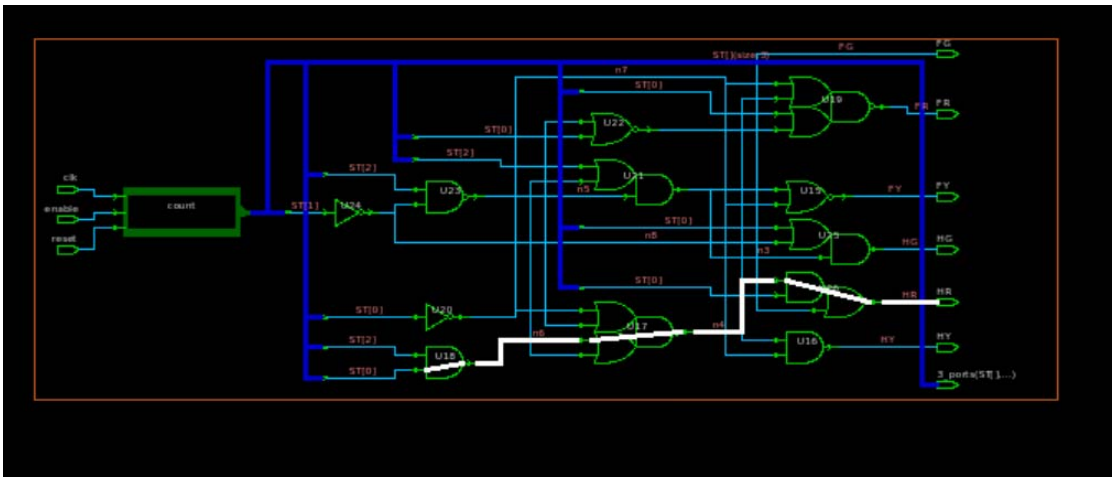
a. Before Synthesis



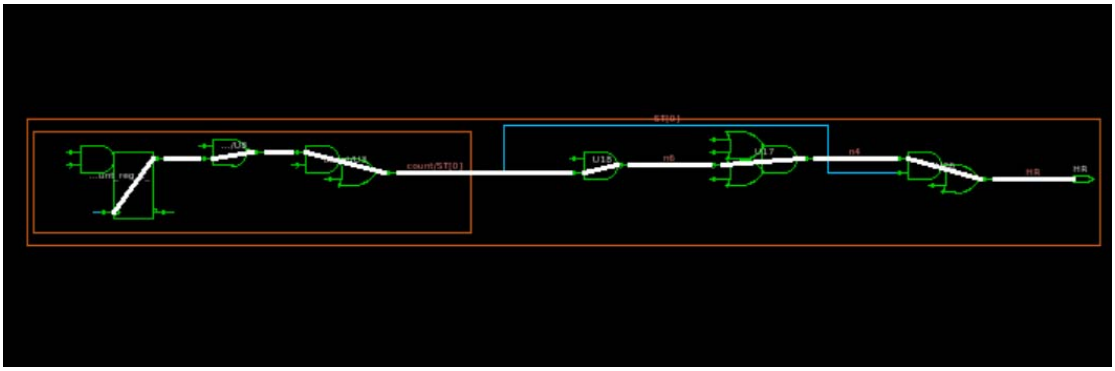
Longest path:



b. After Synthesis



Longest path:



c. Comparison

There is no difference of the critical path before and after synthesis.

2. Area

a. Before Synthesis

```
****************************************
Report : area
Design : traffic_light
Version: P-2019.03
Date   : Sun Dec 10 07:45:58 2023
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    gtech (File: /usr/cad/synopsys/synthesis/cur/libraries/syn/gtech.db)
    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                           18
Number of nets:                           114
Number of cells:                           99
Number of combinational cells:             90
Number of sequential cells:                 6
Number of macros/black boxes:               0
Number of buf/inv:                         33
Number of references:                       6

Combinational area:                118.818001
Buf/Inv area:                        3.394800
Noncombinational area:             144.279003
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                   263.097004
Total area:                 undefined

Information: This design contains unmapped logic. (RPT-7)

***** End Of Report *****
```

Unit: 263.097004 um × um

Area of a NAND2 gate is approximately:

i. 5 um × um for a 0.13um technology

ii. 10 um × um for a 0.18um technology

Gate count = reported area/ area of a NAND2 gate

i. 263.097004/5 = 52.6194008 in 0.13um technology

ii. 263.097004/10 = 26.3097004 in 0.18um technology

Report Qor

```
design_vision> report_qor

****************************************
Report : qor
Design : traffic_light
Version: P-2019.03
Date   : Sun Dec 10 07:51:37 2023
****************************************


  Timing Path Group 'clk'
  -----------------------------------
  Levels of Logic:               4.00
  Critical Path Length:          1.11
  Critical Path Slack:          18.66
  Critical Path Clk Period:     20.00
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:          0.00
  Total Hold Violation:          0.00
  No. of Hold Violations:        0.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:          1
  Hierarchical Port Count:          6
  Leaf Cell Count:                 96
  Buf/Inv Cell Count:              33
  Buf Cell Count:                   8
  Inv Cell Count:                  25
  CT Buf/Inv Cell Count:            0
  Combinational Cell Count:        91
  Sequential Cell Count:            5
  Macro Count:                      0
```

```
Macro Count:                      0
-----------------------------------


Area
-----------------------------------
Combinational Area:      118.818001
Noncombinational Area:   144.279003
Buf/Inv Area:              3.394800
Total Buffer Area:             0.00
Total Inverter Area:           3.39
Macro/Black Box Area:      0.000000
Net Area:                  0.000000
-----------------------------------
Cell Area:               263.097004
Design Area:             263.097004


Design Rules
-----------------------------------
Total Number of Nets:           108
Nets With Violations:             0
Max Trans Violations:             0
Max Cap Violations:               0
-----------------------------------


Hostname: soc08

Compile CPU Statistics
---------------------------------------
Resource Sharing:                 0.00
Logic Optimization:               0.00
Mapping Optimization:             0.00
---------------------------------------
Overall Compile Time:             0.00
Overall Compile Wall Clock Time:  0.00
```

```
Hostname: soc08

Compile CPU Statistics
---------------------------------------
Resource Sharing:                 0.00
Logic Optimization:               0.00
Mapping Optimization:             0.00
---------------------------------------
Overall Compile Time:             0.00
Overall Compile Wall Clock Time:  0.00

--------------------------------------------------------------------

Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0


Design (Hold)  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0

--------------------------------------------------------------------


1
design_vision>
```

Longest path: 1.11

Sequential Cell Count: 5

Combinational Cell Count: 91

Number of logic gates layers: 4

b. After Synthesis

The output result of the area report will be shown as below.

```
****************************************
Report : area
Design : traffic_light
Version: P-2019.03
Date   : Sun Dec 10 02:22:39 2023
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                           18
Number of nets:                            43
Number of cells:                           30
Number of combinational cells:             24
Number of sequential cells:                 5
Number of macros/black boxes:               0
Number of buf/inv:                          3
Number of references:                       8

Combinational area:               196.898402
Buf/Inv area:                      10.184400
Noncombinational area:            144.279003
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  341.177405
Total area:                 undefined

***** End Of Report *****
```

Unit: 341.177405 um × um

Area of a NAND2 gate is approximately:

iii. 5 um × um for a 0.13um technology

iv. 10 um × um for a 0.18um technology

Gate count = reported area/ area of a NAND2 gate

iii. 341.177405/5 = 68.235481 in 0.13um technology

iv. 341.177405/10 = 34.1177405 in 0.18um technology

Report Qor

```
design_vision> report_qor

****************************************
Report : qor
Design : traffic_light
Version: P-2019.03
Date   : Sun Dec 10 03:00:57 2023
****************************************


  Timing Path Group 'clk'
  -----------------------------------
  Levels of Logic:               5.00
  Critical Path Length:          1.47
  Critical Path Slack:          17.53
  Critical Path Clk Period:     20.00
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:          0.00
  Total Hold Violation:          0.00
  No. of Hold Violations:        0.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:           1
  Hierarchical Port Count:           6
  Leaf Cell Count:                  29
  Buf/Inv Cell Count:                3
  Buf Cell Count:                    0
  Inv Cell Count:                    3
  CT Buf/Inv Cell Count:             0
  Combinational Cell Count:         24
  Sequential Cell Count:             5
  Macro Count:                       0
```

```
  Macro Count:                       0
  -----------------------------------


  Area
  -----------------------------------
  Combinational Area:      196.898402
  Noncombinational Area:   144.279003
  Buf/Inv Area:             10.184400
  Total Buffer Area:             0.00
  Total Inverter Area:          10.18
  Macro/Black Box Area:      0.000000
  Net Area:                  0.000000
  -----------------------------------
  Cell Area:               341.177405
  Design Area:             341.177405


  Design Rules
  -----------------------------------
  Total Number of Nets:             37
  Nets With Violations:              0
  Max Trans Violations:              0
  Max Cap Violations:                0
  -----------------------------------


  Hostname: soc08

  Compile CPU Statistics
  ---------------------------------------
  Resource Sharing:                  0.06
  Logic Optimization:                0.72
  Mapping Optimization:              0.16
  ---------------------------------------
  Overall Compile Time:              2.80
  Overall Compile Wall Clock Time:   3.54
```

```
  -----------------------------------
  Cell Area:               341.177405
  Design Area:             341.177405


  Design Rules
  -----------------------------------
  Total Number of Nets:             37
  Nets With Violations:              0
  Max Trans Violations:              0
  Max Cap Violations:                0
  -----------------------------------


  Hostname: soc08

  Compile CPU Statistics
  ---------------------------------------
  Resource Sharing:                  0.06
  Logic Optimization:                0.72
  Mapping Optimization:              0.16
  ---------------------------------------
  Overall Compile Time:              2.80
  Overall Compile Wall Clock Time:   3.54

  --------------------------------------------------------------------

  Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0


  Design (Hold)  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0

  --------------------------------------------------------------------


1
design_vision>
```

Longest path: 1.47
Sequential Cell Count: 5
Combinational Cell Count: 24
Number of logic gates layers: 5

c. Comparison

The area after synthesis is bigger than before synthesis, which is due to the reason of delay setting.
With same number of logic gates layers and sequential cell, the circuit after synthesis has less number of combinational circuits but with a bit longer critical path that might happens in the counter also because of the input and output delay setting.

3. Power

a. Before Synthesis

```
****************************************
Report : power
        -analysis_effort low
Design : traffic_light
Version: P-2019.03
Date   : Sun Dec 10 07:55:18 2023
****************************************


Library(s) Used:

    gtech (File: /usr/cad/synopsys/synthesis/cur/libraries/syn/gtech.db)
    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   5.8311 uW   (97%)
  Net Switching Power  = 179.8703 nW    (3%)
                         ---------
Total Dynamic Power    =   6.0109 uW  (100%)

Cell Leakage Power     = 253.6096 nW
```

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	5.6367e-03	1.0591e-04	1.4527e+05	5.8878e-03	(93.99%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
combinational	1.9441e-04	7.3965e-05	1.0834e+05	3.7671e-04	(6.01%)	
Total	5.8311e-03 mW	1.7987e-04 mW	2.5361e+05 pW	6.2645e-03 mW		

```
***** End Of Report *****
```

Total power: 6.2645e-03 mW

b. After Synthesis

```
****************************************
Report : power
        -analysis_effort low
Design : traffic_light
Version: P-2019.03
Date   : Sun Dec 10 02:56:48 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   5.9761 uW   (94%)
  Net Switching Power  = 361.9794 nW    (6%)
                         ---------
Total Dynamic Power    =   6.3380 uW  (100%)

Cell Leakage Power     = 308.4187 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register       5.6367e-03       1.0591e-04        1.4527e+05         5.8878e-03  (  88.59%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational  3.3941e-04       2.5607e-04        1.6315e+05         7.5863e-04  (  11.41%)
--------------------------------------------------------------------------------------------------
Total          5.9761e-03 mW     3.6198e-04 mW     3.0842e+05 pW      6.6465e-03 mW

***** End Of Report *****
```

Total power: 6.6465e-03 mW

c. Comparison

The circuit after logic synthesis has larger power consumption.

4. Delay

a. Before Synthesis

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
         -sort_by group
Design : traffic_light
Version: P-2019.03
Date   : Sun Dec 10 07:56:25 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: count/count_reg_1_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: count/count_reg_4_
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  count/count_reg_1_/CK (DFFTRX1)          0.00      10.00 r
  count/count_reg_1_/Q (DFFTRX1)           0.52      10.52 f
  count/U10/CO (ADDHXL)                    0.18      10.70 f
  count/U9/CO (ADDHXL)                     0.16      10.86 f
  count/U11/CO (ADDHXL)                    0.16      11.02 f
  count/U14/Y (XOR2X1)                     0.09      11.11 r
  count/count_reg_4_/D (DFFTRX1)           0.00      11.11 r
  data arrival time                                  11.11

  clock clk (rise edge)                   30.00      30.00
  clock network delay (ideal)              0.00      30.00
  count/count_reg_4_/CK (DFFTRX1)          0.00      30.00 r
  library setup time                      -0.23      29.77
  data required time                                 29.77
  -----------------------------------------------------------
  data required time                                 29.77
  data arrival time                                 -11.11
  -----------------------------------------------------------
  slack (MET)                                        18.66
```

Delay type: max
Data arrival time: 11.11(ns)
Setup time: 29.77(ns)
Slack: 18.66(ns)

b. After Synthesis

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : traffic_light
Version: P-2019.03
Date   : Sun Dec 10 02:29:54 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: count/count_reg_2_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: HR (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  count/count_reg_2_/CK (DFFTRX1)          0.00      10.00 r
  count/count_reg_2_/Q (DFFTRX1)           0.52      10.52 f
  count/U8/Y (NAND2X1)                     0.12      10.64 r
  count/U3/Y (AOI21X1)                     0.14      10.78 f
  count/ST[0] (counter)                    0.00      10.78 f
  U18/Y (AND2X2)                           0.19      10.97 f
  U17/Y (OAI22XL)                          0.30      11.27 r
  U26/Y (AO21X1)                           0.20      11.47 r
  HR (out)                                 0.00      11.47 r
  data arrival time                                  11.47

  clock clk (rise edge)                   30.00      30.00
  clock network delay (ideal)              0.00      30.00
  output external delay                   -1.00      29.00
  data required time                                 29.00
  -----------------------------------------------------------
  data required time                                 29.00
  data arrival time                                 -11.47
  -----------------------------------------------------------
  slack (MET)                                        17.53
```

Delay type: max
Data arrival time: 11.47 (ns)
Setup time: 29.00(ns)
Slack: 17.53(ns)

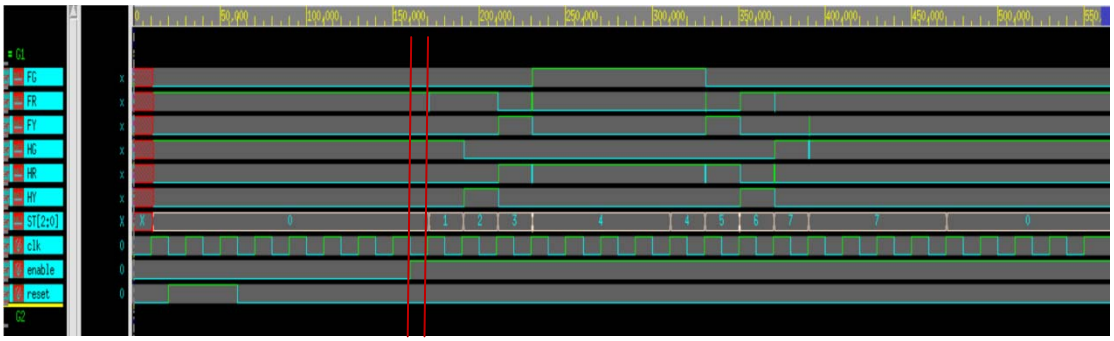
c. Comparison

The slack after synthesis has a smaller slack compare to the one before synthesis.

V. Testbench and Verification

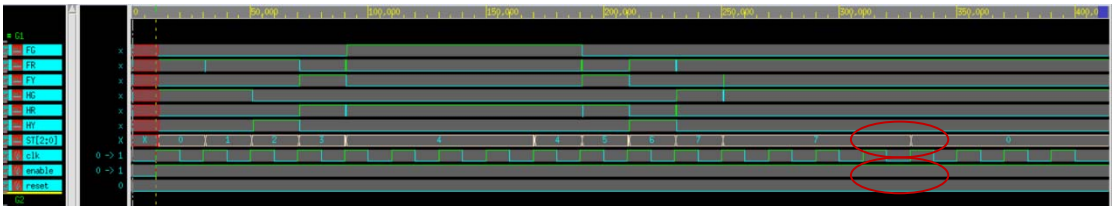
Following are the main function of our circuit, we check each function separately and if they all functioned correctly, then it shows that the circuit can normally work.

1. **When there are cars on farm road, S0->S1**

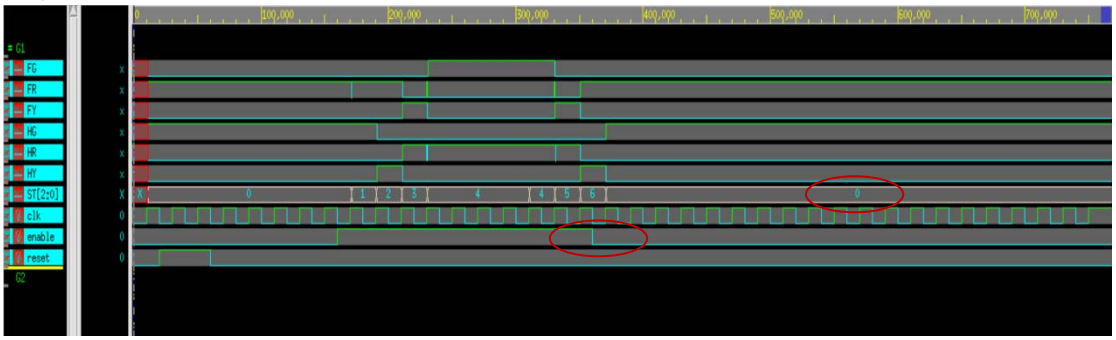


When enable(car detect)=1, the state will change from 0 to 1 after the posedge of clk arrive.
And the states continue normally.

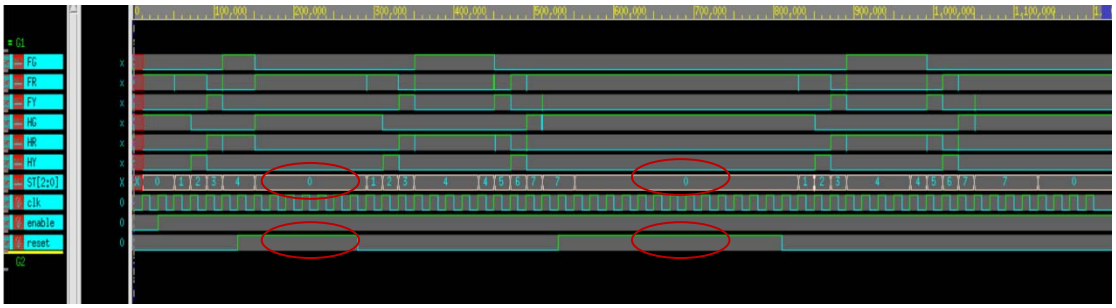
2. **After one turn of the light conversion, if there still have cars on the road, S7->S0**



3. **After the light conversion, if there is no car on the road anymore, current state->S0**



4. **When reset=1, current state-> S0**



VI. Discussion and Reflection

1. Discussion

The reason for the delay effect arises from the difference in the time it takes for signals to reach the output port. In other words, before the signal on the longest path completes its calculation and reaches the output port, signals from other paths with shorter delays will already have arrived.
This causes continuous fluctuations in the output values. In the context of simulating the waveform in the traffic light, this delay effect resembles a signal glitch.

2. Reflection

I feel a big difference between writing HW1 and HW2 with this HW4. Writing combinational circuit and writing sequential circuit has huge difference in the data type and its way of sending signals, to write a sequential circuit, one should be very clear about the circuit they are designing. I got confused with my code several times in the designing process, however, thanks to the help of error message, I figured out my mistake immediately and successfully complete the work.
After having the experience of designing the traffic light controller, I fell that I can really design something that can be apply in the real world, it is a cool thing to be honest, however, this work is really time consuming, I spent most of my time not on writing code but on logic synthesis…. Can’t imagine how much effort will it take on our final project.