Digital Lab 2:

Practice of Logic Gate ICs

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Class: 電機二全英班

Group: Group 8

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VIII. Test Result

1. NOT Gate (7404)

Input A	Output B	Output Voltage Level
0	1	4.444V
1	0	0.066V

2. AND Gate (7408)

Input A	Input B	Output C	Output Voltage Level
0	0	0	0.039V
0	1	0	0.039V
1	0	0	0.039V
1	1	1	4.437V

3. OR Gate (7432)

Input A	Input B	Output C	Output Voltage Level
0	0	0	0.050V
0	1	1	4.438V
1	0	1	4.434V
1	1	1	4.437V

4. NAND Gate (7400)

Input A	Input B	Output C	Output Voltage Level
0	0	1	4.452V
0	1	1	4.453V
1	0	1	4.457V
1	1	0	0.037V

5. NOR Gate (7402)

Input A	Input B	Output C	Output Voltage Level
0	0	1	4.447V
0	1	0	0.040V
1	0	0	0.040V
1	1	0	0.036V

6. XOR Gate (7486)

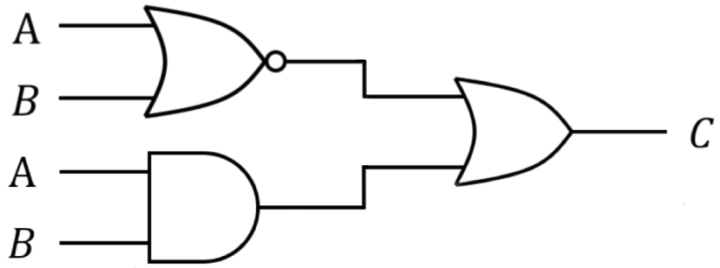
Input A	Input B	Output C	Output Voltage Level
0	0	0	0.041V
0	1	1	4.421V
1	0	1	4.418V
1	1	0	0.046V

7. XNOR Gate

$$C = \overline{A \oplus B} = \overline{\overline{A} \cdot B + A \cdot \overline{B}}$$

$$= (A + \overline{B}) \cdot (\overline{A} + B) = A \cdot \overline{A} + \overline{B} \cdot \overline{A} + A \cdot B + \overline{B} \cdot B$$

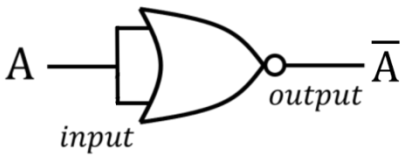
$$= \overline{B} \cdot \overline{A} + A \cdot B = \overline{A + B} + A \cdot B \text{ (NOR) (OR) (AND)}$$



Input A	Input B	Output C	Output Voltage Level
0	0	1	4.431V
0	1	0	0.051V
1	0	0	0.051V
1	1	1	4.432V

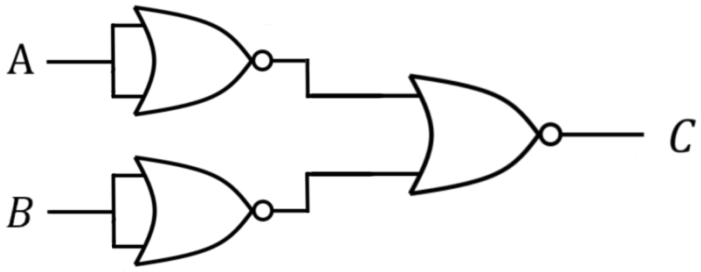
8.

(1) $\overline{A + A} = \overline{A}$



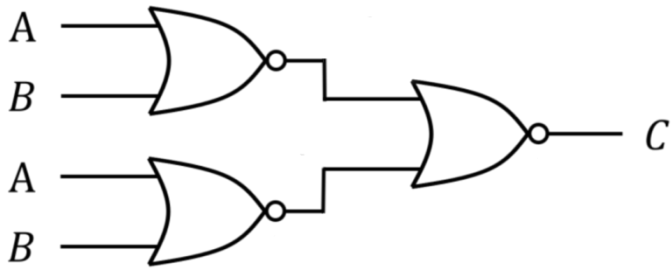
Input A	Output B	Output Voltage Level
0	1	4.402V
1	0	0.036V

(2) $\overline{\overline{A+A}+\overline{B+B}} = \overline{\overline{A}+\overline{B}} = A \cdot B$



Input A	Input B	Output C	Output Voltage Level
0	0	0	0.035V
0	1	0	0.040V
1	0	0	0.040V
1	1	1	3.388V

(3) $\overline{\overline{A+B}+\overline{A+B}} = \overline{\overline{A+B}} = A + B$



Input A	Input B	Output C	Output Voltage Level
0	0	0	0.035V
0	1	1	3.389V
1	0	1	3.389V
1	1	1	3.389V

IX. Problem discussion

We encountered problem when we conduct the experiment of NOR Gate (7402): the output is not the same as we expected. We were confused at first and checked our circuit connection several times, but in no vain. After we asked for TA's help, we found that the only problem is that the pins of 7402 are set in opposite direction compare to other ICs. We have to be much more careful when connecting circuits of NOR Gate.

Nevertheless, we forgot to bring the probe of our multimeters, instead, we used clips to measure the voltage. Although clips can also be used to measure,

the statistics are not as accurate as probes did. At the end, to get more proper statistics, we borrow probes from TA.

X. Review of the experiment

During the logic gate experiment, my group-mate and I gained a deeper understanding of digital electronics and their applications in computing . We were able to construct several different types of logic gates, including AND, OR, NOT, NAND, and NOR gates, and observe how they functioned when presented with different input combinations.

We also had the opportunity to work with integrated circuits (ICs), which made it much easier to construct more complex circuits. Using ICs, we could simply connect the inputs and outputs of the ICs instead of having to build each individual gate from scratch.

In addition to using ICs, we utilized Karnaugh maps (K-maps) to simplify the logic circuits. K-maps are graphical tools used to minimize Boolean expressions and reduce the number of gates required in a circuit. By identifying groups of adjacent 1s in the truth table, we were able to simplify the Boolean expression and reduce the number of gates required to implement the circuit.

Throughout the experiment, we faced challenges in troubleshooting issues with the circuits when they didn't produce the expected output. This required a combination of analytical thinking and hands-on experimentation to identify where the problem was occurring and make the necessary adjustments.

In conclusion, the logic gate experiment was a valuable learning experience that deepened our understanding of digital electronics and their practical applications. We would like to thank our group members and the teaching assistants for their support throughout the experiment.