Digital Lab 3:

Experiment2:

Stepper Motor Control Circuit

Date: 2023/10/12

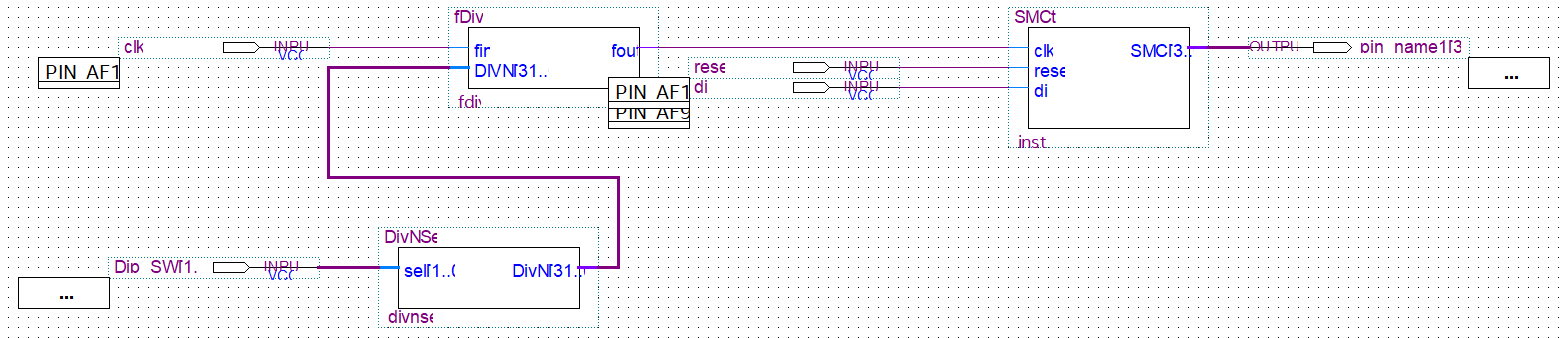
Class: 電機三全英班

Group: Group 11

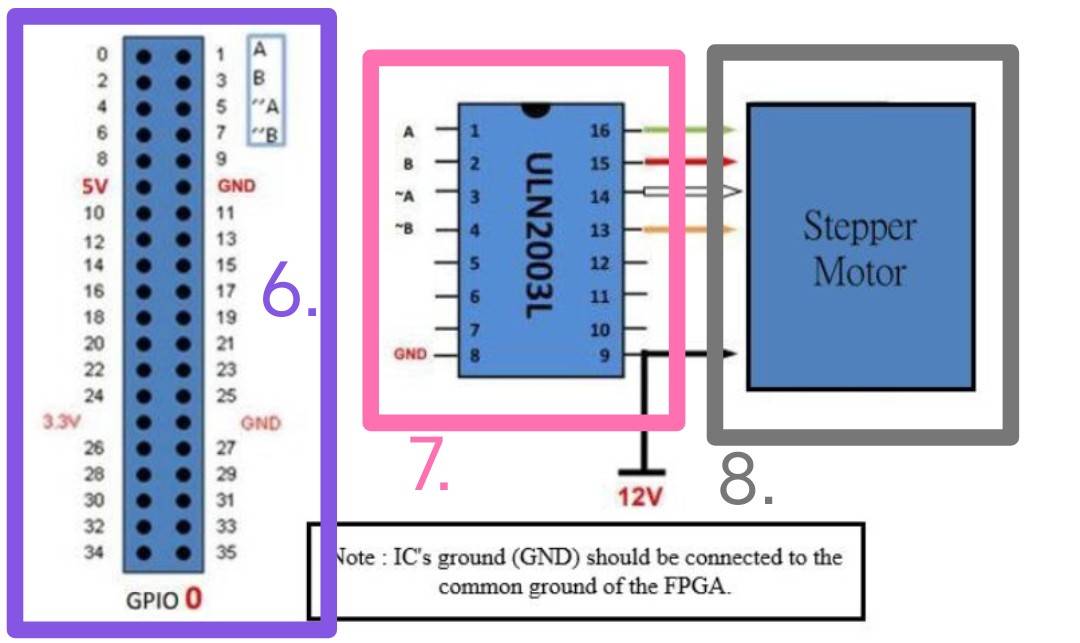
Name: B103105006 胡庭翊

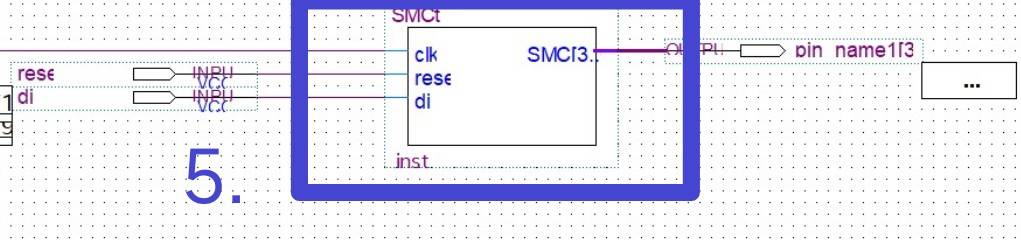
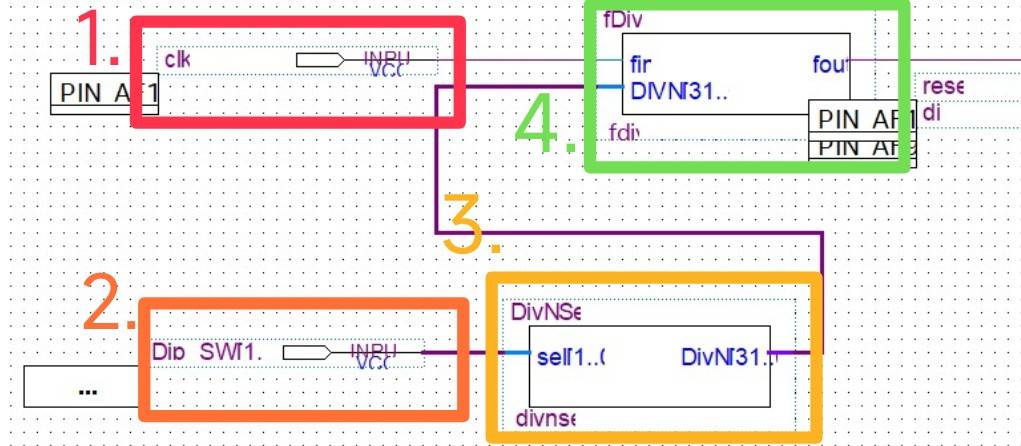
1. Block Diagram

Structure:



Function:



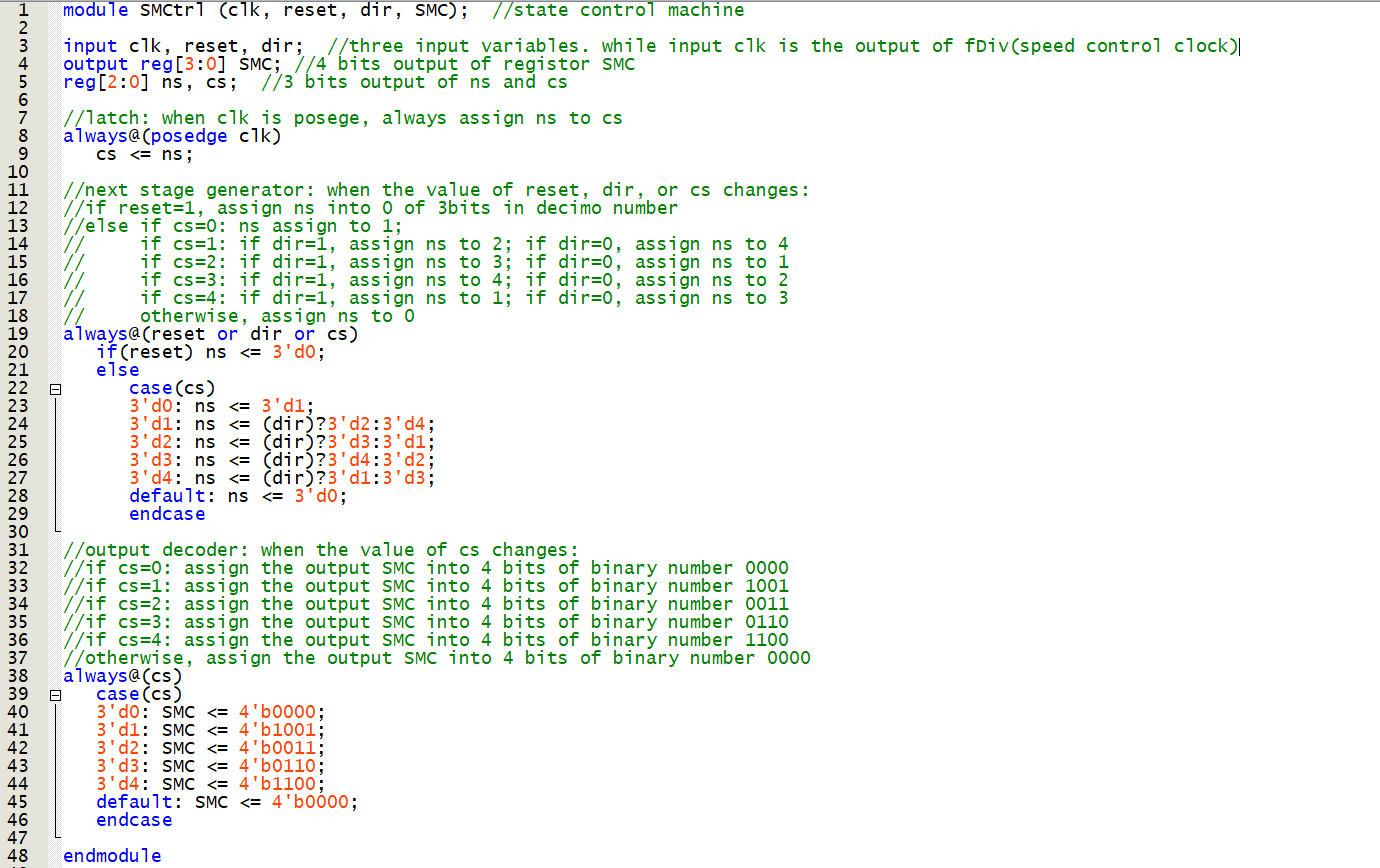


Descriptions:

1. We use 50MHz that set by the board.
2. Use 2 dip switches to be the select of divisor selector.
3. Divisor Selector: Select the specific frequency to be used.
4. Changeable Frequency Divider: Convert the 50MHz input down into specific frequency.
5. State Control Machine: Control the state of Stepper Motor by the State Machine. It can be reset, and changed into inverse direction.

When reset is 1, the state remains S0. Otherwise, when inv is 0, the states transition as follows, S1→S2→S3→S4. When inv is 1, the sequence reverses, S1→S4→S3→S2. (Refer to Figure 8 for reference.)

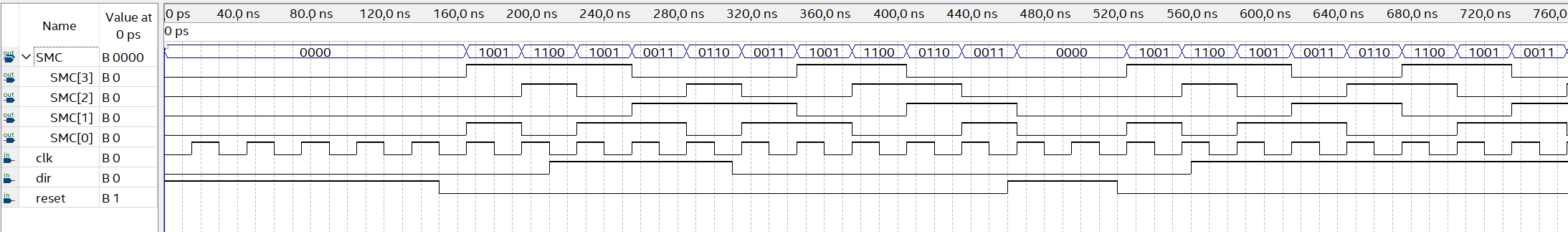
1. The output will be connected to GPIO board. It can be viewed as
2. The ULN2003L is an IC composed of seven sets of Darlington transistors, in order to enhance the output of the circuit, and divert the high current of the motor to the ground.
3. Step Motor: When driving the rotor, if two magnetic fields are in a mutually perpendicular structure, due to the law of magnets “like poles repel, unlike poles attract.” A force will act on the rotor and cause it to rotate.
4. State Control Machine(SMCrtl)
5. Verilog Code and Comment



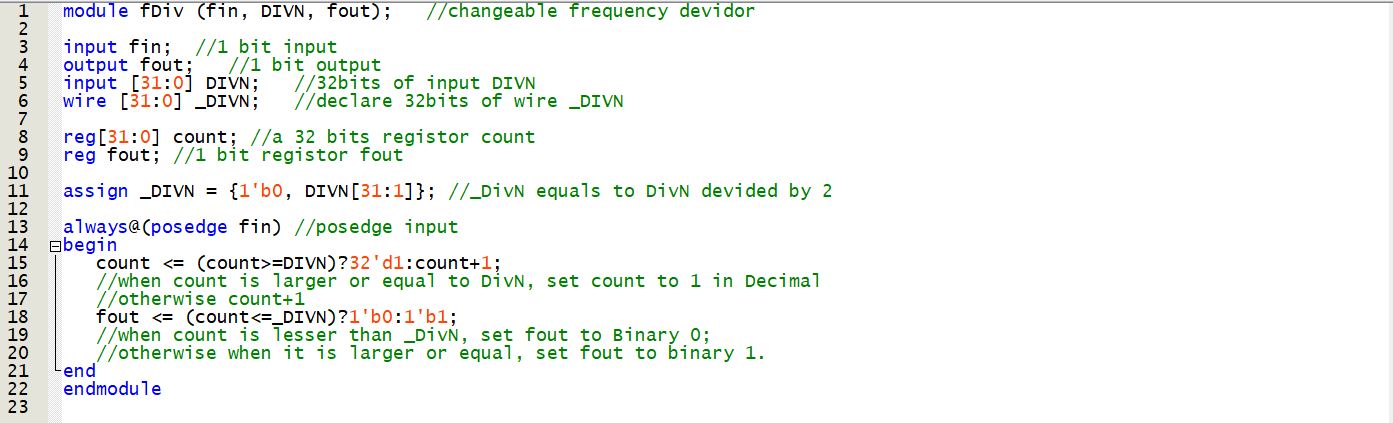
1. Simulation

When reset is set to 1 and the value of clk changes, SMC=0000.

Else, SMC will continuing be assigned into specific value, leading the outcome of clockwise rotation or anticlockwise rotation.

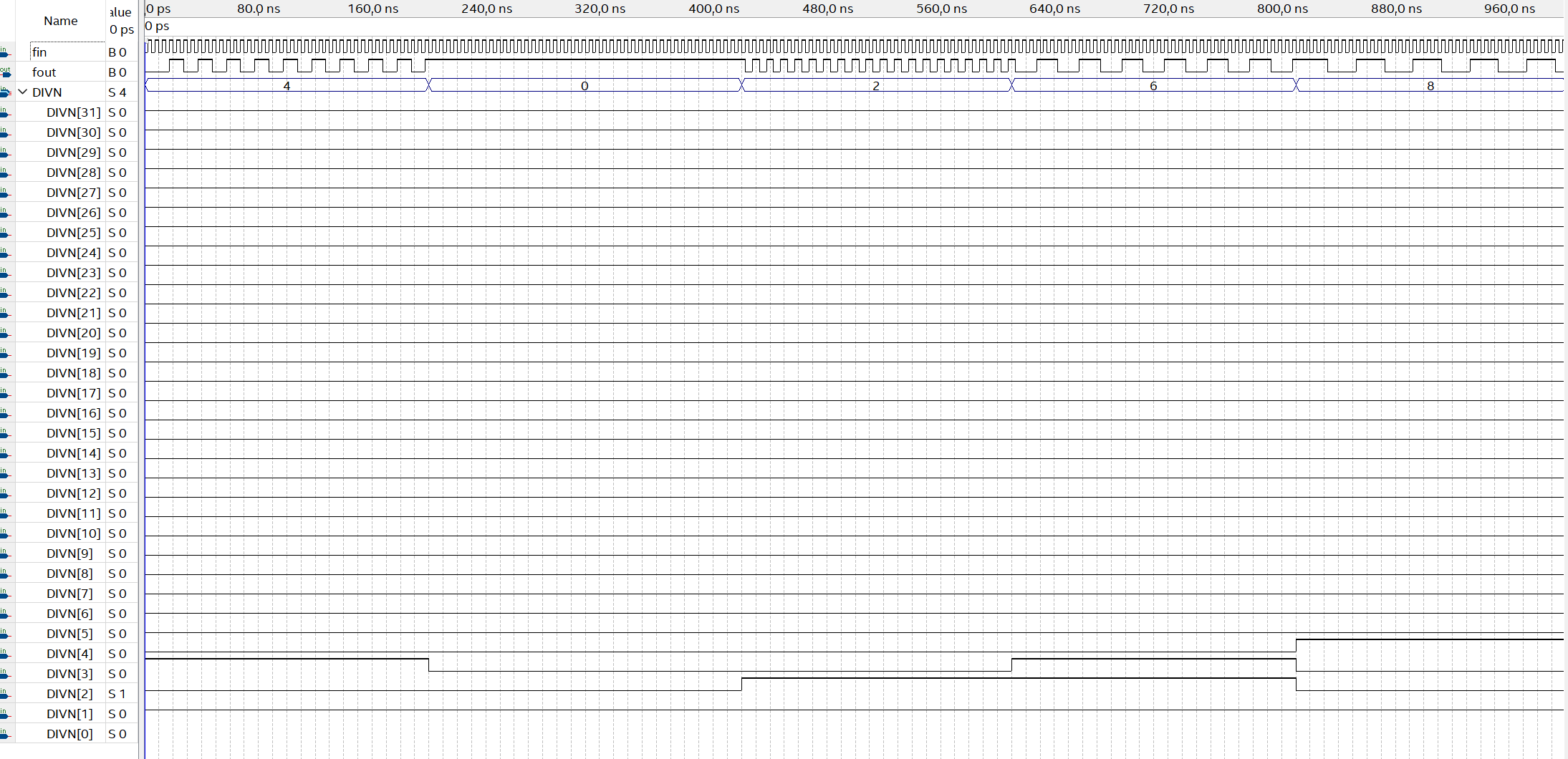


1. Changeable Frequency Divider(fDiv)
2. Verilog Code and Comment

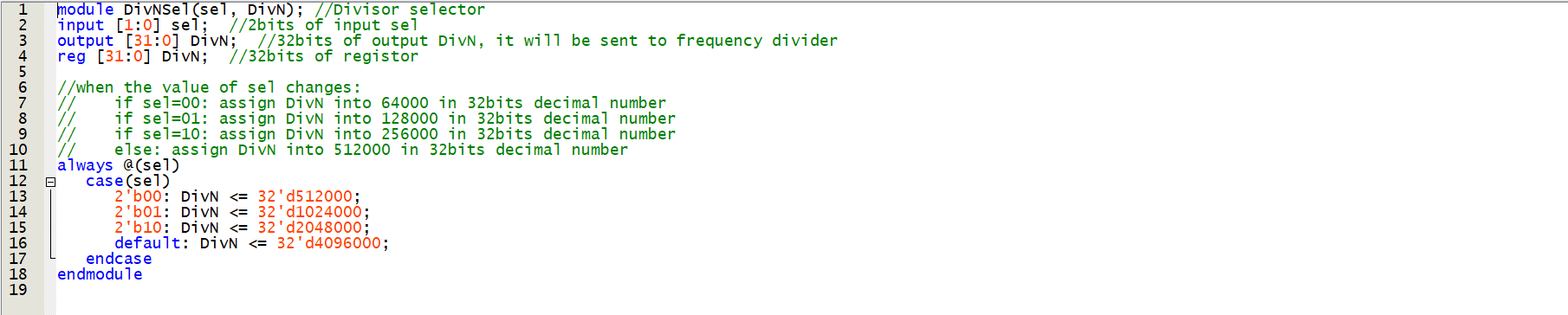


1. Simulation

The value of DIVN will be assigned according to the output of divisor selector, and since we set \_DIVN to DIVN divided by two, the frequency of the output (fout) would be half of the input (fin).

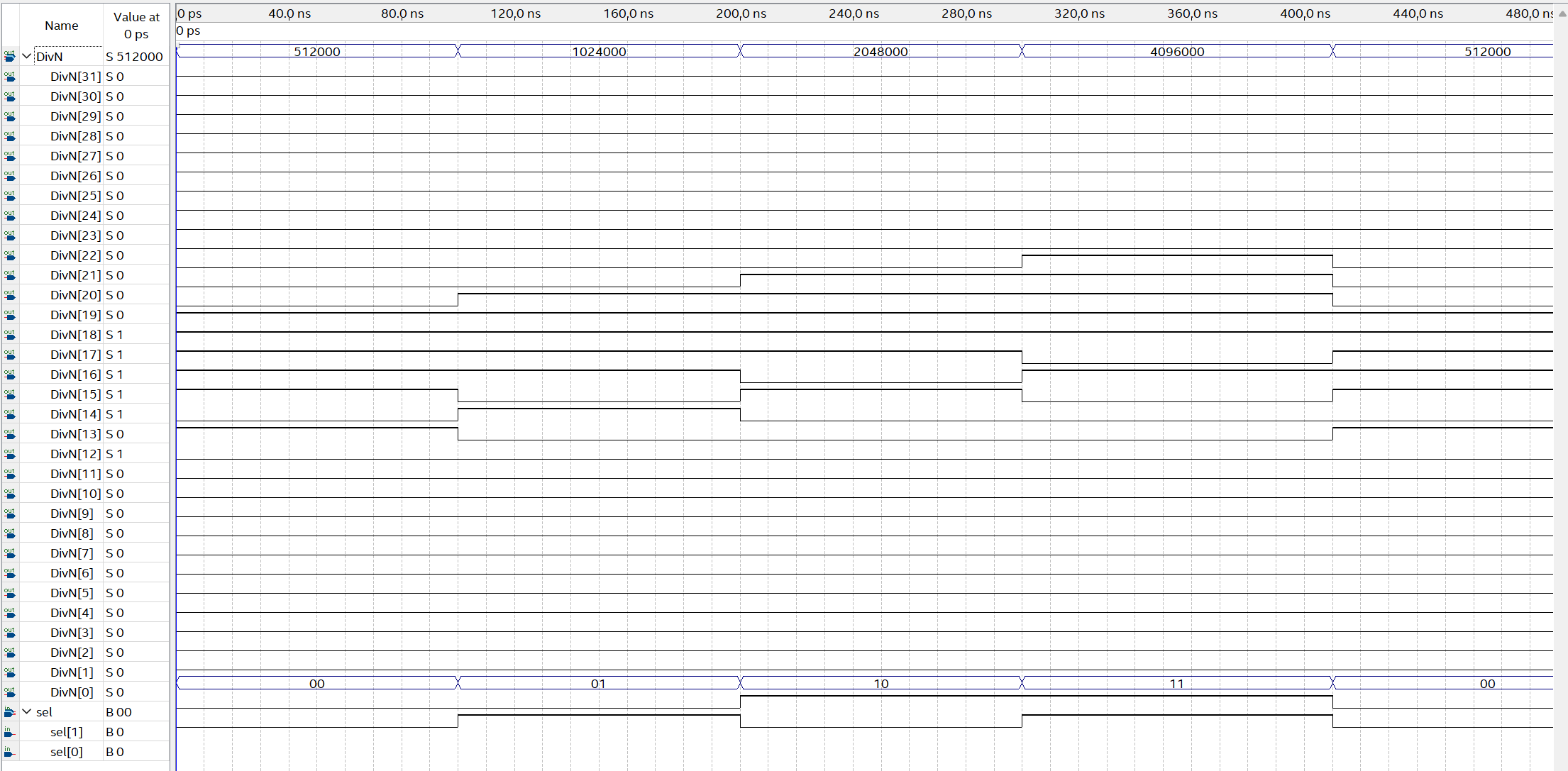


1. Divisor selector (DivNSel)
2. Verilog Code and Comment



1. Simulation

There are four set frequency: 512000, 1024000, 2048000, and 4096000. As input changes, the output would also be changed and sent to the frequency divider.

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1. Reflection

In our recent electrical engineering experiment, we utilized Verilog to design and control a stepper motor. The experiment incorporated components like a Divisor Selector, Changeable Frequency Divider, and a state control machine. With the experience gained from our first attempt, this experiment proceeded much more smoothly.

I realized that preparing the necessary code before class and then implementing it on the board during the lab session could significantly enhance the efficiency of the experiment. This approach can save time and allow for a more focused and productive laboratory experience.