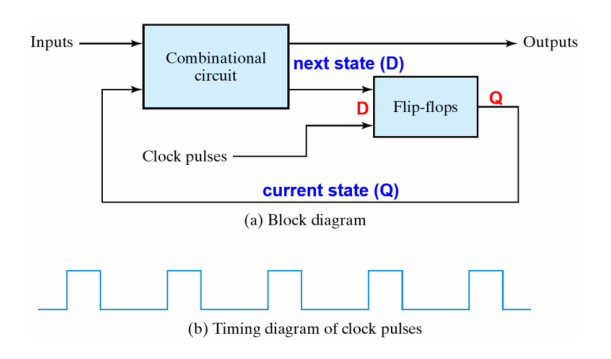
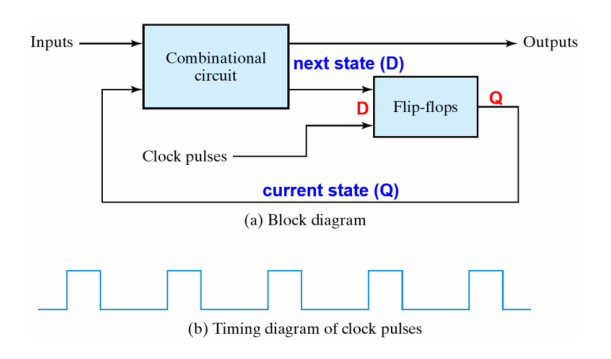
1. Purpose of the experiment
   1. Understand functions of D-type flip-flops and apply to implementing synchronous counters.
   2. Structure of a typical sequential logic design (finite state machine) is illustrated below.

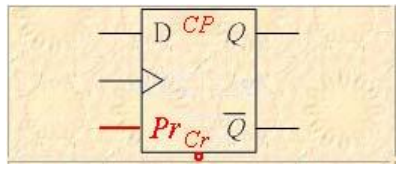


1. Function of the circuit
   1. The designed counter can operate in the following way (3→2→1→0 or 0→1→2→3)
   2. Function of the D-type Flip-flop:
      1. The output of the D-type flip-flop equals its data input where the input data can be stored.



Structure of a typical sequential logic design (finite state machine) is illustrated above.

* + 1. Its circuit design and characteristics are as follows:
       - 1. Block diagram of D-type flip-flop:



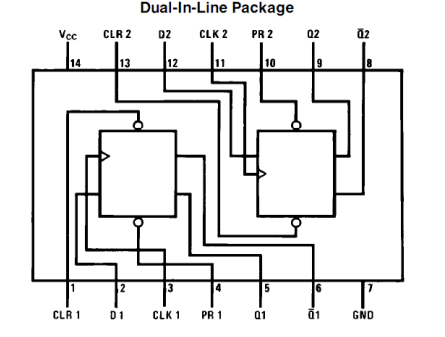
1. A data input: D (data input)

2. Two outputs: 𝑄 and 𝑄̅ are complementary.

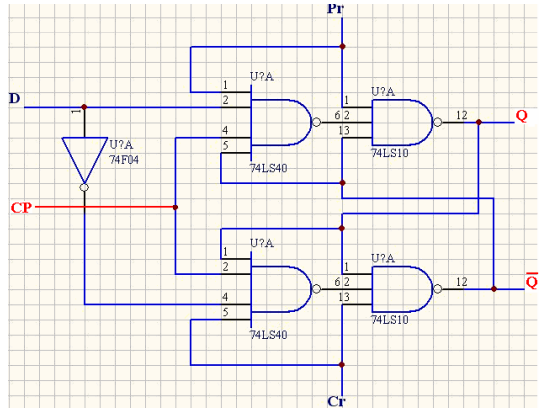
3. Two control inputs:

𝑃𝑟: default (Q = 1); 𝐶𝑟: clear (Q = 0)

* + - * 1. Pin connection of 7474:



* + - * 1. Circuit structure diagram:



* + - * 1. Truth table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | D |  |  |
| 0 | 1 | X | X | 1 |
| 1 | 0 | X | X | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

X: undefined (don’t care)

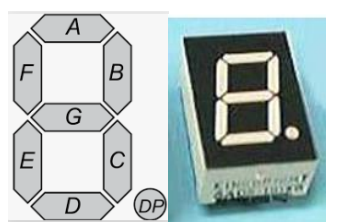
* + - * 1. Characteristic table:

|  |  |  |  |
| --- | --- | --- | --- |
|  |  | D |  |
| 1 | 1 | 0 | 0 |
| 1 | 1 |

* + - * 1. Excitation table:

|  |  |  |
| --- | --- | --- |
|  | | Input Condition |
|  |  | D |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

1. Description of each step of the experiment
   1. Make sure the counter function.



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Pattern |  |  |  |  |
| Number | 0 | 1 | 2 | 3 |
| Corresponding segments | a b c d e f | b c | a b d e g | a b c d g |

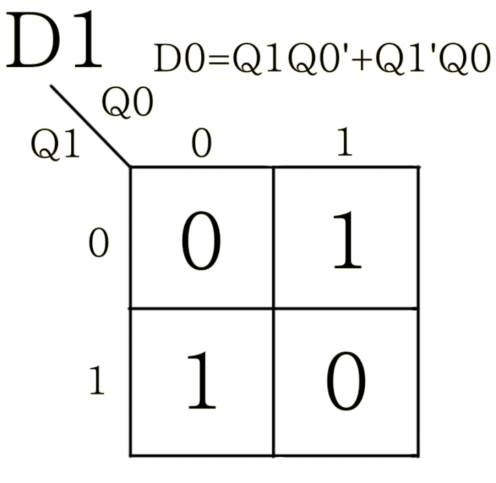
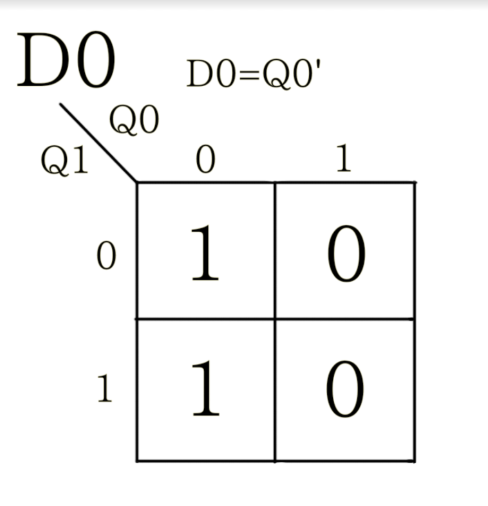
The above table is the desired displayed sequence of the specified numbers. Based on this table, we then design the corresponding counter composed of D flip-flop

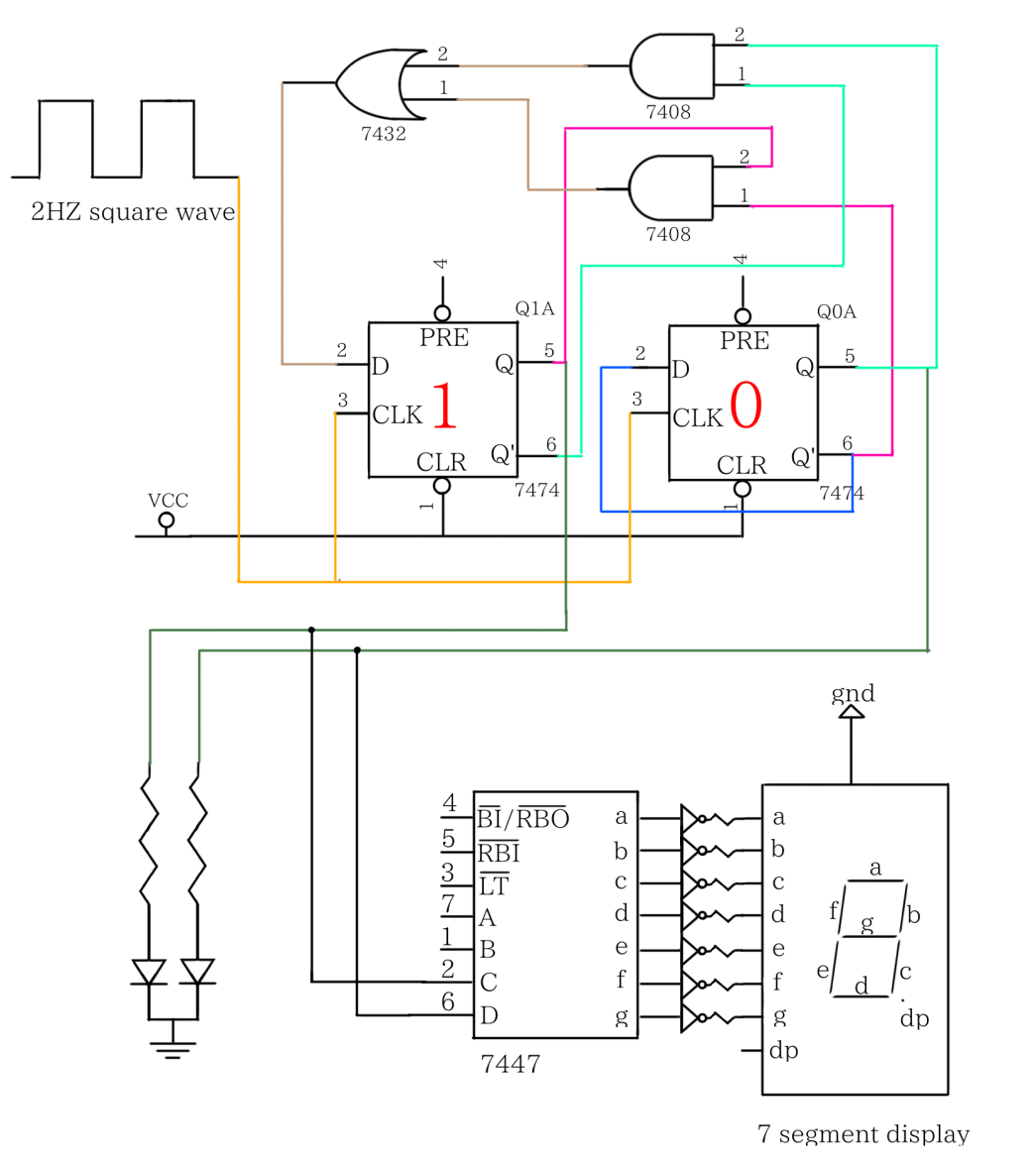
* 1. Generate the following table for the counter state (number) to be displayed:

|  |  |  |
| --- | --- | --- |
| State | (Current state) | (Next state) |
|  | 00 | 01 |
|  | 01 | 10 |
|  | 10 | 11 |
|  | 11 | 00 |

in the above table (MSB to LSB from left to right) are the two data outputs of the D-type flip-flop, which represent the current state; and (MSB to LSB from left to right) are the two data inputs of the D-type flip-flop, which represent the next state.

* 1. Design Karnaugh’s Map by the table from the previous step as follows:



* 1. Implement the logic circuit based on the previous step. 
  2. Apply a square wave input as clock with signal generator.

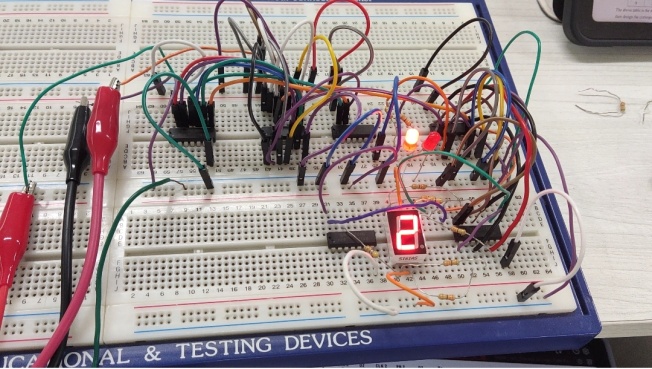
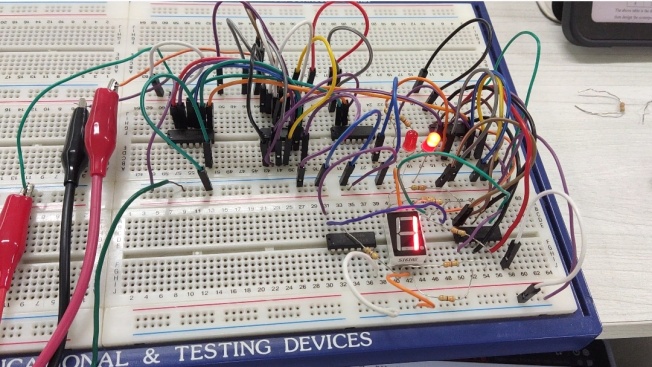
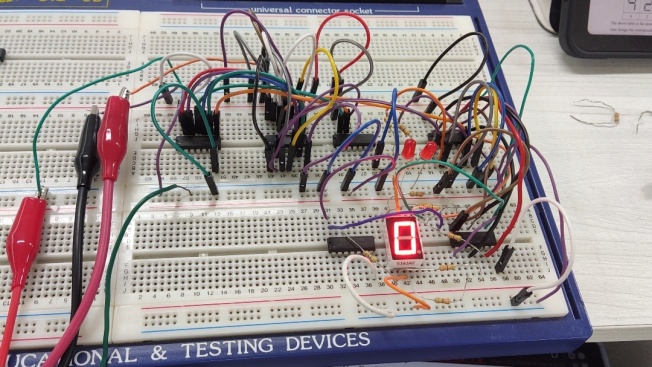
When the above circuit is implemented, use the signal generator to provide square wave as the clock signal. Note that the frequency should not be too high (recommendation: 1~2 Hz) for observation. Also note that the threshold voltage of D-type flip-flop is 1.5V, so the peak-to-peak value of the square wave must be larger than 1.5V, otherwise the sequential circuit cannot be driven.

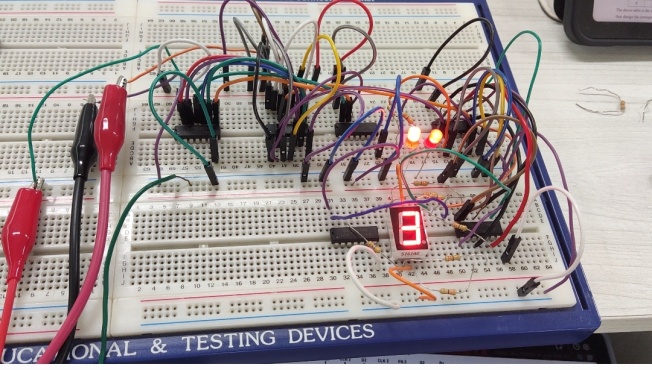
* 1. Test circuit.

When the previous five steps are completed, we can test our circuit. As shown in the circuit diagram, it is suggested to first use the two LEDs for testing. If the result is correct, then the seven segment display is connected (remember to connect to resistors before connecting to seven-segment display in order to prevent from being damaged). Before operating the project, make sure to initialize flip-flops using their set or reset functions (e.g., starting from the 00 state).

* + 1. Record the results

Since we take implement the circuit in the order of 0→1→2→3, our result is as following:





And the number cycled endlessly.

1. Checking item(s)
   1. Each team member must implement the circuits and make measurement. Those teams who have completed the experiment must ask a TA to check, and the TA will ask one of the team members to repeat the experiments and verify the results.
   2. After completing the experiments, all the components must be sorted (placed in the material box), the wires should be returned, and the instrument should be turned off. Clean up the seat and turn off the extension cord switch. After completion, you must ask a TA to check if you can leave.
   3. The IC is placed with the notch facing left, corresponding to the IC pin diagram, and each IC must be biased (VCC is connected to +5V, GND is connected to ground).
   4. When measuring voltage or current, start from the large scale, and then turn it down gradually to avoid damage to the meter.
   5. Reference diagram:

