AVR128DA Silicon Errata and Data Sheet Clarification

AVR128DA28/32/48/64

The AVR128DA28/32/48/64 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002183), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the AVR128DA28/32/48/64 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002183) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- \- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision		
		Rev. A6(1)	Rev. A7	Rev. A8
Device	2.2.1. Some Reserved Fuse Bits Are '1'	X	X	X
	2.2.2. CRC Check During Reset Initialization Is not Functional	X	X	X
CCL	2.3.1. The LINK Input Source Selection for LUT3 Is not Functional on 28- and 32-Pin Devices	X	X	X
CLKCTRL	2.4.1. PLL Status not Working as Expected	X	X	X
DAC	2.5.1. DAC Output Buffer Lifetime Drift	X	X	X
EVSYS	2.6.1. Port Pins PB[7:6] and PE[7:4] Are not Connected to the Event System	X	X	X
NVMCTRL	2.7.1. Flash Mapping Into Data Space not Working Properly	X	X	X
	2.7.2. Flash Multi-Page Erase Can Erase Write Protected Section	X	X	X
PORT	2.8.1. Digital Input on Pin Automatically Disabled When Pin Selected for Analog Input	X	X	X
RSTCTRL	2.9.1. BOD Registers not Reset When UPDI Is Enabled	X	X	X
SPI	2.10.1. SSD Bit Must Be Set When SPIROUTE Value = NONE	X	X	X
TCA	2.11.1. TCA1 Pinout Alternative 2 and 3 not Functional	X	X	X
	2.11.2. Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X	X	X
TCB	2.12.1. CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode	X	X	X
TCD	2.13.1. Asynchronous Input Events not Working When TCD Counter Prescaler Is Used	X	X	X
	2.13.2. CMPAEN Controls All WOx for Alternative Pin Functions	X	X	X
	2.13.3. Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used	X	X	X
TWI	2.14.1. The Output Pin Override Does not Function as Expected	X	X	X
	2.14.2. The 50 ns and 300 ns SDA Hold Time Selection Bits Are Swapped	X	X	X
	2.14.3. Flush Non-Functional	X	X	X
USART	2.15.1. Open-Drain Mode Does not Work When TXD Is Configured as Output	X	X	X
	2.15.2. Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode	X	X	X
ZCD	2.16.1. All ZCD Output Selection Bits Are Tied to the ZCD0 Bit	X	X	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 Some Reserved Fuse Bits Are '1'

For material with date code 2033 (manufactured in the year 2020, week 33) or older, the default fuse values are not compliant with the data sheet. The fuse values will read out as listed below:

- BODCFG = `0x10`
- OSCCFG = `0x78` (The device will use the OSCHF clock source)
- SYSCFG0 = `0xF2`
- SYSCFG1 = `0xF8`

Work Around

None.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.2.2 CRC Check During Reset Initialization Is not Functional

For material with date code 2136 (manufactured in the year 2021, week 36) or older, the CRCSRC bit field in the SYSCFG0 fuse is ignored during Reset initialization. A CRC check will not be performed during Reset initialization. CRCSCAN is only available from the software.

Work Around

None.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.3 CCL - Configurable Custom Logic

2.3.1 The LINK Input Source Selection for LUT3 Is not Functional on 28- and 32-Pin Devices

The LINK option (INSELn in LUT3CTRLB or LUT3CTRLC is '`0x2`') does not work; the output from LUT0 will not get connected as an input to LUT3. This occurs only on 28-pin and 32-pin devices.

Work Around

Connect LUT0 output to LUT3 input using the Event System.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.4 CLKCTRL - Clock Controller

2.4.1 PLL Status not Working as Expected

The PLL Status (PLLS) bit in the Main Clock Status (MCLKSTATUS) register will never be set to '1' if the Run Standby (RUNSTDBY) bit in PLL Control A (PLLCTRLA) register is set to '1' and no peripherals are requesting the PLL oscillator.

Work Around

None.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.5 DAC - Digital-to-Analog Converter

2.5.1 DAC Output Buffer Lifetime Drift

The offset of the DAC output buffer can drift over the device's lifetime if it is powered with the DAC output buffer disabled.

Work Around

Keep the DAC output buffer enabled (OUTEN in DACn.CTRLA is '1') continuously or compensate by measuring the DAC output voltage offset with the ADC and adjust the DAC data register value (DATA[9:0] in DACn.DATA) accordingly.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.6 EVSYS - Event System

2.6.1 Port Pins PB[7:6] and PE[7:4] Are not Connected to the Event System

Port pins PB[7:6] and PE[7:4] are not connected to the Event System. This is true for both input and output signals into the Event System on these pins.

Work Around

None.

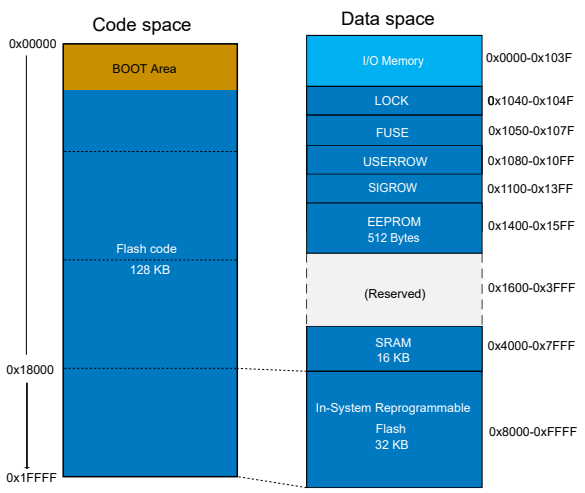
Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

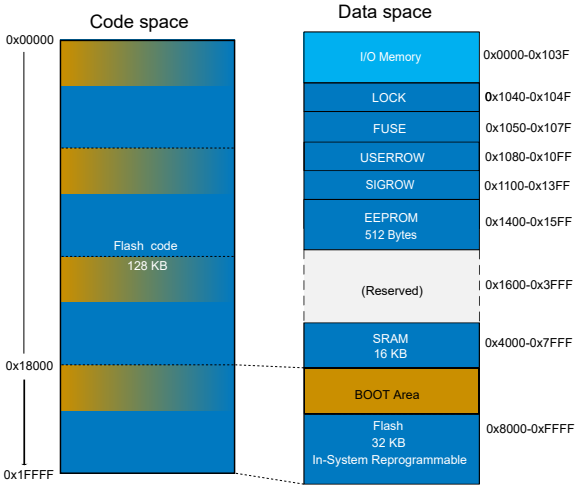
2.7 NVMCTRL - Nonvolatile Memory Controller

2.7.1 Flash Mapping Into Data Space not Working Properly

The inter-section Flash protection mechanism does not take into account the FLMAP bit field when checking if the address is in BOOT, APPCODE or APPDATA areas. It uses for comparison only the address offset between Flash start address in data space (0x8000) and the accessed address. This will cause the mirroring of the BOOT area in each Flash section selected by FLMAP (in blocks of 32 KB). Refer to the image below.



BOOT area for devices without issue



BOOT area for devices with issue

For read operations, the FLMAP bits work as documented when the Boot Read Protect (BOOTRP) bit is not enabled. For write operations, the inter-section Flash protection works properly only when FLMAP is set to `'0x00'`.

Work Around

Use only store program memory `(SPM)` instructions to write and load program memory `(LPM)` instructions to read Flash memory.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.7.2 Flash Multi-Page Erase Can Erase Write Protected Section

When using Flash Multi-Page Erase mode, only the first page in the selected address range is verified to be within a section that is not write-protected. If the address range includes any write-protected Application Data pages, it will erase them.

Work Around

None.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.8 PORT - I/O Configuration

2.8.1 Digital Input on Pin Automatically Disabled When Pin Selected for Analog Input

If an input pin is selected to be analog input, the digital input function for those pins is automatically disabled.

Work Around

None

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.9 RSTCTRL - Reset Controller

2.9.1 BOD Registers not Reset When UPDI Is Enabled

If the UPDI is enabled, the VLMCTRL, INTCTRL, and INTFLAGS registers in BOD will not be reset by other reset sources than POR.

Work Around

None

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.10 SPI - Serial Peripheral Interface

2.10.1 SSD Bit Must Be Set When SPIROUTE Value = NONE

When operating either SPIn module, when the PORTMUX.SPIROUTE selection is NONE, the $\overline{SS}$ pin must be disabled (CTRLB.SSD = 1) to maintain Host mode operation.

Work Around

None

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.11 TCA - 16-Bit Timer/Counter Type A

2.11.1 TCA1 Pinout Alternative 2 and 3 not Functional

It is not possible to configure TCA1 in PORTMUX.TCAROUTEA to use pinout alternatives 2 and 3.

Work Around

Use TCA1 pinout alternative 0 or 1.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.11.2 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to a NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset the count direction to default. The default is counting upwards.

Work Around

None.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.12 TCB - 16-Bit Timer/Counter Type B

2.12.1 CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CCMP and CNT registers act as 16-bit registers for read and write. They cannot be read or written independently.

Work Around

Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.13 TCD - 12-Bit Timer/Counter Type D

2.13.1 Asynchronous Input Events not Working When TCD Counter Prescaler Is Used

When configuring TCD to use asynchronous input events (CFG in TCDn.EVCTRLx is '0x2') and the TCD Counter Prescaler (CNTPRES in TCDn.CTRLA) is different from '0x0', events can be missed.

Work Around

Use the TCD Synchronization Prescaler (SYNCPRES in TCDn.CTRLA) instead of the TCD Counter Prescaler. Alternatively, use synchronous input events (CFG in TCDn.EVCTRLx is not '0x2') if the input events are longer than one CLK_TCD_CNT cycle.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.13.2 CMPAEN Controls All WOx for Alternative Pin Functions

When TCD alternative pins are enabled (TCD0 in PORTMUX.TCDROUTEA is not '0x0'), all waveform outputs (WOx) are controlled by Compare A Enable (CMPAEN in TCDn.FAULTCTRL).

Work Around

None.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.13.3 Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used

Halting TCD and waiting for software restart (INPUTMODE in TCDn.INPUTCTRLA is '0x7') does not work if compare value A is 0 (CMPASET in TCDn.CMPASET is '0x0') or Dual Slope mode is used (WGMODE in TCDn.CTRLB is '0x3').

Work Around

Configure the compare value A (CMPASET in TCDn.CMPASET) to be different from 0 and do not use Dual Slope mode (WGMODE in TCDn.CTRLB is not '0x3').

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.14 TWI - Two-Wire Interface

2.14.1 The Output Pin Override Does not Function as Expected

It overrides the output pin driver but not the output value when TWI is enabled. The output on the line will always be high when the value in the PORTx.OUT register is '1' for the pins corresponding to the SDA or SCL.

Work Around

Ensure that the values in the PORTx.OUT register corresponding to the SCL and SDA pins are '0' before enabling the TWI.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.14.2 The 50 ns and 300 ns SDA Hold Time Selection Bits Are Swapped

The bits corresponding to the SDA Hold Time (SDAHOLD) bit field in the TWIn.CTRLA register are swapped.

Work Around

Use the 50 ns bit field selection for the 300 ns hold time and vice versa.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.14.3 Flush Non-Functional

Issuing a Flush by writing to the FLUSH bit in TWIn.MCTRLB can cause the TWI Host to be stuck in the Unknown bus state (see BUSSTATE in TWIn.MSTATUS).

Work Around

Disable and re-enable the Host using the ENABLE bit in TWIn.MCTRLA. An ordinary operation does not require the use of FLUSH.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.15 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.15.1 Open-Drain Mode Does not Work When TXD Is Configured as Output

When configured as an output, the USART TXD pin can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work Around

Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.15.2 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

The Start-of-Frame Detection feature enables the USART to wake up from Standby sleep mode upon data reception. The Start-of-Frame Detector can unintentionally be triggered when the Start-

of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register is set, and the device is in Active mode. If the Receive Data (RXDATA) registers are read while receiving new data, the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is cleared. This triggers the Start-of-Frame Detector and falsely detects the next falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode. No interrupt will be triggered.

Work Around

Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Re-enable it by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

2.16 ZCD - Zero-Cross Detector

2.16.1 All ZCD Output Selection Bits Are Tied to the ZCD0 Bit

The Zero Cross Detector n Output (ZCDn) bits in the Pin Position (PORTMUX.ZCDROUTEA) register are tied to ZCD0. Any write to ZCD0 will be reflected in the ZCD1 and ZCD2 as well. Writing to ZCD1 and/or ZCD2 has no effect.

Work Around

Use the Event System or CCL to make the output of ZCD1 or ZCD2 available on a pin.

Affected Silicon Revisions

Rev. A6	Rev. A7	Rev. A8
X	X	X

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002183).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
E	12/2023	• Removed data sheet clarifications: – 3.1. Features – 3.2. FUSE - Configuration and User Fuses – 3.3. RSTCTRL - Reset Controller – 3.4. TWI - Two-Wire Interface – 3.5. Electrical Characteristics - Peripheral Power Consumption – 3.6. Electrical Characteristics - Memory Programming Specifications – 3.7. Electrical Characteristics - VREF – 3.8. Electrical Characteristics - DAC – 3.9. Electrical Characteristics - ADC
D	02/2022	• Added data sheet clarifications: – 3.1. Features – 3.2. FUSE - Configuration and User Fuses – 3.5. Electrical Characteristics - Peripheral Power Consumption – 3.6. Electrical Characteristics - Memory Programming – 3.7. Electrical Characteristics - VREF – 3.8. Electrical Characteristics - DAC – 3.9. Electrical Characteristics - ADC • Updated data sheet clarifications: – 3.3. RSTCTRL - Reset Controller – 3.4. TWI - Two-Wire Interface
C	10/2021	• Updated errata: – Device: *Some Reserved Fuse Bits Are '1'* – Device: *CRC Check During Reset Initialization Is Not Functional* – USART: *Start-of-Frame Detection Can Unintentionally Be Enabled in Active Mode When RXCIF Is '0'* • Added errata: – CLKCTRL: *PLL Status Not Working as Expected* – DAC: *DAC Output Buffer Lifetime Drift* – TCD: *Halting TCD and Wait for SW Restart Does Not Work if Compare Value A Is 0 or Dual Slope Mode Is Used* – TWI: *Flush Nonfunctional* – Electrical Characteristics: *Endurance of PFM Cell lower is than specified*

.....continued

Doc. Rev.	Date	Comments
B	11/2020	• Add new device revision (A8) • Added errata: – Device: *Some Reserved Fuse Bits Are '1'* – Device: *CRC Check During Reset Initialization Is Not Functional* – CCL: *The LINK Input Source Selection for LUT3 Is Not Functional on 28- and 32-Pin Device* – RSTCTRL: *BOD Registers Not Reset When UPDI Is Enabled* – TCA: *Restart Will Reset Counter Direction in NORMAL and FRQ Mode* – TCB: *CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode* – TCD: *Asynchronous Input Events Not Working When TCD Counter Prescaler Is Used* – TCD: *CMPAEN Controls All WOx for Alternative Pin Functions* – USART: *Start-of-Frame Detection Can Unintentionally Be Enabled in Active Mode When RXCIF Is '0'* – ZCD: *All ZCD Output Selection Bits Are Tied to the ZCD0 Bit*
A	04/2020	Initial document release

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