

RACHANA AITHAL

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EDUCATION

Georgia Institute of Technology

Aug 2022 - May 2024

Master of Science, Computer Science

GPA: 4.0/4.0

PES University

Aug 2016 - Jul 2020

Bachelor of Technology, Computer Science

CGPA: 9.53/10

RESEARCH EXPERIENCE

Department of Computer Science, Georgia Tech, *Graduate Thesis*

Aug 2023 - Present

- Leveraging Application information for DRAM schedulers.

Department of Computer Science, Georgia Tech, *Graduate Research*

Jan 2023 - Jun 2023

- Leveraging a cache miss predictor to hide memory access latency.
- Use user-level threads and rapid context switching in user space to mitigate the effects of long memory delays.

Center for Cloud Computing and Big Data, PES University, *Undergraduate Research*

Jan 2018 - Jan 2020

- Co-authored a poster paper titled "*Hardware Accelerated Matrix Multiplication using a 400 MHz Systolic Array on a CPU+FPGA Platform*" presented at *VLSI design conference 2020*, the submission won the best poster paper award in the user design track category
- Developed a *patent pending* "Elastic Pipelines for Data Processing (in hardware)", No. 201941028170 filed at the Indian patent office

Department of Computer Science, PES University, *Undergraduate Thesis*

Aug 2019 - Jun 2020

- Co-authored a paper "*Exploration of Cross-lingual Summarization for Kannada-English Language Pair*", Conference Proceedings of *17th International Conference on Natural Language Processing (ICON 2020)*

WORK EXPERIENCE

Google, *HW Intern*

May 2023 - Aug 2023

- Worked with the Google cloud TPU and network chips design and verification teams.
- Built a comprehensive tool for Automatic generation of System Verilog UVM test benches and test environment for a given module design specification.

Amazon, *SDE, SDE Intern*

Jan 2020 - Jul 2022

- Designed and developed support for partners to onboard a new type of feature on the Retail Website Detail page
- Built a transpiler to convert code in a flavour of TypeScript to Java
- Worked on large-scale internal service migration and software upgrades on the Amazon Detail Page
- Was responsible for Retail Website Detail Page preparation for a peak sale event on Amazon worldwide

Walmart Labs, *SDE Intern*

May 2019-July 2019

- Contributed to the B2B website in India, included working on SAP, Spring Boot, and basic Hybris

PROJECTS

- Implemented **fast regular expression matching** on FPGAs using Nondeterministic Finite Automata(NFA)
- Built **NLP preprocessing library** in C
- Designed and developed **pipe stage modules** on FPGAs as an alternative for FIFO queues for data transfer, along with splitter and merger extensions for better data input and output.
- Implemented a C++ simulation of in-order and out-of-order **multi-stage pipeline** and branch prediction.
- Implemented simple **distributed key-value store** that is scalable, available, and resilient to temporary node failure.

ACTIVITIES

- **Teaching assistant** to a Graduate Level 'High Performance Computer Architecture' course in GaTech
- **Teaching assistant** for 'Digital Design and Computer Organization' course and Lab in PESU
- **Runner-up** in the Hactober fest, a coding competition by conducted by ACM-W, PESU
- Volunteer at the Peer Teaching Program at PESU to help other students with their academics

SKILLS

Programming Languages
Tools

Python, C/C++, SQL, Verilog, HTML, JS, PHP, Django, Java
Arduino, Intel Quartus, Shell