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A Comprehensive Study and Validation of a Power-HIL Testbed for Evaluating Grid-Connected EV Chargers

Isuru Jayawardana, *Student Member*, IEEE, Carl N. M. Ho, *Senior Member*, IEEE, and Yi Zhang, *Fellow*, IEEE

***Abstract*— Integration of excessive electric vehicle (EV) chargers into the low voltage (LV) network may introduce new challenges. Power hardware in the loop (PHIL) simulations can be used for evaluating such systems as it provides a flexible testing platform to study the overall system as well as individual devices. To facilitate a proper PHIL simulation, a precise mathematical model of the PHIL testbed is required. This paper presents a comprehensive small signal model capable of describing the dynamics of a PHIL testbed developed for evaluating grid-connected EV chargers. The PHIL testbed consists of a PHIL-based battery emulator (BE) and a grid emulator (GE) to mimic the DC side battery energy storage system (BESS) and the AC side LV grid behavior, respectively. A mathematical framework is developed to analyze the stability and predict the accuracy of both PHIL-based emulators. The BE in this paper considers a switch-mode power amplifier (PA). Thus, design strategies for its linear controller are also discussed in the context of cascaded DC-DC configuration. An experimental PHIL platform based on a real time simulator (RTS has been used to validate theoretical predictions and confirm developed models. Finally, the validated PHIL test has been employed for analyzing the performance of a commercial EV charger and its interactions with a weak LV network simulated in RSCAD™/EMTDC™.**

***Keywords*— Real-time emulation, hardware-in-the-loop, DC-DC power converters, small signal modelling, battery charger.**

NOMENCLATURE

v_B	Output voltage of battery emulator
i_B	Output current of the battery emulator
v_{Bref}	Voltage reference of the PA in PHIL-based BE
f_S	Switching frequency
R_d	Parallel resistance at the DC power source output
P_{cmax}	Maximum power dissipation in R_d during the charging operation
v_{OC}	Open-circuit voltage of the battery model
R_S	Resistance responsible for the instantaneous voltage drop for a step response in the battery model
R_{t_S}, C_{t_S}	Battery model RC values that account for short-term transients
R_{t_L}, C_{t_L}	Battery model RC values that account for long-term transients
r_C, r_L	ESR of the single-stage capacitor and inductor (Battery emulator's PA)
Q	Battery capacity
SOC_{init}	Initial state of charge level
v_{bat}, i_{bat}	Voltage and current of a single Li-ion battery model
N_s, N_p	Series-and-parallel connected batteries in a BESS
v_{Bat}, i_{Bat}	Voltage and current of a BESS model
$Z_{b,eq}$	Small signal equivalent impedance of the BESS
Z_{DUT}	Closed-loop output/input impedance of DUT
Z_{outCL}	Closed-loop output impedance of the load converter during charging
Z_{inCL}	Closed-loop input impedance of the load converter during discharging
R_e	Small signal load resistance when EV battery charger in CV mode
k_P, k_I	Proportional and integral gain of PI controller in Battery emulator's PA
G_M	PWM scheme gain of PI controller in BE PA
H	Voltage sensor feedback gain in BE PA
Z_S	Equivalent grid impedance
R_g, L_g	Grid resistance and inductance
Z_{DUTac}	AC side input impedance of the EV battery charger
T_b	Latency of linear PA
T_a	Cut-off of linear PA
T_{cp}	Time constant of the lead compensator
T_{fil}	Filter cut-off of the current feedback signal
$\tilde{x}$	Small signal term of any given variable x

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I. INTRODUCTION

Electric vehicles (EVs) have become increasingly popular and mature in terms of their technology, and accordingly, their rapid growth is expected to persist in the coming decades [1]. Subsequently, EV charging is on the verge of becoming a

commodity. Among residential communities, the use of onboard EV chargers has become a preferable choice simply for its ability to connect to a single-phase residential plug with functions of grid-to-vehicle (G2V) and vehicle-to-grid (V2G) operations [2], [3]. Extensive addition of EV chargers into the low-voltage (LV) grid may create power quality (PQ) issues such as voltage sag and harmonics, and alternatively, EV chargers could also be affected by PQ issues originated elsewhere [4]. These scenarios have urged to conduct studies for evaluating PQ issues in the LV grid as well as to develop advanced EV chargers.

Most of such grid integration studies have remained at the off-line simulation stage because their hardware implementation and experimental verification are expensive and perhaps not even feasible to reproduce under complete experimental setups [5]. Issue in simulation studies is that the models of non-linear power electronics (PE) converters may not include all the dynamics involved with the actual converter to obtain accurate results [6]. Thus, in some studies, simulation results are validated through experiments by installing a prototype system with standalone source emulators and carrying out laboratory tests. Consequently, real time power hardware in the loop (PHIL) simulations have gained attention in grid integration studies and physical device evaluations as it offers a platform for integrating the PE-based physical hardware with real time (RT) software simulations [7]-[10].

The PHIL simulation can be described as a hybrid technique that decouples the original circuit using a power interface as such, a part of the circuit is being simulated inside the real time simulator (RTS), and the rest of the circuit is completed with an actual device under test (DUT) [11]. The hybrid nature of PHIL simulations makes it well-suited for evaluating grid-connected EV chargers. It allows to test and validate both the physical EV charger and the LV grid it operates with several attractive features such as reduced cost, less time, scalability, repeatability, flexibility and perhaps most importantly with low-risk testing [12]. Moreover, the PHIL concept is already proven and adapted in applications such as grid-connected PV [9], [10] and battery energy storage system (BESS) integrations [13], [14] as a grid emulator. Also, it has been adopted for emulation of PV arrays [15], wind turbines [16], fuel cells [17], battery [18], [19], and electric machines [20], [21] to examine respective interconnected systems. Hereafter, the PHIL setup developed to emulate a source is referred to as a PHIL-based emulator in this paper. Key characteristics, pros, and cons of reported PHIL-based emulators in the literature targeting different applications are summarized in Table I.

In this work, a PHIL testbed configuration composed of two PHIL simulations is considered for evaluating grid-connected EV chargers, as shown in Fig. 1. Unlike conventional PHIL grid integration testbeds based on standalone source emulators [9], [10] both battery source and grid network are emulated through PHIL simulations. The PHIL-based battery emulator (BE) provides a platform for conducting burn-in tests with enhanced flexibility for different commercial battery arrays compared to standalone BEs, and it takes advantage from the grid integration testbed since RTS is already in place [19], [22], [23]. Although

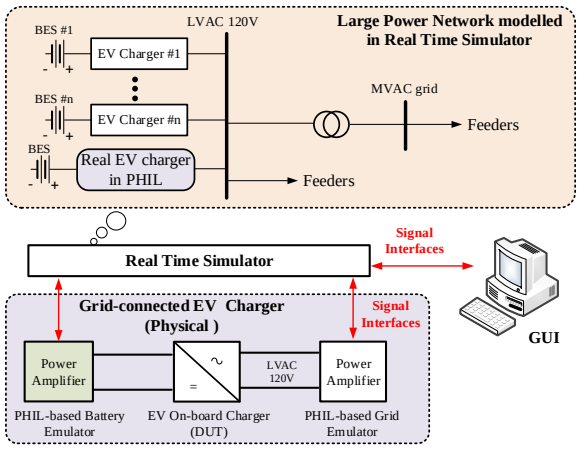


Fig. 1 PHIL test configuration for grid-connected EV chargers.

the implementation of PHIL simulation of battery is well known [18], [19], the detailed modelling and analysis of the PHIL-based BE have not been sufficiently addressed in the literature. The presence of an EV charger at the output of the PHIL-based BE composed of a switch-mode power interface creates a cascaded DC-DC configuration. Thus, a detailed model of the cascaded DC-DC system is necessary to design the classical linear controller of the source-side converter to avoid the negative impedance instability [24], [25]. Further, the stability and accuracy studies of a switch-mode power amplifier (PA) interface for PHIL simulations are mostly developed with small signal models derived considering resistive loads [12], [26]-[28]. Thus, possible stability degradation issues at the common dc link between the PHIL-based emulator and the EV charger have not been assessed in PHIL testbed applications. Therefore, this paper aims to address these deficiencies by deriving a comprehensive small signal model of the PHIL-based BE, including the virtual battery model, power interface and impedance characteristics of the DUT and analyzing the stability and accuracy of PHIL simulation. Design procedure for switch-mode PA controller of BE is provided based on the cascaded DC-DC system small signal model.

Additionally, this work provides a systematic approach for designing and implementing a PHIL testbed with two PHIL simulations to test grid-connected EV chargers and conduct related system studies. The paper is organized as follows. The PHIL simulation concept and its key elements are reviewed briefly in Section II. Section III describes the comprehensive system architecture of the PHIL testbed, including the implementation of power interfaces for both DC and AC sides of the EV charger. Detailed small signal model of the PHIL-based battery emulator with interconnecting EV charger is presented in Section IV for stability and accuracy analysis. Also, mathematical framework of the PHIL-based GE is summarized to determine stability and accuracy analysis. Section V shows the experimental performance of the PHIL testbed with a commercial EV charger to demonstrate the application of the platform. In Section VI, a case study is conducted by integrating the PHIL simulation of EV charger with a weak grid scenario simulated in RTS, and Section VII concludes the paper.

TABLE I
CHARACTERISTICS COMPARISON OF EXISTING PHIL-BASED SOURCE EMULATORS

Applications	Interface Algorithm	Power Amplifier	Pros	Cons
PHIL-based grid emulator [9]	Voltage type Ideal Transformer Method	Linear Power Amplifier	Easy implementation, Accuracy, Enhanced Flexibility in testing interface PE converters	Stability Issues
PHIL-based PV emulator [15]	Current type Ideal Transformer Method	Synchronous Buck Converter	Easy implementation, Accuracy, Enhanced Flexibility in testing PV converters	Stability Issues, Transient response limited by the interface devices
PHIL-based wind turbine emulator [16]	Sim-Stim interface	Voltage Source Converter as a controlled power source	Accuracy, Scaling between software and hardware	Stability Issues, Wind-turbine emulation includes machine side and grid converters
PHIL-based fuel cell emulator [17]	Voltage type Ideal Transformer Method	Commercial DC power source	Easy implementation, Accuracy, Scaling allows reducing the cost and complexity	Stability Issues
PHIL-based battery emulator [20]	Voltage type Ideal Transformer Method	Active frond-end Unit and Voltage Source Inverter	Easy implementation, Accuracy, Flexibility in testing BES converters	Stability Issues

II. REVIEW OF PHIL SIMULATIONS

A basic PHIL simulation can be illustrated by Fig. 2, in which an original circuit is formed into a hybrid configuration of software (i.e., simulation in RTS) and hardware (i.e., DUT) through a power interface. The PA is required to amplify the signals from RTS, and real power is exchanged between the PA and the DUT. The signal links between the RTS and PA/sensor can be either analog or digital depending on the input/output(I/O) devices of both the RTS and the PA [11]. Typically, the power interface consists of PA, analog-to-digital

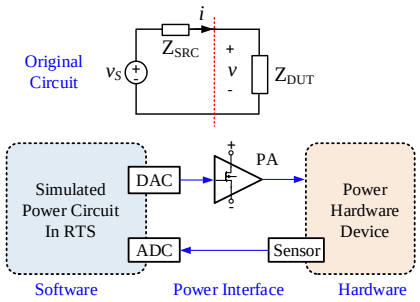


Fig. 2 Orginal circuit vs Basic configuration of the PHIL simulation.

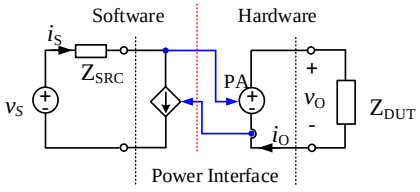


Fig. 3 The PHIL simulation with a voltage-type ITM IA.

converter (ADC), digital-to-analog converter (DAC) and sensor as shown in Fig. 2. In PHIL, the interface algorithm (IA) determines how the signals are exchanged between RTS and DUT. The IA can be either voltage and/or current type, depending on the selected PA. Several IAs are presented in the literature, including the ideal transformer method (ITM), the transmission line model (TLM), the partial circuit duplication (PCD) and the damping impedance method (DIM) and, their performance is analyzed extensively in [11], [29]-[31]. For the purpose of this paper, ITM IA is reviewed. The ITM is the most commonly used IA due to its high accuracy, low computational requirement and easy implementation. E.g., a general configuration of PHIL simulation with a voltage-type ITM TA is shown in Fig. 3, in which voltage is applied to the terminals of the DUT via the PA and current measured from the DUT is sent back to the RTS as a feedback signal.

The PA is also a key element in the PHIL technique, and ideally, it should have infinite bandwidth and zero-time delay. Thus, linear PAs are used in PHIL applications for their high system bandwidth and short time delay [32]. Recently, switch-mode PAs with improved dynamic response are also being used mainly for their advantages of high efficiency, high power density and low cost than linear PAs [33],[34]. In the linear PA, semiconductor switches operate in the linear region (e.g., class A, class B, class AB), whereas semiconductor devices in the switch-mode PA operated in either fully ON or fully OFF states [35]. These differences in the operating principles lead to contrasting characteristics between the linear and switch-mode PAs [32], [33]. Further, switch-mode PAs have been extensively used in literature for standalone BEs targeting accurate emulation of real batteries. The topologies that consider in BEs include; DC-DC buck-boost converter [36], three-phase interleaved boost [37], three-phase synchronous DC-DC buck converter [19], multi-phase synchronous DC-DC buck converter [38], cascaded dual active bridge (DAB) [39]. Multi-phase configurations are considered to maintain a lower output current ripple without raising the switching frequency (f_S). All these topologies must be equipped with a reversible power supply at the front end to handle the reverse current during charging mode. Typically, the reversible supply is realized with an active rectifier circuit [19] or a resistive dissipation circuit with a blocking diode [36].

Key limitation of the PHIL is the components involved in the power interface introduce time delays and limited bandwidth that do not exist in the original circuit. This would affect the stability and accuracy of the PHIL simulation [26]-[31]. Therefore, the stability and accuracy of the PHIL simulations with different IAs such as ITM, damping impedance method (DIM) have been extensively studied in the literature [29], [31]. Most straightforward method to evaluate the stability of a PHIL simulation system is the application of the Nyquist stability criterion on the open-loop transfer function of the PHIL system [27]. Accuracy of a PHIL simulation can be evaluated by methods proposed in [30], [40]. Two crucial factors for the stability of ITM IA are the loop delay and the impedance ratio between simulation and hardware. The time delay of the power interface is primarily determined based on the simulation time step of the RTS and PA characteristics. The required minimum simulation time step depends on the computational capability of

RTS, which again depends on the size of the simulated network, levels of details of the model and simulation hardware [41]. Also, digital link between RTS and PA with Aurora protocol is introduced to eliminate ADC and DAC converters and there by reducing the latency in the power interface [41]. Nonetheless, the ITM interface may pose some stability and accuracy issues in the PHIL experiment depending on case-specific factors like the impedance ratio between simulation and hardware and non-idealities in the power interface. Hence, it is vital to investigate the stability of a given PHIL-based system to understand the impact of power interface and DUT prior to a PHIL experiment.

III. Configuration of the PHIL Testbed

Two PHIL simulations form the PHIL testbed for evaluating EV chargers to emulate both the DC side battery behavior and the AC side LV grid behavior, as shown in Fig. 4. The RT simulations are implemented using the RTS from RTDS Technologies Inc. and the RSCAD™ user interface. The following subsections discuss the critical elements of the PHIL platform in detail.

A. PHIL-based Battery Emulator

As shown in Fig. 4, PHIL-based BE is composed of a battery model in RTS, signal interface, and bi-directional switch-mode PA and implemented using the voltage-type ITM IA. A voltage-type ITM IA is employed since voltage-mode (VM) control is used in the PA. Fig. 5 illustrates how an original BESS simulation is extended to its corresponding PHIL-based simulation via voltage-type ITM IA. The circuit is decoupled at the load converter (i.e., EV charger) connecting point as marked in Fig. 5 (a), and a power interface is added to complete the circuit with a DUT, as shown in Fig. 5. The BESS voltage from the real time battery model in RTS (v_{Bat}) is interfaced to the EV charger output terminals through DAC and switch-mode PA and current measurement of the EV charger (i_B) is sent back to the RTS to complete the virtual battery model simulation. In this way, PA operates to imitate the charge/discharge characteristics of a given battery model and real power is exchanged between PA and EV charger. A digital low-pass filter is used to eliminate the noise associated with the current measurement, and its parameters should be selected to offer an acceptable trade-off between noise reduction, improve stability and system response.

a) Switch-mode PA

The BE should be able to emulate the non-linear characteristics of batteries together with its power flow. Therefore, switch-mode PA of the BE is generally operated in VM control with a possibility of bidirectional power flow to ensure both charging/discharging operations. In this work, the PA is realized using a bidirectional DC-DC synchronous buck converter with a reversible dc power supply and a digital controller. The detailed architecture of the VM PA is shown in Fig. 6. A DC power source with a parallel resistor (R_d) is used for implementing reversible power supply (i.e., front end converter of the BE). The R_d is designed considering the maximum power during the charging operation (P_{cmax}) (i.e.,$R_d < v_S^2/P_{cmax}$). Note that, design and control of active front end converter for the BE is not the scope of this paper. As shown in Fig. 6, a linear PI control with pulse width modulation (PWM) scheme is used to regulate the output voltage of PA (v_B) at given voltage reference (v_{Bref}). The PI control parameters can be designed using cascaded system model as presented in Section IV-A-a.

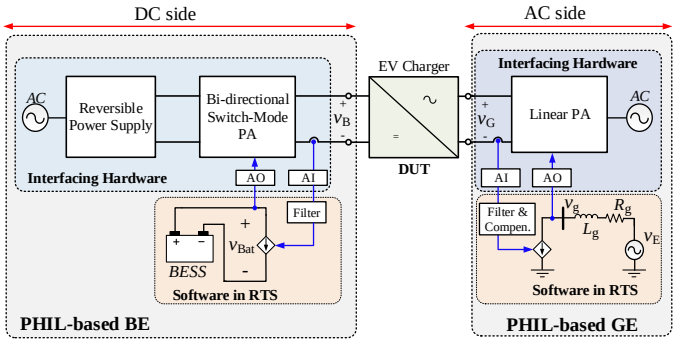


Fig. 4 Detailed block diagram of the PHIL test platform for EV chargers.

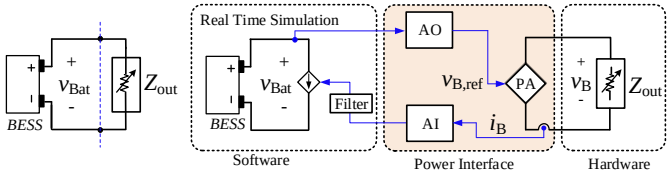


Fig. 5 BESS (a) with real time simulation, and (b) with PHILS.

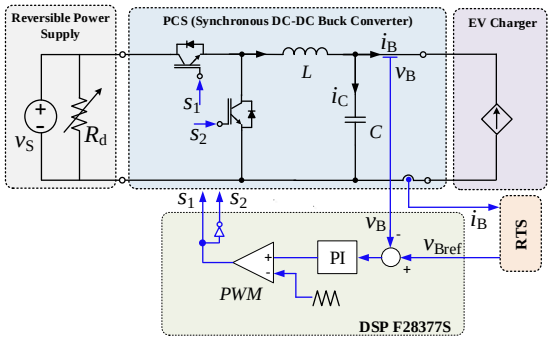


Fig. 6 Architecture of the bi-directional switch-mode PA for BE.

b) Battery Model and Simulation in RTS

The battery model is an integral part of the BE accuracy. It has been developed with various approaches to capture the real battery characteristics for specific purposes, from battery design, performance evaluation to circuit simulation. In BEs, equivalent circuit models (ECM) are often employed to represent the real battery for their simulation ability, less complexity, and offer reasonable accuracy compared to electrochemical models [43]. In this work, the Min/Rincon Mora et al. model [43] is adapted to represent the Lithium-ion (Li-ion) battery dynamics in RT simulation. Li-ion batteries are chosen for emulation in this work as they are commonly used in EVs for their high energy density, long lifetimes, and lightweights. Fig. 7 shows the equivalent electrical circuit of the Min/Rincon Mora et al. model consisting of a series resistor and two RC parallel networks for representing the battery's electrical behavior, including short-term and long-term transient response [43].v_{OC} is the open-circuit voltage; R_S is responsible for the instantaneous voltage

drop of step response; R_{t_S} and C_{t_S} account for short-term transients, while R_{t_L} and C_{t_L} are responsible for long-term transients. However, this model has not considered the thermal dependency of the circuit parameters and the battery lifetime modelling aspects. In [43], all the model parameters have been derived as a function of the state of charge (SOC) based on experimental results of a commercial Li-ion polymer battery (TCL-PL-383562) and its technical specifications are given in Table II. As a function of SOC, expressions for model parameters are given by (1)-(6).

$$v_{OC}(soc) = -1.031e^{-35\,SOC} + 3.685 + 0.2156\,SOC - 0.1178\,SOC^2 + 0.3201\,SOC^3, \quad (1)$$

$$R_S(soc) = 0.1562e^{-24.37\,SOC} + 0.07446, \quad (2)$$

$$R_{t\_S}(soc) = 0.3208e^{-29.14\,SOC} + 0.04669, \quad (3)$$

$$C_{t\_S}(soc) = -752.9e^{-13.51\,SOC} + 703.6, \quad (4)$$

$$R_{t\_L}(soc) = 6.603e^{-155.2\,SOC} + 0.04984, \quad (5)$$

$$C_{t\_L}(soc) = -6056e^{-27.12\,SOC} + 4475. \quad (6)$$

The SOC of the battery can be estimated using the Coulomb counting method, in which the charging/discharging current of the battery is measured and integrated with its value over time [42]. Thus, in RT simulation, SOC can be calculated at each simulation time step (T_S) with trapezoidal rule of integration as given below,

$$SOC[k] = SOC_{init} + \left(\frac{T_S}{Q}\frac{i_{bat}[k] + i_{bat}[k-1]}{2}\right), \quad (7)$$

where Q is the battery capacity, SOC_{init} is the initial SOC level. The V-I characteristics equation of the Li-ion battery is derived by applying Kirchhoff's voltage law for the equivalent circuit model shown in Fig. 7, and it is given in the Laplace domain by,

$$v_{bat}(s) = v_{OC}(s) - Z_b(s) i_{bat}(s), \quad (8)$$

$$\text{where } Z_b(s) = R_S + \frac{R_{t\_S}}{1 + R_{t\_S} C_{t\_S} s} + \frac{R_{t\_L}}{1 + R_{t\_L} C_{t\_L} s}. \quad (9)$$

A single Li-ion battery model can be scaled up to determine the BESS model composed of series-and-parallel connected batteries (N_s, N_p) by modifying v_{OC} and RC network by considering N_s and current injection through the circuit with N_p. This model can be implemented in any RT circuit simulator that accepts embedded programming RTS can complete the calculation within the specified time step in real-time.

TABLE II
TECHNICAL SPECIFICATIONS FOR TCL-PL-383562 LI-ION BATTERY

Parameter	Value	Parameter	Value
Nominal Capacity	0.85 Ah	Max. Charge current	1275mA (1.5C)
Nominal Voltage	3.7 V	Charged Voltage	4.2 V

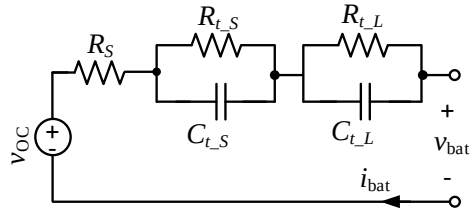


Fig. 7 The electrical equivelant circuit of the Min/Rincon Mora model [43]

B. PHIL-based Grid Emulator

The schematic of PHIL-based GE with all measurement points at hardware and software runtime environment is shown in Fig. 4. Like the PHIL-based BE, it is developed by decoupling the grid network simulation using the voltage-type ITM IA. The AC bus voltage from the simulated power system network in RTS is interfaced to the EV charger input side through a DAC and PA. The current measurement is sent back to the RTS to compute the state of the modelled power system network. In this paper, voltage amplification is realized by using a commercial linear PA that should be able to source real and reactive power. Further, a digital low-pass filter is used to eliminate the noise associated with the current measurement. It would improve the stability margin of the PHIL simulation due to the presence of a left half-plane pole [9], [26]. However, the filter would introduce an additional magnitude attenuation and phase lag in the current feedback signal. Therefore, as suggested in [9], a compensator that offers an origin zero and one pole at a lower frequency than nominal line frequency (i.e., 60 Hz) is added to minimize the magnitude attenuation at the desired frequency range (15 Hz to 300 Hz) and compensate for phase lag associated with the filter. Another important factor for PHIL-based GE is the level of details of the AC network simulated in RTS. A simple grid equivalent network that consists of an AC voltage source in series with grid impedance, as shown in Fig. 4, can be considered when evaluating EV charger performance. For system-level studies, a single-phase equivalent representation of a benchmark LV network can be implemented in RTS, and it should be interfaced to the EV charger through the PA.

IV. MODELLING AND ANALYSIS OF THE PHIL TESTBED

A. PHIL-based Battery Emulator

This Section aims to conduct small signal stability and accuracy analysis of the PHIL-based BE loaded by an EV charger:

1. The cascaded DC-DC system model composed of switch-mode PA and EV charger is presented to design the linear controller of the PA and to evaluate the cascaded system's stability.
2. The detailed model of the PHIL-based BE is presented to investigate overall system stability and predict PHIL simulation accuracy.

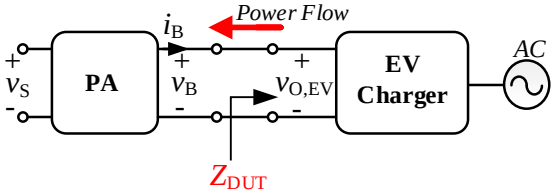


Fig. 8 Cascaded DC-DC configuration between the PA and EV charger.

a) Cascaded system model for control design

Fig. 8 shows the cascaded DC-DC configuration in which the PA is considered as the source converter and the EV charger as the load converter. In the cascaded system model, the load converter can be represented by its closed-loop output/input

impedance (Z_{DUT}) (i.e., seen by the PA) depending on whether the load converter is operated in charging/discharging mode, respectively. Thus, the small signal relation between v_B and i_B is governed by (10).

$$\tilde{v}_B(s) = Z_{DUT}(s)\tilde{i}_B(s), \tag{10}$$

The power stage of switch-mode PA consisting of a buck converter is modelled with filter inductor (L), filter capacitor (C), equivalent series resistor (ESR) of the capacitor (r_C) and ESR of the inductor (r_L). The parasitic resistances are considered to improve the accuracy of modelling. The converter is controlled via pulse with modulated duty cycle command, d. The canonical circuit model of a single synchronous buck converter in continuous conduction mode (CCM) can be developed, as shown in Fig. 9 [44], to represent small signal dynamics of the converter. For the simplicity of the analysis, the cascaded DC-DC system model can be mathematically represented through transfer functions (TFs) by using the single converter canonical model and conventional linear circuit analysis techniques, as shown in Fig. 10. The TFs between input variables (i.e., v_S, i_B and d) and state variables (i.e., v_B and i_L) in Fig. 10 should be derived considering the open-loop converter and eliminating the presence of load resistor (R) since the dynamics of $\tilde{i}_B$ and $\tilde{v}_B$ has been replaced by the Z_{DUT}. The detailed expressions of open-loop TFs required for this study are provided in the Appendix.

Impedance of DUT during charge/discharge

When the PA emulates charging operation (i.e., G2V), Z_{DUT} will be the closed-loop output impedance of the load converter (Z_{outCL}). While in discharging (V2G), Z_{DUT} will be the closed-loop input impedance of the load converter (Z_{inCL}) since power flow is reversed. Therefore, developing a generic mathematical model for Z_{DUT} in designing the PA controller is challenging and may not be accurate. Further, unlike the PA, the topology and control strategy of EV charger is unknown, and it is proprietary for manufactures. Thus, TF of the Z_{DUT} is unknown. However, the closed-loop input impedance of a converter is proven to exhibit negative impedance characteristics when its output is tightly regulated [45]. Thus, in literature, Z_{inCL} of complex PE-based converter is often approximated as a constant power load (CPL) [24], [25]. By linearizing the CPL at an operating point (V_B, P), the Z_{DUT} in discharging mode can be modeled as below,

$$Z_{DUT_{CPL}}(s) = Z_{inCL} = \frac{\tilde{v}_B(s)}{\tilde{i}_B(s)} = -\frac{V_B^2}{P}, \tag{11}$$

where $P = v_B i_B$.

In charging mode, Z_{outCL} is measured experimentally using an impedance analyzer (Bode 100) and used to estimate the TF of Z_{DUT}. This way provides an experimental approach for deriving a case-specific model of the Z_{DUT}. Fig. 11 shows the measured Z_{outCL} characteristics of a commercial EV charger (delta-Q IC1200) when it is operated in both constant current (CC) and constant voltage (CV) charging modes considering a BESS consists of a 7x12 TCL-PL-383562 Li-ion battery array (10Ah/25.9 V). It is seen that the EV charger resembles a capacitive load ($1/c_L s$) when it is operating in CC mode and a resistive load (R_e) in CV mode over the frequency of interest,

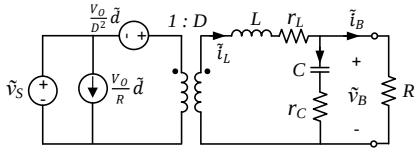


Fig. 9 Canonical circuit model of the single synchronous buck converter with parasitic resistances connected to a resistive load.

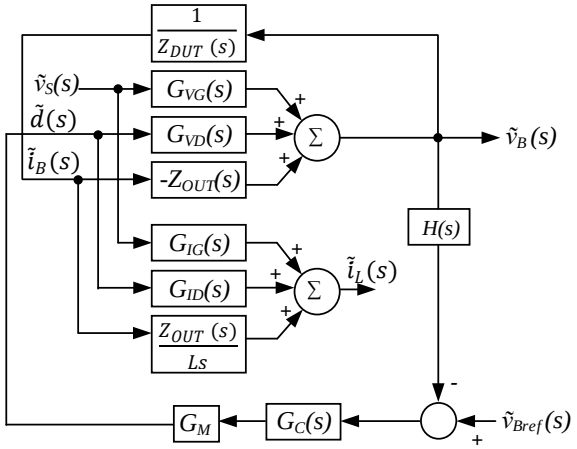


Fig. 10 Mathematical representation of the cascaded DC-DC system.

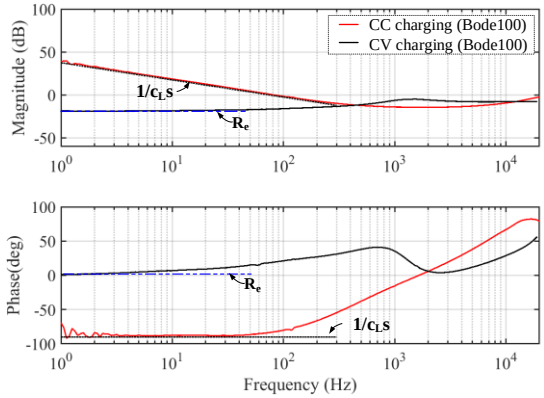


Fig. 11 Output impedance measurement of an EV charger in CC (v_B=26 V, i_B=5 A) and CV v_B=28 V, i_B=2.2 A) mode.

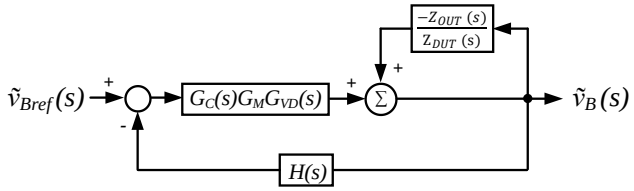


Fig. 12 Control block diagram for PI control design.

Z_{DUT} can be represented analytically as a positive impedance depending on the EV charger's operating mode. To improve the accuracy of Z_{DUT}, a software tool like MATLAB™ can also be used to estimate the TF of Z_{DUT} and estimated TFs for two scenarios in Fig. 11 are given below,

$$Z_{DUT_{cc}}(s) = \frac{\tilde{v}_B(s)}{\tilde{i}_B(s)} = \frac{-1.9s^2 - 2.1*10^4 s - 1.9*10^8}{s^2 - 3.5*10^5 s - 3.6*10^5}, \tag{12}$$

$$Z_{DUT_{cv}}(s) = \frac{\tilde{v}_B(s)}{\tilde{i}_B(s)} = \frac{-1.9s^2 - 2.1*10^4 s - 1.9*10^8}{s^2 - 3.5*10^5 s - 3.6*10^5}. \tag{13}$$

Controller design of the switch-mode PA

To study the voltage control loop dynamics, Fig. 10 can be simplified to Fig. 12 by neglecting the perturbations in input voltage (v_S). Thus, the compensated open-loop TF of the PA can be derived using Fig. 12 and is given by (14).

$$G_{PA\_OL}(s) = G_C(s)G_M H(s)G_{VD}(s)\frac{1}{1+\frac{Z_{OUT}(s)}{Z_{DUT}(s)}}, \qquad (14)$$

where G_M is the PWM scheme gain, and $H(s)$ is the voltage sensor feedback gain. Since Z_{DUT} is known, (14) can be used to design the PI controller (i.e., $G_C(s)$) using any frequency response methods. Typically, the control to output TF ($\hat{v}_B(s)/\hat{d}(s)$) of an ideal buck converter with CPLs has two poles in the right half-plane due to the negative incremental impedance [46]. However, with practical parasitic resistances, the uncompensated plant becomes a stable system, as shown in Fig. 13. Thus, classical linear PI controllers can be used to control the BE with CPL too. The system parameters considered for analysis are listed in Table III. Fig. 14 (a) shows the bode plot of the $G_{PA\_OL}(s)$ with the designed PI controller indicating that the system is stable with enough phase margin (P.M.) under different load impedance scenarios. The step response of the PA is shown in Fig. 14 (b) under the same conditions.

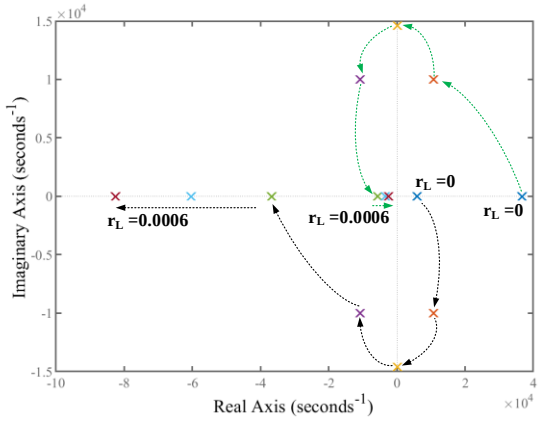
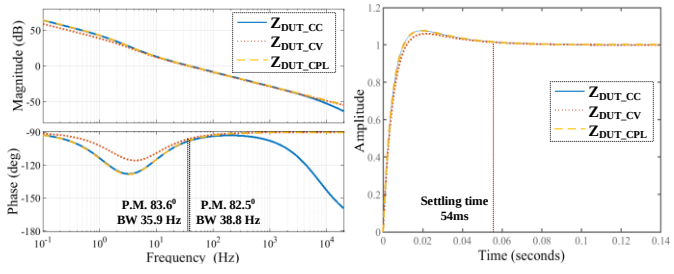


Fig. 13 Pole movement of a buck converter loaded by a CPL with increasing parasitic resistance (from r_L= 0, , r_C= 0 to r_L= 0.0006, , r_C= 0).

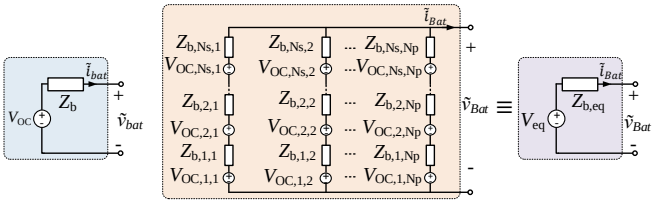


(a) (b)

Fig. 14 The PA response under different load impedances (a) frequency response of the $T_{OL}(s)$. (b) step repsonse.

TABLE III
KEY PARAMETERS OF THE SWITCH-MODE PA ANALYSIS

Parameter	Value	Parameter	Value	Parameter	Value
v_S	60 V	f_S	20 kHz	r_L, r_C	0.1 Ω, 0.001 Ω
L	3.7 V	k_P, k_I	0.4, 16.8	c_p, R_e	21.3 mF, 0.12 Ω
C	4.7 µF	$H(s)$	1	V_B	25 V
R_d	10 Ω	G_M	1	P	125 W



(a) (b) (c)

Fig. 15 The equivalent circuit of the linearised (a) battery model (b) BESS model (c) lumped BESS model.

b) Small signal model of PHIL-based Battery Emulator

The PHIL-based BE small signal model is derived by considering the linearized BESS model, model of each device in the power interface, impedance characteristics of the EV charger, and the sampling effect of digital computation in both RTS and microcontroller of the PA. Unlike other PHIL configurations, the linear model of the BESS is a key element in developing the equivalent control block of the system. The linear model of Li-ion battery is developed by differentiating (8) at a linearization point (V_{OC}, SOC, V_{bat}, I_{bat}) as given below,

$$\tilde{v}_{bat}(s) = V_{OC} - Z_b(s)\tilde{i}_{bat}(s). \qquad (15)$$

It is assumed that the variation of SOC of the battery for a small change in $i_{bat}(\tilde{i}_{bat})$ is negligible. Thus, (15) is derived by neglecting SOC perturbations (i.e., $\widetilde{SOC}$=0) in the small signal analysis. The linearized battery model given in (15) can be represented by an equivalent circuit, as shown in Fig. 15 (a). Based on (15), the BESS model that consists of a $N_s \times N_p$ battery array can be lumped to into an equivalent circuit, as shown in Fig. 15 where, $V_{eq} = N_s V_{OC}$, $Z_{b,eq} = N_S Z_{b,1} // N_S Z_{b,2} // \cdots // N_S Z_{b,N_p}$ and, $i_{bat} = N_p i_b$. Therefore, linearized model of the BESS is described by,

$$\tilde{v}_{Bat}(s) = V_{eq} - Z_{b,eq}(s)\tilde{i}_{Bat}(s). \qquad (16)$$

Thus, the small signal relation between v_{Bat} and i_{Bat} is given by (17).

$$\tilde{v}_{Bat}(s) = -Z_{b,eq}(s)\tilde{i}_{Bat}(s). \qquad (17)$$

To validate the small signal model of BESS, the frequency response of $Z_{b,eq}(s)$ is compared with AC sweep results obtained experimentally through a Gain/Phase analyzer (Bode100). Fig. 16 shows the detailed test configuration for impedance measurement along with the indication of measured variables. A small signal perturbation is introduced in the i_{bat}via a gain-phase analyzer and, the voltage and current of the BESS inside RTS are monitored (i.e., v_{bat} and i_{bat}). The frequency response obtained from Bode100 is super-imposed with the frequency response of the mathematical BESS model in Fig. 17 for two BESS arrays (7x12 and 21x12). It is observed that the experimental results are closely matching with the response of the mathematical model. Thus, this validates the developed BESS model.

By considering the linear model of BESS and other mentioned elements, the PHIL-based BE in Fig. 4 can be represented in a control block diagram, as shown in Fig. 18. The

open-loop TF of the system can be derived using the block diagram in Fig. 18. and, it is given by,

$$T_{OL\_BE}(s) = \frac{Z_{b,eq}}{Z_{DUT}} G_{AO}(s) G_{vv}(s) G_{AI}(s) G_{fil}(s), \quad (18)$$

where $G_{vv}(s)$ is the TF of switch-mode PA, $G_{AI}(s)$ is the model of ADC card in RTS, $G_{\mathrm{AO}}(s)$ is the model of DAC card in RTS, $G_{fil}(s)$ is the TF of the current measurement feedback filter. The delay time of the sensor is much shorter compared to other latencies. Hence, it is neglected from the analysis. Each power interface device can be modelled with its respective TFs and time delays. The $G_{vv}(s)$ is derived by considering both the voltage control loop of the buck converter and the sampling and latency effect of the v_{Bref} by the microcontroller. From (14), the closed-loop TF of voltage-mode buck converter ($G_{PA}(s)$) can be derived, and the sampling effect of v_{Bref} in the microcontroller is modelled as a continuous zero-order-hold (ZOH) with an additional delay function [26] and, it is given by,

$$G_{MCU}(s) = \frac{\tilde{v}_{ref}(s)}{\tilde{v}_{Bref}(s)} = \frac{(1-e^{-sT_{MCU}})}{sT_{MCU}} e^{-sT_{PA}}, \quad (19)$$

Where T_{MCU} is the sampling period for i_{Oref} in the microcontroller and T_{PA} represents the input-to-output signal latency of the PA. The complete model of switch-mode PA is given by,

$$G_{vv}(s) = \frac{\tilde{v}_B(s)}{\tilde{v}_{Bref}(s)} = G_{PA}(s) G_{MCU}(s), \quad (20)$$

$$G_{PA}(s) = \frac{\tilde{v}_B(s)}{\tilde{v}_{ref}(s)} = \frac{G_C(s) G_M G_{VD}(s) \frac{1}{1+\frac{Z_{OUT}(s)}{Z_{DUT}(s)}}}{1+G_C(s) G_M G_{VD}(s) \frac{1}{1+\frac{Z_{OUT}(s)}{Z_{DUT}(s)}} H(s)}. \quad (21)$$

The ADC card in RTS typically consists of an anti-aliasing filter (AAF) and a sampler. The sampling function is modelled as a continuous ZOH that has been widely used in PHIL applications for its ability to capture a wide range of frequencies [26]. The model of ADC card is given by,

$$G_{AI}(s) = \frac{G_{aaf}(1-e^{-sT_{RT}})}{sT_{RT}(1+sT_{aaf})} e^{-sT_{AI}}, \quad (22)$$

where G_{aaf} is the gain of AAF, $T_{aaf} = 1/2\pi f_{aaf}$ is the filter cut-off of the AAF, T_{RT} is the sampling time of the AO, which equals to the time step of the RT simulation and T_{AI} is the conversion time delay of the ADC. The DAC card and digital computational process in RTS are represented by a time delay.

$$G_{AO}(s) = e^{-s(T_{RT}+T_{AO})}, \quad (23)$$

where T_{AO} is the DAC conversion time delay of the analog output card. Total latency of the loop (T_{total}) is given by,

$$T_{total} = T_{PA} + T_{RT} + T_{AO} + T_{AI}. \quad (24)$$

The TF of the voltage measurement/ feedback filter is given by,

$$G_{fil}(s) = \frac{1}{(1+sT_{fil})}, \quad (25)$$

where $\mathrm{T}_{fil} = 1/2\pi f_c$, f_c is the cut-off of frequency of the filter.

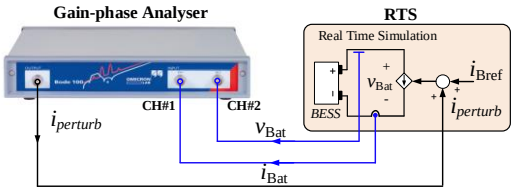


Fig. 16 Connection scheme for Bode100 for frequency response evaluation of battery model.

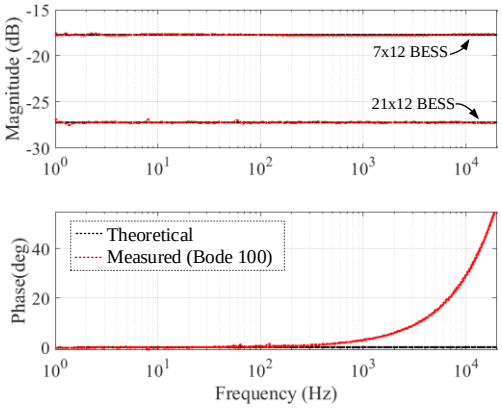


Fig. 17 Comparison of the input impedance of the BESS array when i_{Bat}= -5A and SOC=50% for model validation.

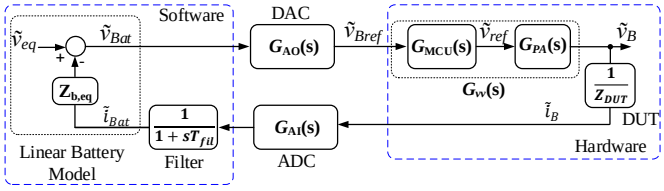
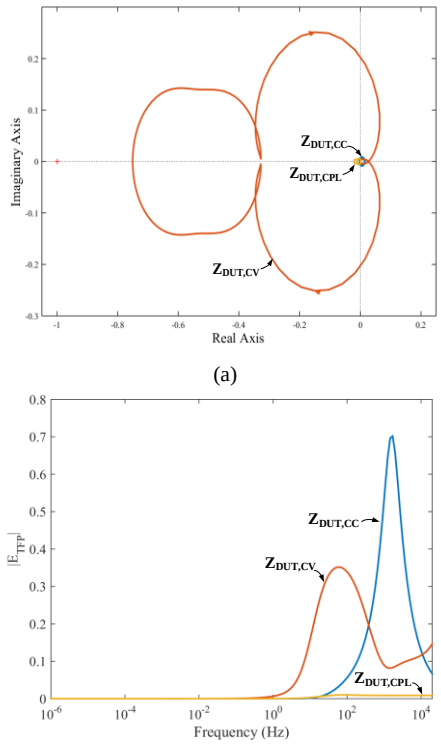


Fig. 18 Block diagram of the PHIL-based BE via voltage-type ITM.

c) *Investigating Stability of the PHIL-based Battery Emulator*

The open-loop TF of PHIL-based BE enables to investigate system stability comprehensively using traditional frequency-domain techniques such as Nyquist plots, Bode plots, Bode stability criterion, and Routh-Hurwitz (R-H) stability criterion [26]-[29]. Both Bode stability criterion and R-H stability criterion measure relative stability for determining exact instability points over the range of variables. However, both methods inherit their own drawbacks for non-minimum phase systems such as PHIL systems that consist of time delays and right half plane zeros. The R-H stability criterion requires approximating the time delay using methods such as the Pade approximation. Hence, it is not preferable for systems with time delays. Unlike the R-H stability criterion, the bode stability criterion does not require the time delay to be approximated to determine stability. It becomes complex in PHIL simulations for analytically determining phase cross points and evaluating the magnitudes. Both Nyquist and bode plots are graphical methods that provide a necessary and sufficient condition for stability and do not require approximating time delays. Considering the above, this work applies Nyquist plots to determine the stability of a defined PHIL-based BE configuration.

The stability analysis is done considering a commercial EV charger (delta-Q IC1200) system at the output. The PHIL-based BE intended to emulate BESS consists of a 7x12 TCL-PL-383562 Li-ion battery array (10Ah / 25.9 V). All the parameters of PHIL-based BE are summarized in Table IV. The Nyquist stability test results for the designed PHIL-based BE under different Z_{DUT} are shown in Fig. 19 (a), which indicates that the system has less stability margin with $Z_{DUT_{CV}}$. The stability of voltage-type ITM is proven to be unstable when the ratio $Z_{b,eq}/Z_{DUT}$ is ≥ 1 [9], [10]. From (11), Fig. 11 and, Fig. 17 show that the $Z_{b,eq}/Z_{DUT_{CV}}$ ratio is close to 1 (0.9328 being the actual value) and, $Z_{b,eq}/Z_{DUT}$ ratios for $Z_{DUT_{CC}}$ and $Z_{DUT_{CPL}}$ are much lower than 1 over the frequency of interest. Thus, designed PHIL-based BE has a higher stability margin for $Z_{DUT_{CC}}$ and $Z_{DUT_{CPL}}$ and has less influence either from the SOC level or the interface parameters to the stability. In summary, the developed mathematical framework can be adopted to ensure a stable operation of the PHIL-based BE with EV charger given that all the interface parameters and, Z_{DUT} are known.



(a)

(b)

Fig. 19 PHIL-based BE (a) stability test results under different Z_{DUT}. (b) TFP error function of v_B over frequency domain.

TABLE IV
PARAMETERS OF THE PHIL-BASED BE INTERFACE

Parameter	Value	Parameter	Value	Parameter	Value
T_{RT}	20 µs	T_{AO}	9.2 µs	G_{AAF}	1
T_{AI}	7.2 µs	f_C	100 Hz	f_{aaf}	10.1 kHz
T_{MCU}	50 µs	T_{PA}	40 µs	T_{total}	76.4 µs
Specification of the Emulated Li-ion Battery Array					
Capacity	10 Ah	N_Sx N_P	7x12	*Target Voltage*	4.2V x 7 = 29.4 V

d) Accuracy Evaluation of the PHIL-based Battery Emulator

The accuracy of the designed PHIL simulation for BESS is evaluated based on the method proposed by W. Ren et al. [30], in which the PHIL simulation error function is derived considering the perturbations caused by non-idealities of the interface as well as external noises. It defines the perturbation comes from non-idealities of the power interface as the transfer function perturbation (TFP). In this work, simulation error comes due to the TFP has only been investigated while noise perturbations are considered to be negligible. The error function due to TFP (E_{TFP}) is given as,

$$E_{TFP} = \left| W_0 \frac{G_{LP}(s)\Delta G_{int}(s)}{(1+G_{LP}(s)(1+\Delta G_{int}(s)))} \right|, \quad (26)$$

$$\Delta G_{int}(s) = G_{int}(s) - 1, \quad (27)$$

where $G_{LP}(s)$ is the open-loop TF of the original circuit (i.e., without interface perturbation), $G_{int}(s)$ is the TF of the non-ideal interface and, W_0 is a weighting function for adding different accuracy levels at different frequencies [30]. From Fig. 18, G_{LP} and $G_{int}(s)$ for PHIL-based BE can be derived and, those are given by (27) and (28).

$$G_{LP}(s) = Z_{b,eq}/Z_{DUT}, \quad (28)$$

$$G_{int}(s) = G_{vv}(s)G_{AO}(s)G_{AI}(s)G_{fil}(s). \quad (29)$$

The E_{TFP} for v_B can be determined by solving (25). The theoretical error results of v_B over the frequency domain under different load conditions are plotted in Fig. 19 (b). The error is equally treated by taking W_0=1. It is seen that the normalized error below 10 Hz is < 0.05, which means that the PHIL interface would not have a significant impact on accuracy by applying PHIL simulation for battery emulation.

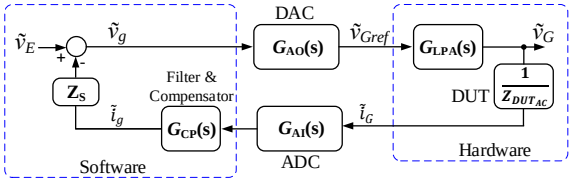


Fig. 20 Block diagram of the PHIL-based GE via voltage-type ITM.

B. PHIL-based Grid Emulator

Similar analysis as in PHIL-based BE can be applied for the PHIL-based GE to evaluate stability and accuracy. The open-loop TF of the PHIL-based GE can be derived from the control block diagram shown in Fig. 20.

$$T_{OL\_BE}(s) = \frac{Z_S}{Z_{DUT_{AC}}} G_{AO}(s)G_{LPA}(s)G_{AI}(s)G_{CP}(s), \quad (30)$$

where Z_S is equivalent grid inductance, Z_{DUTac} is AC side input impedance of the EV charger, $G_{LPA}(s)$ is the linear PA TF, $G_{CP}(s)$ is the TF of the filter and compensator. Expressions for Z_S, $G_{LPA}(s)$ and $G_{CP}(s)$ are given below.

$$Z_S = R_g + sL_g, \quad (31)$$

$$G_{LPA}(s) = \frac{\tilde{v}_G(s)}{\tilde{v}_{Gref}(s)} = \frac{e^{-sT_b}}{1+sT_a}, \quad (32)$$

$$G_{CP}(s) = \frac{sT_{cp}}{1\_sT_{cp}} \frac{1}{1+sT_{fil1}}, \quad (33)$$

where T_b is the latency of linear PA, T_a is the cut-off of linear PA, T_{cp} is the time constant of the lead compensator and, T_{fil} is filter cut-off of the current feedback signal. The Z_{DUTac} is obtained experimentally via frequency response measurements and used that for estimating the TF of Z_{DUTac}. For e.g., the experimental results obtained from the impedance analyzer (Bode100) and estimated Z_{DUTac} are plotted in Fig. 21, in which the estimated TF of Z_{DUTac} closely agrees with experimental results. Thus, this procedure can be followed to obtain Z_{DUTac} for a certain operating point to conduct stability and accuracy evaluations. Nyquist stability test results are presented in Fig. 22 for the designed PHIL-based GE under different Z_S/Z_{DUTac} ratios and different $G_{CP}(s)$. The PHIL simulation is stable for Z_S with paractical R/X ratios under both $G_{CP\_100Hz}(s)$ and $G_{CP\_1000Hz}(s)$ and notioced that system becomes unstable for R_g =0.086 Ω, L_g =2.5 mH with $G_{CP\_1000Hz}(s)$. It confirms that both $G_{CP}(s)$ and Z_s have a significant influence on the stability of the system. The design parameters of the PHIL simulation are tabulated in Table V. Further, the accuracy of the PHIL interface is evaluated based on the procedure explained in Section IV-A-d. The E_{TFP} of v_G is determined by deriving the G_{LP} and $G_{int}(s)$ of PHIL-based GE from Fig. 20. Expression for G_{LP} and $G_{int}(s)$ are given by,

$$G_{LP}(s) = Z_S/Z_{DUT_{AC}}, \quad (34)$$

$$G_{int}(s) = G_{LPA}(s)G_{AO}(s)G_{AI}(s)G_{CP}(s). \quad (35)$$

The predicted error results of v_B over the frequency domain under different conditions are plotted in Fig. 23. Noticed that normalized error is insignificant (<0.02) for frequencies below 1 kHz when Z_S is low (R_g= 0.086 Ω, L_g=88 µH) under both compensators. However, E_{TFP} becomes significant for higher Z_S, as presented in Fig. 23.

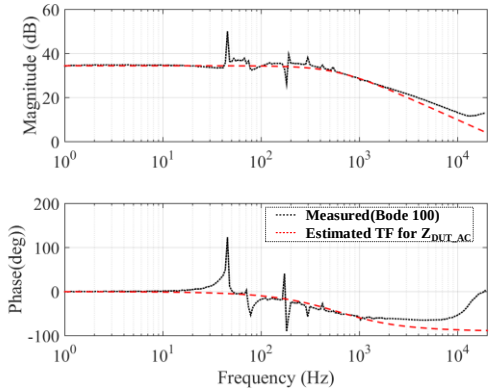
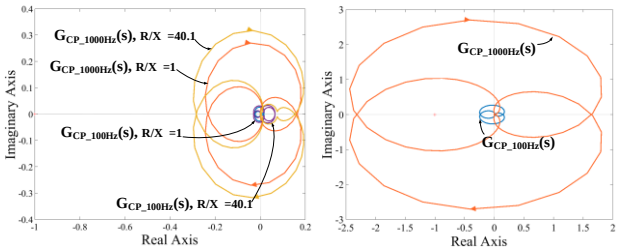


Fig. 21 Input impedance (Z_{DUT_AC}) results from impedance analyser when EV charger in CC (v_B=26 V, i_B=5 A).

TABLE V
PARAMETERS OF THE PHIL-BASED GE INTERFACE

Parameter	Value	Parameter	Value
$G_{CP\_100Hz}(s)$: T_{fil1}, T_{cp}	1.59 ms, 10.6 ms	T_a, T_b	0.4 µs, 6 µs
$G_{CP\_1000Hz}(s)$: T_{fil1}, T_{cp}	0.159 ms, 26.5 ms	Z_{DUT_AC}	$1.9 * 10^5/(s + 3737)$



(a) (b)

Fig. 22 Nyquist stability test results of the PHIL-based GE under different $G_{CP}(s)$ (a) R/X ratio=1 (i.e.,R_g=0.086 Ω, Lg=0.225 mH) and R/X ratio=40 (i.e., R_g=3.97 Ω, Lg=0.264 mH) . (b) R_g=0.0864 Ω, Lg=2.5 mH.

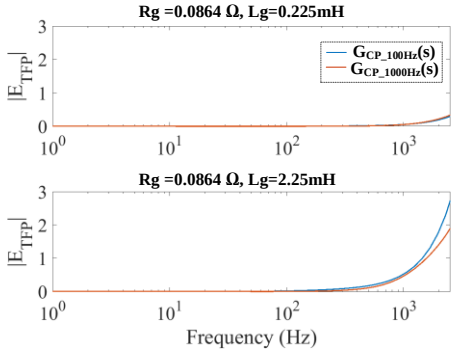


Fig. 23 Predicted variation of TFP error function of v_G over frequency under different compensators and grid equivalent resistances.

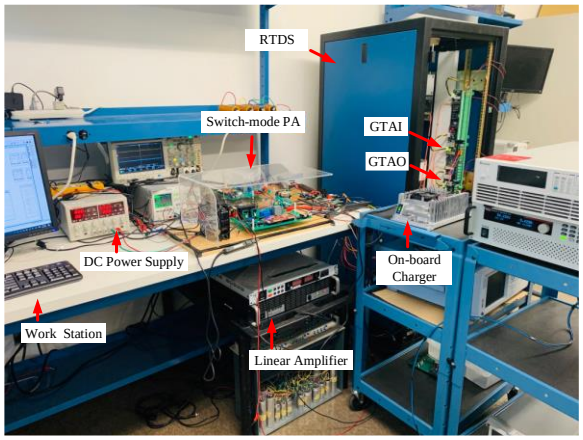


Fig. 24 The PHIL Testbed.

V. EXPERIMENTAL VALIDATION

The PHIL testbed described in Sections III and IV has been implemented for evaluating a commercial EV charger (delta-Q IC1200) experimentally. Fig. 24 shows the experimental test setup of the PHIL testbed. The RTDS© simulator is used as the RTS for developing the RT models of BESS and LV network, and its RSCAD user interface is installed in the workstation for interfacing with the RTDS simulator. A 300W bi-directional DC-DC buck converter prototype with the voltage controller is implemented to emulate the battery array, and Table III shows its design parameters. Throughout the paper, PHIL-based BE is designed to emulate a BESS consists of a 7x12 TCL-PL-383562 Li-ion battery array and PHIL interface parameters, including the battery array details, are listed in Table IV. A 900W AE TECHRON linear PA is used to emulate the grid.

A. PHIL-based BE Validation

The performance of the designed PHIL-based BE is evaluated separately before connecting them with the EV charger. Fig. 25 (a) shows the experimental results of the PHIL-based BE during the charge operation from 25 % SOC to 100% SOC with i_B = - 8A. This experiment is performed by connecting a controlled current source (Chroma 62050H-600S) at the output of the BE. Since the RT battery model has already been validated with real batteries in [43], the accuracy of the PHIL-based BE is evaluated by comparing it with RT simulation results (i.e., software results). As illustrated in Fig. 25, the output waveforms of switch-mode PA (i.e., v_B, i_B) are closely following the simulated waveforms (i.e., v_{Bat}, i_{Bat}). The error between them is quantified by calculating the mean percentage error (MPE) and found out that it is 1 % for v_B and 0.8 % for i_B. Similary, BE performance is evaluated under pulse charging conditions as shown in Fig. 25 (b). It validates that the PHIL-based BE is accurately emulating the RT battery model. Further, the PHIL-based BE discharge operation is tested by connecting a DC electronic load (KEITHLEY 2380-500-30) and the results obtained are plotted in Fig. 26. Noticed a minor steady-state error in v_B under no-load conditions as voltage controller is designed by only considering the CCM operation. Except for that, the results are in good agreement with the RT battery model. Fig. 27 presents the stable operation of PHIL-based BE for a pulse discharge test with a 1C-discharging rate (10.2A), and it verifies that the switch-mode PA can track the battery model transients accurately.

B. PHIL-based GE Validation

By employing $G_{CP\_100Hz}(s)$ and other parameters in Table V to the AC side PHIL implementation, a stable PHIL simulation of delta-Q IC1200 EV charger is obtained with different Z_S as predicted by the stability study. This experiment is conducted according to the configuration shown in Fig. 4, and the EV charger is programmed with a customized charging algorithm to match the 7x12 TCL-PL-383562 Li-ion battery array parameters. The experiment results for a stable PHIL simulation of EV charger with a grid impedance of R_g=3.97 Ω, L_g=0.264 mH is shown in Fig. 28. To examine the stability predictions made in Section III.B, results are obtained by increasing the grid impedance. Fig. 29 shows output waveforms of the PHIL-based GE when the L_g increased from 0.225 mH to 2.25 mH with $G_{CP\_1000Hz}(s)$.These oscillations indicates PHIL simulation of grid is unstable which agrees with theoretical calculations. To demonstrate the accuracy of the PHIL simulation of the grid, PHIL simulation results are compared with the experiment results gathered by directly connecting the EV charger to the local grid. It is approximated that the local grid inherits a similar Z_S (R_g= 0.086 Ω, L_g= 0.225 mH). The comparison results are plotted in Fig. 30 which shows that PHIL simulation results are in close agreement with real system results. The error due to the PHIL simulation is quantified by measuring the apparent power (S) difference between two systems, and error results are summarized in Table VI.

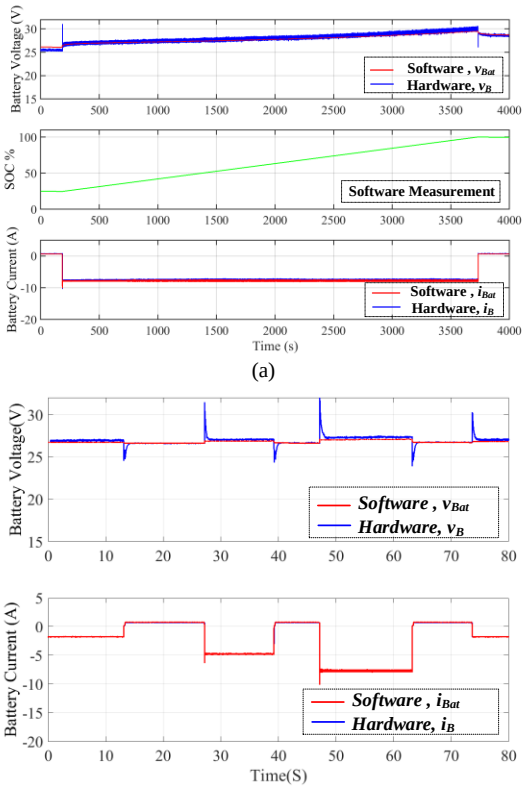


Fig. 25 Experiment results of the PHIL-based BE during charging operation under (a) complete charging cycle (b) pulse charging test.

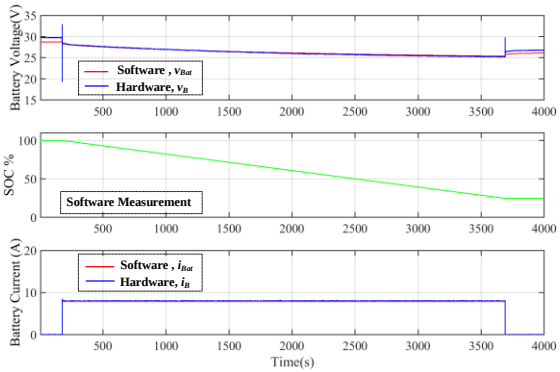


Fig. 26 Experiment results of the PHIL-based BE during discharging operation with i_B=8 A from 100 SOC% to 25 SOC%.

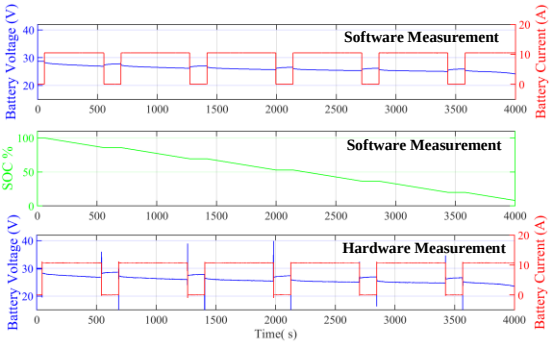


Fig. 27 Pulse discharging test results with 1C (10.2A).

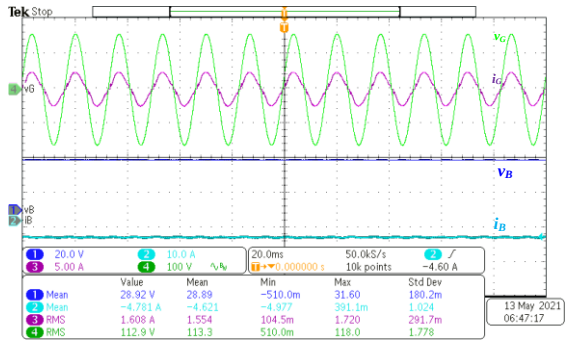


Fig. 28 PHIL simulation results of the delta-Q IC1200 with $G_{CP\_100Hz}(s)$, R_g = 3.97, L_g= 0.264 mH (R/X = 40.1).

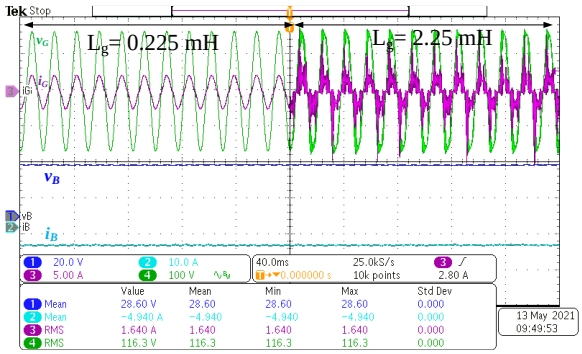


Fig. 29 PHIL simulation results of the delta-Q IC1200 with $G_{CP\_1000Hz}(s)$, R_g = 0.086 when L_g is increased from 0.225 mH to 2.25 mH.

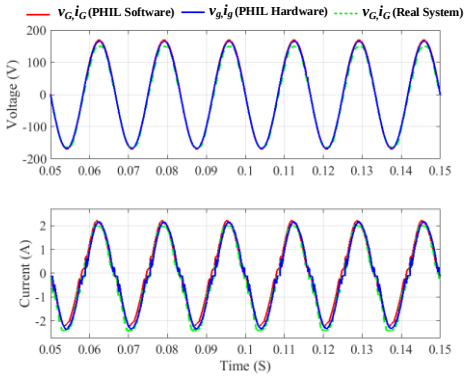


Fig. 30 Comparison of PHIL simulation results of grid emulator with a real experiment (R_g= 0.086 Ω, L_g= 0.225 mH with $G_{CP\_1000Hz}(s)$)

TABLE VI
ERROR EVALUATION OF THE PHIL-BASED GE

Z_S	System in Grid-side	P (W)	Q (var)	THD %		Error % in S
				v_G	i_G	
R_g=0.086Ω, L_g=0.225mH	Real Experiment	173.7	*25.6*	*2.3%*	*11.7%*	-
	PHIL Simulation	179.1	*36.5*	*0.1%*	*11.1%*	*-4.1%*
R_g=0.086Ω, L_g=2.5mH	Real Experiment	178.2	*26.2*	*3.1%*	*12.3%*	-
	PHIL Simulation	176.45	*79.0*	*0.2%*	*10.8%*	*-7%*

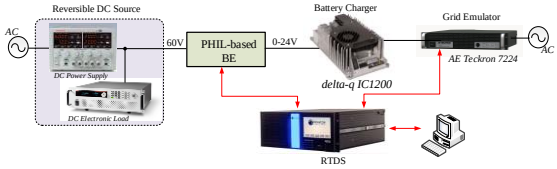


Fig. 31 PHIL test setup with the EV charger.

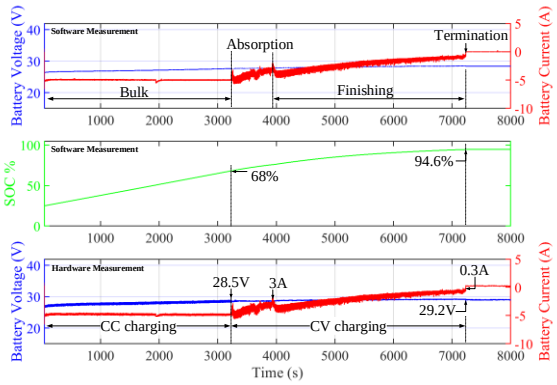


Fig. 32 The charge cycle for an EV charger algorithm with PHIL-based BE emulating 7x12 Li-ion battery array.

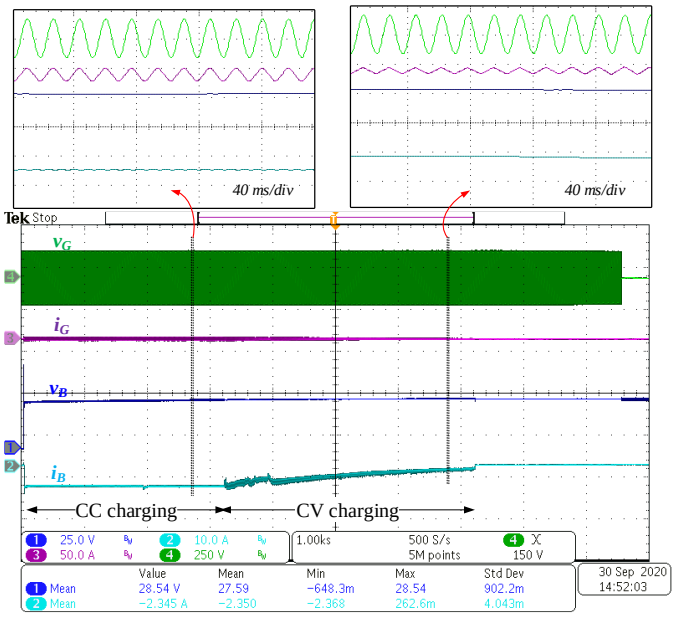


Fig. 33 Hardware measurement on both AC and DC side of the EV charger during the charge cycle.

C. EV Charger Performance Evaluation

Experiments are performed using the validated PHIL testbed for investigating the charging algorithm of the EV charger as well as for determining the EV charger response with grid side PQ impacts. The schematic of the experimental test configuration is shown in Fig. 31. The charging algorithm is customized based on the Li-ion battery array parameters listed in Table IV. Fig. 32 shows the experimental charge cycle results for a customized algorithm when the delta-Q IC1200 charger is connected to the emulated Li-ion battery array. This experiment is performed by setting the SOC% of the PHIL-based BE to 25% at the beginning, and results show that the EV charger is immediately started operating in CC charging mode and changed to CV mode once the BE voltage is increased to 28.5 V. Identified three different charging phases namely, bulk charging, absorption and finishing phase as shown in Fig. 32. The algorithm is terminated when the current tapers to a minimum charging current of 0.3 A. Fig. 33 shows both AC and DC side results of the same experiment captured at the oscilloscope. The transient performance of the EV charger is

investigated under voltage fluctuations by applying voltage sag, 23 % of the nominal v_G and corresponding experimental waveforms are shown in Fig. 34. Results reveal that grid current controller adjusts the input current to maintain constant power with a response time less than 1ms. Further, the protection scheme of the EV charger is tested by applying an extreme voltage sag, as shown in Fig. 35. Results indicate that the EV charger disconnects from the grid after 19 cycles. Likewise, the designed PHIL testbed can be employed to test and validate the control system design of a grid-connected EV charger with different battery array configurations and evaluate their overall performance under transient conditions.

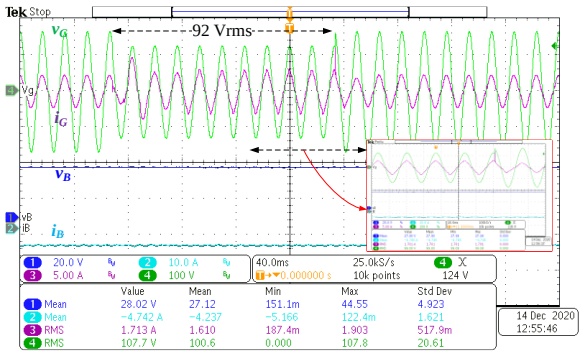


Fig. 34 Transient response of the EV charger under grid voltage fluctuations (120 Vrms-92 Vrms-120Vrms).

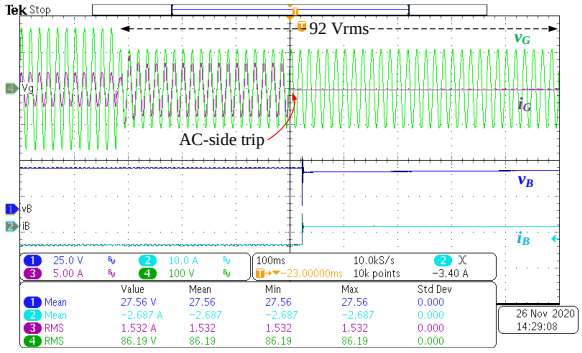


Fig. 35 Transient response of the EV charger for an extreme voltage sag (120 Vrms-78 Vrms).

D. Evaluating LV Network: A Case Study

An LV network shown in Fig. 36 is implemented in the RTDS™ simulator to study the EV charger interactions with a weak grid scenario. The LV network is designed with a short circuit ratio (SCR) of 4 and a PV system rated at 10 kW for representing a weak grid behavior. A PV system modelled as a P-Q source is placed at the point of common coupling (PCC) bus. Voltage and frequency support functions of the PV system are disabled and operated with only P-Q control (i.e., P and power factor (pf) to evaluate the system under voltage variations. The delta-Q IC1200 charger is connected to the PCC bus as the DUT and multiple EV charger units are modelled inside RTS as P-Q load rated with 8 kW/1.25kvar. From the nominal operating conditions, EV load is increased from 8 kW to 14 kW to study the grid behavior, and PHIL simulation results are plotted in Fig. 37. Grid voltage has reduced by 15% (from 118 Vrms to 90 Vrms) as no reactive support in the network. Although the system is stable, this indicates that the network requires reactive power support to regulate the grid voltage within +/- 5%. Fig. 38 shows the PHIL test results of the EV charger under a sudden power drop of the PV system. It indicates that the EV charger has disconnected from the grid after few cycles due to under voltage. Likewise, this approach can be used to design PV system controllers and analyze the power system behavior under different contingency test scenarios.

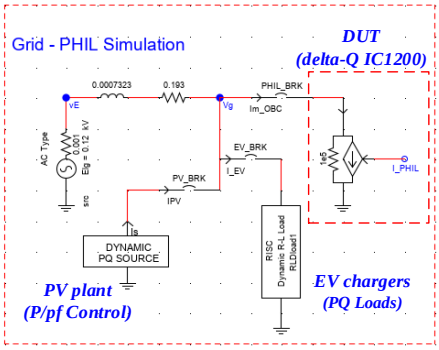


Fig. 36 The LV network simulated in RTS software.

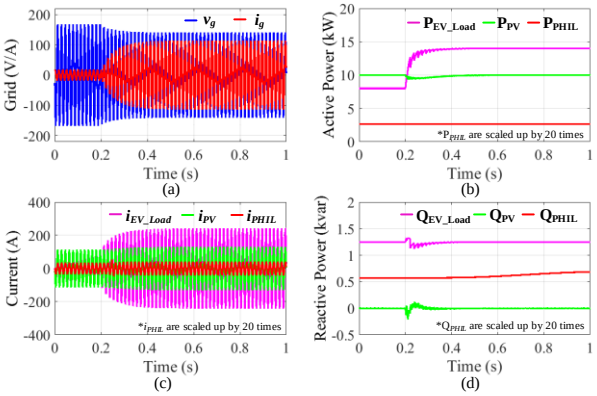


Fig. 37 PHIL simulation results under a sudden load step change in EV loads (virtual) from 8 kW to 14 kW (a) grid voltage and current, (b) active power, (c) currents (d) reactive power, of EV loads, the PV system and, DUT.

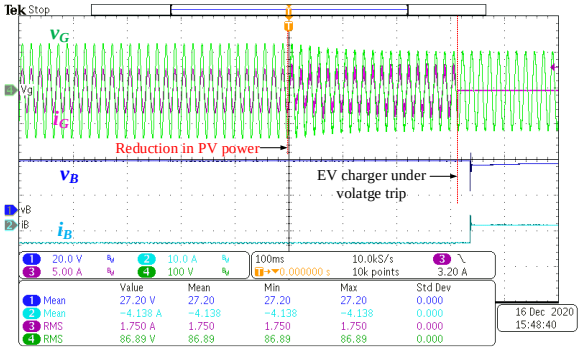


Fig. 38 Experimental results of delta-Q IC1200 under sudden decrease in PV power from 10 kW to 100W on a weak LV grid (SCR= 4).

VI. CONCLUSION

In this paper, a comprehensive small signal model capable of describing the dynamics of a PHIL testbed composed of PHIL-based BE and PHIL-based GE is presented, targeting stability and accuracy analysis. The PHIL-based BE model is

developed considering dynamic relationships between the virtual battery model, switch-mode PA, and the impedance characteristics of the EV charger. Procedures to conduct stability and accuracy analysis of the PHIL simulation are presented. Further, design considerations for the linear controller of the switch-mode PA to ensure cascaded DC-DC system stability have been discussed. The impedance characteristics of DUT are obtained experimentally, which appears to be the more practical method for accurate analysis. A similar analysis is conducted for PHIL-based GE with a linear PA in the power interface. The stability predictions made through models are validated experimentally using a PHIL test platform with an RTDS™ simulator. Performance of both PHIL-based emulators is investigated experimentally, and the accuracy of PHIL simulations is determined. The designed PHIL testbed has been used to evaluate the performance of an EV charger experimentally under both strong grid and weak grid through various PHIL tests. After all, the presented modelling and analysis approach can be directly adapted by researchers, utilities, and vendors to develop a PHIL testbed capable of testing advanced EV chargers and conducting power system studies to investigate possible PQ issues that can be raised by multiple onboard chargers in an LV network.

APPENDIX

Derived open-loop TFs of the buck converter with parasitic resistances required for this study are as follows:

$$G_{VD}(s) = \frac{\tilde{v}_B(s)}{\tilde{d}(s)}\Big|_{\tilde{v}_S,\tilde{i}_B=0} = \frac{V_S}{\left(1+\frac{r_C}{R}\right)LCs^2+\left(\frac{L}{R}+r_LC\left(1+\frac{r_C}{R}\right)+r_CC\right)s+\left(1+\frac{r_L}{R}\right)} \quad \text{(A.1)}$$

$$Z_{OUT}(s) = \frac{\tilde{v}_B(s)}{-\tilde{i}_B(s)}\Big|_{\tilde{v}_S,\tilde{d}=0} = \frac{(Ls+r_L)(1+r_CCs)}{\left(1+\frac{r_C}{R}\right)LCs^2+\left(\frac{L}{R}+r_LC\left(1+\frac{r_C}{R}\right)+r_CC\right)s+\left(1+\frac{r_L}{R}\right)} \quad \text{(A.2)}$$

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