

L1 Instruction Cache

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Warp Scheduler (32 thread/clock)

Dispatch Unit (32 thread/clock)

Register File (16,384 x 32-bit)

FP64	INT	INT	FP32	FP32		
FP64	INT	INT	FP32	FP32		
FP64	INT	INT	FP32	FP32		
FP64	INT	INT	FP32	FP32	TENSOR CORE	TENSOR CORE
FP64	INT	INT	FP32	FP32		
FP64	INT	INT	FP32	FP32		
FP64	INT	INT	FP32	FP32		
LD/ST	LD/ST	LD/ST	LD/ST	LD/ST	LD/ST	LD/ST
ST	ST	ST	ST	ST	ST	ST
						SFU

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LD/ST	LD/ST	LD/ST	LD/ST	LD/ST	LD/ST	LD/ST
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FP64	INT	INT	FP32	FP32		
FP64	INT	INT	FP32	FP32		
LD/ST	LD/ST	LD/ST	LD/ST	LD/ST	LD/ST	LD/ST
ST	ST	ST	ST	ST	ST	ST
						SFU

128MB L1 Data Cache / Shared Memory

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