**UART Verification plan**

**Goals:**

Verify UART IP feature by running in synopsis simulation tool with a SV/UVM based testbench.

Develop and run all tests based on the testplan and meet the coverage.

**Testbench architecture**

**Block diagram.**

TOP

TEST

ENV

scoreboard

Virtual seq

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Master\_agent

Slave\_agent

M

Seqr D

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M

Seqr

D

**Top level**

Instantiate UART interface and set the interface handle to the uvm\_config\_db ,connect back to back receiver and transmitter. Import the test packages and uvm packages.

**Test**

Declaring the handles for the different components and setting environment config and the base test.

**Score board**

Scoreboard is used for comparing the data from the monitors of transmitter and the receiver . To check the actual and expected data.

**Interface**

The Interface is used to encapsulate communication between blocks. Here used to connect the the interfcae back to back to the monitor and receiver. All the connection signals are defined here .

**Virtual sequence:**

Virtual sequence is used to start multiple sequences on different sequencers.

**Virtual sequncer:**

Virtual sequencer contains all the handles of the target sequenc

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**UART Agent**

UART agent is used to drive and monitor the UART items ,which also provides basic coverage on data,parity and different baud rate values etc.

**Sequencer**

Sequencer is a UVM component through which seq are send to driver.Sequencer and driver will maintain a handshake mechanism for passing sequences to DUT.

**Driver**

Driver drives the UART items

**Monitor**

monitor is responsible for capturing signal activity from the design interface and translate it into transaction level data objects that can be sent to other components.