1. Special language used to define hardware components is called _____.

A. TTL

B. VHDL

C. C

D. Unix

(L1)

Ans : VHDL

Details: VLSI hardware descriptive language

2. A microprocessor containing several processors in the same chip

A. Embedded systems

B. Data Processors

C. Multi core processors

D. Servers

Ans: C. Multi core processors

(L1)

3. For a color display using 8 bits for each of the primary colors (reed, green and blue) per pixel and with a resolution of 1280 x 800 pixels, what would be the sizes of the frame buffer to store a frame? (L2)

A. 4 MB

B. 8 MB

C. 16MB

D. 24MB

Ans. A. 4 MB

8 bits x 3 colors = 24 bits/pixel = 4 bytes/pixel

1280 x 800 pixels =1024000 pixels x 4bytes /pixel = 4096,000 bytes = 4MB

4.

Processor	Clock rate (in Hz)	CPI
P1	2	1.5
P2	1.5	1.0
P3	3	2.5

Which processor has highest performance? (L1)

5. Find IPC for each processor

A. 2.12×10^9, 3.2×10^9, 4.8×10^9

B. 1.12×10^9, 1.2×10^9, 1.8×10^9

C. 1.33×10^9, 1.5×10^9, 1.2×10^9

D. 2.20×10^9, 2.82×10^9, 3.8×10^9

Ans. C

P2 has highest performance

Performance of p1(instruction/sec) = $2 \times 10^9/1.5 = 1.33 \times 10^9$

Performance of p2(instruction/sec) = $1.5 \times 10^9/1.0 = 1.5 \times 10^9$

Performance of p3(instruction/sec) = $3 \times 10^9/2.5 = 1.2 \times 10^9$

6. Consider two different implementations of the same instruction set architecture. There are four classes of instruction A, B, C, D. The clock rate and CPI of each implementation is given as following table. What is the clock cycles required for each instruction?

	Clock rate	CPI Class A	CPI Class B	CPI Class C	CPI Class D
P1	1.5 Hz	1	2	3	4
P2	2 Hz	2	2	2	2

A. 32×10^5 , 22×10^5

B. 25×10^5 , 32×10^5

C. 28×10^5 , 22×10^5

D. 20×10^5 , 22×10^5

Ans. C

Clock cycles of P1= $10^5 \times 1 + 2 \times 10^{5\,x} \times 2 + 5 \times 10^5 \times 3 + 4x\,2x\,10^5$

$= 28 \times 10^5$

Clock cycles of P1= $10^5 \times 2 + 2 \times 10^{5\,x} \times 2 + 5 \times 10^5 \times 2 + 3x\,2x\,10^5$

$= 22 \times 10^5$

7.Consider two different implementations, P1 and P2, of the same instruction set. There are five classes of instructions A, B, C, D, E in the instruction set. The clock rate and CPI of each class is given below. (L2)

		Clock rate	CPI class A	CPI Class B	CPI class C	CPI class D	CPI class E
A	P1	1	1	2	3	4	3
A	P2	1.5	2	2	2	4	4
B	P1	1	1	1	2	3	2
B	P2	1.5	1	2	3	4	3

What are the peak performances of P1 and P2 expressed in instructions per second?

A. 2 G, 1 G inst/s
1.0 G, 0.7G inst/s

B. 2.5 G, 1 G inst/s

1.5 G, 1.5 G inst/s

C. 1.5 G, 0.8G inst/s

2.5 G, 0.7G inst/s

D. 1 G, 0.7 G inst/s ,

1 G , 1.5 G inst/s

Ans. D

Hint

Clock cycles of P1 = ∑ CC x CPI for each class

Performance of p1(instruction/sec) = ∑ clock cycles/CPI for each class (inst/s)

a. 1G, 0.7G inst/s

b.1G, 1.5 G inst/s

8. The table shows instruction-type break down for different programs.

			Instruction			
		Compute	Load	Store	branch	Total
a.	Program1	1000	400	100	50	1550
b.	Program2	1500	300	100	100	1750

The number of cycles taken by each instruction as compute = 1, load and store = 10, Branch = 3

Calculate execution time for each program on a 3Hz processor. (L3)

A.

a. 2.00 µs

b. 1.83 µs

B.

a. 2.00 µs

b. 1.50 µs

C.

a. 1.50 µs

b. 1.93 µs

D.

a. 2.05 µs

b. 1.93 µs

Ans. D

Hint.

Time = No of instructions x CPI /Clock rate

Total time = sum of each instruction execution time

a. 2.05 µs

b. 1.93 µs

	Compiler A		Compiler B	
	No. of Instructions	Execution time	No. of Instructions	Execution time
a.	1.00E09	1s	1.20E+09	1.4s
b.	1.00E09	).8s	1.20E+09	0.7s

9. For same program, two different compilers are used. The above table shows the execution time of two different compiled programs. What is the average CPI for each program given that processor has a clock cycle time of 1 ns.

A. Compiler A CPI Compiler B CPI

a. 1.00 a. 1.17

b. 0.80 b.0.58

B. Compiler A CPI Compiler B CPI

a. 1.00 a. 1.11

b. 1.80 b.0.68

C. Compiler A CPI Compiler B CPI

a. 1.10 a. 2.17

b. 0.80 b.0.58

D. Compiler A CPI Compiler B CPI

a. 1.10 a. 1.17

b. 1.80 b.0.58

Ans. A

10. A new version of processor has following characteristics (L2)

Version	Voltage	Clock rate
Version 1	5V	0.5 Hz
Version 2	3.3 V	1 Hz

How much capacitive load have been reduced between two versions if the dynamic power has been reduced by 10%.

A. 1.01

B. 1.00

C. 1.02

D. 1.03

Ans. D

Power1 = V^2xclock rate X C

Power2 = 0.9 Power1

C2(capacitive load)/C1(capacitive load) = $0.9 \times 25 \times 0.5 \times 10^9 / (3 \times 9 \times 1 \times 10^9) = 1.03$

11. For the same table

By how much has the dynamic power has been reduced if the capacitive load doesn't change? (L2)

A. 0.35

B. 0.67

C. 0.87

D. 0.95

Ans. C

Power2/ Power1 = $V2^2$xclock rate2/ $V1^2$xclock rate1

Power2 /Power1= 0.87

12. Assuming that the capacitive load of version 2 is 80% of version 1, calculate the voltage for version 2 if the dynamic power of version 2 is reduced by 40 % from version 1. (L2)

A. 3.00 V

B. 3.06 V

C. 3.12 V

D. 3.15 V

Ans. B.

Power2 = $V2^2$x clock rate2x0.8x C1

Power1= $V1^2$xclock rate1 x C1

$V2^2$x clock rate2x0.8x C1 = $V1^2$xclock rate1 x C1

V2 = 3.06V

13. As shown in table

	FP instruction	Int instruction	Load/Store instruction	Branch instruction	Total time
a.	35	85	50	30	200
b.	50	80	50	30	210

How much is the total time reduced if the time for FP operation is reduced by 20% ?

A. For 'a' Reduction 4.00 %, For 'b' Reduction 5.00 %

B. For 'a' Reduction 3.50 %, For 'b' Reduction 4.70 %

C. For 'a' Reduction 4.10 %, For 'b' Reduction 4.70 %

D. For ‘a’ Reduction 4.20 %, For ‘b’ Reduction 3.50 %

Ans: B

For a T_{fp} =35 x 0.8 = 28s , Tp1 = 28 + 85 + 50 +30 =193 s ,Reduction = 3.5%

For b T_{fp} =50 x 0.8 = 40s , Tp1 = 40 + 80 + 50 +30 = 200 s ,Reduction = 4.7%

14. By how much time for Int operations reduced if the total time is reduced by 20% ? (L2)

A. For ‘a’ Reduction 41.00 %, For ‘b’ Reduction 57.00 %

B. For ‘a’ Reduction 47.00 %, For ‘b’ Reduction 52.40 %

C. For ‘a’ Reduction 48.00 %, For ‘b’ Reduction 54.70 %

D. For ‘a’ Reduction 44.20 %, For ‘b’ Reduction 53.50 %

Ans: B

15. Can the total time be reduced by 20% by reducing only the time for branch instruction ? (L2)

A. For ‘a’ Yes, For ‘b’ NO

B. For ‘a’ Yes, For ‘b’ Yes

C. For ‘a’ NO, For ‘b’ Yes

D. For ‘a’ NO, For ‘b’ NO

Ans: D

16.

	Wafer diameter	Dies per wafer	Defects per unit area	Cost per wafer
a.	15 cm	90	0.018 defects/cm2	10
b.	25 cm	140	0.024 defects/cm2	20

Calculate the yield and cost per die? (L2)

A.

Yield a = 0.97 , cost a = 0.12

Yield b = 0.92 , cost b = 0.16

B.

Yield a = 0.92 , cost a = 0.14

Yield b = 0.82 , cost b = 0.16

C.

Yield a = 0.91 , cost a = 0.12

Yield b = 0.98 , cost b = 0.16

D.

Yield a = 0.98 , cost a = 0.16

Yield b = 0.91 , cost b = 0.15

Ans. A.

Wafer area = π x 7.5 x 7.5 = 176.70 m x m

Dies Area = wafer area / dies for wafer

Yield = 1 / (1 + (defect per area + die area)/2) ^{2}

Cost per die = cost per wafer /(dies per wafer x yield)

Yield a = 0.97 , cost a = 0.12

Yield b = 0.92 , cost b = 0.16

17. Using the same table

If the number of dies per wafer is increased by 10%and the defects per unit area increased by 15%, calculate the yield.

A.

Yield a = 0.97 , Yield b = 0.92

B.

Yield a = 0.98 , Yield b = 0.92

C.

Yield a = 0.97 , Yield b = 0.93

D.

Yield b = 0.91 , yield b = 0.92

18.

	Processors	Routine A (in ms)	Routine B (in ms)	Routine C (in ms)	Routine D (in ms)	Routine E (in ms)
a.	2	20	80	10	70	5
b.	16	4	14	2	12	2

In this multiprocessor specifications it is expected to improve performances by improving execution time of part of routines. Calculate total execution time and how much it is reduced if the time of routines A, C, E is improved by 15%. (L3)

A. For a = 2.1 % , For b = 3.5 %

B. For a = 2.0 % , For b = 3.5 %

C. For a = 2.9 % , For b = 3.5 %

D. For a = 2.7 % , For b = 3.5 %

Ans. C

Total time (a) for processors(2) = 185 ns

Total time (b) for processors(16) = 34 ns

For (a)

Reducing time in routines

T(A) = 17 ns , T(C) = 8.5 ns, T(E) =4.1 s

Total time = 179.6 ns

Reduction = 2.9 %

For (b)

Reducing time in routines

T(A) = 3.4 ns , T(C) = 1.7 ns, T(E) = 1.7 ns

Total time = 32.8 ns

Reduction = 3.5 %

19. For following program performs translation from C object code to MIPS.

a = b + c + d + e

a = b + (c + 5)

How many MIPS assembly instructions are needed to perform this C statement. (L2)

A. 4, 1

B. 2, 2

C. 3, 2

D. 2, 3

Ans. C.

First instruction

Add a , b, c

Add a, a, d

Add a, a, e

Second instruction

addi a,c, 5

addi a, a, e

20.

In the following table individual stages has following latencies.

	IF	ID	EX	MEM	WB
Instruction 1	300ps	400ps	350ps	500ps	100

What is the clock cycle time in pipelined and unpipelined processor ?

A. 400, 1650

B. 500, 2000

C. 500, 1650

D. 1650, 500

Ans. C

Pipelined = 500ps

Unpipelined = 1650ps (add all)