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A Power-Line Communication Modem based on OFDM

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Abstract

In this paper, we present the design and implementation of a PLC (Power-Line Communication) Modem based on Orthogonal Frequency Division Multiplexing (OFDM). The PLC device implements OFDM in both transmitter and receiver using VHDL programming. The OFDM processor is synthesized in a Field Programmable Gate Array (FPGA) that acts as a Core Processor in the PLC Modem. Furthermore, the prototype includes the design and implementation of the stages needed to inject the signal into the power-line and to recover the same signal in other point of the PLC network. An analysis of several noise sources show that the PLC Modem performance produced a bit error percentage of 4.46% in the worst case, while 0.89% in the best case for the transmission/reception tested.

Index terms *– Power-line Communications, OFDM, VHDL, FPGA, Coupling Circuit.*

1. Introduction

The communication systems based on PLC are attracting attention because PLC is a promising technology to deploy communication networks in remote places taking advantage of the existent electrical infrastructure [7]. The major drawbacks are related to the hostile nature of the channel because it is particularly aggressive with the data transmission. A variable frequency response, distortion, variable impedance depending on time and location, different kinds of noise, attenuation and multipath are the major problems that a trusted communication system deployed over the power-line must face (see e.g. [1]-[3]).

However, a trusted communication network not only depends on the problems aforementioned but the processing done over the signal before injecting the signal and after extracting the signal from the power-line also is determinant in the overall performance of the communication system. The probabilities of the extracted signal of being attenuated, distorted or even lost are very high. This is the reason why the receiver must be able to identify and sample successfully the signal sent by the transmitter. Reference [3] proposed an effective solution to overcome the natural drawbacks of the power-line based on wavelet packet analysis technique for PLC signal processing. This technique, implemented at the receiver, offers a more precise frequency resolution than other methods such as wavelet transform or FFT *(Fast Fourier Transform).* Also, the authors suggest that implementing OFDM combined with this technique increases the speed and performance of the PLC technology. In [5], an analysis of the PLC under different noise scenarios is analyzed.

This paper proposes a PLC Modem that implements OFDM. The OFDM processor is synthesized in a Field Programmable Gate Array (FPGA) that acts as a Core Processor in the PLC Modem. Also, a complete coupling stage to inject and extract the signal from the power-line is implemented. The data rate provided by the FPGA needs to be limited due to the characteristics of the external hardware. However, the OFDM implementation aims to increase the speed of the system and the performance of the recovering process. Simulation and experimental results show the effectiveness of the OFDM technique when the transmitted data is recovered.

The rest of the present paper is organized as follows. Section 2 presents the design of the OFDM transmitter and receiver. Also, a simulation of the performance of both transmitter and receiver is presented. Section 3 shows the PLC Modem prototype. It includes the amplification and coupling stages before injecting the signal into the power-line and the decoupling, filtering and analysis stages after extracting the OFDM signal from the power-line. Also, the PC application is described in this section. Section 4 presents the experimental results obtained from the PLC Modem testing. A noise analysis is also performed. Finally, the conclusions are given in Section 5.

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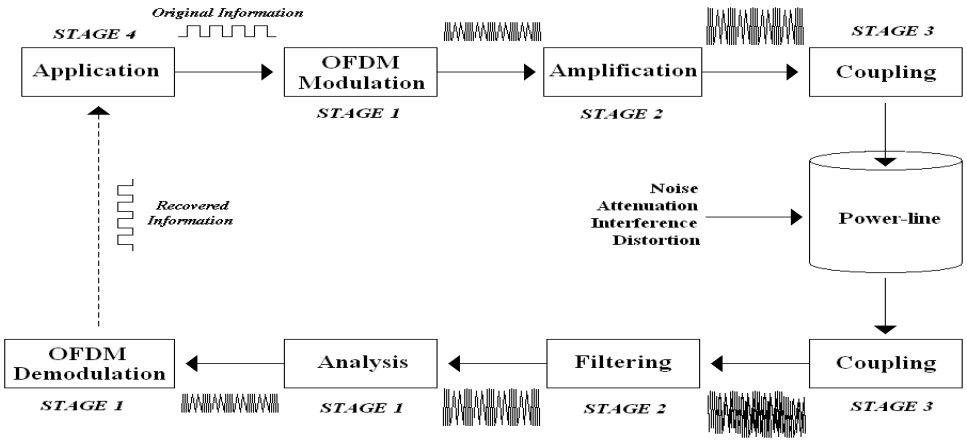


Figure 1. PLC Modem [3]

2. Design of the PLC Modem

The PLC Modem based on OFDM comprises the following stages: 1) To design and implement an OFDM transmitter and receiver. Both are programmed in VHDL to be synthesized in a FPGA. 2) To design and build the needed stages to inject and extract data from the power-line. 3) To design the components needed to couple the PLC device to the power-line. 4) To develop a PC application that controls the transmission and reception of information using the serial port of a PC.

The recent advances in the transmission and reception techniques and the development of programmable devices such as the FPGA have let to the development of powerful communication systems. These systems can be easily updated, redesigned or improved [4]. Figure 1 shows the architecture of the PLC Modem. This figure shows a clear difference between the logical hardware design, the physical construction with discrete components, the PC application development, and the power-line coupling. The prototype implements only the physical layer of the OSI *(Open Systems Interconnection)* model. Although an application was developed, it does not need the rest of the layers because it only writes and reads the serial port at the lowest level. This is due to the fact that the rest of the layers are not implemented. That is, flow control, detection and correction of errors, and retransmission techniques are not developed here. The PLC prototype reported in this paper works when the characteristics of the line are 120 Volts RMS *(Root Mean Square)* with a frequency of 60Hz.

2.1 The OFDM Modulation

The design of the transmitter follows the schema suggested in [5]. The PLC transmitter comprises five stages of processing since the information is received from any device until it is ready to be injected into the power-line (see Figure 2).

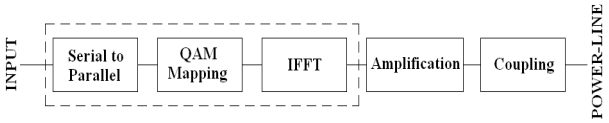


Figure 2. The OFDM Modulator

However, it is not possible to design logically all the stages that are shown in Figure 2 because both amplification and coupling block, previous to the injection to the power-line, use discrete components. Then only the first three stages are developed and implemented in the FPGA. The last two stages are implemented externally using discrete components. The OFDM modulator design suggested above comprises the following modules:

- Detection and sampling of the serial signal
- Storage control of the sampling process
- QAM-Constellation modulation
- Operations control of the main memory
- Complex numbers
- Storage memory for the initial sampling
- Operations control of the IFFT
- IFFT Core
- Storage memory for the results
- Output control for the results

Figure 3 shows the entity of the OFDM modulator with the input signals on the left and the output signals on the right. The particular characteristics of the OFDM modulator are the following:

- Base clock of 50 MHz
- 31 sub-channels
- 4-QAM Constellation (2-bit symbols)
- IFFT of 64 points (6-bit input, 8-bit output)

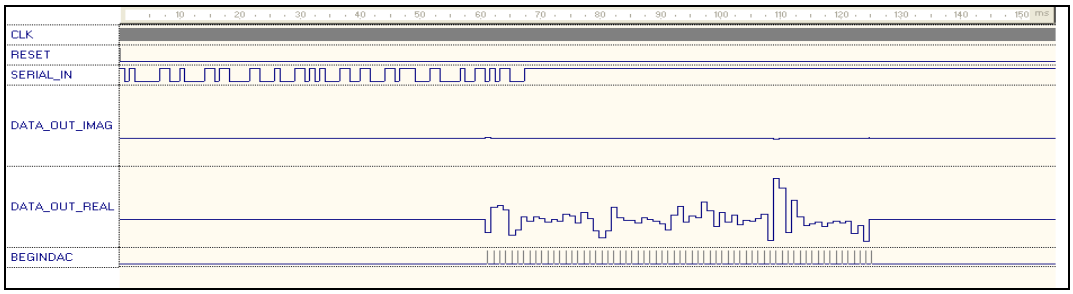
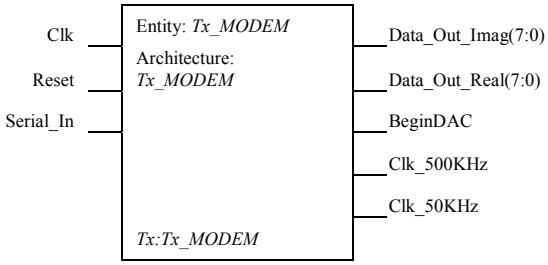


Figure 4. OFDM Modulator Simulation

- OFDM frequency signal of 9.6 kHz at the FPGA output.

The OFDM modulator shown in Figure 3 receives and saves a signal through *Serial_in* input that comes from the serial port of a PC. Then, the modulator applies the OFDM process over the data structure received and sampled. At the end of the process, the size of the data group delivered is equal to the number of channels defined for the system. These data group is ready to be sent over the power-line.



Component Name: *Tx*
Architecture and entity related: *Tx_MODEM*

Figure 3. OFDM Modulator Entity

The signals *Data_Out_Imag* and *Data_Out_Real* represent the data to be sent over the power-line. *Data_Out_Imag* is discarded because it is null due to the fact that the IFFT implemented in the transmitter operates over a vector with Hermetian Symmetry. The *BeginDAC* signal permits to control the conversion in the external DAC converter. *Data_Out_Real* has all the OFDM information to transmit then this signal is injected to the power-line only.

2.2 Simulation of the OFDM Modulator

It is important to present the initial conditions that must be assumed for simulation purposes. These initial conditions emulate the real performance of the FPGA and the serial port. These are equally applied to both transmitter and receiver. The initial conditions are the following:

- Modem clock base: 50 MHz
- Transmitter and Receiver clock base: 50 MHz (Generated internally by the FPGA)
- Initial impulse to *RESET* from 0 to 10 ns (Restores the initial conditions)
- Serial port clock base: 9.6 kHz
- Compatibility with the following serial port configuration: 9600 bps, 7-bit data, no parity, 1-bit stop

Figure 4 shows the simulation results of the OFDM modulator. The signal *SERIAL_IN* emulates the serial port and how it sends the information. Regarding the output, once the result of the IFFT is arranged, the result is sent sequentially through the *DATA_OUT_REAL* terminal. The arranged IFFT result is actually the OFDM information to be transmitted over the power-line. Each level of the signal delivered by the *DATA_OUT_REAL* terminal represents a channel in the OFDM modulation. A total of 64 channels result from the OFDM modulation stage. The signal *DATA_OUT_IMAG* also represents an output however it is ignored because it is assumed null. It is only shown for demonstrative purposes.

2.3 The OFDM Demodulation

The design of the receiver also follows the schema suggested in [5]. The PLC receiver of Figure 5 shows five stages of processing since the information is received from the power-line until it is delivered to an external device as a PC.

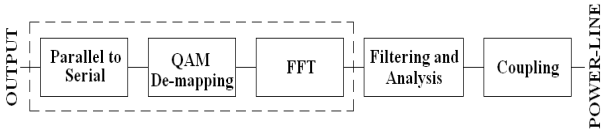


Figure 5. The OFDM Demodulator

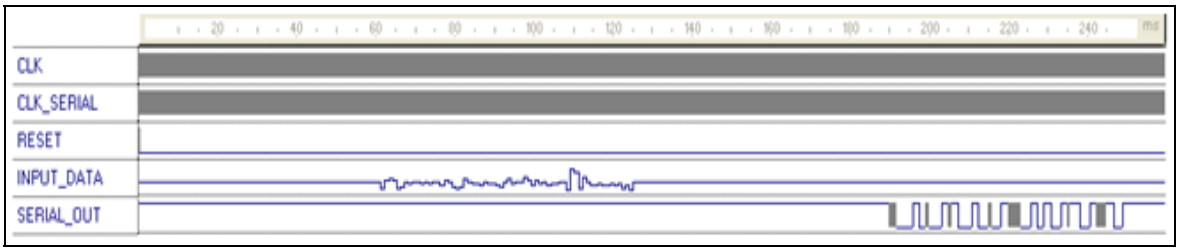


Figure 7. OFDM Demodulator Simulation

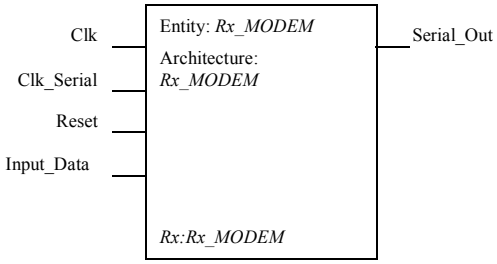
Since the coupling, filter and analysis block use discrete components, these stages are implemented externally using several discrete components. The designed OFDM demodulator comprises the following modules:

- Detection and sampling of the OFDM signal
- Storage memory for OFDM sampling
- Operations control of the FFT
- FFT Core
- Storage memory for the FFT results
- Operations control of the storage memory
- QAM-Constellation demodulation
- QAM Assembling results
- Storage memory of the final result
- Output control of the serial signal

The particular characteristics of the OFDM demodulator are the following:

- Base clock of 50 MHz for the receiver system
- Base clock of 9.6 kHz for the serial port
- 31 sub-channels
- 4-QAM Constellation (2-bit symbols)
- FFT of 64 points (8-bit input, 10-bit output)
- OFDM frequency signal of 9.6 kHz at the FPGA output.

Further details of both OFDM transmitter and receiver can be found in [6]. Figure 6 shows the entity of the OFDM demodulator with the input signals on the left and the output signals on the right.



Component Name: *Rx*
Architecture and entity related: *Rx_MODEM*

Figure 6. OFDM Demodulator Entity

The input referred as *Input_Data* has a similar OFDM signal injected to the power-line. When the signal is identified the inverse process to the transmission is started. First, the OFDM signal recovered is sampled and stored in a memory to apply the inverse OFDM process which includes basically the application of the FFT over the sampled data. A QAM demodulation is also performed over the FFT results. Finally, the resulting data is sent through the *Serial_Out* terminal to the serial port of the FPGA which is connected directly to the serial port of the PC.

2.4 Simulation of the OFDM Demodulator

Figure 7 shows simulation results of the OFDM receiver, its input and output signals. The signal *INPUT_DATA* receives the OFDM signal, made by the 64 channels originally sent by the transmitter, to be sampled. This signal is obtained after filtering and analyzing the extracted signal from the power-line. After the 64 OFDM channels have been successfully sampled, these are saved in a memory temporally. The OFDM inverse process operates over them to recover the original serial signal produced by the PC serial port. After performing all the inverse OFDM process, the terminal *SERIAL_OUT* delivers all the recovered information serially to the PC serial port. Note that since the frequency of the information recovered is the same to the originally transmitted, the serial port of the PC is able recognize the recovered information. Both signals *SERIAL_OUT* and *SERIAL_IN ??* from Figure 4 may be compared to verify that the transmitted signal and the recovered signal are the same. Notice that both simulations have a different time scale. For the design and simulation of the OFDM Modem, *Aldec 7.2 Student Version* is used. *Xilinx 9.2i* is used for the synthesis and implementation in the FPGA.

3. PLC Modem Prototype

The PLC Modem is made of the OFDM modulation and demodulation schemas implemented in the FPGA and the external PLC system. The external circuits that are necessary for the signal amplification, the DAC and ADC conversion, the signal filtering, and the injection and recovering of the OFDM signal from the power-line are denominated as external PLC System. From Figure

1, OFDM modulation, amplification, and coupling blocks [8] compose the PLC transmitter. The decoupling [8], filtering and analysis, and OFDM demodulation compose the PLC receiver. The four stages denominated external PLC system are implemented using discrete components. The PLC modem completely implemented in which both transmitter and receiver are integrated in a unique prototype is shown in Figure 8. However, the PLC Modem is not only integrated by the external PLC system but it also integrates the OFDM modem developed in the FPGA. Then, an interface between the PLC modem and the FPGA is needed. Also, an interface FPGA-Serial PC port is required. Figure 8 shows the extern PLC system plugged to the FPGA. The injection and extraction of the OFDM signals are done from independent connections to the power-line. The prototype presented here is able to use the power-line for both generate its own voltage lines and as communication channel. Then, only one cable plugged to the power-line is needed for working.

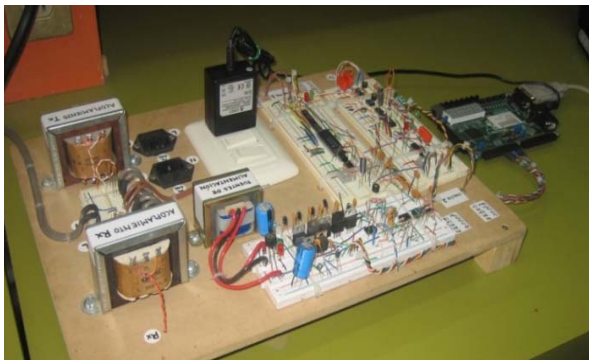


Figure 8. Extern PLC System-FPGA interface

The purpose of a computer application is to coordinate the transmission and reception of data to and from the PLC Modem. The application has demonstrative purposes because the data sent and received can be seen graphically. If a failure in the connections exists, the application informs to the user the nature of the error. The application interface is very intuitive and friendly besides being very practical. The user can write a text line to be sent and waits for the text line received from the power-line after being processed. The same PC acts as transmitter as receiver then both the transmitted line text and the received line text can be easily compared.

4. Experimental Results

In this section, we assess the performance of the proposed PLC Modem. The processing applied to the signal through the different blocks that are part of the OFDM transmission and reception is described in Section 2 (see Figure 1). The upper part of Figure 9 shows the OFDM signal generated by the FPGA to transmit whereas the lower part represents the OFDM signal modulated in frequency before being injected into the power-line.

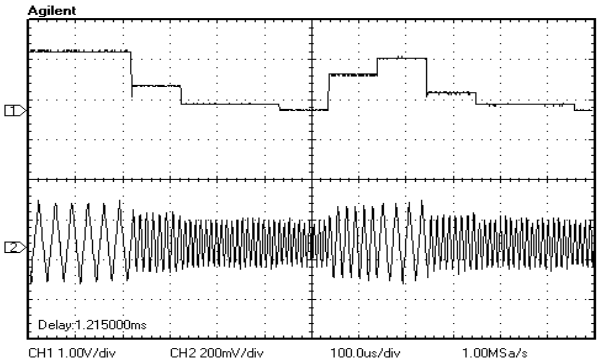


Figure 9. OFDM modulated signal

Figure 10 shows the original signal (top) and the recovered signal (bottom) after being extracted from the power-line. Originally, the extracted signal is modulated in frequency. Then, it needs to be filtered and analyzed by the external PLC system. The effectiveness of the external PLC system can be seen by comparing both signals of the figure. Finally, the OFDM inverse process is applied over the recovered signal to obtain the serial signal to be sent to the PC serial port.

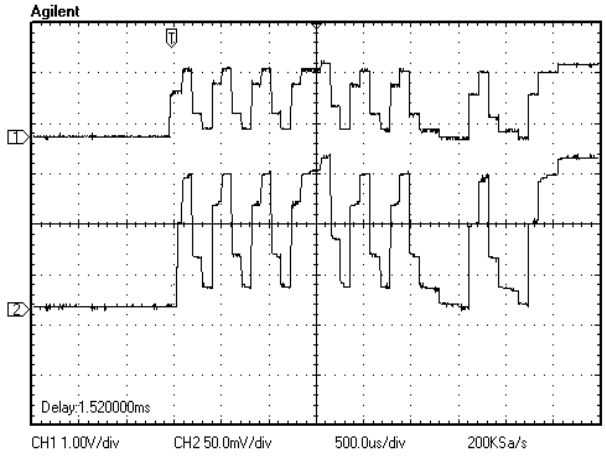


Figure 10. OFDM recovered signal

In [5], several sources of noise are analyzed to assess the PLC Modem such as colored background, synchronous periodic impulsive and asynchronous periodic impulsive. These are the most important noises to consider due to their characteristics. The *colored background noise* is caused by some electronic devices as computers, dimmers, and hair dryers. These devices may cause interference in frequencies up to 30MHz. It is characterized by a low PSD *(Power Spectral Density)*. It also pollutes specific band frequencies. The *Synchronous*

periodic impulsive noise is produced by commutation-based devices. Dimmers and DC Sources are good examples of devices that produce this noise. The harmonics produced by impulses affect a wide frequency spectrum reaching some hundred of kHz. The *Asynchronous periodic impulsive noise* is produced also by commutation-based devices however the repetition range is multiple of the fundamental frequency and the commutation frequency is higher. Some devices that produce this noise are television, computer monitor or DC sources. The PSD affects the frequency range of MHz. These noises sources are induced to assess the OFDM transmission/reception. Further details of how the noises were induced and tested can be found in [6]. Table 1 shows a summary of the bit error percentages obtained from the testing performed.

Table 1. Bit error percentages for several noise sources

Type of Noise	Error percentage. Characters	Error percentage. Bits
Colored background	Low Level: 10.71% Medium L.: 14.29% High Level: 35.71%	Low Level: 1.79% Medium L.: 2.23% High Level: 4.46%
Synchronous periodic impulsive	7.14%	0.89 %
Asynchronous periodic impulsive	7.14%	0.89 %

It can be seen in Table 1 that the colored background noise is one of the noises that affect more the transmissions of the PLC Modem. The bit error percentage obtained for this source of noise is higher compared to the rest of the noises tested. However, it is lower that the bit error percentage obtained using other modulation techniques like FSK (see e.g. [6]). Other noise sources do not affect the transmissions in the same form. The PLC Modem can deal with these sources. The error bit percentage is lower compared with FSK implemented also in this PLC Modem for the last two noise sources [6].

5. Conclusions

In this paper, we have presented a PLC device which is able to transmit and receive data over the power-line even with the presence of noise. The bit error percentages obtained from the testing are quite acceptable compared to those obtained from implementing other modulation techniques like FSK or DPSK (see e.g., [3], [6]) over this PLC Modem. The good performance is due to the fact that the OFDM implementation done in the FPGA and the stages implemented that inject and extracts the OFDM signal of the power-line. However, this device can be still improved to increase the performance and reduce the bit error percentage. The higher bit error percentages may be reduced using more sophisticated signal processing techniques or improving the quality of the filters to improve or even overcome the bit error percentage compared to the one obtained here (0.89%) for all the noise sources tested.

The speed of OFDM transmitter inside of the FPGA is 14.2857Mbits/second. However, this speed needs to be decreased due to the frequency carrier used in the external PLC System which is around 75 kHz. Then, the actual speed of the OFDM Modem is 16800bps. Also, this speed is limited by the configuration characteristics of the OFDM Modem. Furthermore, under normal noise conditions the range of operation of the PLC device presented here is up to 40m. This range of operation may be good to deploy a LAN network based on PLC.

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