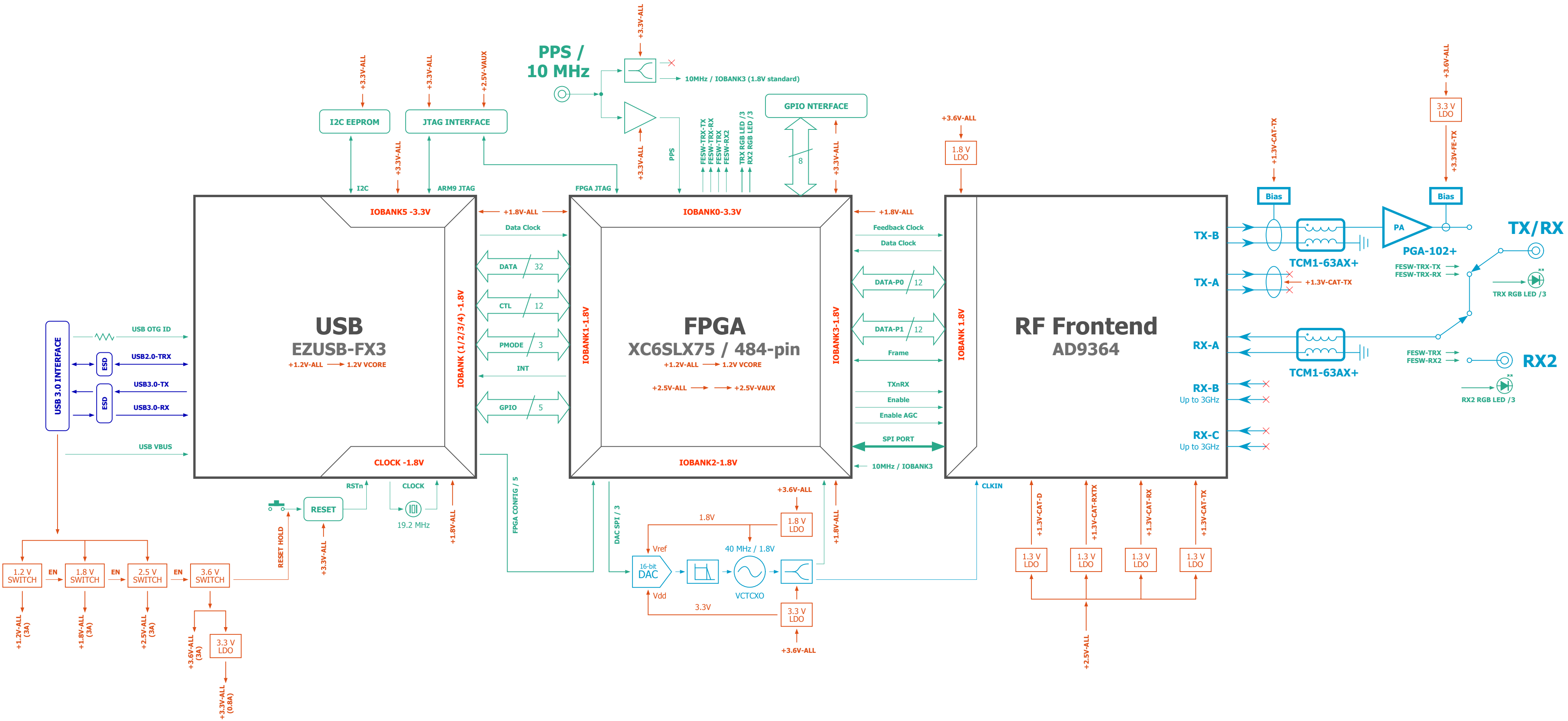


Revisions		1
REV	Description	



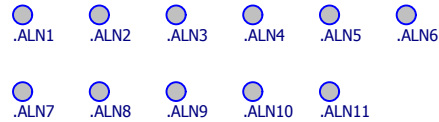
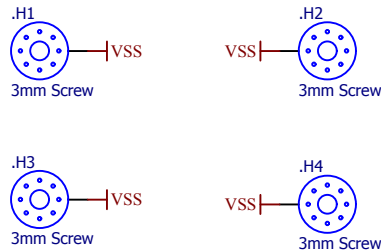
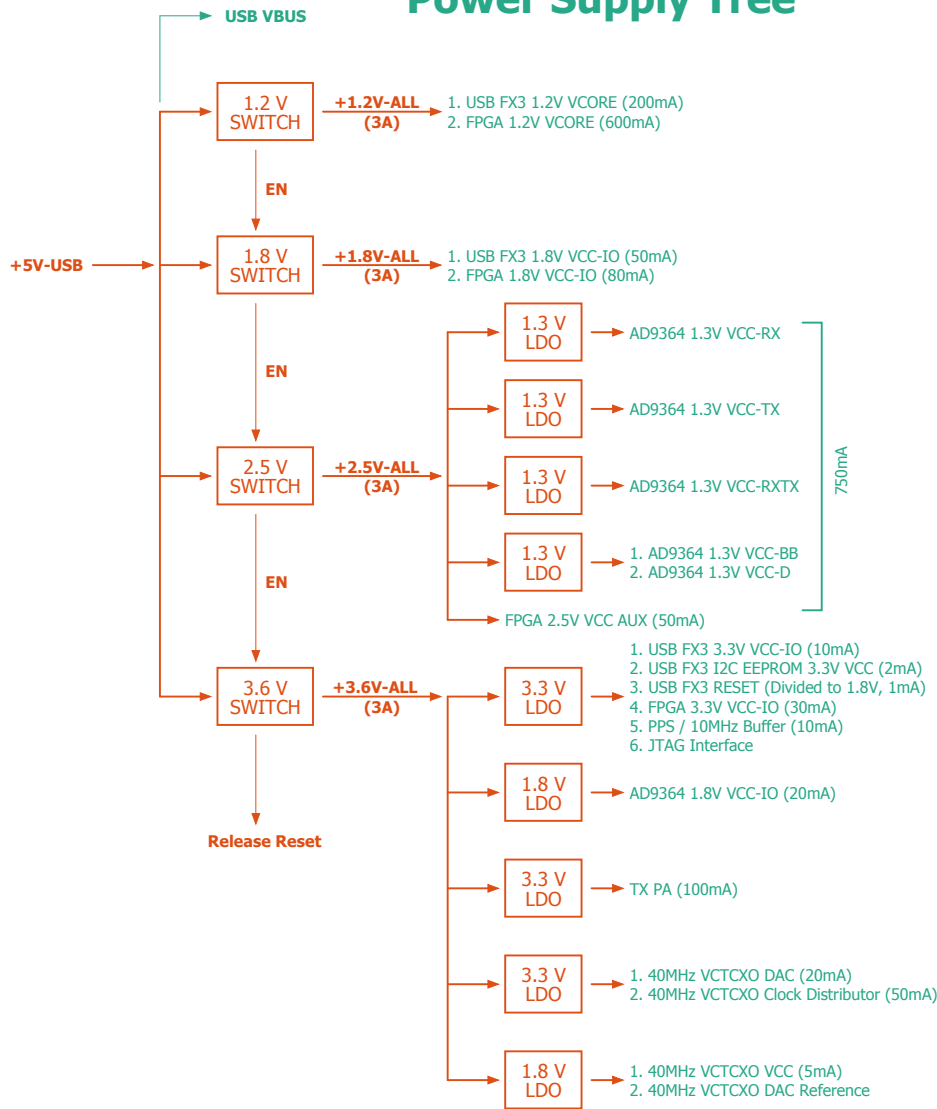
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Design Team		<div><div><div>Ettus</div><div>Research</div><div>A National Instruments Company</div></div><div>4600 Patrick Henry Drive Santa Clara, CA 95054 USA</div></div>	
DRAWN BY SHYU LEE (XU LI)	DATE 01/30/2015		
REVISOR BY -	DATE -	System Block Diagram	
VERIFIED BY MATT E, JON K, BEN H	DATE -	USRP, B200 MINI, 1X1, 70MHZ-6GHZ	
TECHNICIAN RYAN REYES	DATE -	SIZE D	REV 1
ENGINEER SHYU LEE (XU LI)	DATE 8/13/2015	DOC CODE 610-159035A-01	FILE NAME 01_BlockDiagram.SchDoc

Power Supply Tree



.LOGO1



.LOGO2

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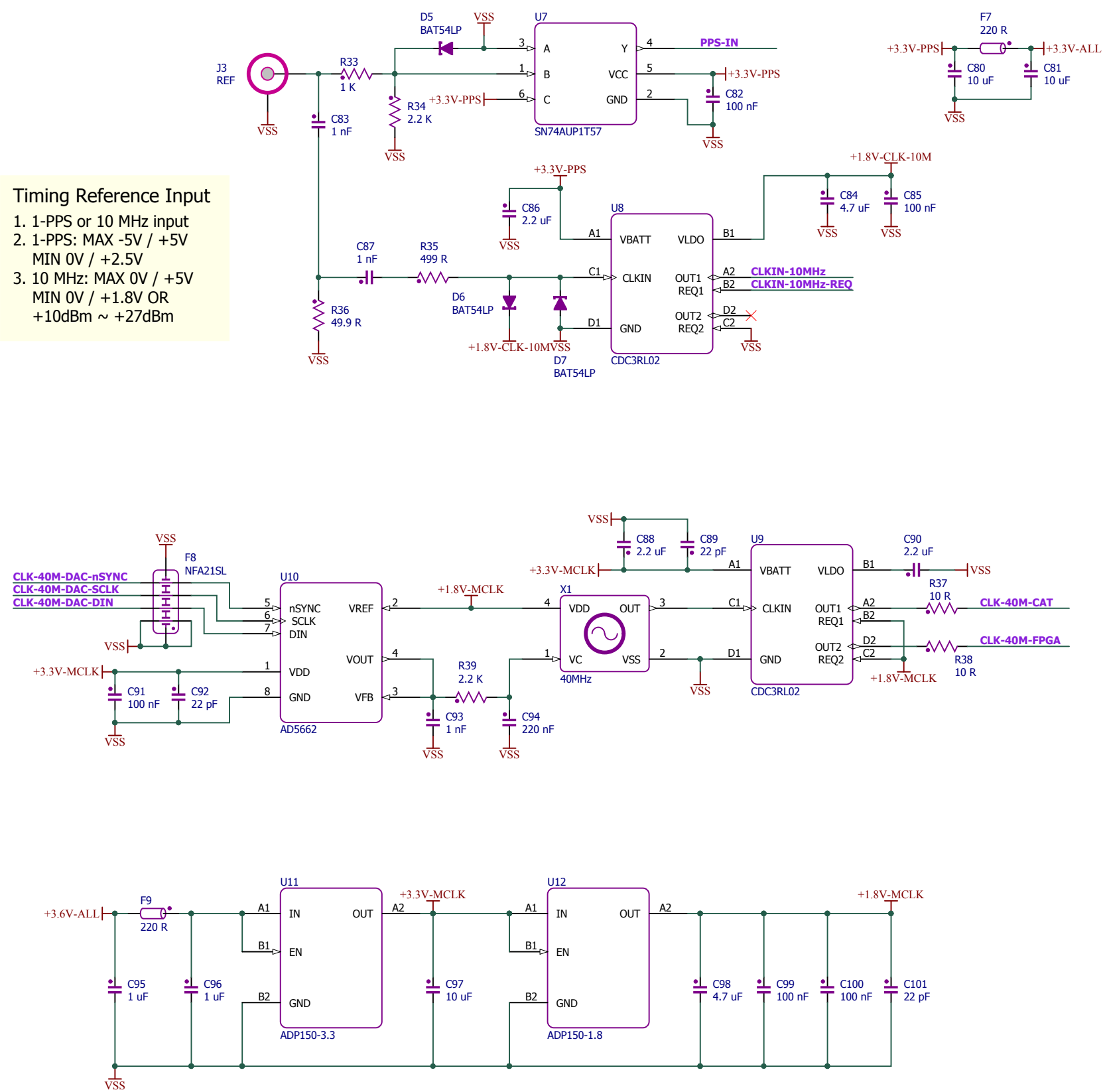
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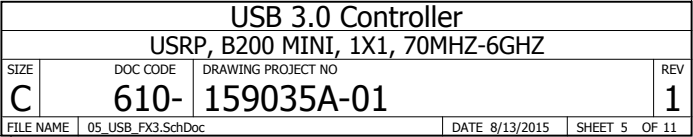
Essential Hardware Elements			
USRP, B200 MINI, 1X1, 70MHZ-6GHZ			
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FILE NAME 02_EssentialElements.SchDoc		DATE 8/13/2015	SHEET 2 OF 11

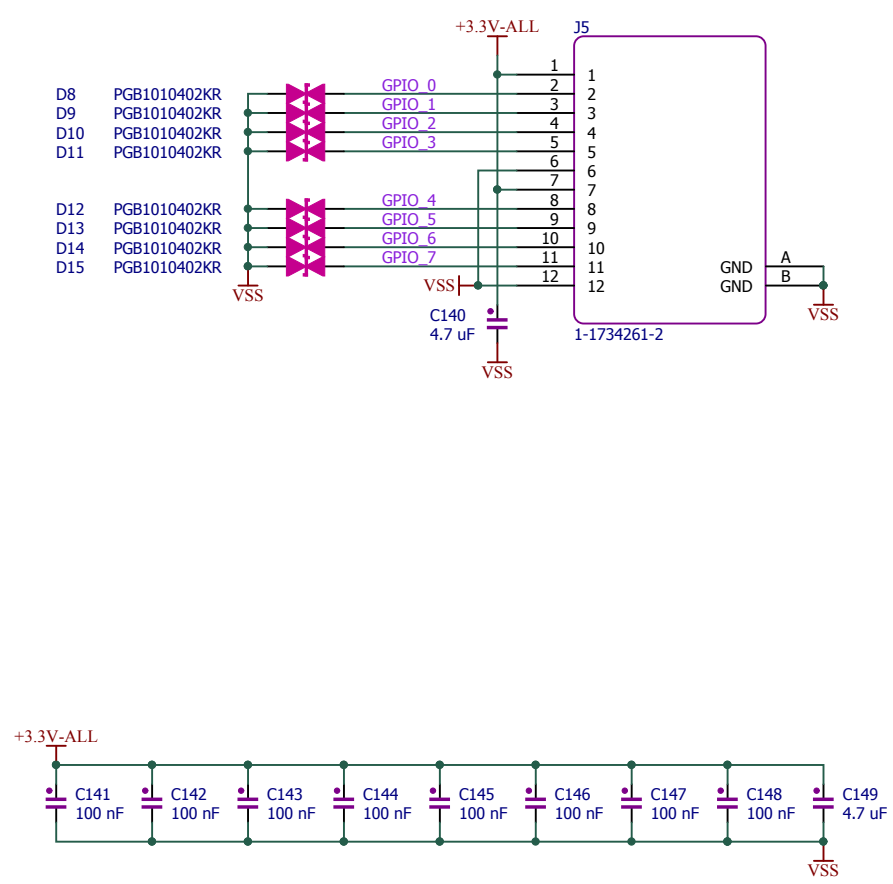
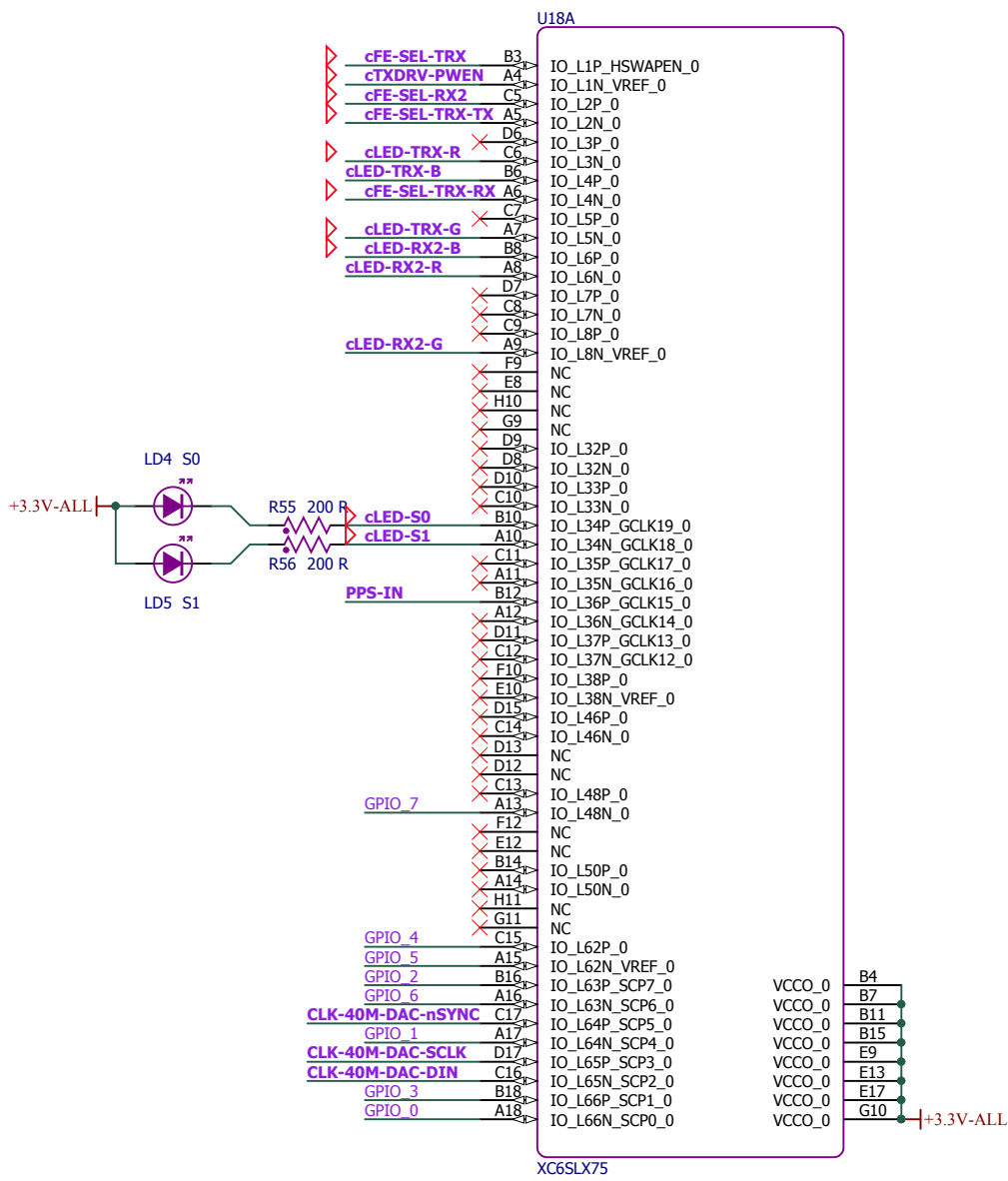


Timing Reference Input

- 1-PPS or 10 MHz input
- 1-PPS: MAX -5V / +5V  
MIN 0V / +2.5V
- 10 MHz: MAX 0V / +5V  
MIN 0V / +1.8V OR  
+10dBm ~ +27dBm



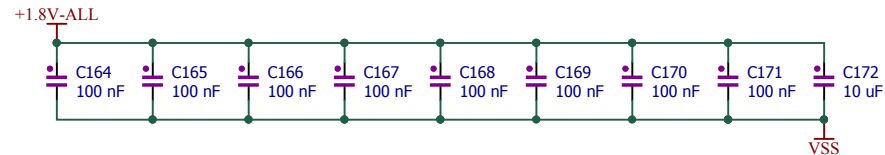
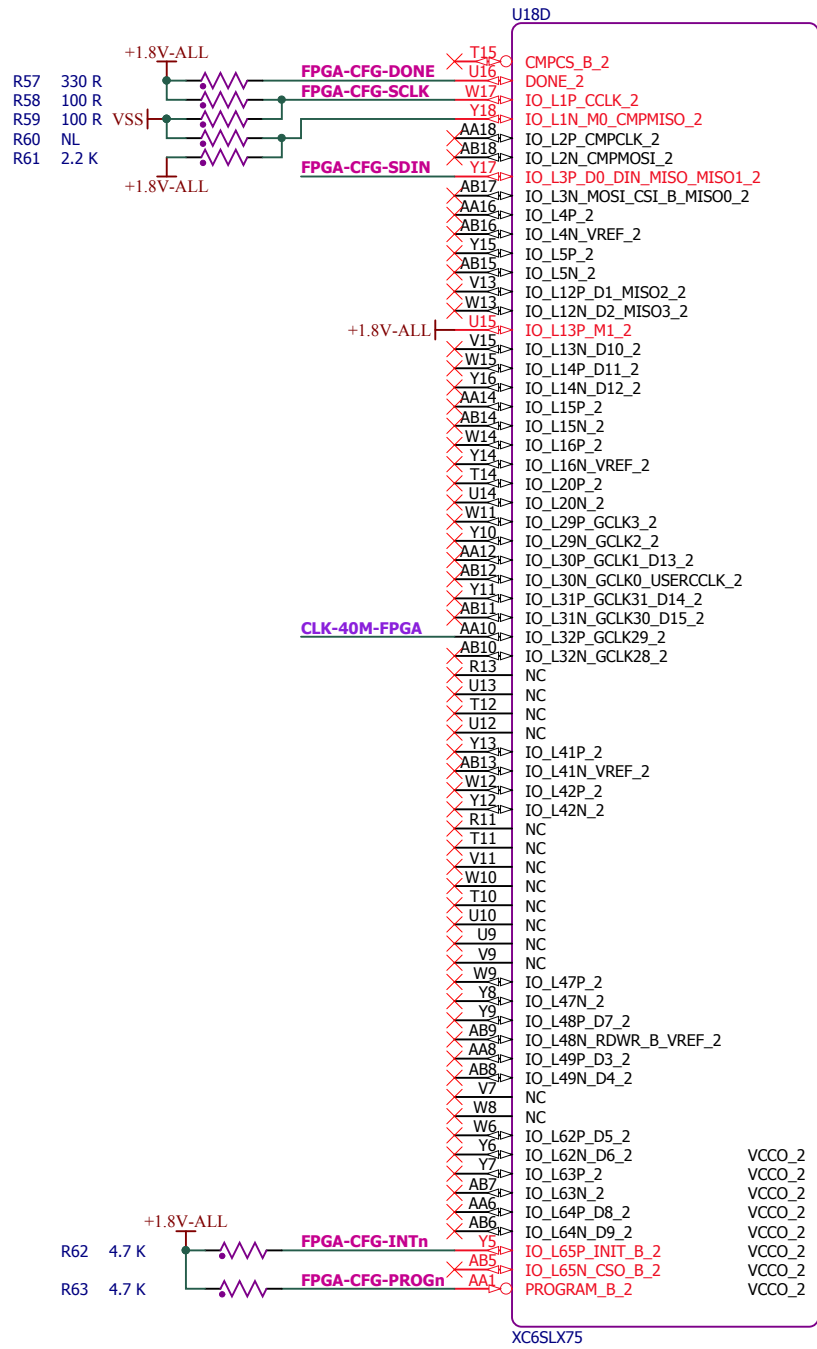




FPGA Part A: All 3.3V I/O			
USR, B200 MINI, 1X1, 70MHZ-6GHZ			
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C	610-	159035A-01	1
FILE NAME 06_FPGA_A.SchDoc		DATE 8/13/2015	SHEET 6 OF 11



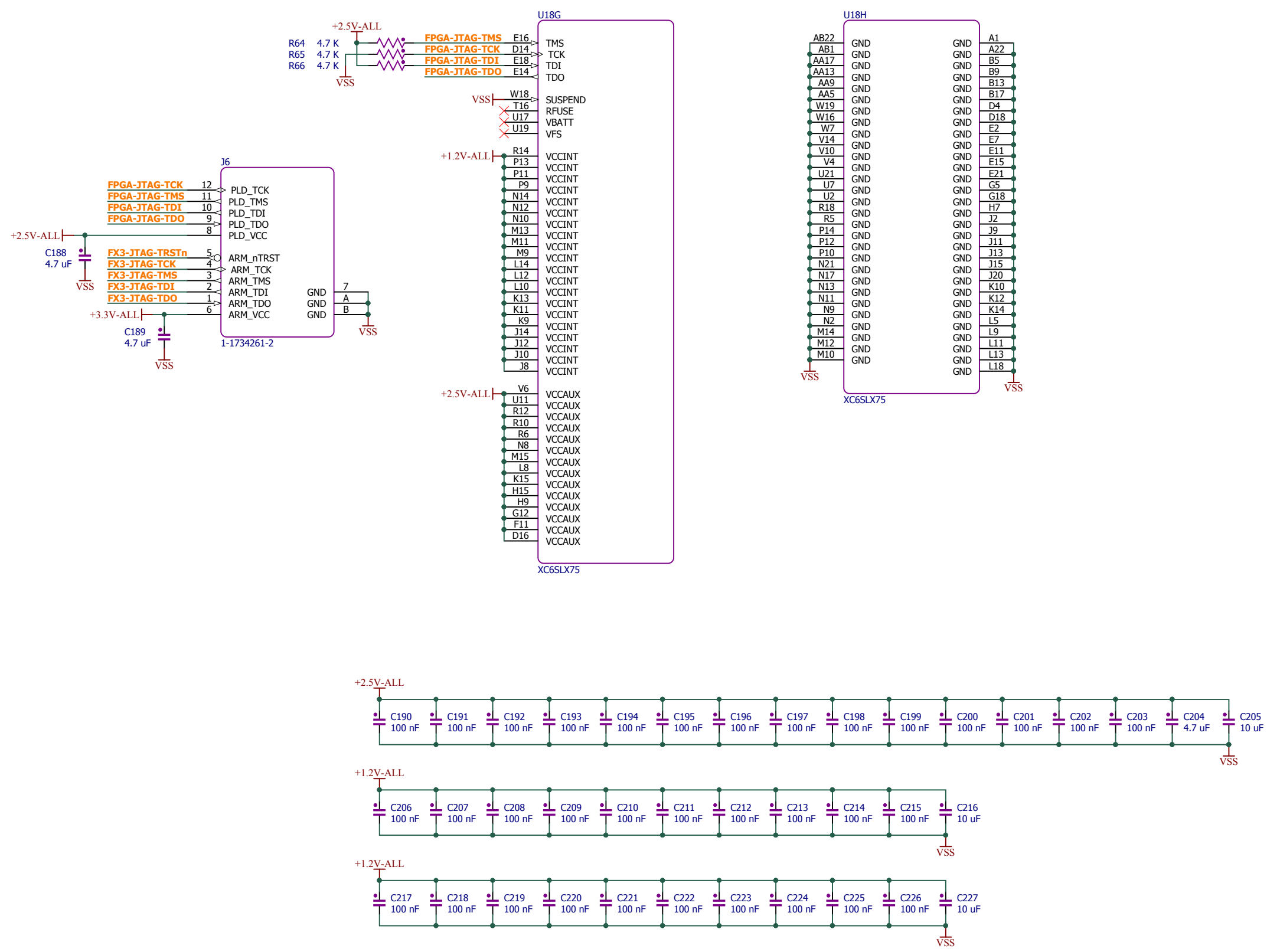




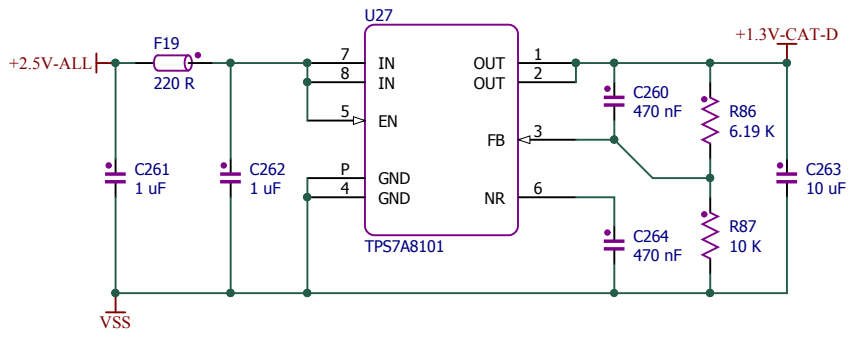
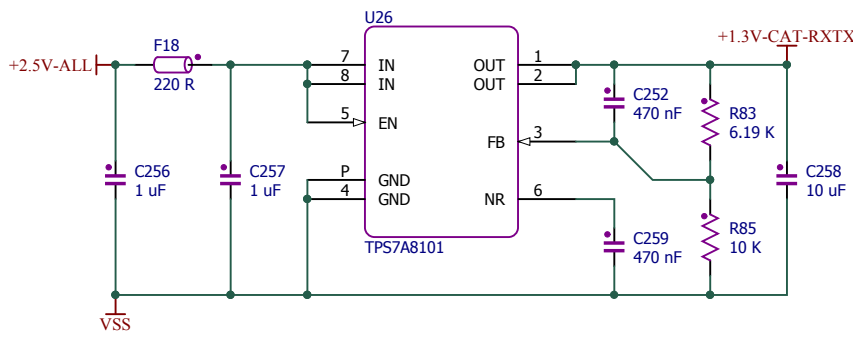
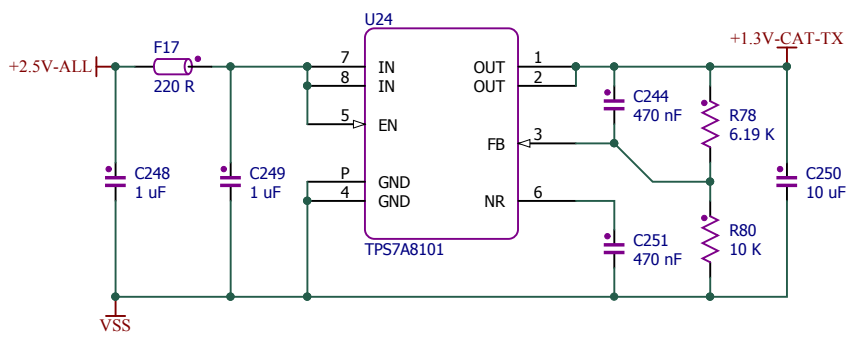
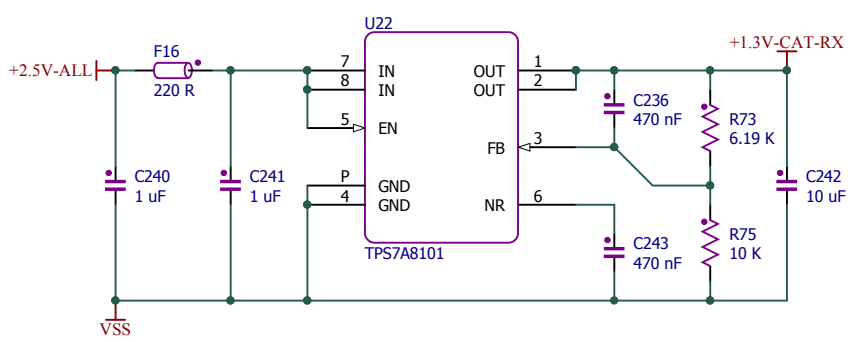
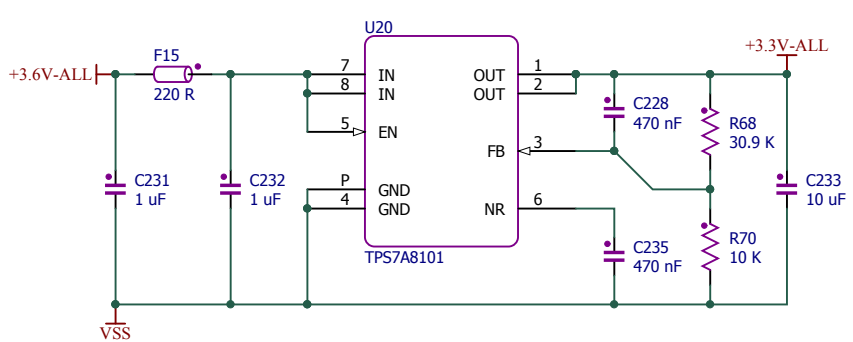
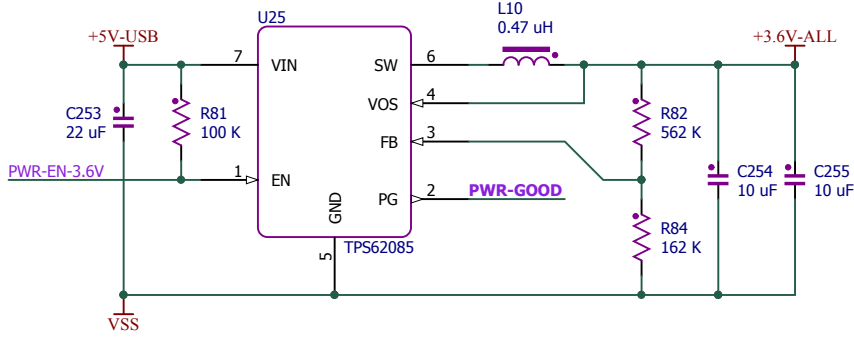
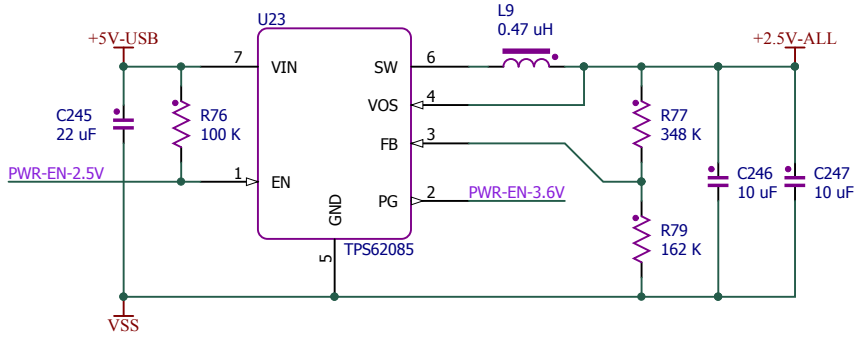
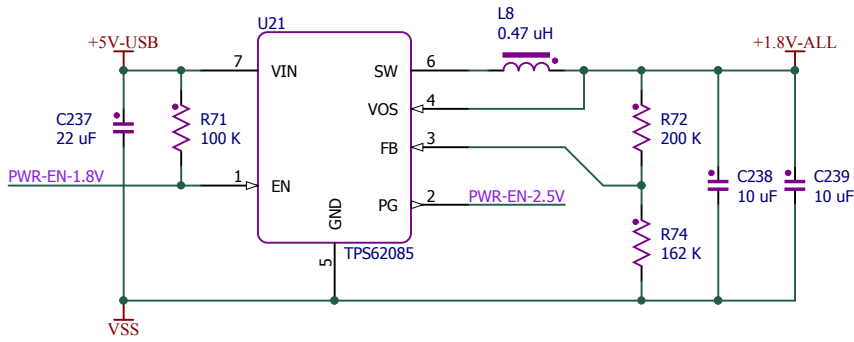
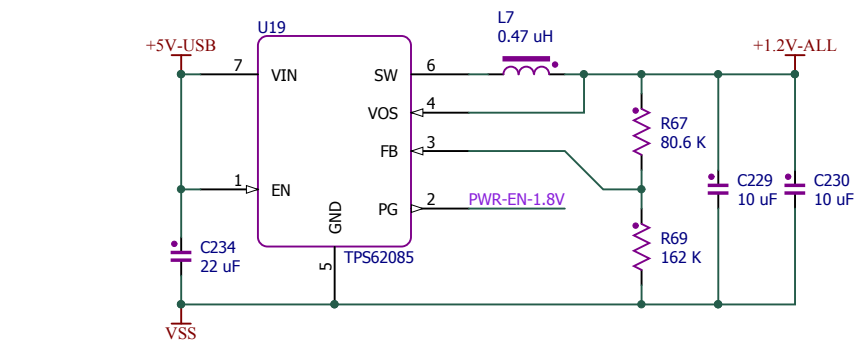
FPGA Part C: Serial Configuration Pins and Other				
USRP, B200 MINI, 1X1, 70MHZ-6GHZ				
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FILE NAME	08_FPGA_C.SchDoc	DATE	8/13/2015	SHEET 8 OF 11







FPGA Part E: Core Power and JTAG				
USRP, B200 MINI, 1X1, 70MHZ-6GHZ				
SIZE	DOC CODE	DRAWING PROJECT NO		REV
C	610-	159035A-01		1
FILE NAME	10_FPGA_E.SchDoc		DATE 8/13/2015	SHEET 10 OF 11



Power Supply				
USRP, B200 MINI, 1X1, 70MHZ-6GHZ				
SIZE	DOC CODE	DRAWING PROJECT NO		REV
C	610-	159035A-01		1
FILE NAME		11_PowerSupply.SchDoc	DATE 8/13/2015	SHEET 11 OF 11