

# Efficient CMOS Bandgap Reference Circuit

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**Abstract**— This work presents efficient bandgap reference(BGR) design using self bias current mirror circuit. This design removes one complementary-to-absolute-temperature(CTAT) bipolar device in voltage reference branch , which reduced the chip area[1]. This design shares the bipolar device used to generate proportional-to-absolute-temperature (PTAT) voltage, thus reducing overall power consumption. Use of self bias current mirror instead of traditionally used operational amplifier also reduces the power requirement, complexity and area of circuit. Different techniques like cascode current mirror [2] and symmetrically matched current mirrors[3] can be used to improve output. Design and simulation of the circuit will be in 28nm CMOS process , for a temperature range of -40°C to 125°C.

## I. INTRODUCTION

In many applications as stable voltage reference is needed which is independent of power supply and temperature variations. BGRs are extensively employed as reference circuits as they have weak dependence on process, temperature and voltage variations. There are mainly two types of BGR circuits: (a) using operational amplifier (op-amp) (b) using current mirror. Use of op-amps have some disadvantages over current mirrors like (a) op—amps require more power which can be constraint in low power applications. (b) require more number of transistors which makes it area inefficient. Current mirror based BGRs lacks in terms of power supply rejection (PSR) as compared to op-amp based design but it is simpler to design, requires less power and area with only marginal decrease in performance which makes it an attractive choice for modern applications. The PSR of simple current mirror (CM) based BGR can be improved by using cascoded current mirror (CCM) [2] or symmetrically matched current mirror (SMCM) [3]

## II. CIRCUIT DESCRIPTION

Figure 1(b) shows the core part of the proposed BGR circuit [1] in comparison with traditional circuit. From the figure it is clear that proposed circuit uses one bipolar device less in reference branch. The BJT  $Q_2$  is used for generation of PTAT voltage across the resistor  $R_1$  and voltage across it adds to  $V_{REF}$ . This modification helps is reduction in power and area.

Calculations of  $R_1$  and  $R_2$  can be done by the formulas given below

$$R_1 = V_T \ln(N) / I_1 \quad (1)$$

$V_{R2}$  is the PTAT voltage across the resistor  $R_2$  and is given by the equation below for this architecture.

$$V_{R2} = (R_2/2R_1) \cdot V_T \cdot \ln(N) \quad (2)$$

For zero temperature coefficient of the circuit derivative of  $V_{REF}$  with respect to temperature must be zero.

$$\frac{dV_{REF}}{dT} = \frac{d(V_{BE2} + \alpha V_T)}{dT} = 0 \quad (3)$$

Where  $\alpha$  is  $(R_2/2R_1) \cdot \ln(N)$  a constant. Assuming  $dV_T/dT = 85\mu V/^\circ C$  and average  $dV_{BE2}/dT$  can be assumed  $-1.6mV/^\circ C$  although this can vary according to process

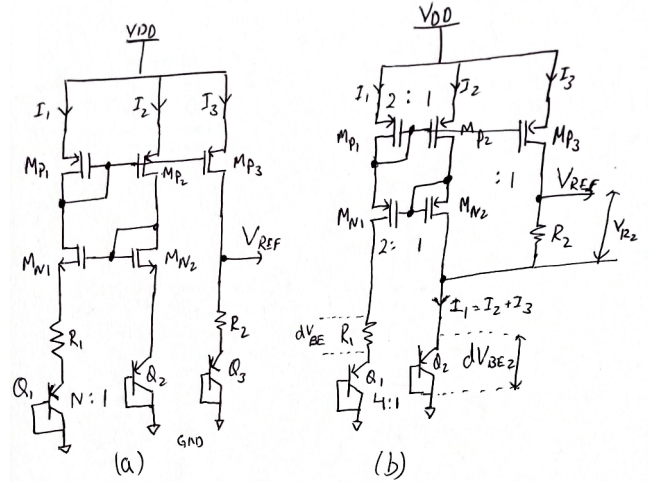


Fig 1: (a)Traditional BGR circuits, (b) Proposed BGR circuit [1]

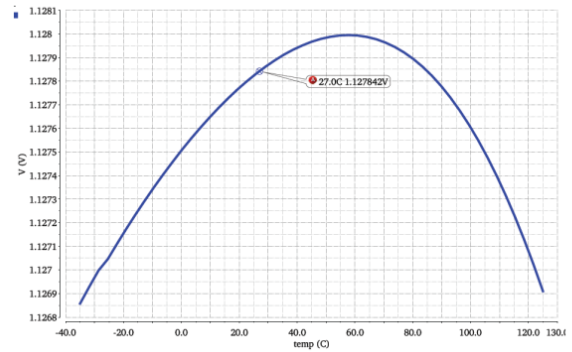


Fig 2: Simulation result from [1] VREF vs Temp for 0.06mm

TABLE I. PERFORMANCE PARAMETERS OF REFERENCE DESIGN[1] AND EXPECTED AREA

Process node	0.06 $\mu$ m
Power supply (v)	3.3-5
Temperature range ( $^\circ$ C)	-40 - 125
Reference voltage	1.15v
Temperature Coefficient	6.3 ppm/ $^\circ$ C
Line regulation	16mV/V
PSR @DC/1hz	40dB/35dB
Expected Area for 28nm	0.0200 mm <sup>2</sup>

## III. REFERENCES

- [1] Sarangi, Santanu & Tripathy, Dhananjaya & Mahapatra, Subhra & Rout, Saroj. (2020). A Power and Area Efficient CMOS Bandgap Reference Circuit with an Integrated Voltage-Reference Branch. DOI:10.31224/osf.io/4x9g8.
- [2] Wu, W., Zhiping, W., and Yongxue, Z. (2007). An Improved CMOS Bandgap Reference with Self-biased Cascoded Current Mirrors. In 2007 IEEE Conference on Electron Devices and Solid-State Circuits, pages 945–948. DOI: 10.1109/EDSSC.2007.4450282.
- [3] Lam, Y. and Ki, W. (2010). CMOS Bandgap References With Self-Biased Symmetrically Matched Current-Voltage Mirror and Extension of Sub-1-V Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 18(6):857–865, ISSN: 1063-8210, DOI: 10.1109/TVLSI.2009.2016204.