



SALEAGLE® FPGA

Datasheet

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1 Introduction

1.1 Features

■ Distributed and Embedded RAM

- Up to 156 Kbits distributed RAM
- Up to 1.1 Mbits Embedded Block RAM
- Embedded block RAM with 9Kbits storage, can be configured as true dual-port, 8Kx1 to 512x18
- ERAM9K has dedicated FIFO control logic
- Embedded block RAM with 32Kbits storage, can be configured as true dual-port, 2K*16 or 4K*8.

■ Programmable Logic Blocks (PLBs)

- Optimized LUT4/LUT5 combinatorial design
- Dual-port distributed Memory
- Arithmetic Logic
- Fast carry chain logic
- Single Slice support two M18x18s or four M9x9s

■ Source Synchronous I/O Interface

- I/O unit contains DDR register
- Generic DDR x1
- Generic DDR x2

■ High Performance, Flexible I/O

Buffer

- Single-Ended I/O standard
- LVTTL
- LVCMOS (3.3/2.5/1.8/1.2V)
- PCI
- Following differential I/O standards are available by configuration
 - LVDS, LVPECL
 - Hot Socketing
 - Programmable pull-up and pull-down mode
 - On-chip 100Ω differential resistance

■ Clock Resource

- Two fast clocks for optimizing Global clock
- Two IOCLKs per Bank for high-speed I/O interface
- 16 lines of global clock
- Support Up to four PLLs for frequency synthesis
- Five clock output
- Division factor from 1 to 128
- Five clock output cascading
- Dynamic phase selection

**■ Configuration**

- Master SPI (MSPI)
- Slave Serial (SS)
- Master Parallel x8 (MP)
- Slave Parallel x8 (SP)
- JTAG mode (IEEE-1532)

■ Unique 64-bit DNA for each chip**■ BSCAN**

- Compatible with IEEE-1149.1

■ Embedded Hard Core IP

- ADC
- 8-bit SAR
- Eight analog Input
- 1MHz Sampling Rate (MSPS)

■ Package

- FBGA
- QFN

Table 1-1 EAGLE FPGA Selection Guide

General feature	EAGLE_4X20	EAGLE_4A20
Number of LUTs	19,600	19,600
Number of FFs	19,600	19,600
Equivalent Number of LUTS	23,520	23,520
Number of Dis-Ram bits	156,800	156,800
Number of ERAM9K	64	64
Number of ERAM32K	16	16
Total ERAM bits	1,114,112	1,114,112
Number of DSP	29	29
PLL	4	4
Low-skew GCLOCKk in chip	16	16
User IO Banks	8	8
Maximum user IOs	193	196



Table 1-2 EAGLE FPGA Package

Packages	EAGLE_4X20	EAGLE_4A20
144 TQFP (20x20, 0.5mm pitch)	-	
256FBGA (17x17, 1.0mm pitch)	193/89	196/90
QFN88 (10x10, 0.4mm pitch)		71/17
LQFP144 (20x20, 0.5mm pitch)	107/47	

Note: 193/89 indicates the available IO number/ available LVDS pairs for users



1.2 EAGLE Devices Introduction

EAGLE family FPGA locate low-cost and low power consumption programmable markets. EAGLE family devices are targeted for mass, cost-sensitive applications, which can meet designers growing bandwidth requirements while reducing cost.

Built on an optimized low power consumption technology, EAGLE family devices deliver high performance that serve as the most ideal solution for low-cost and small applications in many markets like telecommunication, audio, industrial and mobile.

Several available design tools that allow complex designs to be efficiently implemented by using the EAGLE family devices. Along with the industry-leading synthesis, place and route tools, EAGLE family devices provide a strong guarantee for users to design high-quality products.

2 EAGLE Architecture Overview

The EAGLE family devices contain an array of programmable logic block that is the kernel resources being surrounded by I/O Buffers. ERAM9K and DSP are embedded in the middle of PLB.

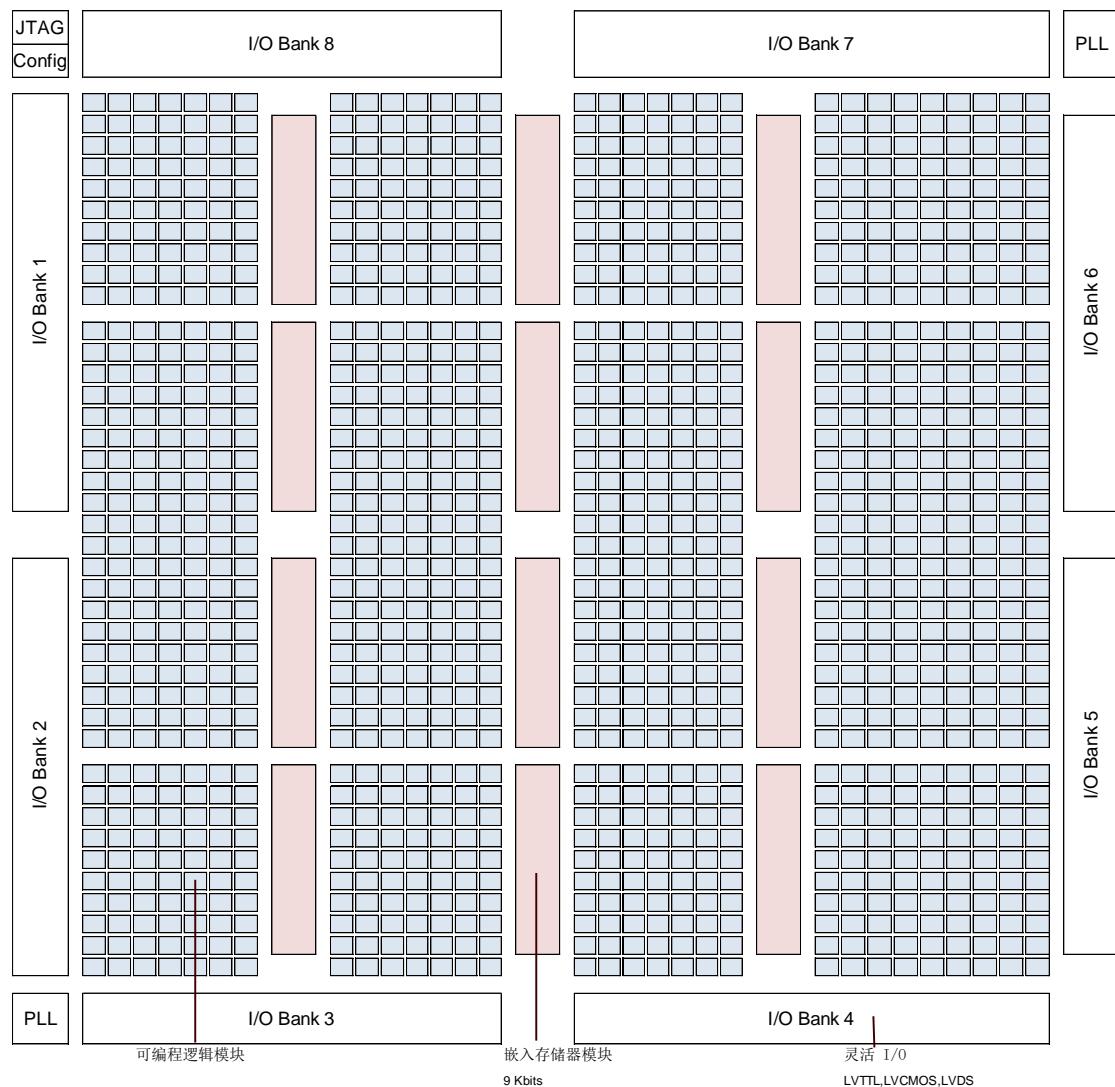


Figure 2-1 EAGLE Simplified Diagram

The logic blocks of LUTs contain logical programmable module (LSLICE) and memory logical module (MSLICE), which all have logic and arithmetic functions. While MSLICE supports distributed RAM and ROM functions. Both LSLICE and MSLICE have been optimized that allows complicated design to be implemented efficiently.

The EAGLE family devices contain multi-column 9Kbits ERAM, supporting fast data access. Each Memory block can be independently configured as 1-18bits width single or dual-port applications.



The I/O Buffer of EAGLE is divided into 8 banks, supporting single and double-ended voltage standards. I/O from left and right sides can be configured as LVDS transmitting/receiving pairs.

EAGLE devices contain 2-4 multi-functional PLL blocks, which are located at the four ends of the device and be connected to 2 PLL input by dedicated clock routes. The PLLs have divide/multiply/phase shifting capabilities that are used to manage the clock.

2.1 PFB Blocks

Programmable Logic Blocks (PLB) are arranged in a two-dimensional grid with rows and columns. Each PLB has programmable Routing and Programmable Functional Block (PFB). PFB is the kernel resource of FPGA, which has logic, arithmetic, distributed RAM, ROM and signals latch capabilities. PFB contains four SLICE numbered 0 to 3. Slice 0,1 are MSLICE, SLICE 2,3 are LSLICE.

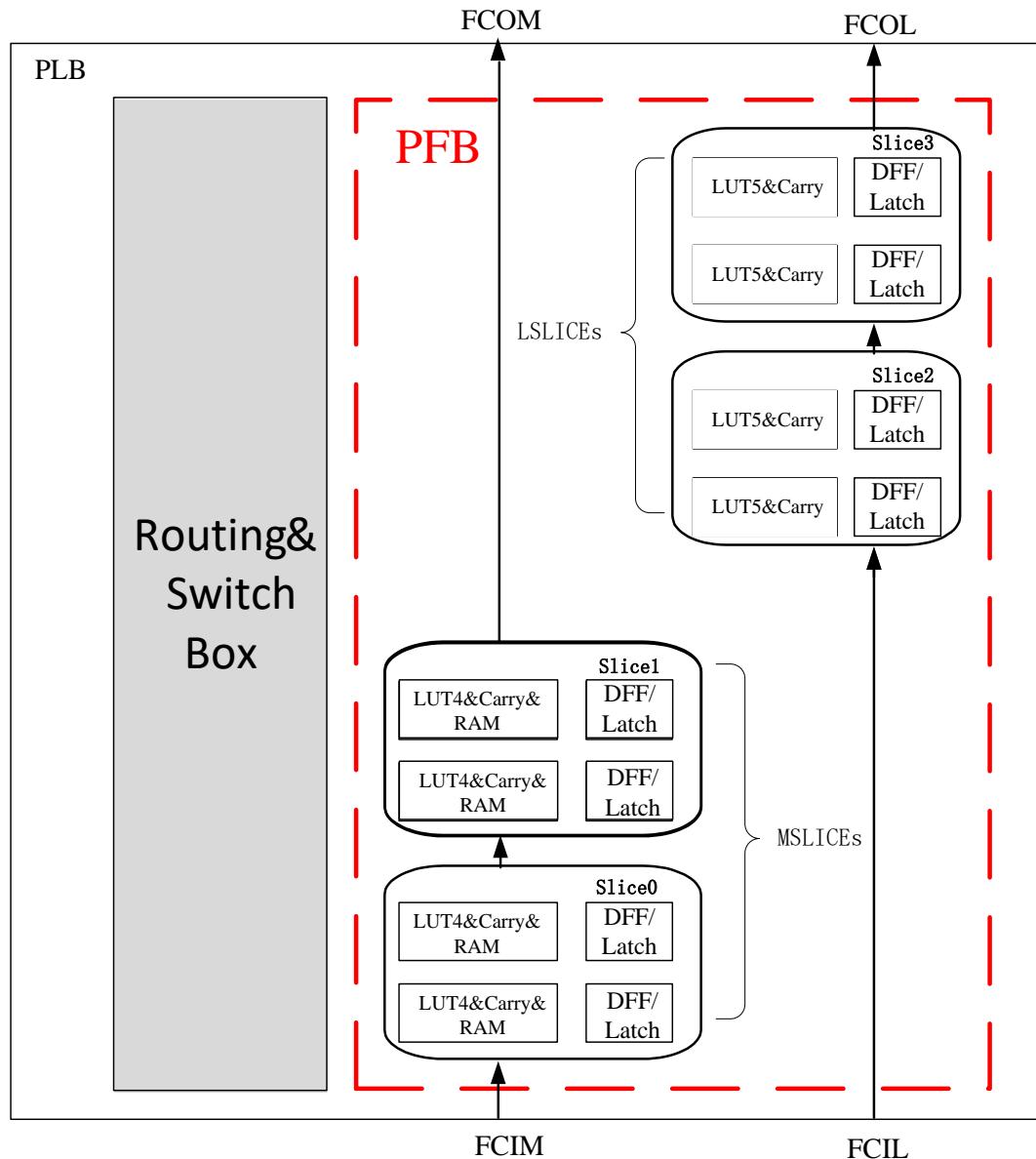


Figure 2-2 Programmable Functional Blocks (PFB) Diagram

2.1.1 SLICE

EAGLE PFB contains two SLICE: MSLICE and LSLICE

a) MSLICE

MSLICE contains 2 LUT4s, 2 registers and two-level carry chain. MSLICE can also be configured as distributed RAM based on LUT. SLICE 0-1 in PFB are MSLICE, which can be configured as 16x4 RAM. The internal logic of MSLICE can implement the interconnection of LUT4s that can perform the function like LUT5. 2 MSLICE can be combined to perform LUT6.

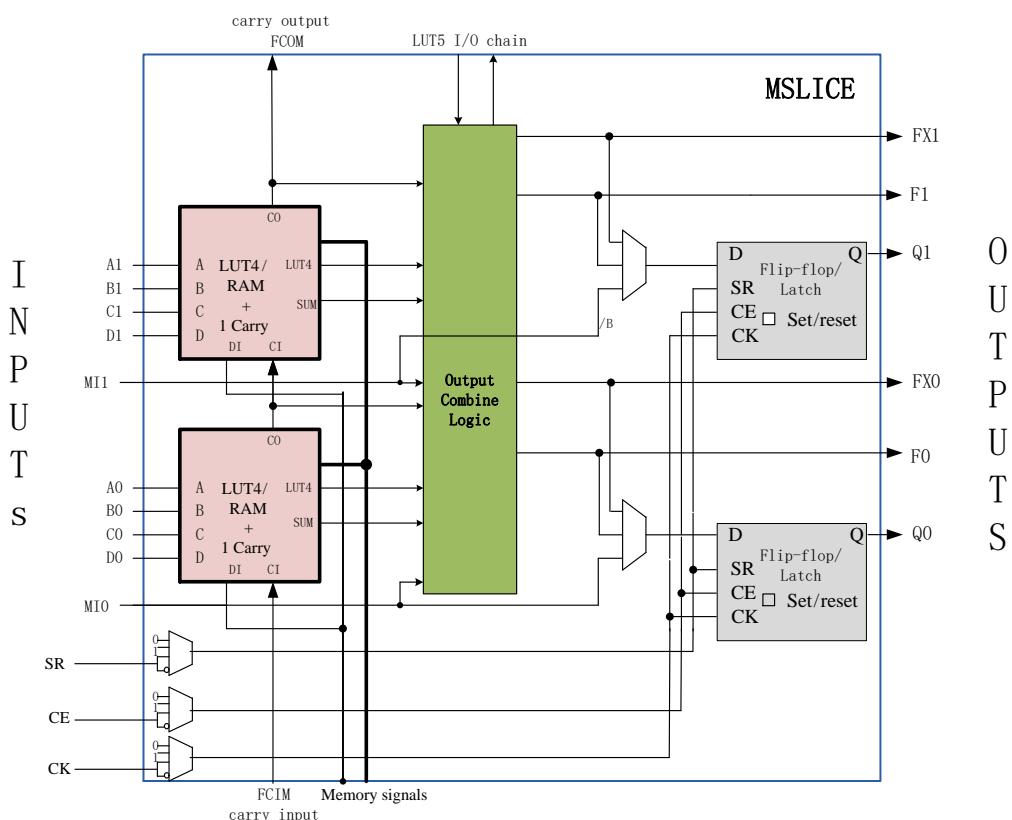


Figure 2-3 MSLICE Structure Diagram

The internal logic of MSLICE as shown in the figure 2-3. It has 2 LUT4s and RAM written decoder with distributed RAM control logic in PFB that allow each LUT4 to perform 16x1 bits RAM Memory, two MSLICEs can be combined with one RAM controller to perform 16x4 dual-port RAM. And each LUT4 in MSLICE can be combined with internal logic and internal input (FCIM) to implement 1bit full adder. 1 MSLICE can implement 2bits addition/subtraction and fast carry/borrow output. (FCOM)

MSLICE and LSLICE have same internal registers that can be configured as DFF

or LATCH.

b) LSLICE

LSLICE contains 2 enhanced LUT5s, 2 registers and four-stage carry chain. SLICE 2,3 are LSLICE. LSLICE internal logic allows 2 LUT4s dissembled from one LUT5 and implements more function like LUT5, LUT6. The combination of 2 LSLICE can implement the function of LUT7.

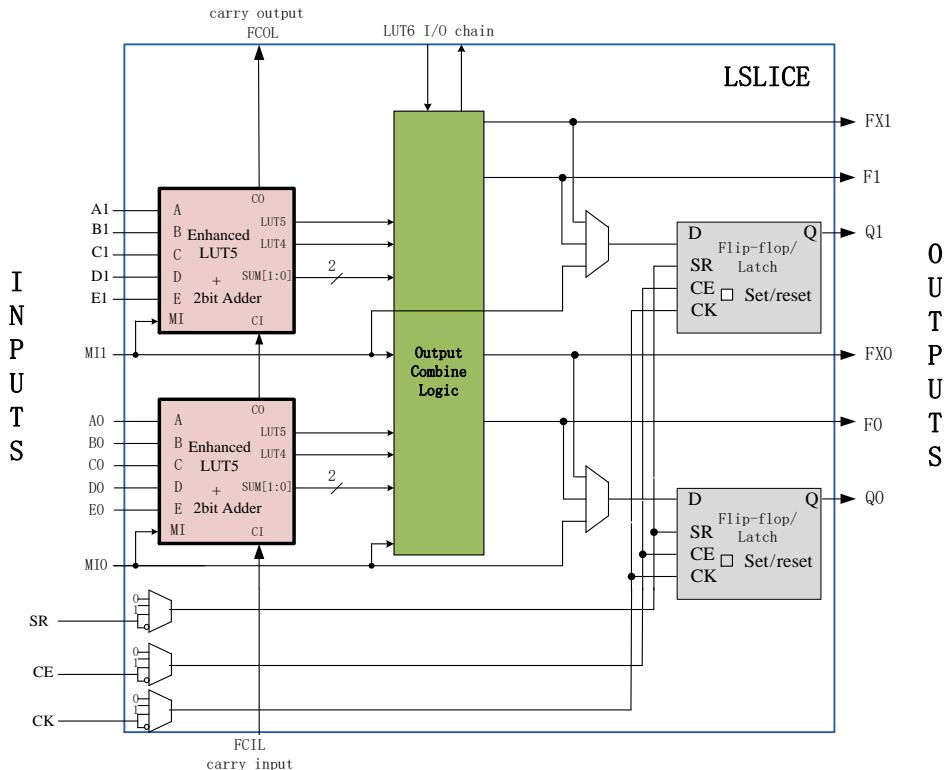


Figure 2-4 LSLICE Diagram

The internal logic of LSLICE as shown in the figure 2-4. There are four LUT4s and selection logic that can be combined to perform multi-logic functions: four LUT4s; two LUT4s + one LUT5; two LUT5s; one LUT6. Combined with internal carry logic, each enhanced LUT5 and carry input can realize 2-bit full adder. Each LSLICE can implement 4-bit addition/subtraction and fast carry/borrow output (FCOL).

2. 1. 2PFB Operation Mode

MSLICE has four modes of operation: logic, arithmetic, distributed RAM and ROM.

LSLICE has three modes of operation: logic, arithmetic and ROM.

a) Logic Mode

In this mode, the LUT4s in MSLICE are configured as 4-input combinatorial lookup table, and any four input logic function can be implemented through this look-up table. The enhanced LUT5 in LSLICE can be configured as multi-combinatorial lookup table. LUT in SLICE can implement larger scale look-up table by cascading internal output circuit.

Table 2-1 Logic Implementation

LUT5	1 MSLICE	1/2 LSLICE
MUX4	1 MSLICE	1/2 LSLICE
LUT6	2 MSLICE	1 LSLICE
LUT7		2 LSLICE

b) Arithmetic Mode

The arithmetic mode can perform fast, efficient implementation by using SLICE internal fast carry chain. Both MSLICE and LSLICE support arithmetic mode. The supported function contains addition, subtraction, add/ subtractor with selection control, counter, multiplier and comparator.

There are two carry chains inside the PFB, which are connected to vertical MSLICE and vertical LSLICE respectively. It can implement wide-bit arithmetic by cascading vertically adjacent PFBs.

c) Distributed RAM Mode

MSLICE can be configured as this mode, two MSLICE: SLICE0 and SLICE1 can be combined with to be configured as 16x4 Simple dual-port RAM (one port write/ one port read)

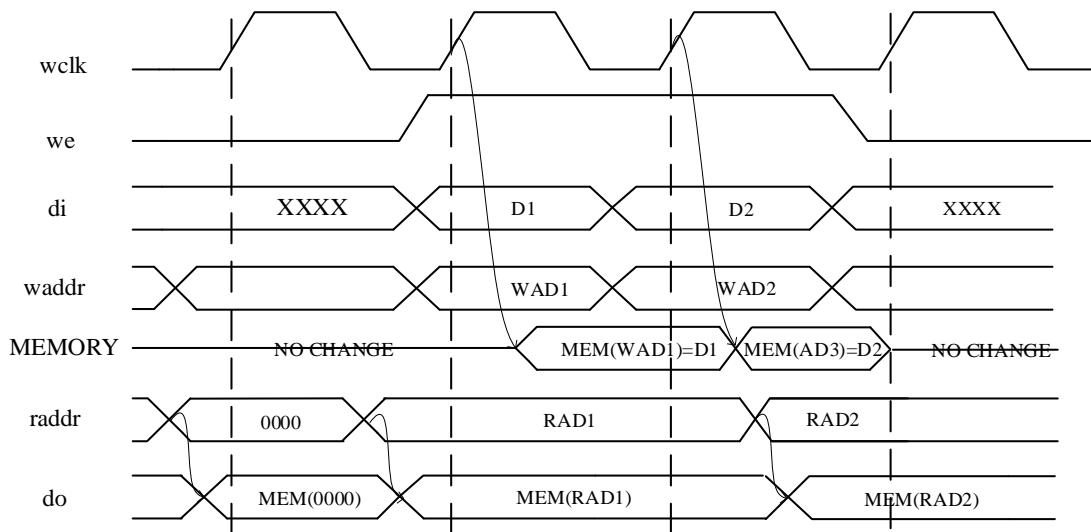


Figure 2-5 DRAM Synchronous Write/Asynchronous Read Timing Sequence

d) ROM Mode

All Slices can be used in ROM Mode under LUT logic. Users can set ROM initial value through the programming interface.

2.1.3 Register

Each SLICE in PFB contains 2 programmable registers, which can latch the output of LUT or MI input from routing. Register configuration options:

- DFF or LATCH
- Reset 0 or set 1, Reset synchronously or asynchronously
- With/Without ClockEnable
- CLK/CE/SR with rising edge/falling edge 0/1 selection.

2.1.4 Routing

There are many resources provided in the EAGLE devices to route signals between different functional blocks. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments. The EAGLE family devices contain buffers that guarantee the high-speed transmission and reliable signal integrity.

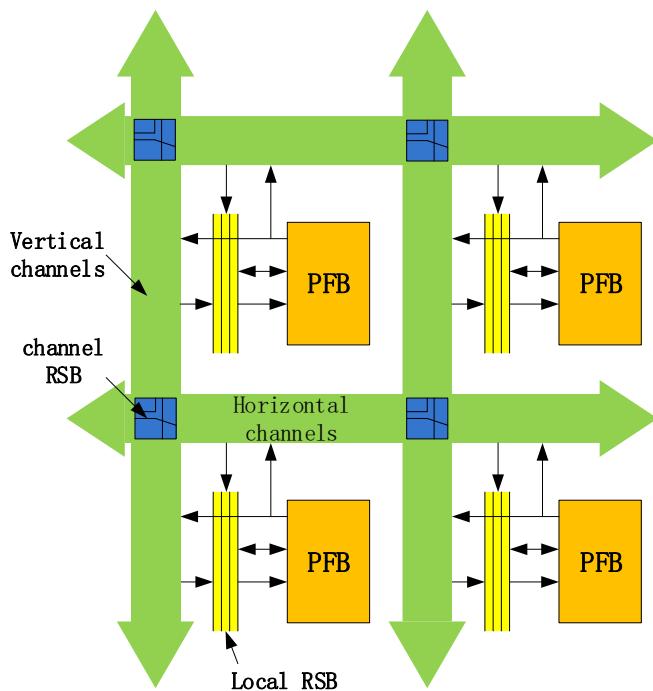


Figure 2-6 Routing Structure

Signals between PFB can be transmitted through horizontal and vertical channels. RSB (Routing switch box) is used for switching channels. Signals on the transmission path can enter into PGB through local RSB.

2.2 ERAM

2.2.1 Introduction

EAGLE family devices support ERAM, which have two types of ERAM: ERAM9K and ERAM32K.

ERAM9K has the capacity of 9Kbits per block, and multi-ERAM9K blocks arranged by column in PFB. The height of ERAM9K is equivalent to 2.25 PFB. The height of four ERAM9K is equivalent to that of 9 PFB.

ERAM32K has the capacity of 32Kbits per block, which is arranged in the gap of 10.

ERAM9K can support the following operation modes:

- Single Port RAM/ROM
- True Dual-port RAM
- Simple Dual-port RAM (Pseudo Dual-port)



- FIFO (ERAM9K has embedded hardware FIFO controller)

ERAM9K special features:

- 9216 (9k) bits/ per block
- Independent A/B port clock
- A/B port data width can be configured independently, true dual-port range from x1 to x9, supporting x18 simple dual-port (one port read/ one port write)
- 9-bit or 18-bit write operation with Byte Enable control
- Option to output register (Support one-stage pipeline)
- Data can be initialized in RAM and ROM Mode (to initialize ERAM9K DATA during configuration process through initial document)
- Write operations mode: Normal, Read-before-write, Write-through

Table 2-2 ERAM9K Features

Type	Features
Capacity	9K
Configuration (Depth x Width)	8192 x 1, 4096 x 2, 2048 x 4, 1024 x 8 or 9, 512 x 16 or 18
Parity bits	8+1, 16+2
Byte enable	Supported (Optional)
Input address/ Data Register	Yes
Single-port mode	Supported
Simple dual-port mode	Supported
True dual-port mode	Supported
ROM Mode	Supported
FIFO Mode	Supported
Data output register	Yes (Optional)
Independent data output register enable	Yes

Read-during-write	read before write write through
RAM initialization before operation	Supported

Byte Enable

ERAM9K supports Byte enable, which can mask the input data byte-by-byte so that only specific bytes of data are written to RAM. The Byte Enable [1:0] signal corresponds to the datain [15:8] and datain [7:0] of written data.

Read-during-Write

EAGLE family devices ERAM9K supports same-port read-during-write. Read-during-write refers to users reading data to output port while input data in single-port RAM or true dual-port RAM Mode. By default, non-rdw choice, output data remains No change.

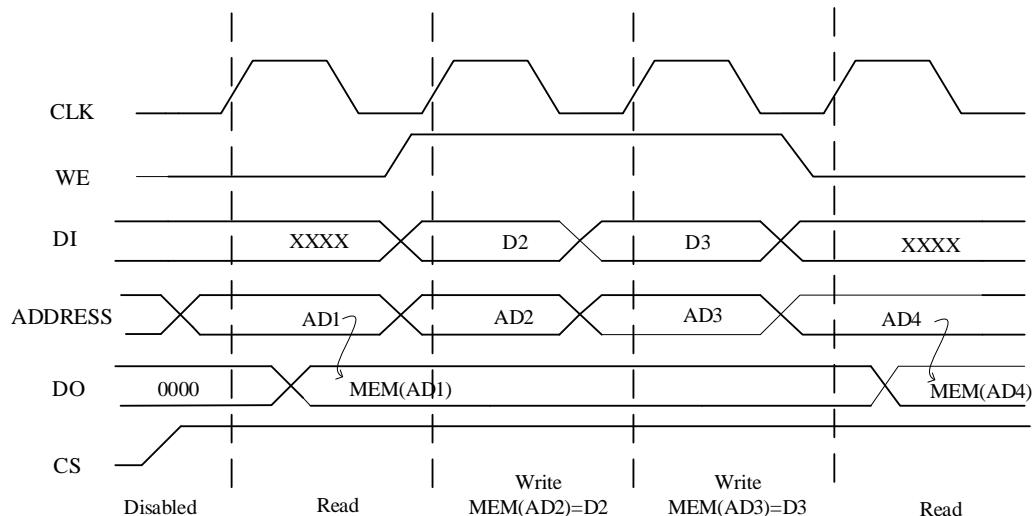


Figure 2-7 No change Waveform

Users have two choices in RDW mode: Read before Write; Write through.

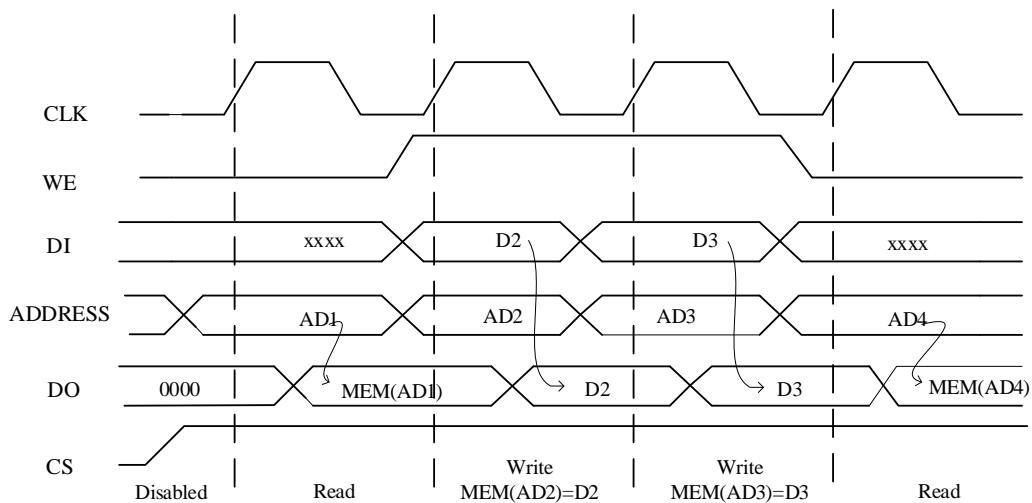


Figure 2-8 Write Through waveform

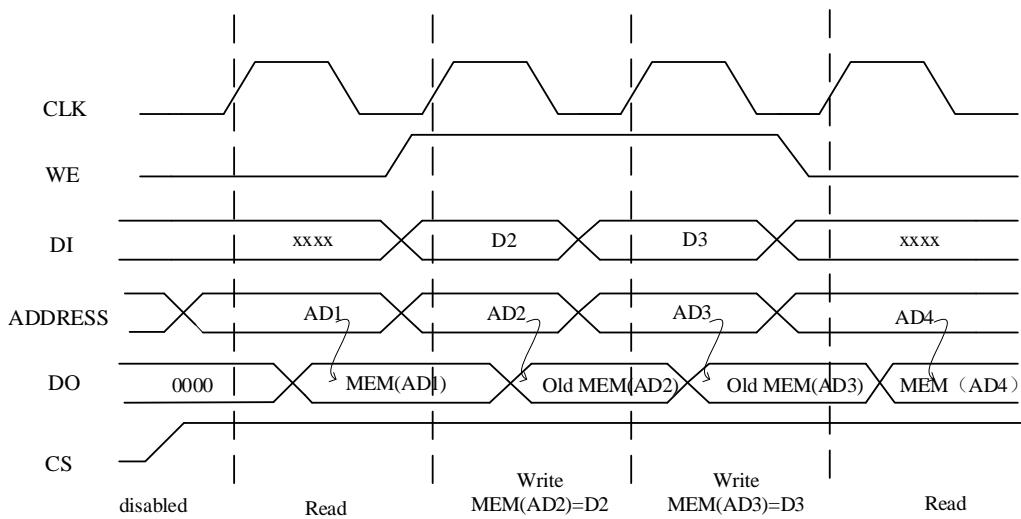


Figure 2-9 Read Before Write waveform

2.2.2 RAM Memory Mode

ERAM9K can implement RAM Memory Mode (including ROM) and FIFO mode. User port name and setting have slightly different.

ERAM9K is independent A/B dual-port RAM in RAM mode, supporting multi-mode synchronous RAM and ROM operations.

2.2.3 Ports Signals in RAM mode

Control and clock signal of ERAM9K A/B port are completely independent, input control signals as following:



ChipSelect

Clock Enable

Input/ Output register reset control signal (RST)

Write/ Read Enable

Data output register latch enable (OCE)

Byte Enable [1:0]

Table 2-3 Control Signal Logic

Operation	CLK	CS	ClockEnable	RST	WE
Write	Rising edge	1	1	0	1
Read	Rising edge	1	1	0	0
IDLE	x	1	0	0	x
Save power	x	0	0	0	x

The ports of ERAM9K as shown in following table:

Table 2-4 Port signal in RAM Mode

Port A	Direction	Description
dia[8:0]	Input	Data input to Port A, as low 9-bit data input of simple dual-port 18-bit mode
addr[12:0]	Input	Address input to port A, [12:4] remains valid as word address, [3:0] is decided by bit mode In simple dual-port 18-bit mode, addr[1:0] multiplexing as byte enable signal Byte Enable[1:0]
doa[8:0]	Output	Data output to port A, as low 9-bit data output of simple dual-port 18-bit mode
clka	Input	Clock input to port A, by default rising edge is valid (reversible), simple dual-port 18-bit mode as input



		address/ data port clock
rsta	Input	Port A reset signal, by default high valid (reversible), can be configured synchronous/asynchronous reset
cea	Input	Port A Clock valid control signal, by default high valid (reversible)
wea	Input	Port A write/ read operation control, 1 refers to write, 0 refers to read; Simple dual-port 18-bit mode sets as 1 when write
csa[2:0]	Input	Port A 3-bit chipselect signal (reversible) When csc[2:0]=3' b111, ERAM is selected to carry operation. 3-bit signal can be set as inverted or not separately.
oceA	Input	Port A data register clock enable, by default high valid (reversible). It is valid when output register is used (REGMODE_A= "OUTREG").
Port B	Direction	Description
dib[8:0]	Input	Data input to port B, as high 9-bit data input in simple dual-port 18-bit mode.
addrB[12:0]	Input	Address input to port B, [12:4] remains valid as word address, [3:0] is decided by bit mode.
dob[8:0]	Output	Data output to port B, as high 9-bit data input in simple dual-port 18-bit mode.
clkB	Input	Clock input to port B, by default rising edge valid (reversible), simple dual-port 18-bit mode as output address/data port clock.
rstB	Input	Port B reset signal, by default high valid (reversible), can be configured as synchronous/asynchronous reset

ceb	Input	Port B clock valid control signal, by default high valid (reversible)
web	Input	Port B write/ read operation control, 1 refers to write, 0 refers to read; simple dual-port 18-bit set as 0 when read.
csb[2:0]	Input	Port B 3-bit chipselect signal (reversible), When csb[2:0]=3' b111, ERAM is selected to carry operation. 3-bit signal can be set as inverted or not respectively.
oceb	Input	Port B data register clock enable, by default high valid(invertible). It is valid when (REGMODE_B= “OUTREG”) is used.

■ Multi Chipselect Signal

The ERAM9K in RAM and FIFO Mode can be generated by 3-bit reversible chipselect input. The logic as shown in following figure (CSA, CSB in RAM Mode/ CSW, CSR in FIFO Mode)

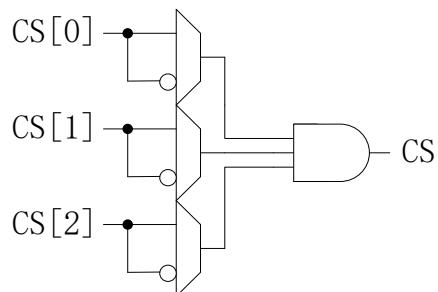


Figure 2-10 Chip Select Logic

Address decoding can be realized by 3-bit CS input inverted configuration without extra logic, which can further expand 2^8 RAM blocks RAM conveniently.

■ Byte Enable (18-bit Mode)

ERAM9K supports byte enable, which can mask the input data byte-by-byte so that only specific bytes of data are written to RAM. Byte Enable [1:0] signal corresponds to input data datain [16:9] and datain[8:0]. For example, Byte Enable [1:0]==00, neither bytes will not be written; Byte Enable[1:0]==01, write at low byte (dia). In 18-bit mode, Byte Enable [1:0] signal and port addra [1:0]

multiplexing.

■ Read-during-Write

EAGLE ERAM9K supports same port read-during-write, which refers to users reading data to output while writing data at the same address in single port RAM mode or true dual-port RAM mode. By default, Normal mode, output data remains No change.

Users have two choices: Read Before Write; Write Through.

2.2.4 Configuration of RAM Mode

a) Single-Port Mode

Single-Port Mode supports non-simultaneous read or write operation to the same address. There are two read/write control logics that manage Port A and Port B respectively. Therefore, ERAM9K can implement RAM or ROM in two single-port mode. ROM works in this mode generally.

ERAM9K supported port width in single-port mode

- 8192 x 1 (independent port A or port B)
- 4096 X 2 (independent port A or port B)
- 2048 x 4 (independent port A or port B)
- 1024 x 8, 1024 x 9 (independent port A or port B)
- 512 x 16, 512 x 18 (combined port A with port B)

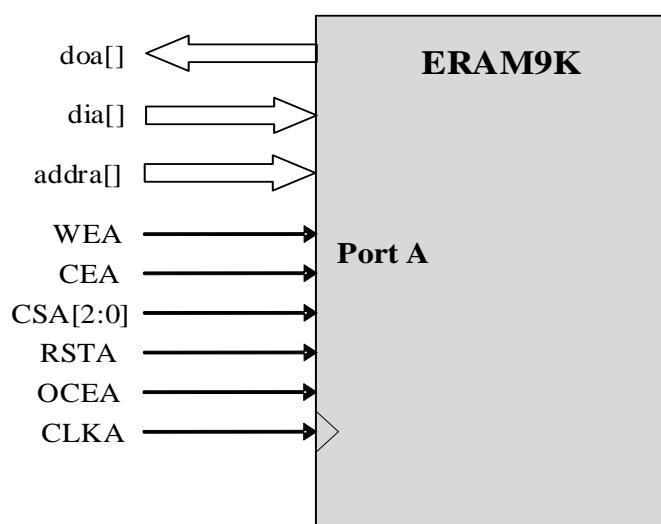


Figure 2-11 Single Port RAM (<=9 bits) with Port A

b) Simple Dual-Port Mode

When one ERAM9K is configured as 18-bit write/ read, true dual-port mode is not available, but single-port and simple dual-port mode are available. The simple dual-port mode configuration shown as following. In 18-bit mode, control signal of Port A is used as write control signal, and the control signal of Port B is used as read control signal. As 18-bit write, DIB[8:0] is used as high 9-bit data input, DIA[8:0] is used as low 9-bit data input; As 18-bit output, DOB[8:0] is used as high 9-bit data output, DOA[8:0] is used as low 9-bit data output.

When using 8/16-bit bandwidth, DIA[9], DIB[9], DOA[9], DOB[9] are forbidden to avoid mapping misalignment of internal data due to different read/write bandwidths.

Table 2-5 Simple Dual-port (9/18 bits) Data port Connection Relationship

Mode	ERAM9K RAM Port	User Port
W=18 bit R=18 bit	DIA[8:0]	wdata[8:0]
	DIB[8:0]	wdata[17:9]
	DOA[8:0]	rdata[8:0]
	DOB[8:0]	rdata[17:9]
W<=9 bit R=18 bit	DIA[]	wdata[]
	DOA[8:0]	rdata[8:0]
	DOB[8:0]	rdata[17:9]
W=18 bit R<=9 bit	DIA[8:0]	wdata[8:0]
	DIB[8:0]	wdata[17:9]
	DOB[]	rdata[]

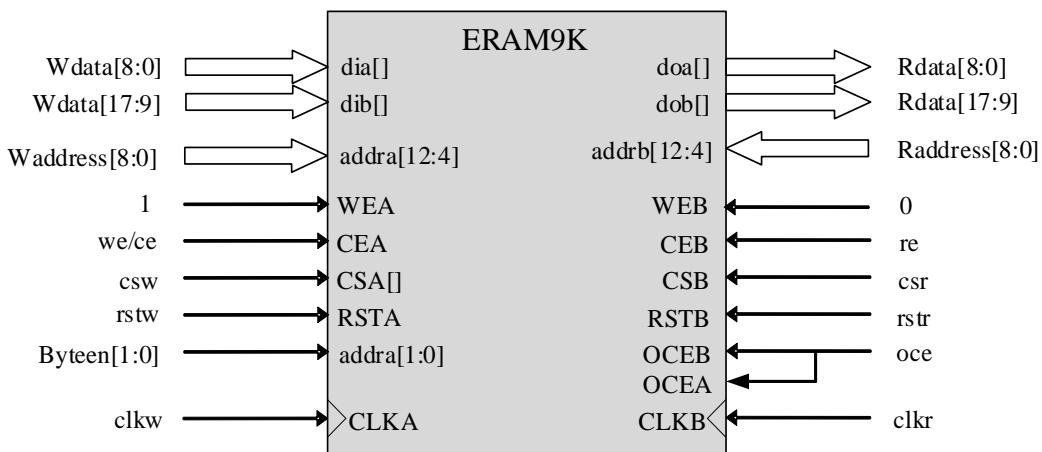


Figure 2-12 Simple Dual-ports 18-bit Write/18-bit Read Port Connection

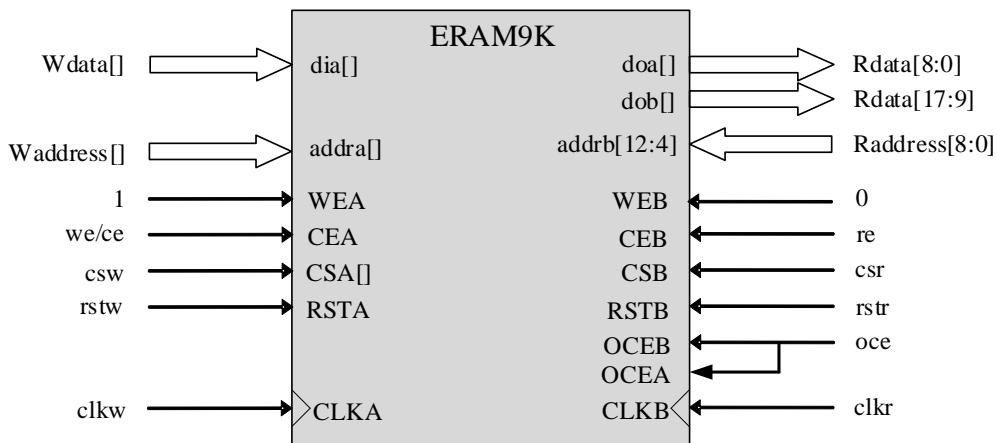


Figure 2-13 Simple Dual-ports <=9-bit Write/18-bit Read Port Connection

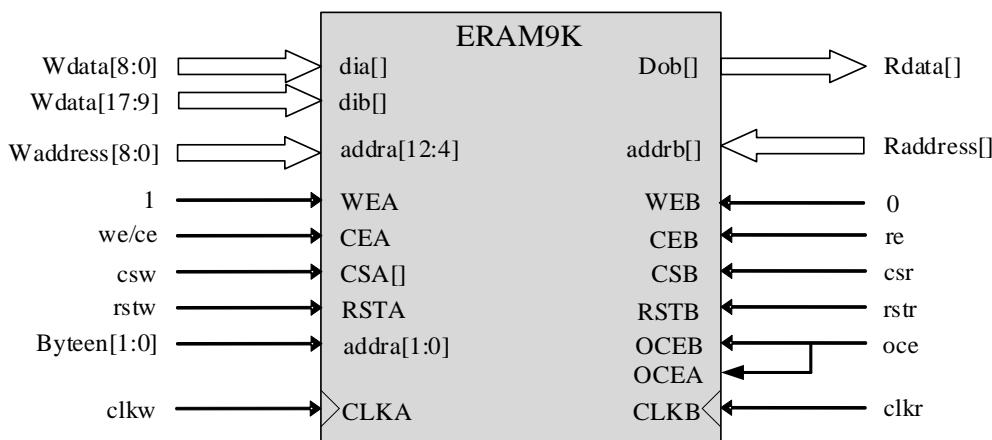


Figure 2-14 Simple Dual-ports Mode with Write(18 bits)/Read(<=9 bits) Port Connection

In simple dual-port mode, ERAM9K supports port A and port B hybrid port width selection.

Table 2-6 Configuration of Hybrid Port Bit Width

Read Port	Write Port						
	8Kx1	4Kx2	2Kx4	1Kx8	512x16	1Kx9	512x18
8Kx1	✓	✓	✓	✓	✓		
4Kx2	✓	✓	✓	✓	✓		
2Kx4	✓	✓	✓	✓	✓		
1Kx8	✓	✓	✓	✓	✓		
512x16	✓	✓	✓	✓	✓		
1Kx9						✓	✓
512x18						✓	✓

Table 2-7 WORD (16/18) and Low Address Mapping Relationship in Hybrid Width

	Port Width	Address Width	DOB[8]	DOA[8]	Corresponding WORD internal data bit of lowest 4-bit address addr[3:0]													
	18	9	0		0													
	9	10	1	0	1													
	4	11	X	X	3		2			1		0						
	2	12	X	X	7	6	5	4	3	2	1	0						
	1	13	X	X	15	14	13	12	11	10	9	8	7	6	5	4	3	2
18/16 bit WORD internal data bit			17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2

c) True Dual-Port Mode

True dual-port mode supports read, write and combined operation independently of port A/ port B: both read ports, both write ports, one write port and one read port.

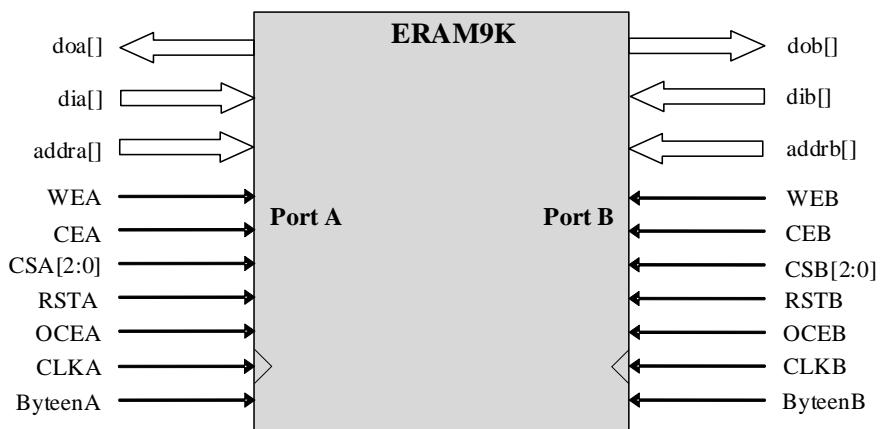


Figure 2-15 Bit Width <= 9-Bit Port A/B Dual-port RAM

Table 2-8 Supported Hybrid Port Width Configuration in True Dual-port Mode

Read Port	Write Port				
	8Kx1	4Kx2	2Kx4	1Kx8	1Kx9
8Kx1	✓	✓	✓	✓	
4Kx2	✓	✓	✓	✓	
2Kx4	✓	✓	✓	✓	
1Kx8	✓	✓	✓	✓	
1Kx9					✓

d) ROM Mode

ERAM9K supports ROM mode. ROM content is reserved in the initialized file and be written to ERAM9K during chip programming download. The initialized file can be set by MIF document during IP generation. ROM output can be latched with or without register. The read operation of ROM is in the same sequence as the read operation of single-port RAM.

2.2.5 FIFO Mode

ERAM9K integrates FIFO controller internally, and hardware supports synchronous/ asynchronous FIFO mode. ERAM9K bit-width setting is same as simple dual-port RAM in FIFO mode, supporting up to 18-bit input and output.



Table 2-9 Port in FIFO Mode

Input Port	Direction	Description
dia[8:0]	Input	Data input to FIFO, as low 9-bit data input in FIFO mode (16/18-bit input).
dib[8:0]	Input	Only as high 9-bit data input in FIFO mode (16/18-bit mode), other bit-width unused.
clkw	Input	Clock input to FIFO write port, by default rising edge is valid (invertible).
rst	Input	FIFO internal write pointer/read pointer reset signal (invertible).
we	Input	FIFO write enable, 1 refer to write operation, 0 refer to none operation.
csw[2:0]	Input	FIFO write port 3-bit chipselect signal (invertible), similar to RAM mode.
Output Port	Direction	Description
doa[8:0]	Output	Only as low 9-bit data output in FIFO mode (18-bit output), other bit-width unused.
dob[8:0]	Output	<=9bit as data output, as high 9-bit data output in FIFO mode (18-bit output).
clkr	Input	Clock input to read port, by default rising edge valid. (invertible)
rprst	Input	FIFO read pointer reset signal
re		FIFO read enable, 1 refers to read, 0 refers to none operation.
csr[2:0]	Input	FIFO read port 3-bit chipselect signal (invertible), similar to RAM mode
orea	Input	doa port data register clock enable, by default high active (invertible). It is active when (REGMODE_B="OUTREG") is used.
oreb	Input	dob port data register clock enable, by default high active (invertible). It is active when (REGMODE_B=



		“OUTREG”) is used.
FIFO Flag	Direction	Description
empty_flag	Output	FIFO read empty flag, synchronize to clkr
aempty_flag	Output	FIFO almost read empty flag, synchronize to clkr. The advance relative to empty_flag depends on latency is decided by AE_POINT parameters
full_flag	Output	FIFO Full flag, synchronize to clkw. FIFO full capacity is decided by FULL_POINTER Parameters.
afull_flag	Output	FIFO almost full flag, synchronize to clkw. FIFO almost full capacity is decided by AF_POINTER parameters

Table 2-10 Supported Hybrid Port Bit-Width Configuration in FIFO Mode

Read Port	Write Port						
	8Kx1	4Kx2	2Kx4	1Kx8	512x16	1Kx9	512x18
8Kx1	✓	✓	✓	✓	✓		
4Kx2	✓	✓	✓	✓	✓		
2Kx4	✓	✓	✓	✓	✓		
1Kx8	✓	✓	✓	✓	✓		
512x16	✓	✓	✓	✓	✓		
1Kx9						✓	✓
512x18						✓	✓

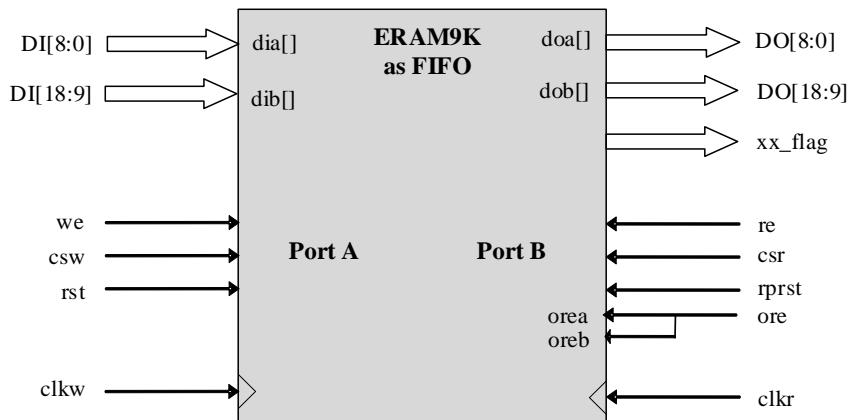


Figure 2-16 18-bit input/ 18-bit output FIFO mode

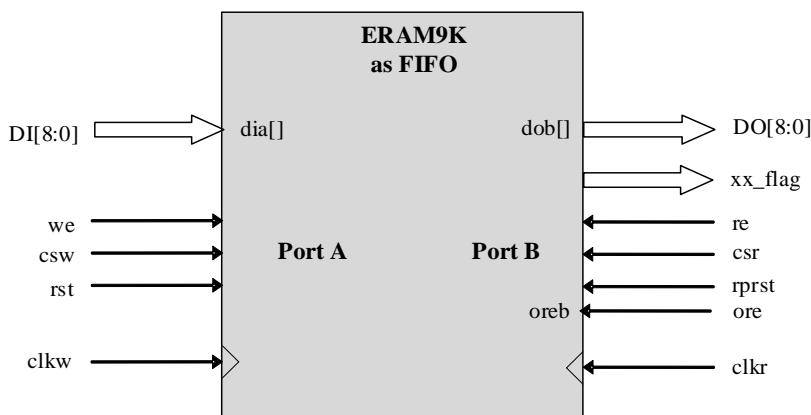


Figure 2-17 <= 9-Bit Input/ <=9-Bit Output FIFO Mode

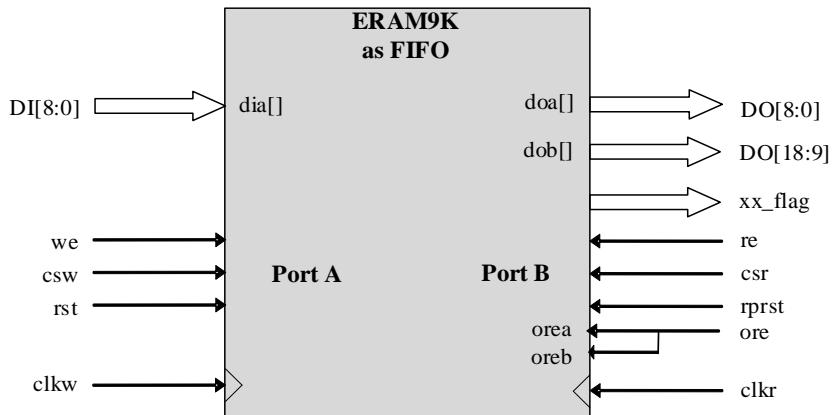


Figure 2-18 9-Bit Input/ 18-Bit Output FIFO Mode

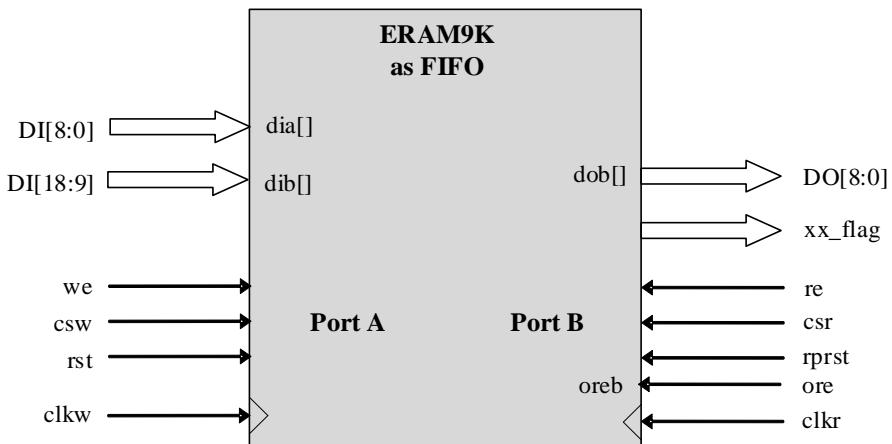


Figure 2-19 18-Bit Input/ 9-Bit Output FIFO Mode

■ Full and Empty Flag Setting

In FIFO mode, users can configure FIFO full and empty flag by using software. Empty_flag(EF), almost_empty(AE), full_flag(FF), almost_full(AF). When the counter is counted to the flag value, FF/AF/EF/AE ports output high voltage.

Table 2-11 Programmable FIFO Flag Ranges

FIFO Flag Name	Description	Range
FF	Full flag	1 to Max
AF	Almost full	1 to Full-1
AE	Almost empty	1 to Full-1
EF	Empty setting	0

■ FIFO Mode Common Configuration

The interface logic of CSW/SCR in FIFO mode is similar to that of CSA/CSB in RAM mode. In order to avoid pointer overflow when FIFO writes full or read empty, the full signal can be inverted and connect to CSW and the empty signal is inverted and connect to CSR.

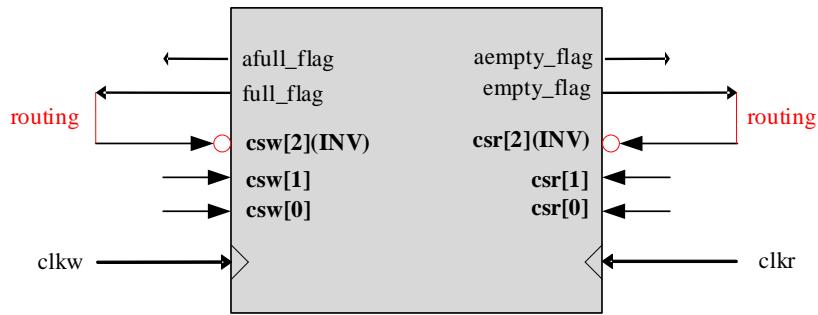


Figure 2-20 Single ERAM9K FIFO Mode Connection

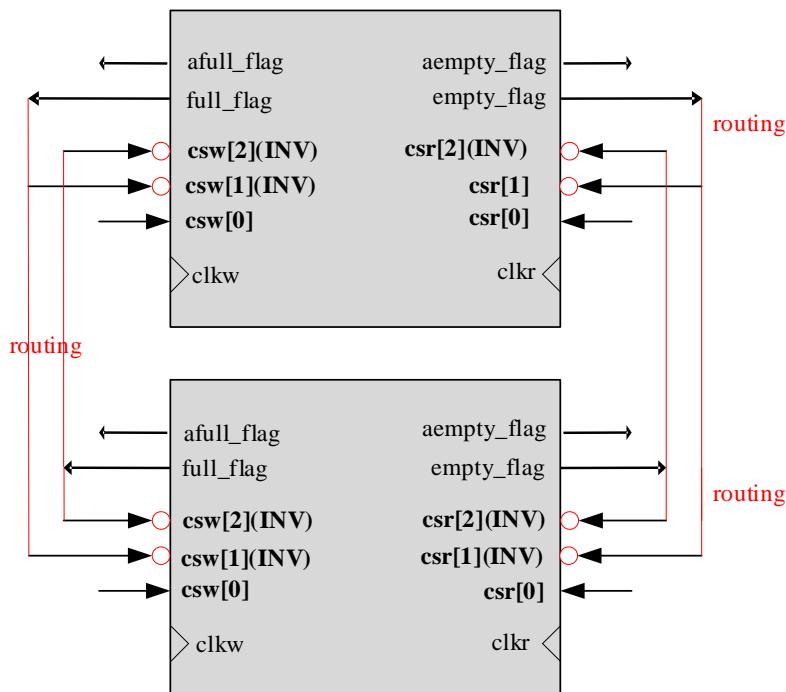


Figure 2-21 Two ERAM9Ks Cascade

2.2.6 ERAM32K

To achieve larger scale capacity, EAGLE family devices added embedded true dual-port memory block ERAM32K with capacity up to 32Kbits.

ERAM32K can implement:

- Single-Port RAM
- Dual-Port RAM

ERAM32K special features:

- 32 Kbits per block, can be configured as 2K x 16 or 4K x 8
- Port A/B clock independently

- Port A/B can configure bit-width independently, supporting 8-bit/ 16-bit widths
- Option to output latch (Support one-stage pipeline)
- 2 write operations: Normal, Write-through

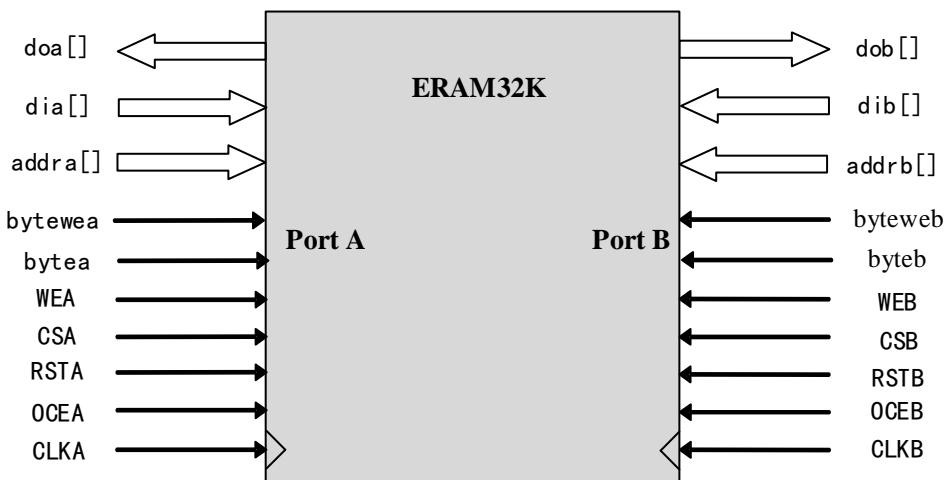


Figure 2-22 ERAM32K dual-port RAM

Table 2-2-12 ERAM32K Port Signal

Port A	Direction	Description
dia[15:0]	Input	Data input to port A, dia [7:0] is valid in 8-bit input mode.
addra[10:0]	Input	Address input to port A, 2K depth
bytewea	Input	Port A 16-bit mode, enable 8-bit write mode high active. In 8-bit mode connect 0
bytea	Input	As low bit address input in 8-bit input mode; In 16-bit mode and wbyte_ena=1, when bytea=1, high 8-bit write, when bytea=0, low 8-bit write.
doa[15:0]	Output	Data output to port A, only doa[7:0] is active in 8-bit output mode.
clka	Input	Clock input to Port A, by default rising edge is active (reversible)
rsta	Input	Data output to Port A register synchronous reset signal. By default high active (invertible).



csa	Input	Port A chipselect, by default high active (invertible)
wea	Input	Port A write/ read control, 1 refers to write, 0 refers to read.
oceaa	Input	Port A data register clock enable, by default high active (invertible). It is active when (REGMODE_A=“OUTREG”) is used.
Port B	Direction	Description
dib[15:0]	Input	Data input to port B, dib[7:0] is active in 8-bit input mode.
addrb[10:0]	Input	Address input to port B, 2K depth
wbyte_enb	Input	Port B enable 8-bit write high active in 16-bit mode in 8-bit connect 0.
byteb	Input	As lowest address input in 8-bit mode; When wbyte_enb=1 in 16-bit mode, byteb=1 selects high 8-bit write, when byteb=0 selects low 8-bit write.
dob[15:0]	Output	Data output to Port B, dob [7:0]is active in 8-bit output mode.
clkb	Output	Clock input to Port B, by default rising edge is active (invertible).
rstb	Input	Data output to Port B register synchronous reset signal. By default high valid (invertible).
csb	Input	Port B chipselect, by default high active (invertible)
web	Input	Port B write/read operation control, 0 refers to write, 1 refers to read
oceb	Input	Port B data register clock enable, by default high valid (invertible). It is valid when (REGMODE_B=“OUTREG”) is used.



2.3 Clock Resource

EAGLE family FPGA contains three clock resources. Firstly, GCLK that drive core logic, embedded memory, IOL and DSP. The second one is IOCLK that support high-speed input/output serial/parallel conversion, the third one is fast clock that support clock quickly input to IOCLK and PLL input.

2.3.1 Global Clock

The global clock of EAGLE family devices contains dedicated clock input, buffers and routing networks. Clock resources provide 16 low-latency, low-skew and interconnected global clock networks. Global network can provide unified high-performance, low-jitter, low-skew clock resource. And global clock can be used for high fan-out signal.

There is one level dynamic clock enable logic on the global clock transmission path, which can realize the dynamic clock enable without burrs that feed global clock choosing from PLL output, clock pin, internal divider, internal logic feedback. A total of 32 clock resources are sent from the four sides to the center 36:1 MUX through delay balance on the transmission path, which in turn are sent to four quadrants to feed users' logic DFF.

The whole chip is divided into four quadrants by horizontal and vertical middle lines, and each quadrant has 16 independent global clock resources.

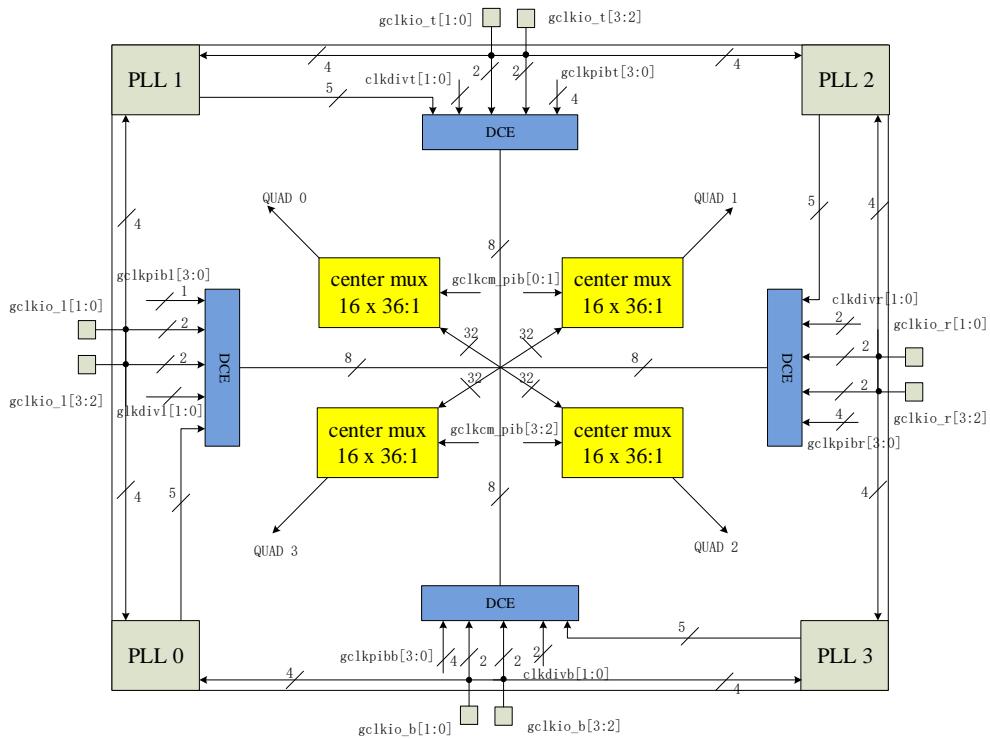


Figure 2-23 Global Clock Diagram

2.3.1.1 Dynamic Clock Enable (DCE)

DCE block allows users to dynamically control clock network using logic description. When the chosen clock is forbidden, all logic blocks fed by this clock will be static to reduce power consumption.

2.3.1.2 Clock Switching Block (CSB)

Each EAGLE device has two global clock dynamic clock switching blocks. The CSB takes all 32 global clock level 1st MUX output as input signal. It can be configured as a synchronous or asynchronous 2:1 MUX with two clock input without burrs.

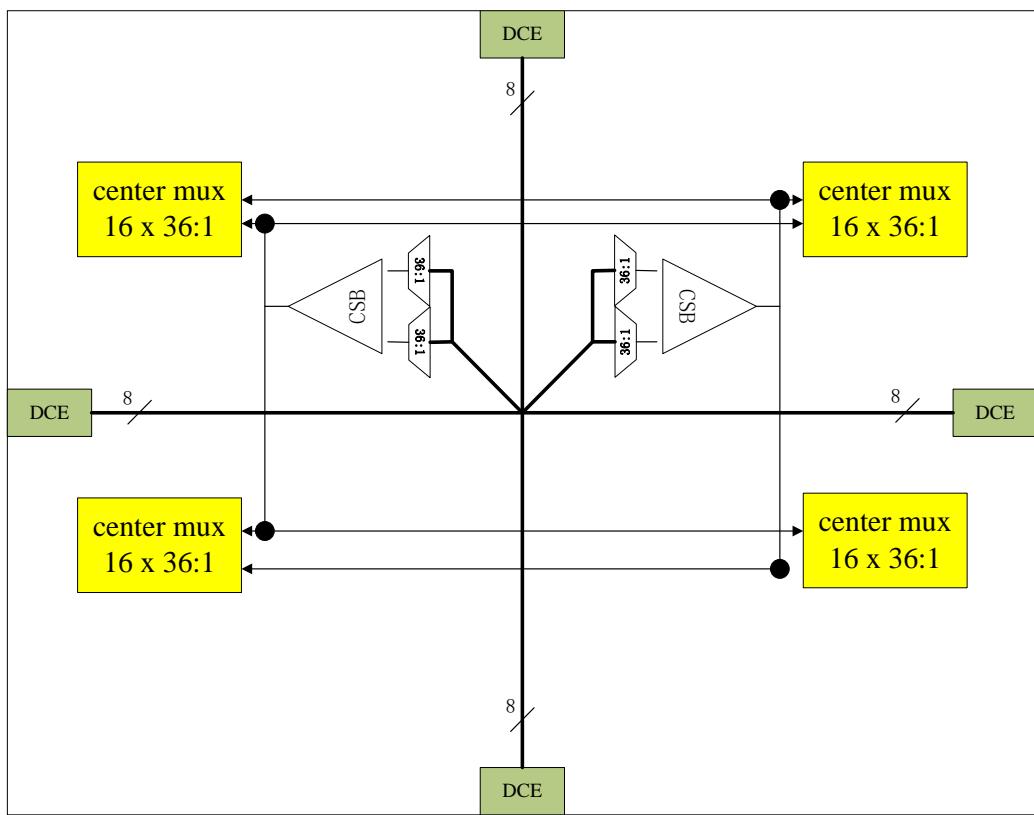


Figure 2-24 CSB Diagram

Work sequence of CSB block as shown in the following figure

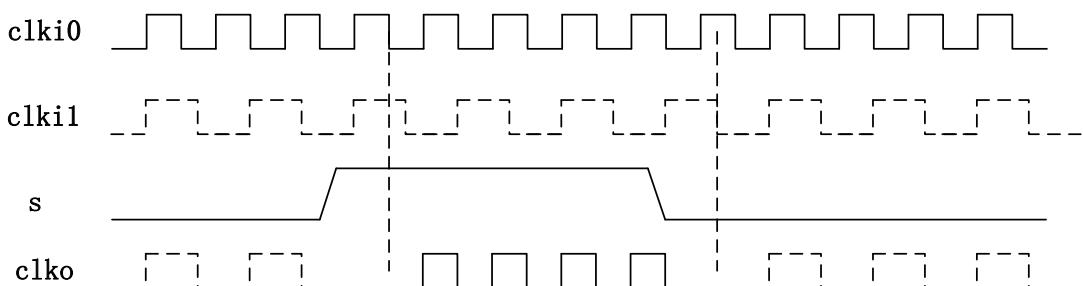


Figure 2-25 CSB Timing Sequence

Table 2-13 DCS Operation Mode

Mode	S		Description
	1	0	
BUFGMUX	clk1	clk0	Clock switch with glitch

2.3.2 Input/ Output Clock

The input/output clock (IOCLK) is a kind of clock buffer that is used in EAGLE devices. IOCLK feeds a dedicated clock network in I/O column that is independent from global clock. Thus, BUFI0 can ideally fit in synchronous data sampling (transmission/receiver/clock allocation). IOCLK can be fed by clock capable I/O at the same clock domain, also by PLL output signals. Typical I/O bank has two IOCLKs. Each IOCLK can feed one I/O clock network at the same domain or bank. IOCLK cannot feed logic resources (PLB, ERAM, etc), because IOCLK clock network can only cover the I/O column at the same bank or same clock domain.

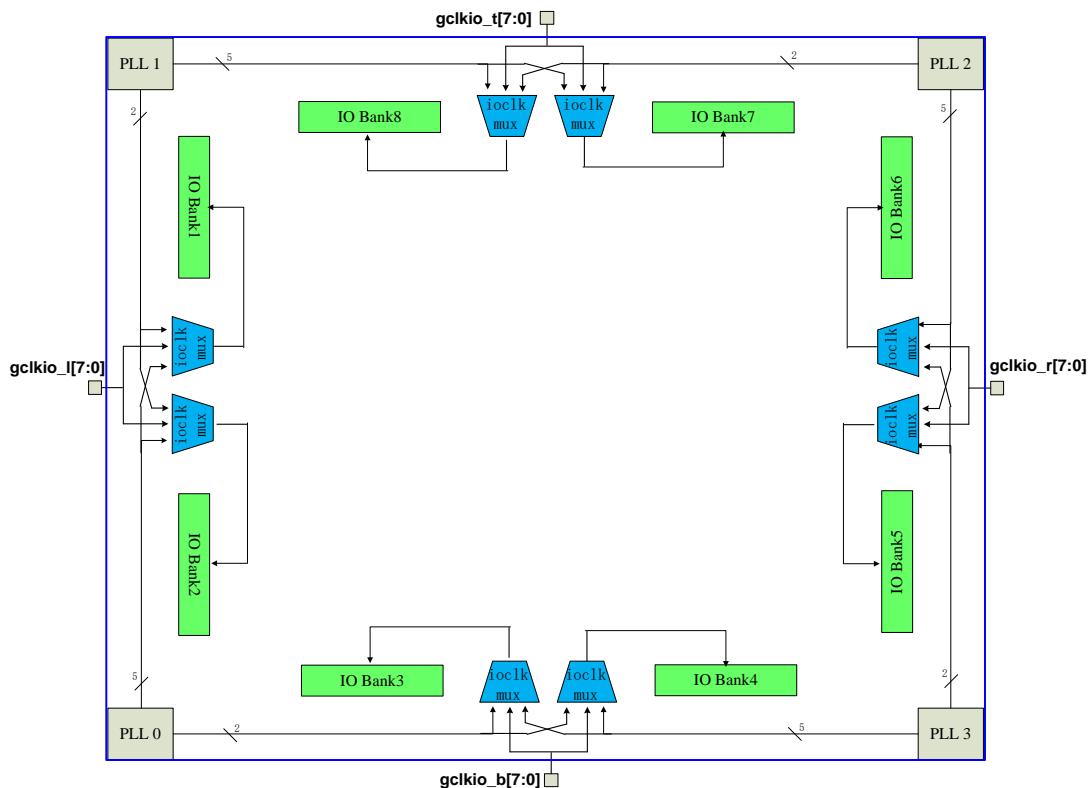


Figure 2-26 IOCLK Diagram

■ Clock Divider

There are two clock dividers in each I/O Bank of EAGLE family devices. It

divides input clock. The input comes from input/output clock at the same I/O bank. The output dividing frequencies can be either 1/2/4.

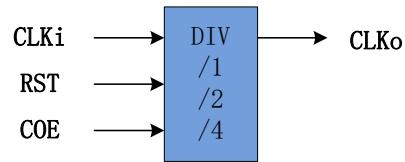


Figure 2-27 Clock Divider

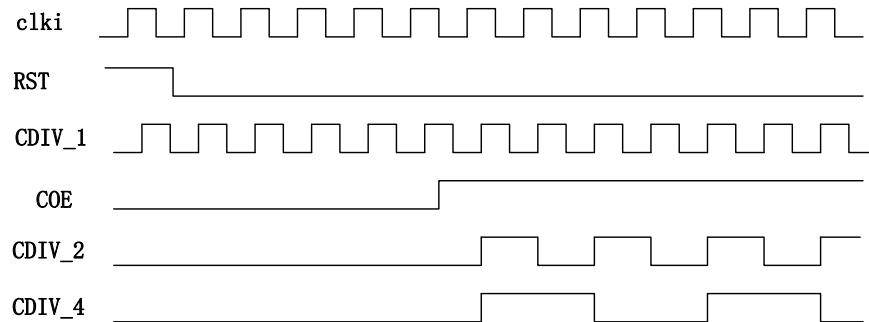


Figure 2-28 Clock Divider Timing Sequence

2.3.3 Fast Clock

Fast clock is used to implement a single clock quick routing to multiple IOCLK and PLL input applications, which enable more flexible common clock input.

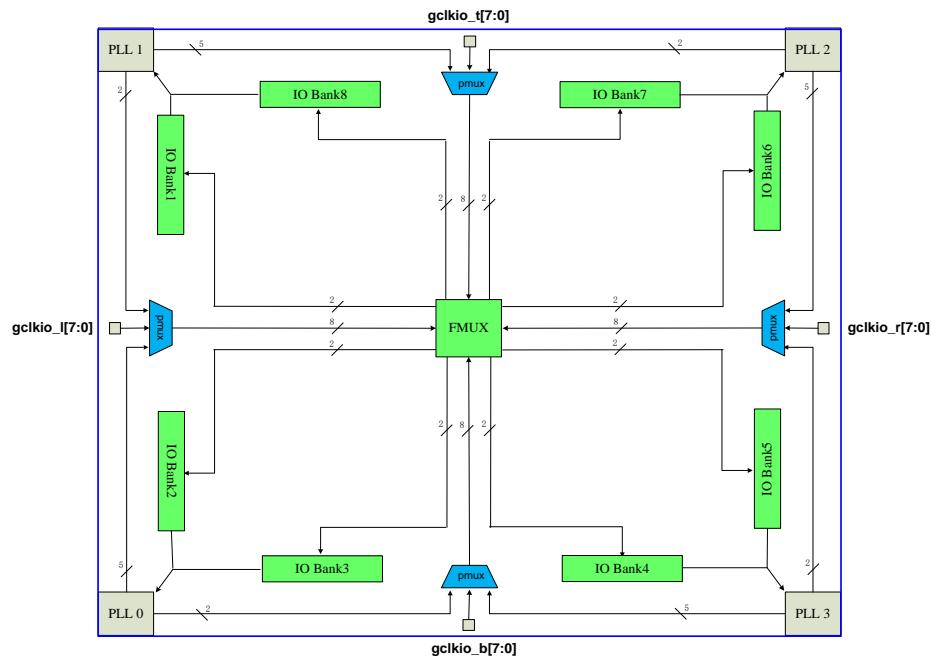


Figure 2-29 Fast Clock Architecture

2.4 Phase Locked Loop (PLL)

2.4.1 Introduction

EAGLE family FPGA has embedded four multi-functional PLLs (PLL0–PLL3), which can implement clock management function with high performance. Each PLL can implement clock divide/multiply/input and feedback clock alignment/multiphase clock output functions.

Users should pay attention to whether the PLL Lock signal is high or not, and do not reset PLL until the input signal become stable, which can ensure stable frequency and PLL output phase.

Input reference clock input for PLL: output clock network, interconnection output and internal oscillator output.

Feedback Clock input for PLL: output clock network, internal register clock node, interconnection output, PLL internal feedback clock and phase shift clock C0–C4.

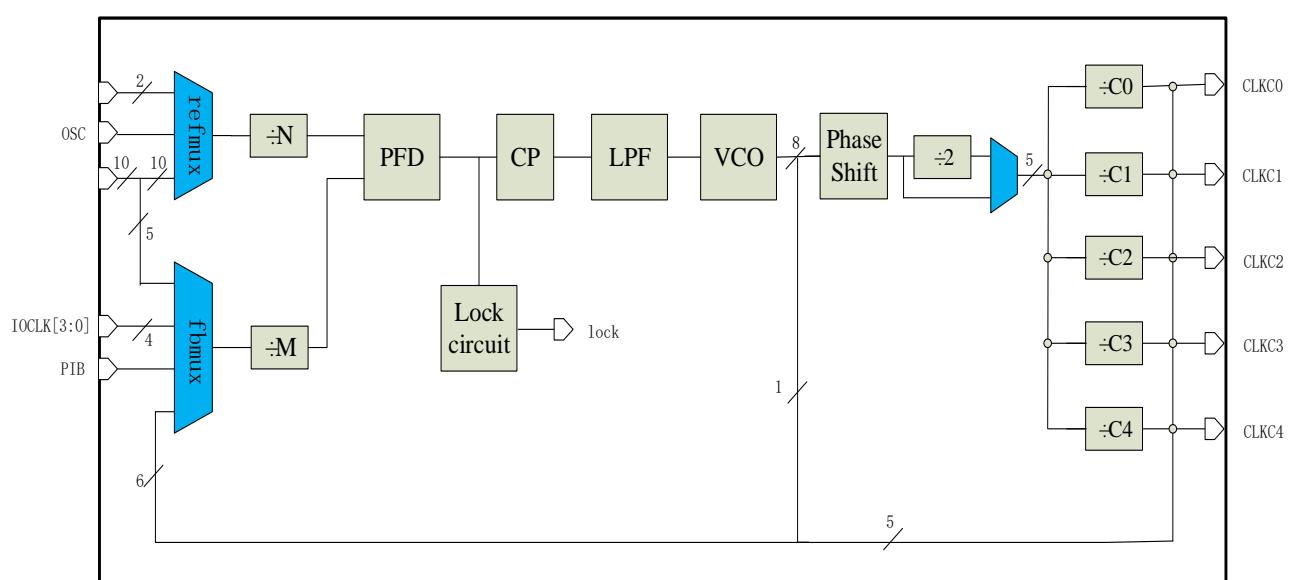


Figure 2-30 EAGLE PLL Diagram

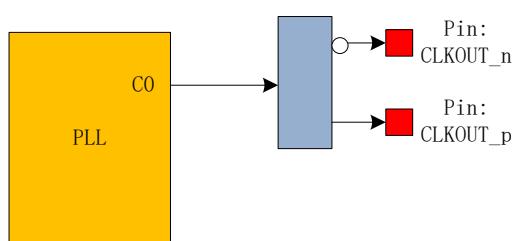


Figure 2-31 EAGLE C0 Directly Output to The Clock Output 10 pin (Differential)



Table 2-14 EAGLE PLL Features

Feature	EG4 PLL
Range of input clock frequency	10–400 Mhz
Range of output clock frequency	4–400 Mhz
Range of VCO frequency	300–1200 Mhz
Number of output ports	5 (Individual phase for each port)
Reference clock division factor (N)	1 to 128
Feedback clock division factor (M)	1 to 128
Output clock division factor (C0–4)	1 to 128
Phase shift resolution	45° (Relative to VCO)
Output Port optional phase offset (°)	0, 45, 90, 135, 180, 225, 270, 315
Users dynamically phase shift control	Support (+/- 45° phase shift per unit, relative to VCO)
Lock-out state	Lock
Dedicated clock output pin	Support

2.4.2 Dynamic Phase Shift

EAGLE family devices PLL supports dynamic phase shift. EAGLE PLL control attribute is static configuration. Static configuration is implemented by generating bitstream from the software, which is unchangeable after power-on download.

Static configuration parameters:

- Reference/feedback clock input/output selection
- Reference clock division factor (N)
- Feedback clock division factor (M)

- Output clock division factor (C0-C4)

Users can dynamically modify independent output phase by this feature. Changing output clock phase can be realized by increasing or decreasing the given counter in real time. Each phase shift step is 1/8 VCO period. The following table lists the control signals for dynamic phase shift.

Table 2-15 Dynamic Phase Shift Control Signal

Signal	Description	Source	Signal Destination
PSCLKSEL[2:0]	Select clock signal for dynamic phase shift, select one channel from C0-C4 simultaneously	PIB or IO	PLL reconfiguration circuit
PSDOWN	Dynamic phase shift direction select 1=UP, 0= DOWN. Sampling on the rising edge of PSCLK	PIB or IO	PLL reconfiguration circuit
PSSTEP	PSSTEP=1, enable dynamic phase shift	PIB or IO	PLL reconfiguration circuit
PSCLK	Dynamic phase shift clock	GCLK or IO	PLL reconfiguration circuit
PSDONE	PSDONE=1, it indicates phase adjustment completion. Sampling on the rising edge of PSCLK.	PLL reconfiguration circuit	PIB or IO

For dynamic phase shift, you can only adjust one channel output phase, PIB interface PSCLKSEL[2:0] to select one channel of C[4:0], as shown in the following table.

Table 2-16 Dynamic Phase Shift Output Select

PSCLKSEL[2:0]	PLL Output Select
000 (default)	C[0]
001	C[1]
010	C[2]
011	C[3]
100	C[4]

To perform one dynamic phase shift step, as the following steps:

- 1) Set PSDOWN and PSCLKSEL as required
- 2) Turn on phase adjustment, PSSTEP phase adjustment at least require four PSCLK cycles. Each PSSTEP pulse allows one phase shift
- 3) Turn off phase adjustment
- 4) Wait for PSDONE to go high
- 5) Repeat steps 1 through 4 as many times as required to perform multiple phase shifts.

PSCLKSEL[2:0], PSSTEP, PSDOWN signals are synchronous to PSCLK, and then sent to PLL.

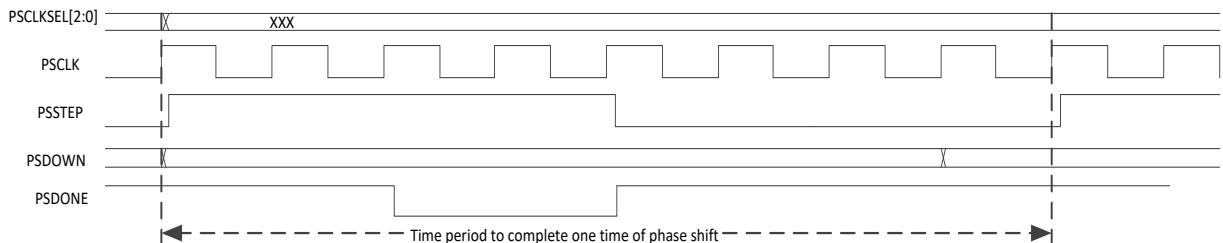


Figure 2-32 PLL Dynamic Phase Shift

The PSSTEP signal is latched on the rising edge of PSCLK, as above figure shown. PSSTEP must be triggered for one time within four PSCLK cycles. PSDONE signal turn to low and last for about 3 VCO cycles. PSDONE turn high indicates that phase shift completed. The next output clock cycle after PSDONE signal being pulled high, dynamic phase shift go effect.

Note: The adjusted clock may produce glitch during the dynamic shift.

2.4.3 Clock Feedback Mode

Each PLL of EAGLE family devices support four feedback modes. Each mode allows clock multiplication/ division and phase shifting.

a) Source-Synchronous Mode

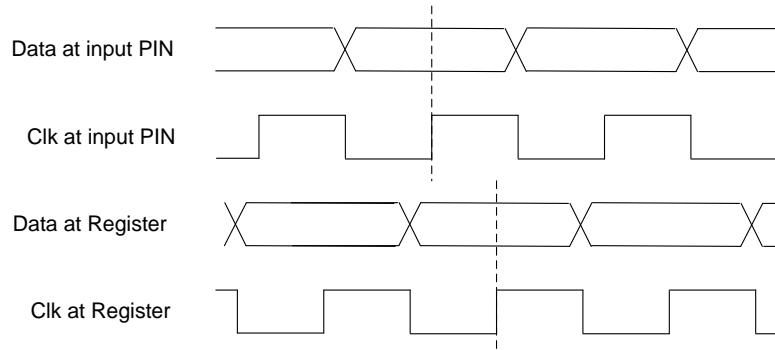


Figure 2-33 Source Synchronous Mode

As figure 2-33 shows that source synchronous mode adjusts clock phase that ensure delay from data at input PIN to IOB register is equal to that of from clock at input PIN to IOB register. (when data and clock input port mode are same).

b) No Compensation Mode

In this mode, the PLL does not compensate for any clock networks. This mode provides better jitter performance because PLL adopts internal feedback.

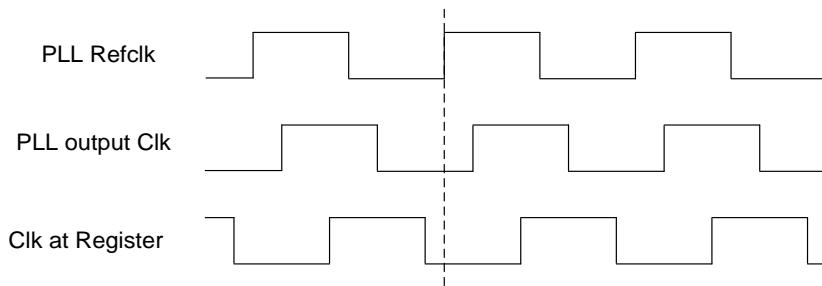


Figure 2-34 No Compensation Mode

c) Normal Mode

In this mode, the PLL compensates for the delay introduced by the GCLK network, which ensure the clock at register being phase-aligned to the PLL Refclk.

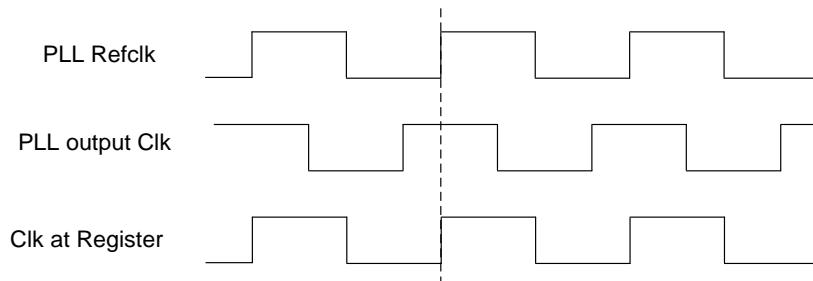


Figure 2-35 Normal Mode

d) Zero-Buffer Mode

In this mode, PLL output clock is phase-aligned with the PLL Refclk input.

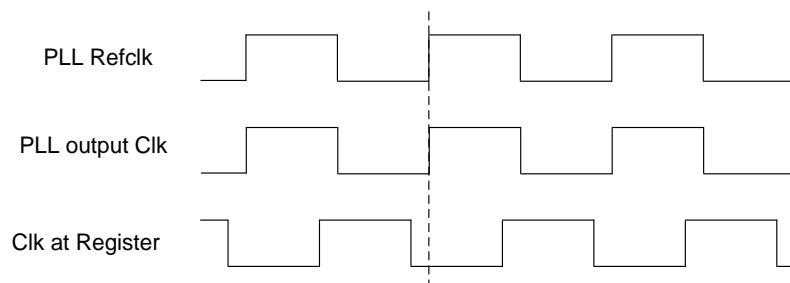


Figure 2-36 Zero-buffer Mode

2.5 Digital Signal Process (DSP)

With the combination of on-chip resources and external interfaces in EAGLE family devices, you can build DSP systems with high performance, low system cost, and low power consumption. You can use EAGLE devices on its own or as a DSP co-processor to improve price-to-performance ratios of DSP system.

2.5.1 Architecture

The figure 2-37 shows that the embedded multiplier column is highly correlated with adjacent PLBs. The embedded multiplier is either configured as one 18x18 multiplier, or two 9x9 multipliers. Each embedded multiplier is consisted of the following elements:

- Multiplier stage
- Input and Output Registers
- Input and Output Interfaces

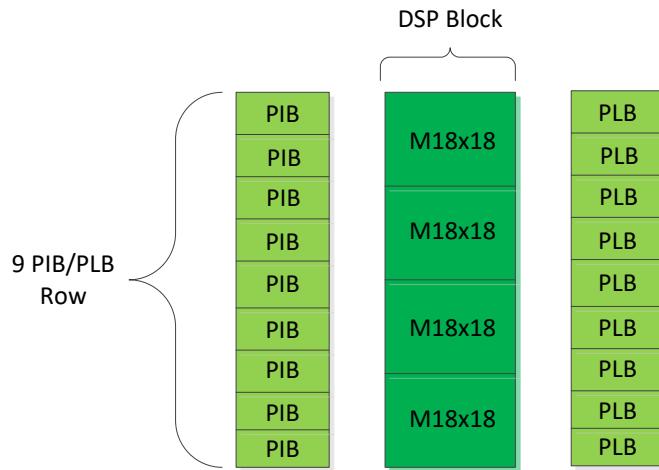


Figure 2-37 Embedded Multipliers Arranged in Columns Adjacent to PLB

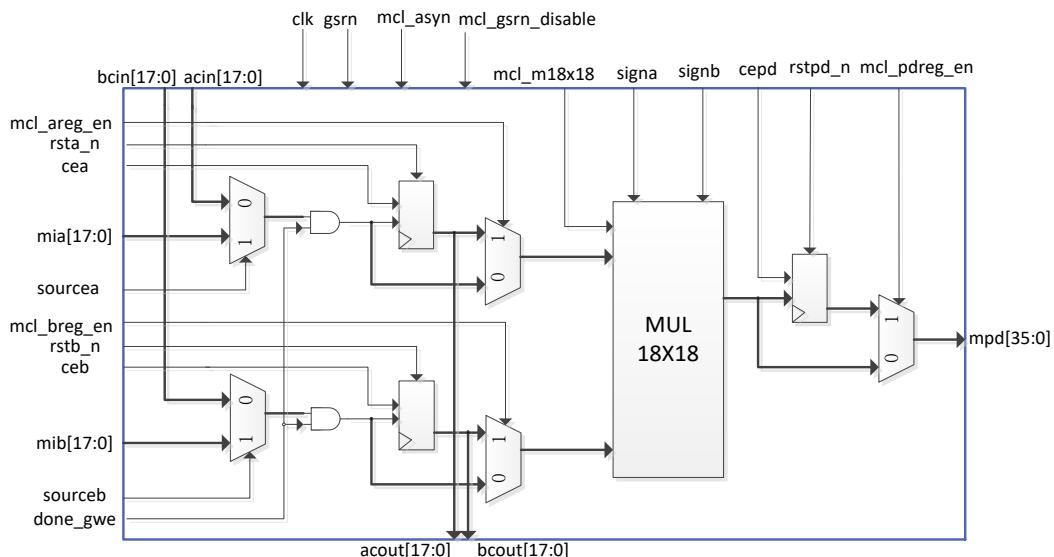


Figure 2-38 Multiplier Module Architecture

a) Input Register

Depending on multiplier mode, you can connect input signal of each multiplier to input register or directly connect to internal multiplier in 9bit or 18bit form. Each multiplier input can be set as using input register or not independently. For example, you can connect the multiplier mia signal to a register and connect the mib signal directly to the multiplier.

The following control signals can be used for every input register of embedded multiplier:

- Clock
- Clock Enable

■ Synchronous/Asynchronous Clear

All input and output registers in a single embedded multiplier are fed by the same clock, clock enable and asynchronous clear signal, which can be configured independently.

b) Multiplier Stage

The multiplier stage of an embedded multiplier blocks supports 9x9 or 18x18 multipliers and other multipliers in between these configurations. Depending on the data width or operational mode of the multiplier, a single embedded multiplier can perform one or two multiplications in parallel.

Each multiplier operand is a unique signed or unsigned number. Two signals, signa and signb, control an input of a multiplier and determine if the value is signed or unsigned. If the signa signal is high, the mia operand is a signed number. If the signa signal is low, the signa operand is an unsigned number.

The following table lists the sign of the multiplication results for the various operand sign representations. The results of the multiplication are signed if any one of the operands is a signed value.

Table 2-17 Multiplier Sign Representations

mia		mib		Result
Signa	Logic Value	Signb	Logic Value	
Unsigned	0	Unsigned	0	Unsigned
Unsigned	0	Signed	1	Signed
Signed	1	Unsigned	0	Signed
Signed	1	Signed	1	Signed

Each embedded multiplier block only has one signa signal and signb signal for the representation of controlling module input data. If the embedded multiplier has two 9x9 multipliers, the mia and mib would share the same signa signal and signb signal. You can dynamically change the signa and signb signals to modify the sign representation of the input operands at the run time. You can send the signa and signb through a dedicated input register. The multiplier offers full precision, regardless of the sign representation.

c) Output Register

You can register the embedded multiplier output using output registers in



either 18 bit or 36 bit sections based on multiplier mode. The following control signals are available for each output registers in the embedded multiplier:

- Clock
- Clock Enable
- Synchronous/ Asynchronous clear

All input and output registers in a single embedded multiplier are fed by the same clock, clock enable and asynchronous clear signals, which can be configured independently.

The following table lists the description of DSP port:

Table 2-18 Description of Multiplier Ports

Name	Direction	Width	Description
mia	Input	18	DSP operand input from PIB. With register input mode
acin	Input	18	Cascading data input connect to acout port from pre-level DSP. With register input mode
acout	Output	18	Cascading data output in acin port that connect to next-level DSP
mib	Input	18	DSP operand input from PIB. With register input mode.
bcin	Input	18	Cascading data input connect to bcout port from pre-level DSP. With register input mode.
bcout	Output	18	Cascading data output in bcin port that connect to next-level DSP.
cea	Input	1	Clock enable signal for input register. When cea in high level, amux output to register.
ceb	Input	1	Clock enable signal for input register. When ceb in high level, bmux output to register
cepd	Input	1	Clock enable signal for output register. When cepd in high level, DSP data output to register.
clk	Input	1	Clk is the input clock for DSP, which both apply to all internal registers
rsta_n	Input	1	Reset signal to input register. When rsta_n in low



			level, register output is “0”.
rstb_n	Input	1	Reset signal to input register. When rstb_n output in low level, register output is “0”.
rstpd_n	Input	1	Reset signal to output register. When rstpd_n is in low level, register output is “0”
sourcea	Input	1	First level data selector control signal. When sourcea in high level, MUX output is “a” ; when source in low level, MUX output is acin,
sourceb	Input	1	First level data selector control signal. When sourceb in high level, MUX output is “b” ; When sourceb in low level, MUX output is bcin
mpd	Output	36	DSP multiplication data output

2.5.2 Operational Modes

You can use either of two operational modes, depending on the application needs:

- One 18x18 multiplier
- Up to two 9x9 independent multipliers

You can also use embedded multipliers of the EAGLE devices to implement multiplier adder and multiplier accumulator function. Parts of multiplier function is implemented by using embedded multiplier. The adder or accumulator are realized in logic elements.

a) 18-Bit Multipliers

You can configure each embedded multiplier to support a single 18x18 multiplier for input widths of 10 to 18bits. The following figure shows the configured embedded multiplier to support an 18-bit multiplier

All 18-bit multiplier inputs and results are independently sent to registers. The multiplier inputs can accept signed integers, unsigned integers, or a combination of both. Also you can dynamically change the signa and signb and send these signals through dedicated input registers.

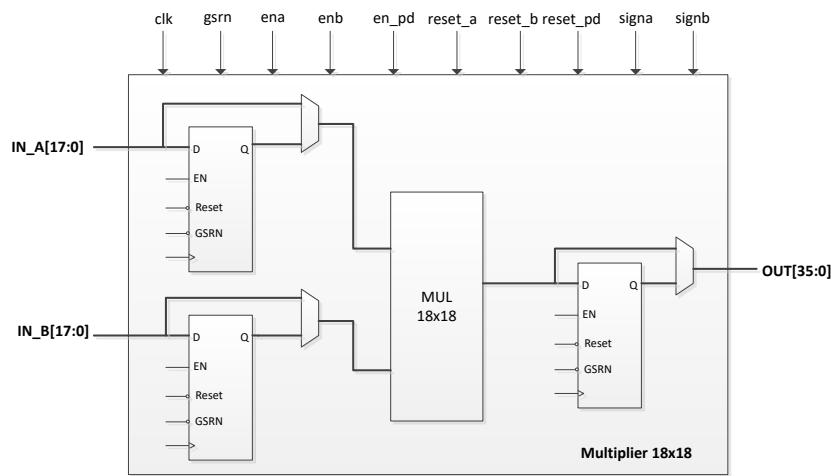


Figure 2-39 18-bit multiplier mode

b) 9-Bit Multipliers

You can configure each embedded multiplier to support two 9x9 independent multipliers for input widths of up to 9 bits. The following figure shows the configured embedded multiplier to support two 9-bit multipliers

All 9-bit multiplier inputs and results are independently sent to registers. The multiplier inputs can accept signed integers, unsigned integers, or a combination of both. Each embedded multiplier block has only one signa and signb signal. Therefore, the mia input data of both multipliers share the same signal representation. And the mib input data of both multipliers share the same signal representation.

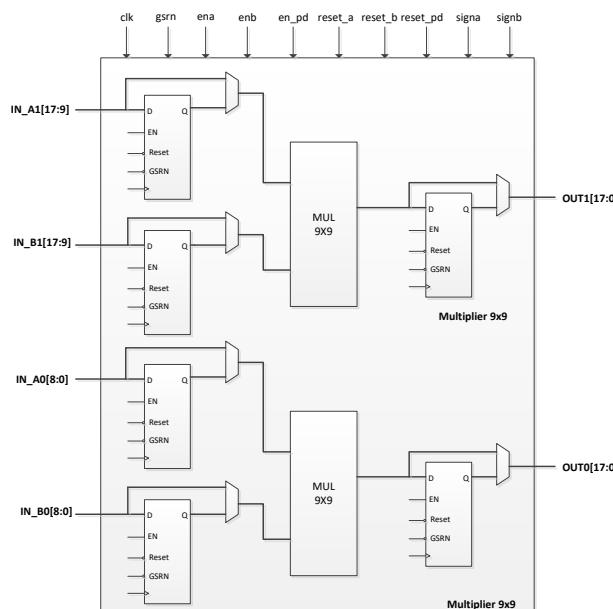


Figure 2-40 9-Bit Multiplier Mode

2.6 Input/ Output Logic (IOL)

The IOL of EAGLE devices support multiple modes. This chapter mainly describes the configuration of IOL resources for various modes.

2.6.1 Input Register Logic

The input register in IOL is used to condition high-speed interface before they are passed to the logic core. Input registers all contain programmable delay elements for data sampling. It also enhanced the support for general double data rate (GDDR).

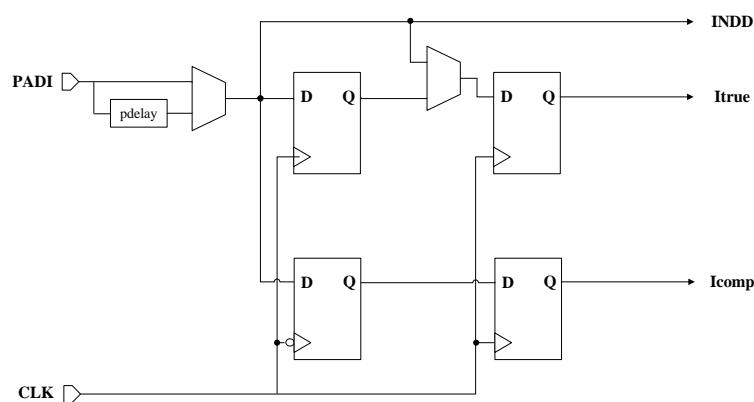


Figure 2-41 Input Register

a) Normal Input Mode

The following figure shows the IOL logic in normal mode, signals directly entered into FPGA internal logic in this mode.

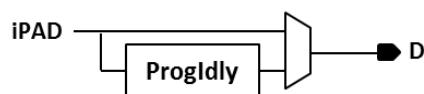


Figure 2-42 Normal Mode

b) SDR Input Mode

As the following figure shown, SDR mode adopts IOL register, which can effectively improve IOL timing performance compared to normal mode.

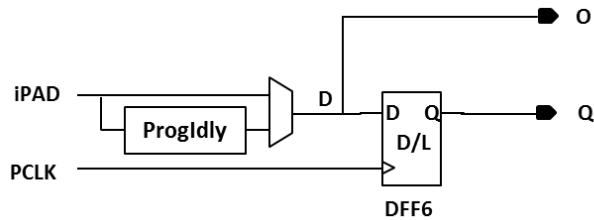


Figure 2-43 SDR Input Mode

c) DDR Input Mode

EAGLE device 10L has dedicated registers to support iDDRx1 and iDDRx2

■ iDDRx1 Same Edge Input Mode

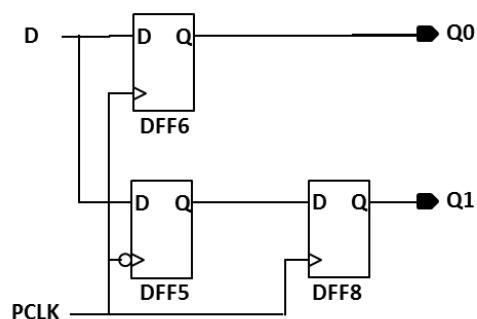


Figure 2-44 iDDR same edge input mode

In iDDRx1 same edge mode, DFF5 and DFF6 sample input data on the falling and rising edges of the clock, DFF8 synchronizes Q1 data to the rising edge of clock. As Q1 passing through DFF8, it is one clock period later than Q0. The timing diagram as following figure shown.

D	A0	A1	B0	B1	C0	C1	D0	D1	E0
PCLK	XX								
Q0	XX	A0	B0	C0	D0	XX	XX	XX	XX
Q1	XX	XX	A1	B1	C1	XX	XX	XX	XX

Figure 2-45 iDDR Same Edge Input Mode

■ iDDRx1 Same Edge Pipelined Input Mode

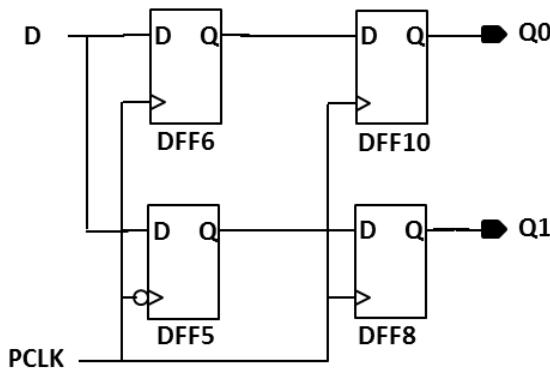


Figure 2-46 iDDRx1 Same Edge Pipelined Input Mode

In iDDRx1 Same edge mode, Q1 is one clock period later than Q0. Introducing DFF10 to compensate for the delay, as the above figure shown. The timing diagram as shown in the following figure.

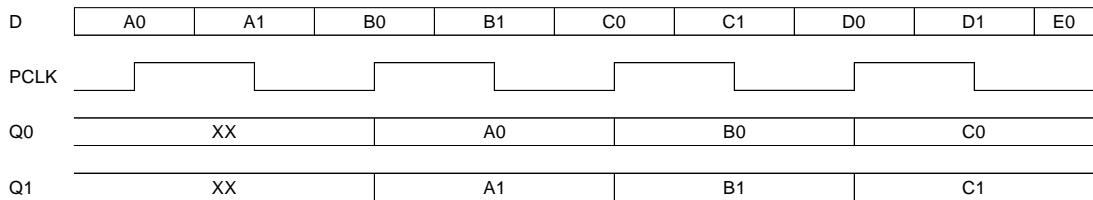


Figure 2-47 iDDR Same Edge Pipelined Input Mode

■ iDDRx2 Input Mode

In this mode, the higher IO speed is available. The internal logic speed ratio of PAD and FPGA is 4:1. The first stage DFF sampling is triggered by SCLK, realizing high-speed data sampling and 1:2 separations. The second stage of DFF separation is triggered by PCLK of FPGA system, realizing same frequency between data and internal logic. The speed of PCLK is half of that SCLK.

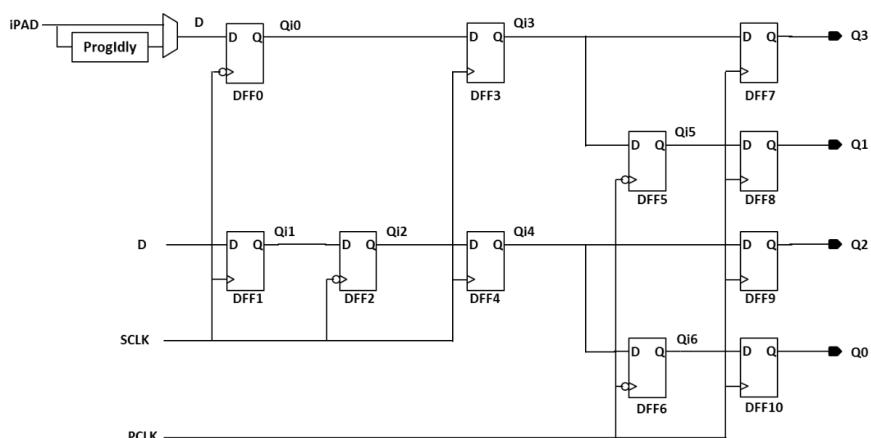


Figure 2-48 iDDRx2 Input Mode

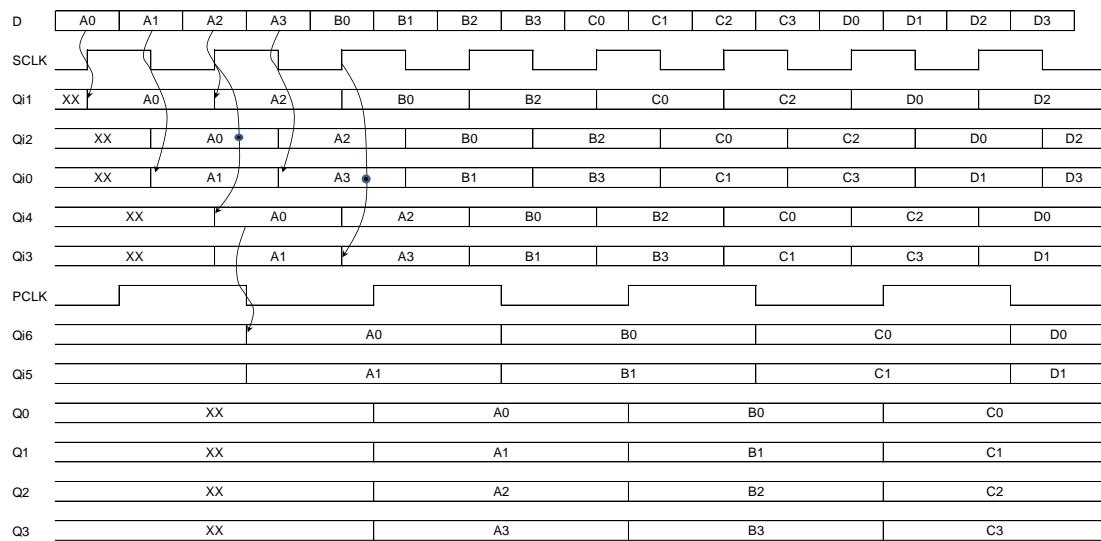


Figure 2-49 iDDRx2 Input Mode Timing

■ Input Delay Unit

Each IOL logic unit contains a programmable input delay unit supporting 32-level adjustment with the maximum 3.8ns delay. Supports static control delay.

2.6.2 Output Register

The output register of IOL is used to process timing from internal core logic to high-speed I/O interface. The following figure shows the output register.

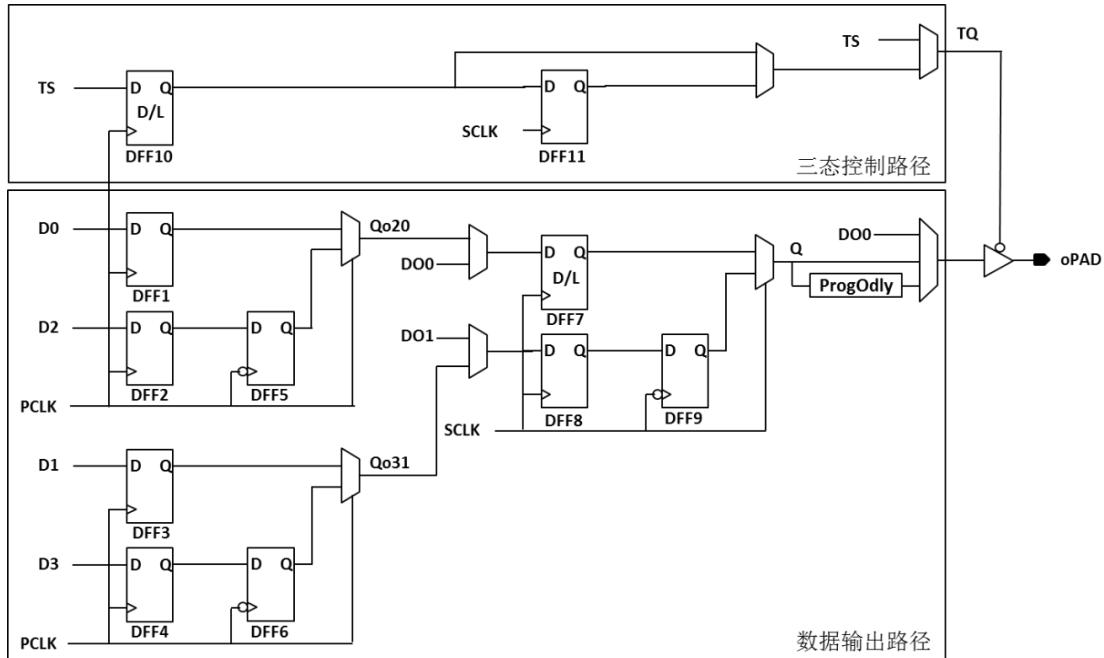


Figure 2-50 Output Register

a) Normal Output Mode

The IO logic in Normal mode as following figure shown. Signals are directly sent from FPGA internal logic to PAD.

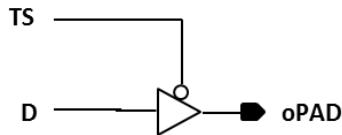


Figure 2-51 Normal Output Mode

b) SDR Output Mode

SDR Mode adopts IOL Register, which can effectively improve IO timing performance compared to Normal Mode.

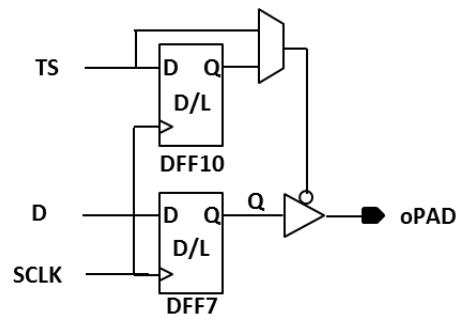


Figure 2-52 SDR Output Mode

c) DDR Output Mode

EAGLE device IOL has dedicated registers to support oDDRx1 and oDDRx2 modes

■ oDDRx1 Output Mode

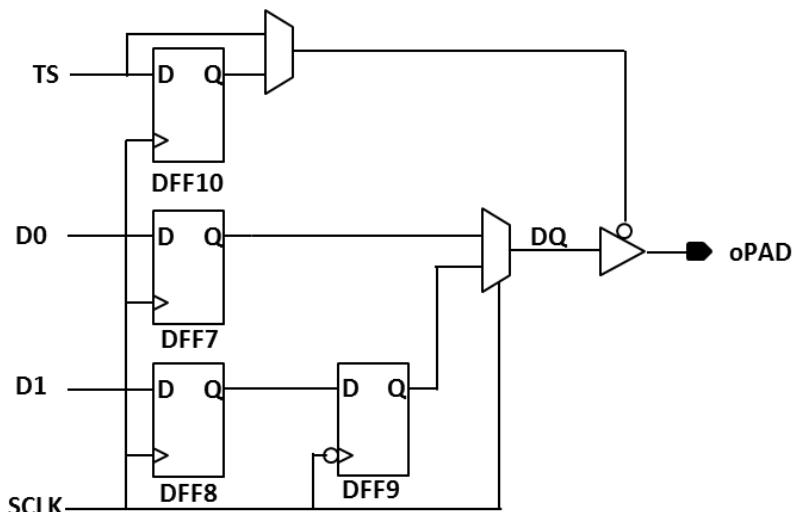


Figure 2-53 oDDRx1 Output Mode

In oDDR_{x1} Mode, data D00 and D01 are sampled by SCLK at the same edge to DFF7 and DFF8, and be sent to oPAD along the rising edge and falling edge, the timing diagram as shown in the following figure.

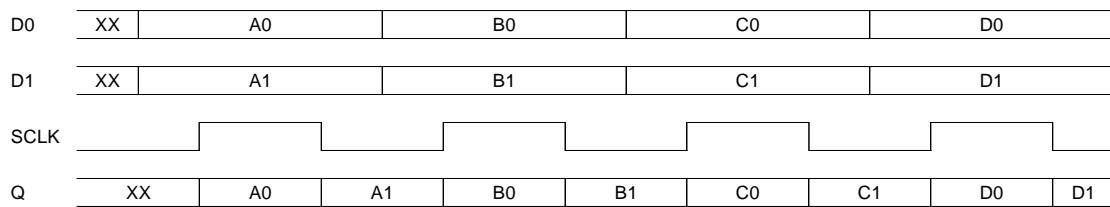


Figure 2-54 oDDR Output Mode

■ oDDR_{x2} Output Mode

In oDDR_{x2} Mode, the higher 10 speed is available. The internal logic speed ratio of PAD and FPGA is 4:1. The first stage of DFF is triggered by PCLK of FPGA system, realizing data sampling and 2:1 switch from parallel to serial. The second stage of DFF is triggered by high-speed SCLK, realizing data high-speed serial output. The speed of PCLK is half of that SCLK.

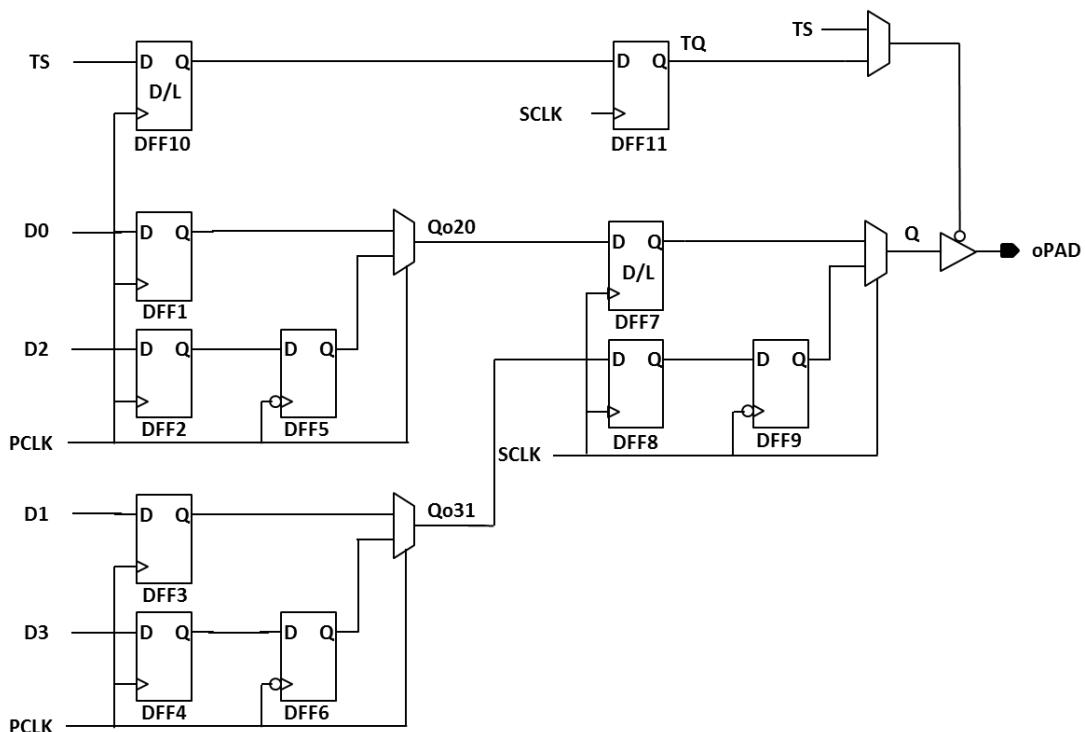


Figure 2-55 oDDR_{x2} Output Mode

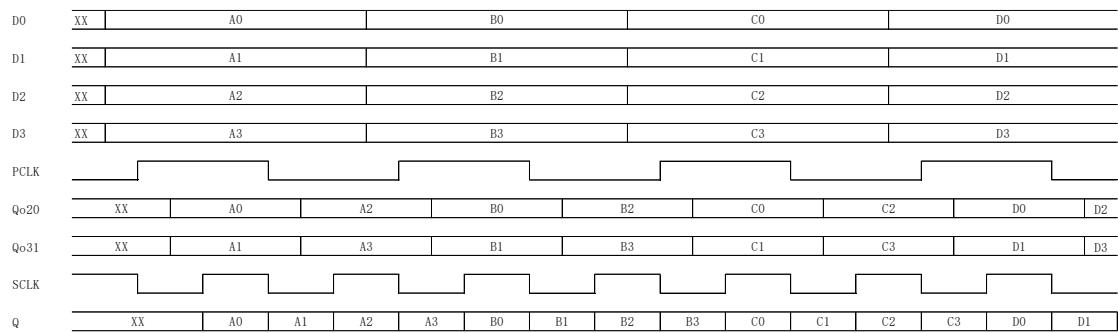


Figure 2–56 oDDRx2 Output Mode Timing Sequence

■ oDDRx2L Output Mode

Compared with oDDRx2, oDDRx2L Mode adopts the two division of internal SCLK as PCLK, saving one CLK. Data output is one SCLK clock period later than oDDRx2 mode.

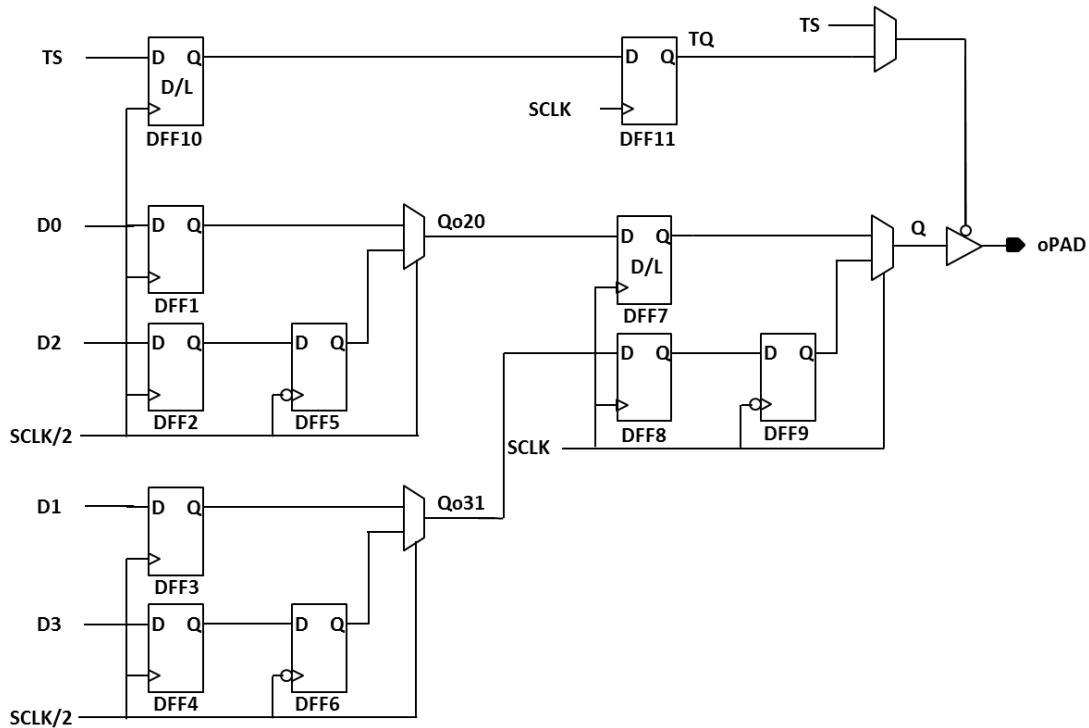


Figure 2–57 oDDRx2L Output Mode

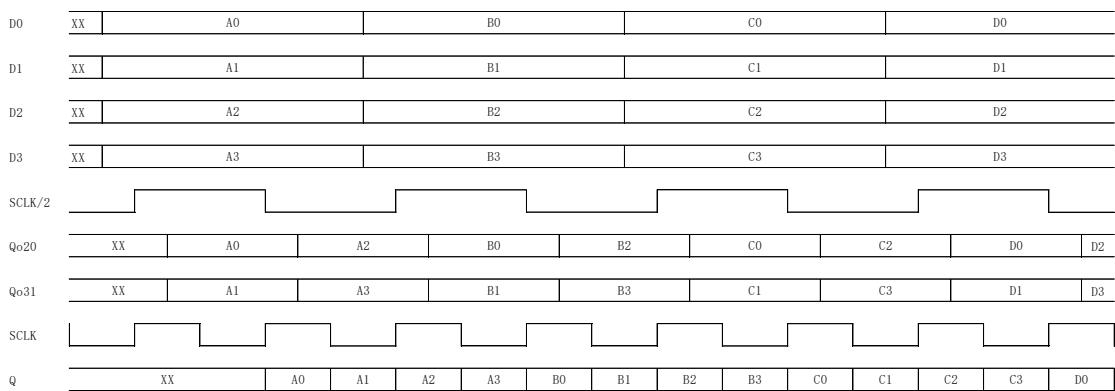


Figure 2-58 oDDRx2L Output Mode Timing Sequence

d) Output Delay Unit

Each IOU Logic Unit contains a programmable output delay unit supporting four-level adjustment with a delay of 100ps of each level. It supports static control delay.

2.7 Input/ Output Buffer (IOB)

2.7.1 Introduction to IOB

EAGLE family devices contain programmable I/O driver and receiver with high-performance that support various standard interfaces. The powerful function set contains programmable control on output strength and slew rate.

Each IOB contains input, output and tri-state drivers, which are configured according to various I/O standard. Differential I/O use two IOB at the same block.

- Single-ended I/O standard (LVCMOS, LVTTL, PCI)
- Differential I/O standard (LVDS, LVPECL)

IOB also supports these following configurations:

- Output drive strength control
- Output Slew Rate control
- Weak Pull-up/Pull-down resistor selection configuration
- PCI Clamp Enable
- Bus Hold Enable

As the following figure shows the basic IOB and its internal logic connect

to device pad.

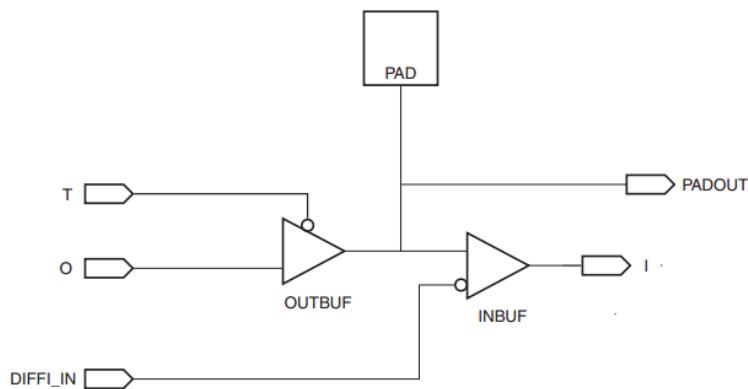


Figure 2-59 Basic IOB

Each IOB is directly connected to IOL forming input/output logic pairs, which contains input and output logic resource that are used to control tri-state of IOB and data.

2.7.2 High-speed LVDS Interface

EAGLE family devices supported differential standards as shown in the following table:

Table 2-19 EAGLE Supported Differential Standards

Differential standards	I/O Location	Receive		Transmit	
		Support	Internal Resistor	Support	External Resistor
LVDS	Left/Right	Yes	No	Yes	No
	Up/Bottom/Left/Right	Yes	Yes	Yes	3R
LVPECL	Left/Right	Yes	No	—	—
	Up/Bottom/Left/Right	Yes	Yes	Yes	3R

True LVDS and Emulated LVDS can be used as LVDS25 standard input, the maximum input frequency is 400MHz (800Mbps)

As output, True LVDS output adopts LVDS25 voltage standard without external resistor. As shown in the figure 2-60, the maximum output frequency is 400MHz (800Mbps).

As output, Emulated LVDS output adopts LVDS25E standard with the maximum

output frequency of 166MHz. It is necessary for you to connect an external 3R resistors network to fade voltage amplitude meeting LVDS standard, as figure 2-61 shown. You can modify resistor network to reduce power consumption or change noise-margin.

The following table lists the recommended resistance and signal amplitude of Emulated LVDS.

Table 2-20 Emulated LVDS recommended Resistance Value

Resistance (Ω)		Signal Amplitude (mV)	
R_s	R_p	LVDSE25	LVDSE33
300	118	195	256
210	127	270	355
150	140	365	483
115	160	460	610

Note 1: Value listed in Table 2-19 set as 8mA based on drive strength, the 100 Ω terminal resistor for receiver can be either on-chip resistor or off-chip. When the signal amplitude of receiving end greater than 500mv, you must connect an off-chip resistor. Chip internal resistance is 20 Ω .

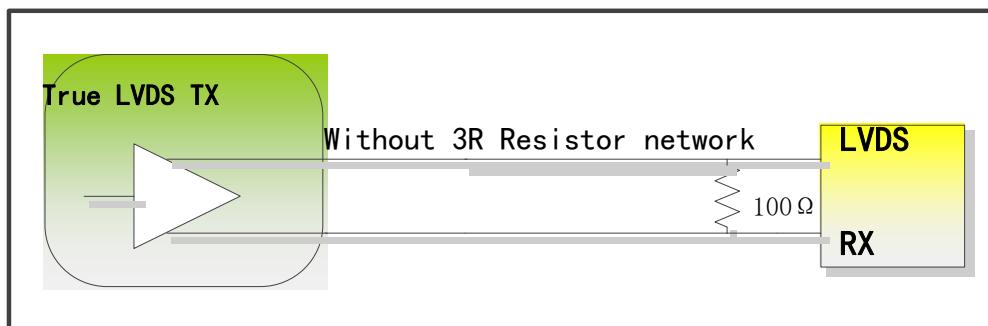


Figure 2-60 True LVDS Output

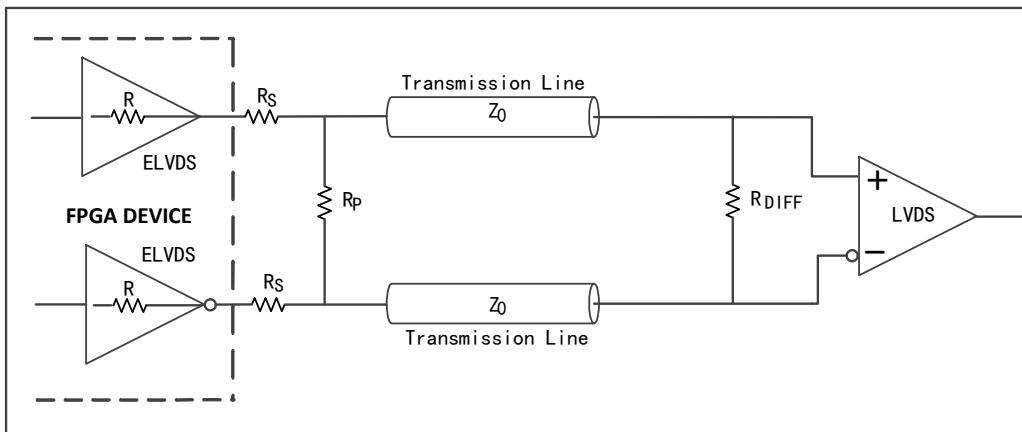


Figure 2-61 Emulated LVDS Output 3R Resistor network

2.7.3 LVPEL

EAGLE family FPGA support LVPECL input. When receiving LVPECL input signal, an external bias circuit is required to adjust common-mode voltage of differential signals that ensure LVDS with normal functionality. Different V_{CCIO} voltage corresponds to different bias resistance. The LVPECL recommended AC coupling circuit as shown in the figure 2-62. Normally, the LVPECL external devices send a greater differential signal, which needed to be faded at board level. The R_{series} is used to adjust signal amplitude at receiving side. You can choice the resistor based on LVPECL signal amplitude at sending end, $30\sim50\Omega$ by recommendation. R is DC bias resistor; $140\sim150\Omega$ by recommendation. R_{diff} is termination resistor, you can choose internal 100Ω or board-level 100Ω resistor. Figure 2-62 shows the configuration of resistance when LVPECL as input.

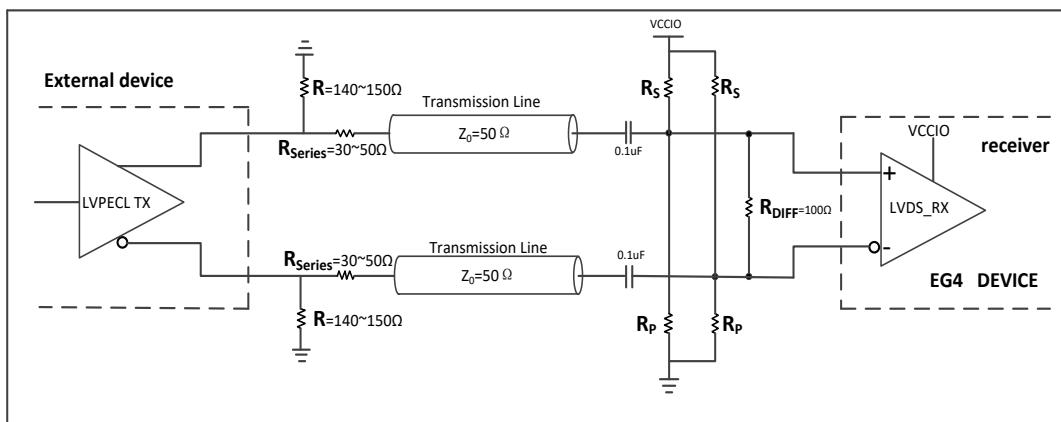


Figure 2-62 LVPECL Recommended AC Coupling Circuit

Table 2-21 LVPECL Recommended Resistance

V_{CCIO} (V)	Resistance (Ω)	
	R_s	R_p
3.3	6.5k	4.1k
2.5	5k	5k
1.8	4.5k	9k

For EAGLE family FPGA, I/O only support LVPECL_E output. When LVPECL_E set as output, it requires an external 3R resistors network to fade voltage amplitude meeting differential standard. Figure 2-63 indicates LVPECL_E output 3R resistors network. Table 2-22 lists LVPECL_E recommended resistance and signal amplitude.

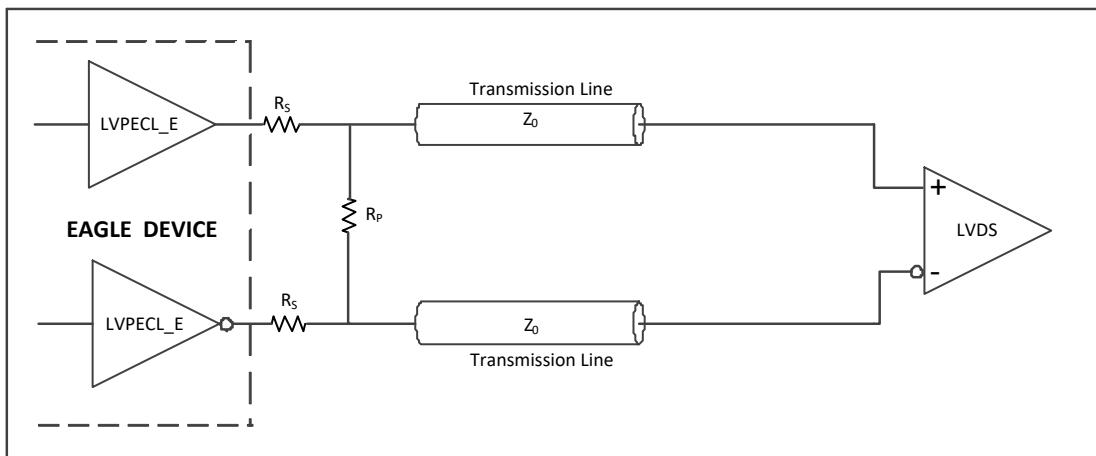


Figure 2-63 LVPECL_E Output 3R Resistance Network

Table 2-22 LVPECL_E Recommended Resistance

Resistance (Ω)		Signal Amplitude (mv) $ V_{op}-V_{on} $
R_s	R_p	LVPECL_E
93	196	800
115	160	460

Note1: Table 2-21 set as LVCMS33 16mA based on drive strengthen, receiver equips with 100Ω external termination resistor.

2.7.4 I/O Bank

EAGLE family devices have eight I/O banks: two users I/O banks per side. Bank 1 locates below logic configuration, containing dedicated/ shared configuration interface.

Each I/O bank contains two reference voltage input. Each I/O bank is powered by corresponding VCCIO.

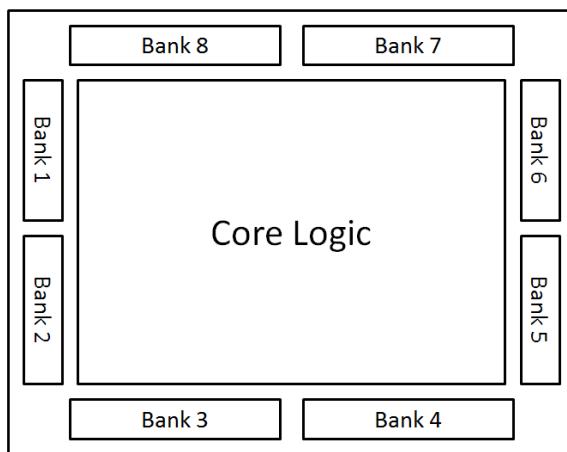


Figure 2-64 I/O Bank Diagram

2.7.5 Compatible with 5V Input

EAGLE I/O is capable of working at 1.8–3.3V voltage range, and is incompatible with direct 5V input. If the 5V voltage drives the input of EAGLE devices, you should connect an external resistor. PCI clamping diode inside EAGLE I/O is opened in the software to reduce the voltage received by the input port to the safe range of the device.

Resistance value is decided by the current features of PCI clamping diode, the voltage and current features of diode as shown in table 2-23.

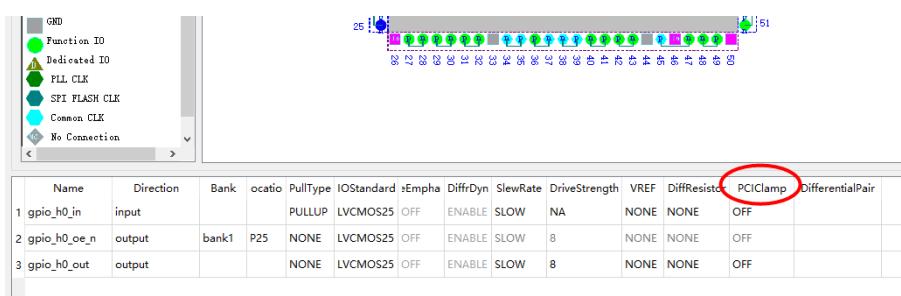


Figure 2-65 Clamping Diode Switch Setting

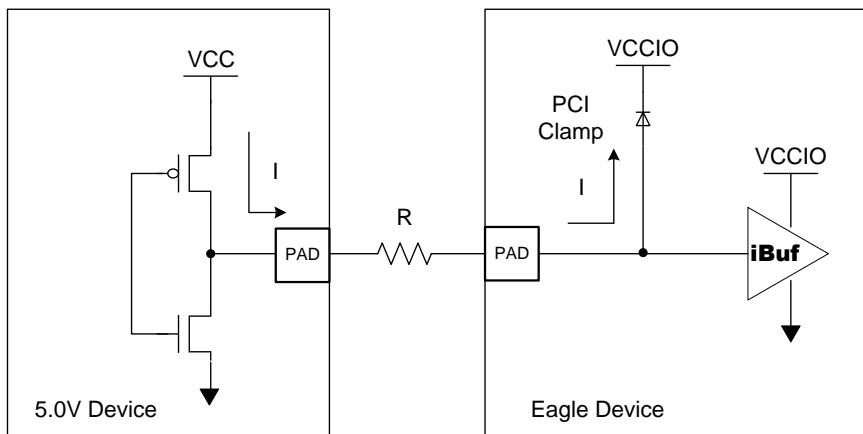


Figure 2-66 5V Input Fed Eagle Device

Table 2-23 PCI Clamping diode Current Features

V_D (V)	I_{max}	Unit
0.0	0.92	μA
0.1	9.2	μA
0.2	20	μA
0.3	30.4	μA
0.4	43.3	μA
0.5	76.5	μA
0.6	0.15	mA
0.7	0.36	mA
0.8	2.85	mA
0.9	9.42	mA

To support 5V input, it is recommended to operate VCCIO at the range of 2.5–3.0V otherwise device operating at exceeded safety voltage for extended periods of time may reduce device lifetime.

Design completed, voltage on circuit PAD should not exceed 3.75V, and 5V signal should not be connected before entering to user mode unless using an external clamping diode.

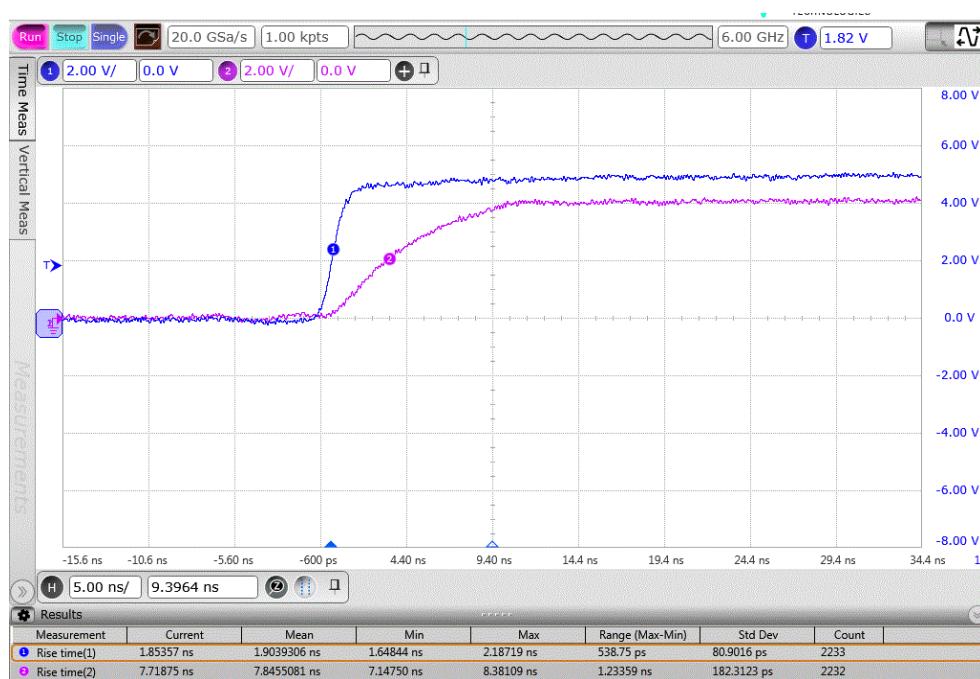
The absolute maximum tolerance voltage of I/O devices is $V_{IMAX}=3.7V$, setting $VCCIO=2.5V$, the voltage of IO input $V1=3.3$ after division, and the voltage on

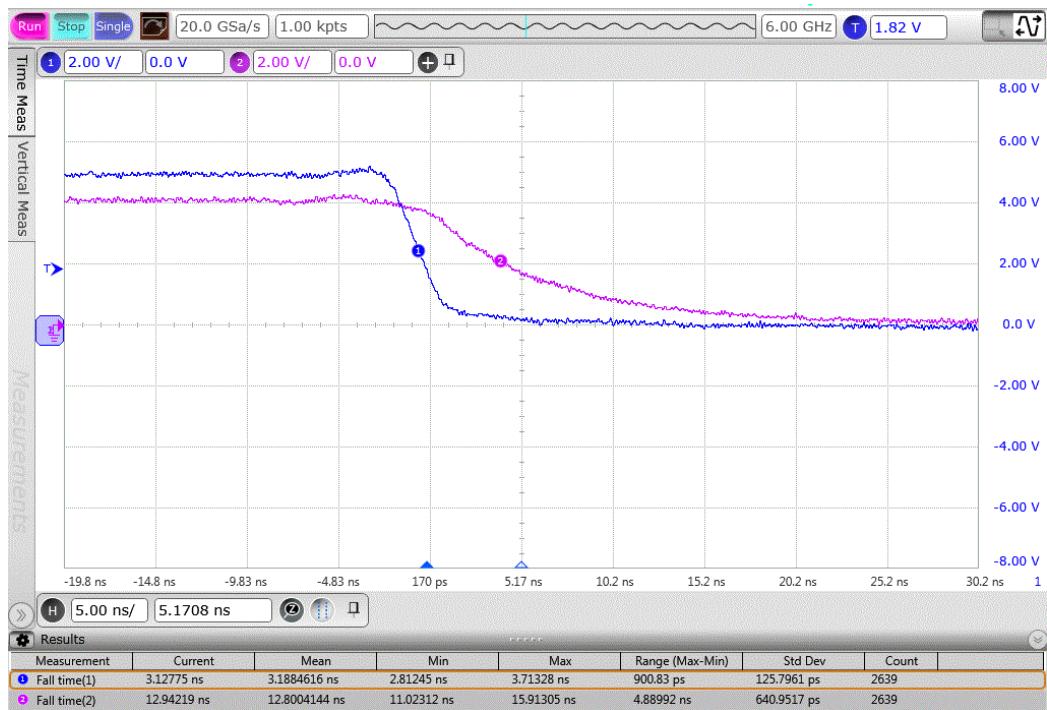
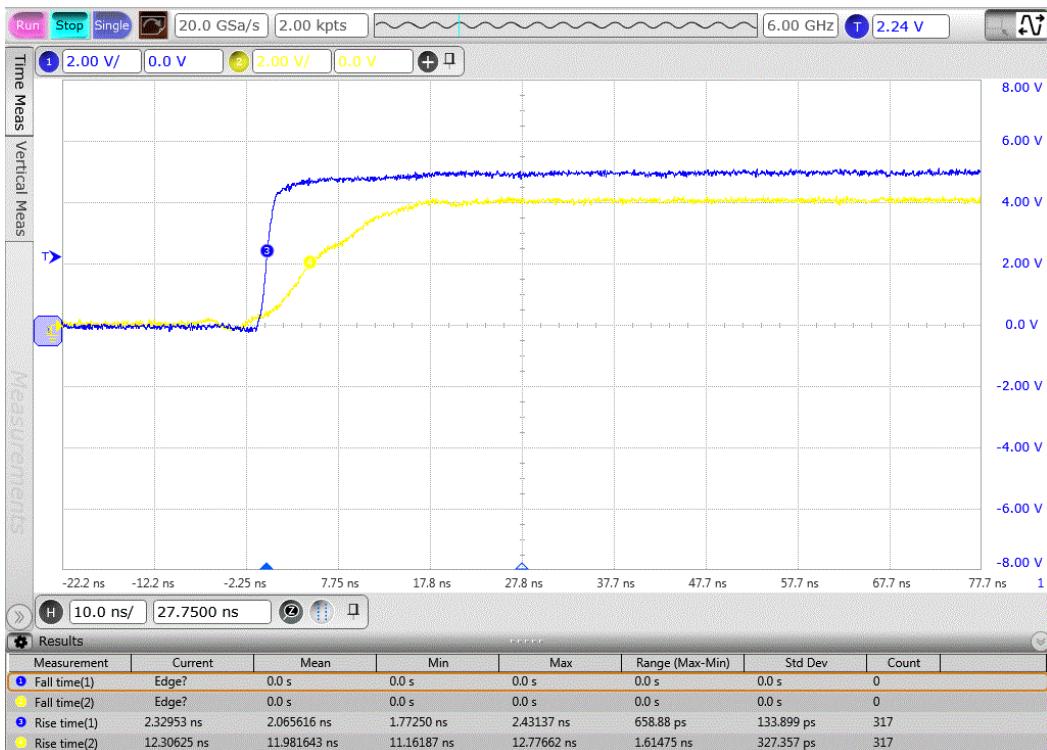
clamping diode is reduced to 0.8V. $V_{D10}=V_1-V_{CC10}=3.3-2.5V= 0.8V$. $I_{D10} @ 0.8V = 2.85mA$, $R = (5 - 3.3)V/2.85 \text{ mA} = 596\Omega$.

Connecting different resistor at the input of clamping diode, receives detected wave at the EAGLE end.

Connecting resistor $R=330 \Omega$, rising time is 7.8 ns and falling time is 12 ns. As shown in figure 2-67.

Connecting resistor $R=600 \Omega$, rise time is 12ns and falling time is 21ns, as shown in figure 2-68.



Figure 2-67 5V Input Fed EAGLE Devices Receiving End Waveform @ $R=330\Omega$ 

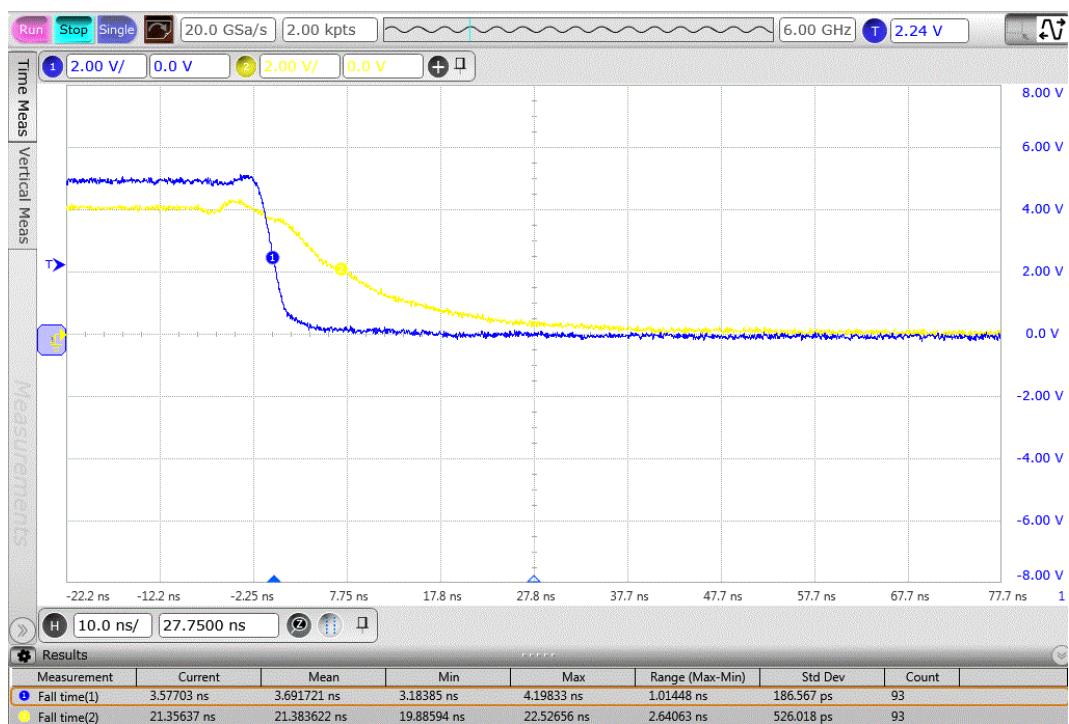


Figure 2-68 5V Input Fed EAGLE Device Rising/Falling Edge @R=600Ω



2.8 EAGLE FPGA Configuration

EAGLE FPGA has two kinds of IO layout: EG4A and EG4X are configured by loading configuration data to internal FPGA. EAGLE FPGA has some dedicated pins and multiplexed pins. The software can configure multiplexed pins, which can be used as general purpose input/output after configuration.

2.8.1 Configuration mode

EAGLE FPGA supports five configuration modes: slave serial (SS), slave parallel (SP), master parallel (MP), MSPI mode and JTAG mode. Configuration mode is decided by MSEL [2:0] and M [1:0] signals, as shown in the following tables:

EAGLE family FPGA configuration bitstream is 4.8M~6Mbits, which is related to ERAM initialized data size. It requires FPGA capacity is greater than or equivalent to 6M bits. Configuration FPGA can use industrial standard serial SPI interface FLASH, e.g. M25Pxx, SST25LFxxx, S25FLxxx etc. EAGLE FPGA also supports SPI FLASH with 0X03 read commands.

a) EG4 Configuration Mode 1

Table 2-24 EG4 Configuration Mode and Pin 1

Configuration Mode						
Configuration Pin	Type	SS	SP	MSPI	MP	JTAG
		Slave serial	Slave Parallel	Master SPI Standard	Master Parallel (X8)	
MSEL[2:0]	Multiplexing	000/001	110/111	010/011/100	101	XXX
PROGRAMN	Multiplexing	PROGRAMN				
INITN	Multiplexing	INITN				
DONE	Multiplexing	DONE				
CCLK	Multiplexing	CCLK				
CSN	Multiplexing	CSN	CSN	CSN	CSN	—
TMS TCK TDO TDI	Multiplexing	—	—	—	—	TMS CK TDO TDI



D[7:2]	Multiplexing	-	D[7:2]	-	D[7:2]	-
D[1]/ MOSI	Multiplexing	-	D[1]	MOSI	D[1]	-
D[0]/DIN/ MISO	Multiplexing	DIN	D[0]	MISO	D[0]	-
SPICSN	Multiplexing	-	-	SPICSN	-	-
CSON/DOUT	Multiplexing	CSON /DOUT	CSON	CSON /DOUT	CSON	-

Note:

- (1) Above configuration modes are available to EG4A20BG256

EG4A multiplexing configuration pins include:

- Configuration Mode Selection Pin MSEL[0], MSEL[1], MSEL[2])
- Configuration Clock Pin (CCLK)
- Configuration Start Signal Pin (PROGRAMN)
- Configuration Done Pin (DONE)
- Configuration Error Indication Pin (INITN)
- Mode Configuration ChipSelect Pin (CSN)
- Configuration Cascaded ChipSelect Pin/Data Output Pin (CSON/DOUT)
- Boundary Scan Pins (TDI, TDO, TMS, TCK)
- Configuration Data Input Pin (D[7:0]) , where D[1] can also be used as MOSI in MSPI mode, D[0] can be used as DIN in slave mode and MISO in MSPI mode
- MSPI Mode Flash Chipselect Pin (SPICSN)
- PROG INIT DONE signal multiplexing may lead to the problem of reload, not recommended used as input, while can be used as output pin.

b) EG4 Configuration Mode 2

Table 2-25 EG4 Configuration Mode and Pin 2

Configuration Pin	Type	Configuration Mode					JTAG
		SS Slave serial	SP Slave Parallel	MSPI Master SPI Standard	MP Master Parallel (X8)		
M [1:0]	Multiplexing	11	10	01	00	XX	
PROGRAM_B	Multiplexing	PROGRAM_B				—	
INIT_B	Multiplexing	INITN_B				—	
DONE	Multiplexing	DONE				—	
CCLK	Multiplexing	CCLK				—	
CSI_B/MOSI	Multiplexing	—	CSI_B	MOSI	CSI_B	—	
TMS TCK TDO TDI	Multiplexing	—	—	—	—	TMS CK TDO TDI	
D[7:1]	Multiplexing	—	D[7:1]	—	D[7:1]	—	
D[0]/DIN/ MISO	Multiplexing	DIN	D[0]	MISO	D[0]	—	
CS0_B	Multiplexing	—	CS0_B	CS0_B	CS0_B	—	
DOUT	Multiplexing	DOUT	—	DOUT	—	—	

Note:

- (1) Above configuration modes are available to EG4X20BG256, EG4A20NG88, EG4X20LG144.

Following are configuration multiplexed pins:

- Configuration Mode Selection Pin (M[0], M[1])
- Configuration Clock Pin (CCLK)
- Configuration Start Signal Pin (PROGRAM_B)
- Configuration Completion Pin (DONE)



- Configuration Error Indication Pin (INIT_B)
- Parallel Mode Configuration Chipselect Pin (CSI_B)
- MOSI in MSPI Mode (MOSI)
- Configuration Parallel Cascading Chipselect Pin/ MSPI Flash Chipselect pin (CS0_B)
- Configuration Cascading Serial Data Output Pin (DOUT)
- Boundary Scan Pins (TDI, TDO, TMS, TCK)
- Configuration Data Input Pin (D[7:0]), D[0] can be used as DIN in slave mode and MISO in MSPI mode

Based on different configuration modes, CCLK can either be FPGA clock output or input of peripheral circuit. DONE/INITN/INIT_B are open-drain output with internal pull-up.

Multiplexing signals like PROGRAM/PROGRAM_B INITN/INIT_B DONE can cause reload. And these signals are not recommended to use as input when multiplexing pin. But they can be multiplexed as output pin.

2.8.2 Configuration Sequence

The configuration sequence of EAGLE FPGA is composed of three stages. Firstly, device enters reset until chip power-on reset or system reset signal is active. And device enters initialization stage, clear internal configuration data. After Initialization, configuration data is written to FPGA. Writing finishes, FPGA enters wake-up stage.

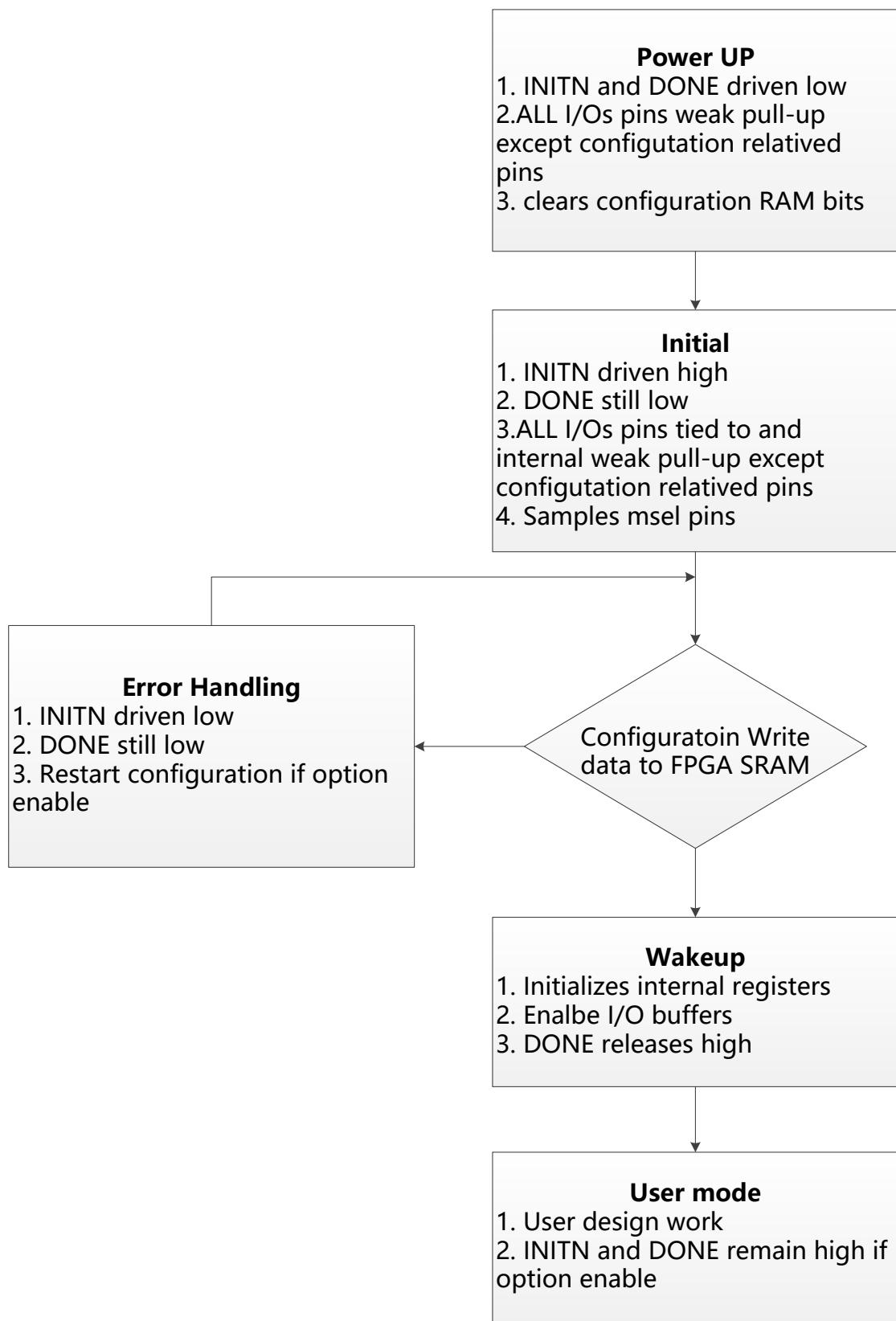


Figure 2-69 EG4A MSPI Configuration Sequence

1. Power-up and Initialization



When power is first applied to the EAGLE FPGA, system must be firstly initialized and then enters configuration download stage. If users need to re-download configuration data, pulling PROGRAM/PROGRAM_B down, system begins to initialize, on which FPGA clear all configuration points and reset internal registers.

2. Configuration Data Written

After the initialization completes, INITN/INIT_B signals driven high when user configuration data can be written to EAGLE FPGA

INITN/INIT_B driven high, FPGA sampling mode select signal voltage that determines configuration mode. INITN/INIT_B driven high in JTAG configuration mode. JTAG mode can be entered in any mode.

During configuration, INITN/INIT_B driven low indicates configuration bitstream wrong. You can choice reload.

3. Wake-up Stage

EAGLE FPGA proceeds to wake-up stage after finishing all configuration points and block RAM data written. It can mainly execute these following functions;

- 1) Release DONE signal. DONE signal driven high from low indicating EAGLE FPGA completing data configuration. If the signal does not change, the data configuration fails.
- 2) Release global tri-state signal (GTS), which can release all I/O pins.
- 3) Release global reset/set signal (GRS), enabling all flip-flops to change status.
- 4) Release global write enable signal (GWE), enabling all RAM and flip-flops to be written.

2.8.3 MSPI Configuration Mode

In MSPI mode, EG4A20BG256 provides two dedicated signals MOSI and SPICSN for SPI interface, MOSI provides read command, address and such information; SPICSN is SPI chipselect; EG4X20BG256, EG4A20NG88 and EG4X20LG144 provide two dedicated signals MOSI and CSO_B for SPI interface, MOSI command provides read command, address and such information, CSO_B is SPI chipselect.

In MSPI mode, CCLK is generated by internal oscillator in MSPI mode. Users can select CCLK frequency. When FPGA power-on, CCLK set as a default low frequency.

Users can modify CCLK frequency through frequency option, the frequency of CCLK range from 2.5MHz, 5MHz, 7.5MHz, 10MHz, 12MHz, 14.5MHz to 16MHz.

SPI FLASH data written can be realized by using FPGA download line through JTAG. Offline downloader or other dedicated programmer equipment can be used for writing in mass production.

As the figure 2-70 shows the diagram of EG4A20BG256 MSPI configuration, PROGRAM signal control EAGLE FPGA reset configuration. The INITN and DONE signals both are internal pull-up open drain output signals. When DONE signal driven high, it indicates configuration success and chip starts to work. Configuration sequence as shown in the figure 2-71.

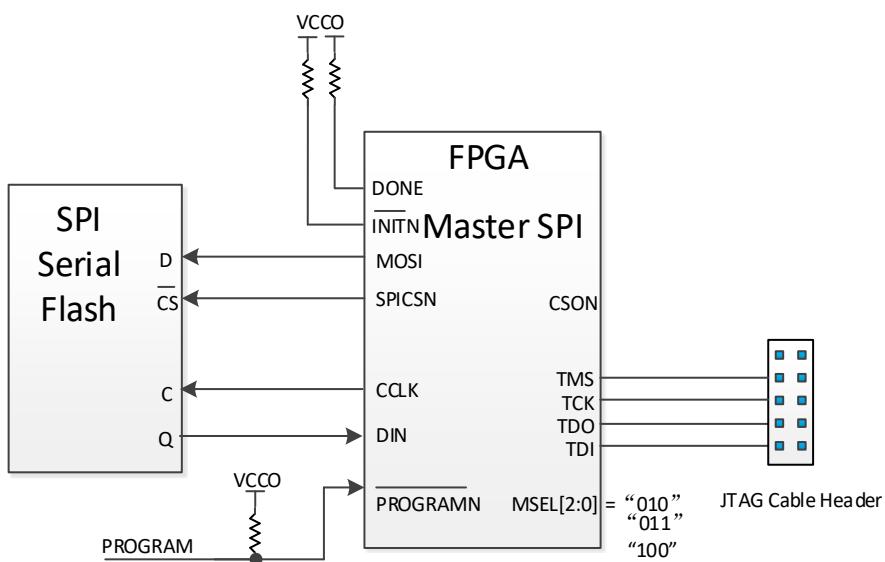


Figure 2-70 EG4A20BG256 MSPI Configuration Scheme

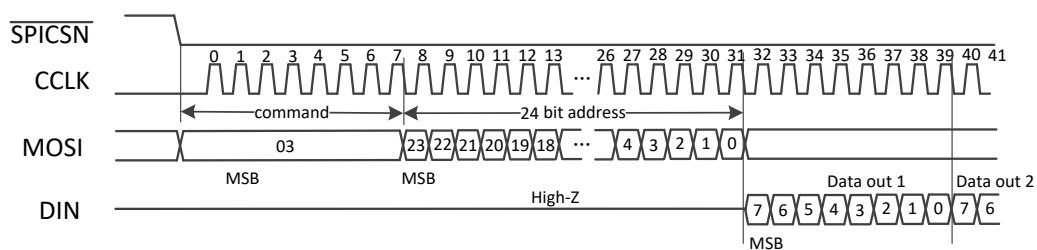


Figure 2-71 EG4A20BG256 MSPI Configuration Timing

2.8.4 Slave Serial Configuration Mode

In Slave Serial Mode, FPGA can be loaded through MCU. The software can generate bin file (EG4X20BG256, EG4A20NG88) or rbf file (EG4A20BG256) for MCU loading.

MCU can write data to FPGA through CCLK and DIN signals in serial way. EGALE FPGA receives data in each rising edge of CCLK, after data sending, DONE signal pulled up indicates configuration completing, if not, INITN/INIT_B signal will be pulled down.

EG4A20BG256 slave serial configuration timing as shown in the following figure.

When PROGRAMN pulled down, INITN signal pulled down indicating that FPGA starts to initialize. After initialization, signal INITN driven high, configuration starts while FPGA is sampling configuration data on the rising edge of CCLK. After configuration, DONE signal driven high indicates configuration success and chip starts to work.

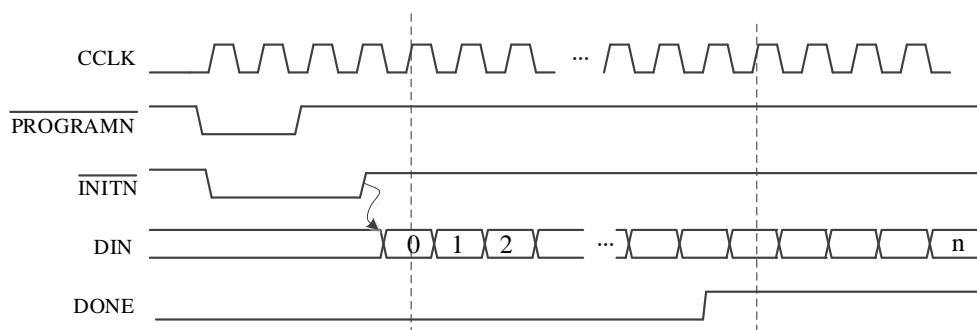


Figure 2-72 Slave Serial Timing Sequence 1

The Slave Serial configuration timing of EG4X20BG256, EG4A20NG88, EG4X20LG144 as shown in the following figure.

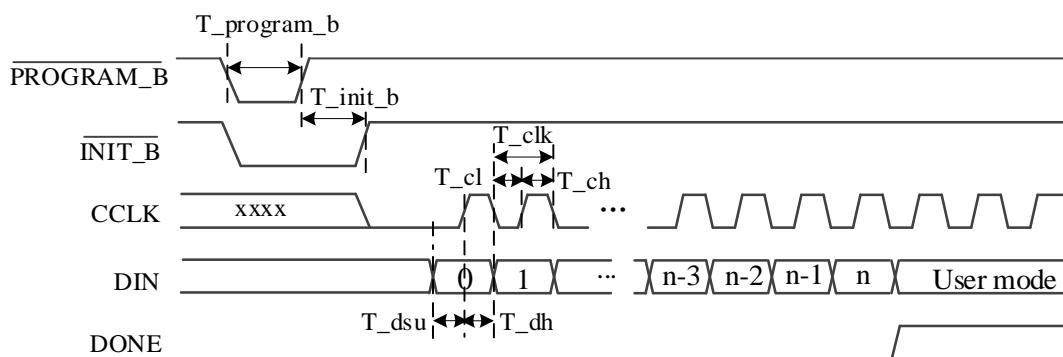


Figure 2-73 Slave Serial Configuration Timing Sequence 2

Table 2-26 EAGLE Slave Serial Timing Specification

Symbol	Parameters	Min	Max	Unit
T_program_b	PROGRAM_B low pulse width	1	-	us



Symbol	Parameters	Min	Max	Unit
T_init_b	INIT_B low pulse width	–	10	ms
T_clk	CCLK period	33	–	ns
T_ch	CCLK high time	15.5	–	ns
T_cl	CCLK low time	15.5	–	ns
T_dsu	Data setup time	16.5	–	ns
T_dh	Data hold time	6	–	ns

When EG4 devices loading in slave serial configuration mode, CCLK should at least last for 6us plus 10 clock period after done signal driven up, which can ensure EG4A20BG256 D[0]/DIN/ MISO, D[1]/ MOSI, SPICSN, CS0N/DOUT, CCLK pins or EG4X20BG256, EG4A20NG88 and EG4X20LG144 D[0]/DIN/ MISO, CSI_B/MOSI, CS0_B, DOUT, CCLK pins entering into user mode.

2.8.5 Serial Configuration Mode Cascading

When multiple FPGAs are required to work together, you can use the cascading configuration. EG4A20BG256 supports Flow Through mode, cascading mode is designated by the commands in bitstream.

When EG4A20BG256 configuration data is downloading, if adopts Flow Through mode, the first FPGA configuration done, output CS0N to activate the second chip start to configure. Cascade configuration chip DONE and INITN pins are connected with other through pull-up resistor line. After two chip configuration done, through DONE two chips start to work simultaneously.

Following figure shows EG4A20BG26 serial configuration mode Flow Through cascading mode. Here with two FPGA cascading configuration, the first one adopts master serial mode, the second adopts slave serial mode.

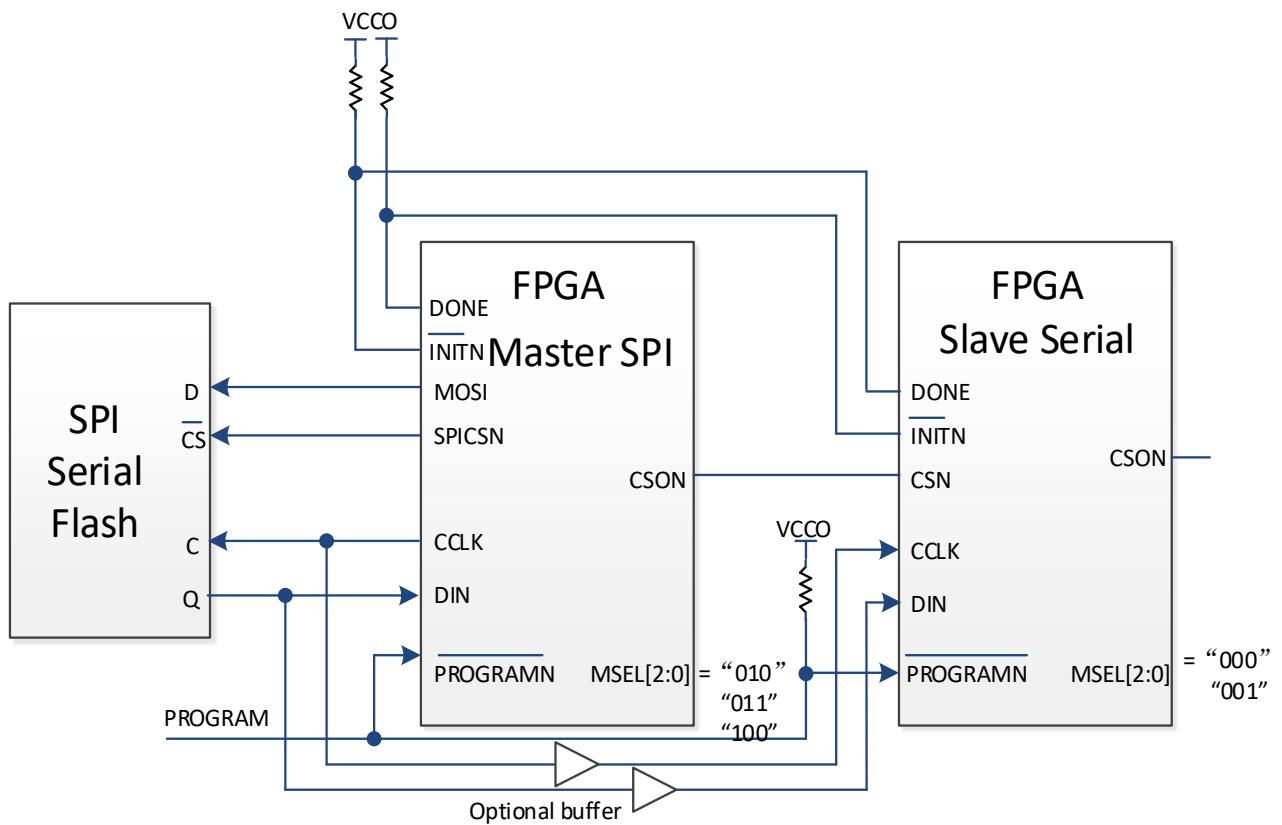


Figure 2-74 Master, Slave Serial Using Flow-Through Cascading Configuration

2.8.6 Slave Parallel Configuration Mode

In slave parallel configuration, MCU, CPU or such controller should be adopted to assist configuration. It can achieve higher configuration speed through writing 8-bit parallel data.

When EG4A20BG256 MSEL[2:0] signal set as 110/111, as shown in the following figure, where shows multiple CSN signals can select multiple configuration devices.

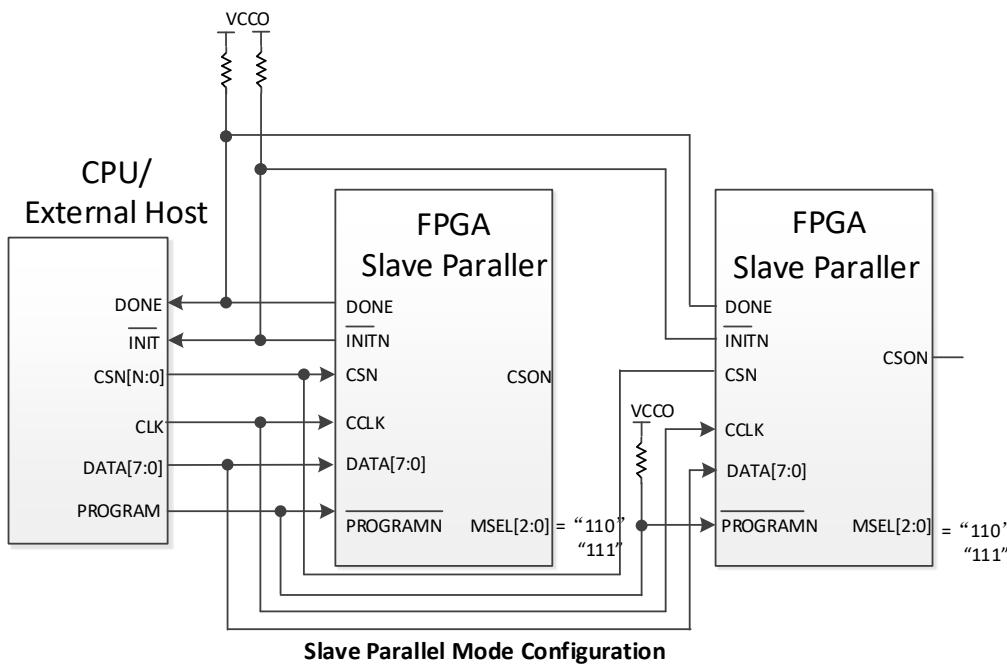


Figure 2-75 EG4A20BG256 Slave Parallel Configuration Scheme

EG4A20BG256 slave parallel timing diagram as shown in the figure 2-78. The initialization timing is same as that of serial configuration. After initialization completes, CSN signal valid, the configuration data is written to EAGLE FPGA on the rising edge of CCLK. Configuration completes, DONE signal driven high.

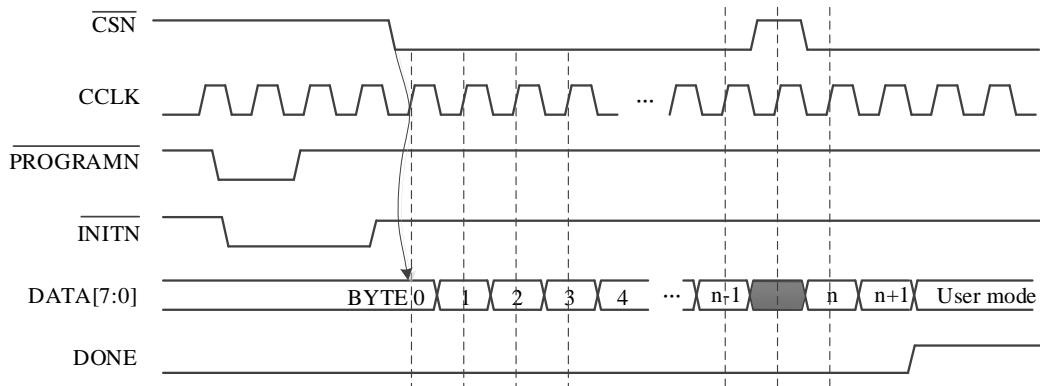


Figure 2-76 Slave Parallel Configuration Timing Sequence 1

EG4X20BG256, EG4A20NG88 and EG4X20LG144 slave parallel configuration mode M[1:0] set as 10, and multiple CSN signals can select multiple configuration chips.

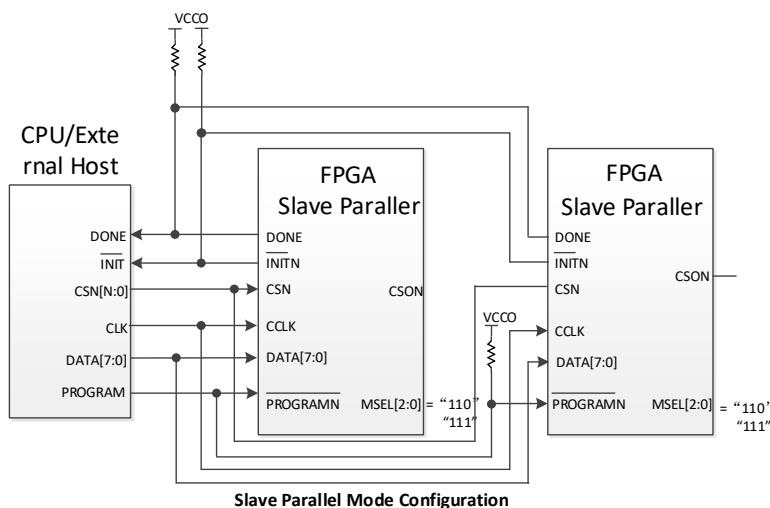


Figure 2-77 Slave Parallel Configuration Timing Sequence 2

EG4X20BG256, EG4A20NG88, EG4X20LG144 slave parallel timing diagram as shown in the 2-80 figure. The initialization timing is consistent with that of the serial configuration. After initialization, when the chipselect CSI_B is active, the configuration is written to EAGLE FPGA on the rising edge of clock. Configuration completes, DONE signal driven high.

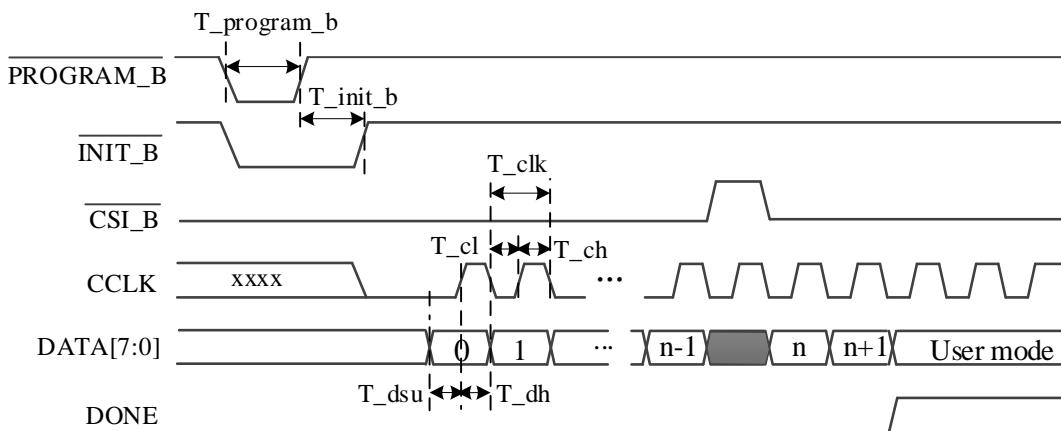


Figure 2-78 Slave Parallel Configuration Timing Sequence 2

Table 2-27 EAGLE Slave Parallel Timing Specification Diagram

Symbol	Parameter	Min	Max	Unit
T_program_b	PROGRAM_B low pulse width	1	-	us
T_init_b	INIT_B low pulse width	-	10	ms
T_clk	CCLK period	33	-	ns

T_ch	CCLK high time	15.5	-	ns
T_cl	CCLK low time	15.5	-	ns
T_dsu	Data setup time	16.5	-	ns
T_dh	Data hold time	6	-	ns

When EG4 devices loading in slave parallel configuration mode, CCLK should at least last for 6us plus 10 clock output periods after done signal being pulled up, which can ensure D[0]/DIN/ MISO, D[1]/ MOSI, SPICSN, CS0N/DOUT, CCLK signal pin of EG4A20BG256, device or D[0]/DIN/ MISO, CSI_B/MOSI, CSO_B, DOUT, CCLK of EG4X20BG256, EG4A20NG88, EG4X20LG144 signal pin entering to user mode.

2.8.7 Master Parallel Configuration Mode

Master parallel configuration is similar to slave parallel configuration; the differences lie in CCLK is provided by FPGA.

2.8.8 JTAG Configuration Mode

EGALE FPGA also can be configured in JTAG mode. JTAG configuration mode has TDI, TDO, TMS, TCK pins. After INITM/INIT_B signal driven high, JTAG mode can interrupt other mode by command and enter JTAG configuration mode regardless of any ongoing configuration mode.

In JTAG configuration mode, using dedicated USB download line and the software, you can check the configuration success or not.

JTAG configuration mode reference timing and timing specification as shown in figure 2-81 and table 2-28.

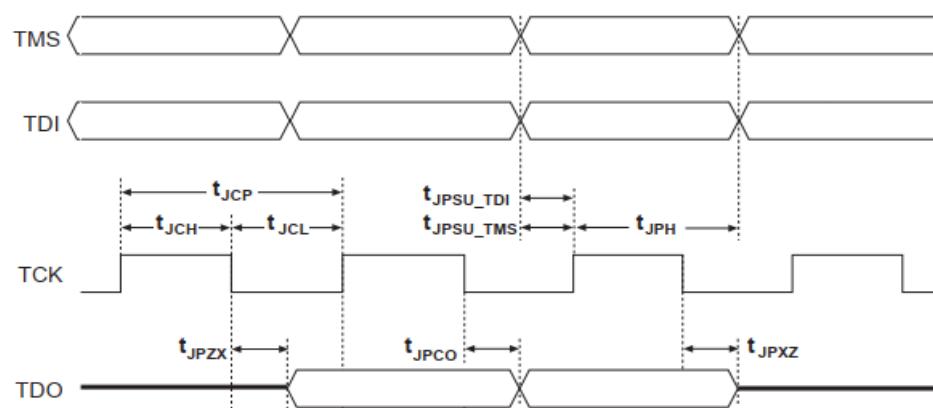




Figure 2-79 EAGLE JTAG Timing Sequence

Table 2-28 EAGLE JTAG Timing Specification

Symbol	Parameter	Min	Max	Unit
t_{JOP}	TCK Clock period	100	—	ns
t_{JCH}	TCK High-Level Time	48	—	ns
t_{JCL}	TCK Low-Level Time	48	—	ns
t_{JPSU_TDI}	TDI Setup Time	6	—	ns
t_{JPSU_TMS}	TMS Setup Time	8	—	ns
t_{JPH}	JTAG Port Hold Time	10	—	ns
t_{JPco}	JTAG Port Clock to Output Delay	—	16	ns
t_{JPZX}	JTAG Port High-Z to valid output switch time	—	16	ns
t_{JPXZ}	JTAG Port valid output to High-Z switch time	—	16	ns

Note:

1. If adopt MSPI mode and update external FLASH data through JTAG non-background mode, the frequency of tck should greater than or equal to 100K.
2. When EG4 in JTAG mode, done signal being asserted and should at least last for 6us plus 10 cycles clock output, which can ensure EG4A20BG256 D[0]DIN/MISO, D[1]/ MOSI, SPICSN, CSNO/DOUT, CCLK signal pin or EG4X20BG256, EG4A20NG88 and EG4X20LG144 devices D[0]/DIN/MISO, CSI_B/MOSI, CSO_B, DOUT, CCLK signal pin entering into user mode.

2.8.9 IEEE 1149.1 Boundary Scan Test

All EAGLE family devices 10 integrate scan cells which are accessed through an IEEE 1149.1 TAP. The boundary scan test commands can access 10 cells in any mode. (SAMPLE commands can only be used in user mode).

2.8.10 MSPI DUAL BOOT Function

In MSPI mode When adopted SPI FLASH capacity is greater than 12Mbit, EAGLE FPGA support MSPI dual boot function. When the Primary bitstream download fails, EAGLE FPGA automatically switch to address set by users and read golden bitstream. As figure 2-82 shows the data space distribution of spi FLASH in dual boot.

Dual boot FLASH map	
0x000000	Primary bitstream
.....	
0x0C0000	Dummy
.....	
0x0D0000	Golden address
.....	Golden bitstream

Figure 2-80 EAGLE FPGA Dual Boot SPI FLASH Data Space Distribution

2.8.11 MSPI MULTI BOOT Function

In MSPI mode, users can set multi boot function through the software. When entering into user mode, application itself can trigger rebootn=0 and re-download bitstream from designated SPI FLASH address, which can either come from user interface or the software. Noticeably, rebootn=0 signal remain at low level should greater than 2.5us.

2.8.12 FPGA DNA Security Features

EAGLE FPGA provides the unique 64-bit DNA value for each FPGA during production, this data cannot be modified or cleared. Users can utilize DNA data to protect user design. The software provides IP interface that can access DNA data. As figure 2-83 and 2-84 shown. Usr_dna_in is the shift data input for interface testing.

clk frequency range is 0~20MHz. Sending dna_shift along the clock falling

edge by recommendation to meet timing sequence.

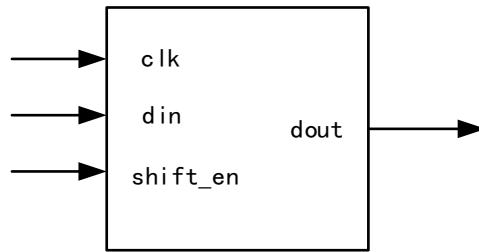


Figure 2–81 EAGLE FPGA DNA IP

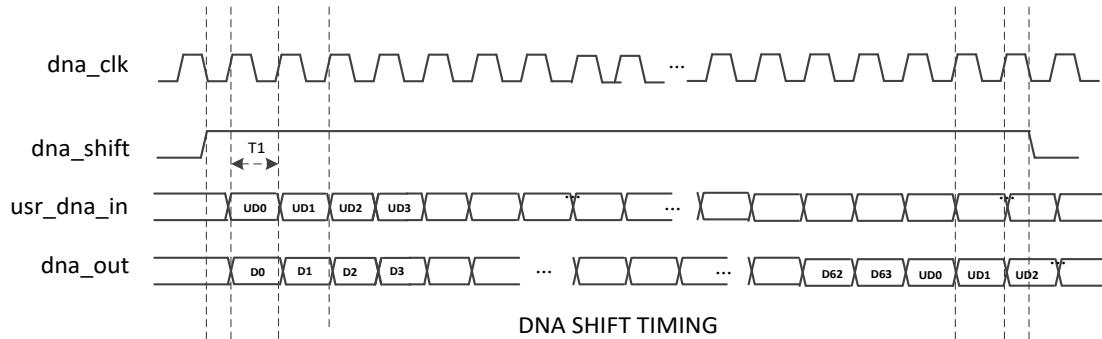


Figure 2–82 EAGLE FPGA DNA Timing Sequence

2.8.13 FPGA I/O Pin Setting During Configuration

Some FPGA Pins have dedicated pull-up/down resistors. During configuration, the majority of user I/O pins have optional pull-up resistor during configuration. EG4A and EG4X pins enable pull-up resistor is decided by HSWAPEN signal.

2.8.14 FPGA I/O Pin State during Configuration

1) Non-Configuration I/O

After device power-up and before loading program, non-configuration related I/O remain at tri-state.

During the loading stage, the state of General purpose I/O is controlled by HSWAPEN signal and can be set as weak pull-up or tri-state.

Entering into user mode, the I/O pin stage decided by users, the unused pin in the weak pull-up state.

2) FPGA I/O pin state, as shown in the table 2-29, 2-30.

In EG4A, HSWAPEN is one-bit control register CTRL [31], default value is 1, this register can only be modified by bitstream.

Table 2-29 EG4 Pin Termination 1

Pin	Pre-configuration		Post-configuration
	HWSWAPEN=0 (enable)	HWSWAPEN=1 (disable)	
MSEL[2:0]	Pull-up to Vccio	Pull-up to Vccio	User I/O
PROGRAMN	Pull-up to Vccio	Pull-up to Vccio	Software ProgPin Setting
INITN	Pull-up to Vccio	Pull-up to Vccio	Software InitPin Setting
DONE	Pull-up to Vccio	Pull-up to Vccio	Software DonePin Setting
CCLK	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin Setting
CSN	Pull-down to Gnd	Pull-down to Gnd	User I/O
TMS TCK TDO TDI	Pull-up to Vccio	Pull-up to Vccio	Software JtagPin Setting
D[7:2]	Pull-up to Vccio	Pull-up to Vccio	User I/O
D[1]/ MOSI	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin Setting
D[0]/DIN/MISO	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin Setting
SPICSN	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin Setting
CSON/DOUT	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin Setting



Pin	Pre-configuration		Post-configuration
	HSWAPEN=0 (enable)	HSWAPEN=1 (disable)	
Others	Pull-up to Vccio	High-Z	User I/O
USRCLK ³	Pull-up to Vccio	Pull-up to Vccio	User I/O

Note:

1. EG4A20BG256 CSN(J3) cannot remain at pull-up mode in JTAG, SS and MSPI modes.
2. EG4A20BG245 F15(I0_R1_6) out of HSWPANE control and remain at weak pull-up state.
3. USRCLK is only for test.

In EG4X20BG256, EG4A20NG88 and EG4X20LG144, HSWAPEN is an I/O pin, by default remain at weak pull-up, as shown in table below.

Table 2-30 EG4 Pin Termination 2

Pin	Pre-configuration		Post-configuration
	HSWAPEN=0 (enable)	HSWAPEN=1 (disable)	
M[1:0]	Pull-up to Vccio	Pull-up to Vccio	User I/O
PROGRAM_B	Pull-up to Vccio	Pull-up to Vccio	Software ProgPin setting
INIT_B	Pull-up to Vccio	Pull-up to Vccio	User I/O
DONE	Pull-up to Vccio	Pull-up to Vccio	Software DonePin setting
CCLK	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin setting
CSI_B/MOSI	Pull-down to Gnd	Pull-down to Gnd	Software SpiPin setting
TMS TCK TDO TDI	Pull-up to Vccio	Pull-up to Vccio	Software JtagPin setting
D[7:1]	Pull-up to Vccio	Pull-up to Vccio	User I/O
D[0]/DIN/M ISO	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin setting



Pin	Pre-configuration		Post-configuration
	HWSWAPEN=0 (enable)	HWSWAPEN=1 (disable)	
CS0_B	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin setting
DOUT	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin setting
HWSWAPEN	Pull-up to Vccio	Pull-up to Vccio	User I/O
Others	Pull-up to Vccio	High-Z	User I/O

Note:

1. EG4X20BG256, EG4A20NG88 and EG4X20LG144 CSI_B pin cannot remain at pull-up state in JTAG, SS and MSPI modes;
2. EG4X20BG256 IO_R7P_3 (L3) out of HSWAPEN control and remain at weak pull-up state.
- 3) If the following pins of EG4 family devices set as output or inout type in code, it cannot maintain at high resistance state during loading otherwise it will output high pulse or low pulse signals. Users should better avoid these pins when having requirements on pins state during loading. Or to avoid by setting in the software. For more information, please refer to TR303, TR305.
Uncontrolled pins of EG4 family FPGA as listed in the following table.

Table 2-31 Uncontrolled Pins of EG4 FPGA during Configuration

Device	Pin
EG4X20BG256	M15, M16, L12, K15, P16, L13, K1, L14, T13, R15, L16, L1, T6, P11, L10, M10, N9, P9
EG4X20LG144	—
EG4A20BG256	L7, M6, P1, P2, C14, G5, A5, A13, C6, F7, A7, A3, B4, A4, D5, D6
EG4A20NG88	—

2.9 Embedded ADC

EGALE has an embedded 8-channel 12-bit 1 MSPS ADC. ADC requires an independent 3.3V analog operational voltage, an analog ground and an independent VREF voltage input. Multiplexing 8 channels input and user IOs, the available channels for users vary with package. When users do not need ADC, its pins can be set as general purpose IO. Multiplexing IO setting is independent, the unused ADC channel pin can be used as General purpose IO.

EG4A20NG88 and EG4X20LG144 do not support ADC function.

Table 2-32 ADC External/Internal Ports

Port	Port Type	Description
ADC_VDDD	Power supply PAD	3.3V Digital voltage input
ADC_VDDA	External Power supply PAD	3.3V Analog voltage input
ADC_VSSA	External Power supply PAD	3.3V Analog ground
ADC_VREF	External PAD	Independent input, Sampling reference analog voltage input and input voltage range 2.0V~3.3V, not exceed VDDA
ADC_HC<7:0>	External PAD	8 channels of sampling signal input, multiplexed with user IO
Internal Port	Port Direction	Description
clk	Input	ADC Work Clock
pd	Input	ADC power down in LP mode
s<2:0>	Input (From FPGA)	ADC Channel input selection
soc	Input (From FPGA)	Sampling enable input signal, high active
eoc	Output (To FPGA)	ADC conversion completion, high active
b<11:0>	Output (To FPGA)	ADC conversion result of corresponding channel

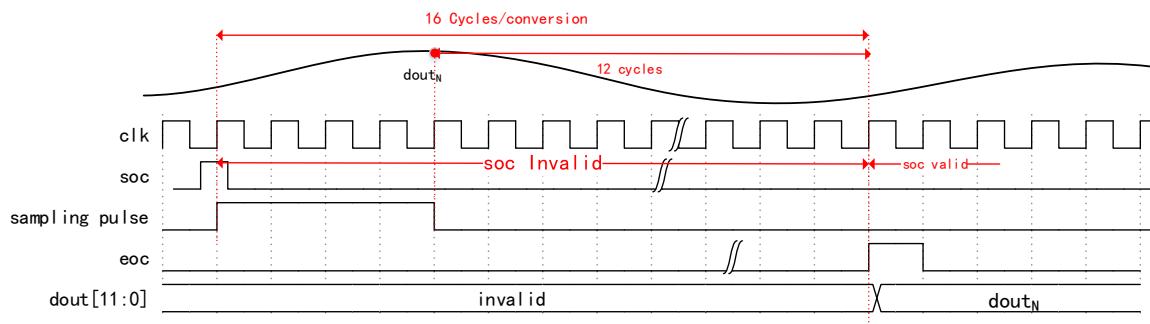


Figure 2–83 Eagle ADC Sampling Control Timing

3 DC/AC Characteristics

All parameters refer to the worst supply voltage and junction temperatures. Unless otherwise specified, the following information is available to: same commercial and industrial AC and DC characteristic. All parameters are values when the voltage is applied to the ground.

3.1 DC Characteristics

3.1.1 Maximum Absolute Rating Value

Table 3-1 Maximum Absolute Rating

Symbol	Parameter	Min	Max	Unit
V_{CCINT}	Supply Voltage for Core	-0.5	1.32	V
V_{CCAUX}	Auxiliary Supply Voltage	-0.5	3.75	V
V_{CCIO}	I/O Fed Supply Voltage	-0.5	3.75	V
V_I	DC Input Voltage	-0.5	3.75	V
V_{ESDHBM}	Human Body Model Discharge Voltage	-	± 2000	V
V_{ESDCDM}	Machine Model Discharge Voltage	-	± 500	V
T_{STG}	Storage Temperature	-65	150	°C
T_J	Operating Junction Temperature	-40	125	°C

Conditions outside the range listed in the absolute maximum ratings tables may cause permanent damage to the device. Conditions listed in the above table only indicates that working at these conditions will not cause damage to the device but it does not mean devices having normal function in these conditions. The functionality of device based on any maximum absolute rating may cause permanent damage to the device. Additionally, devices operation at the absolute maximum ratings for extended periods will greatly undermine device reliability.

During transition, input signals may overshoot or undershoot as shown in the figure 3-1, and table 3-2 list the overshoot and undershoot duration as percentage

of high time over 10-year life time.

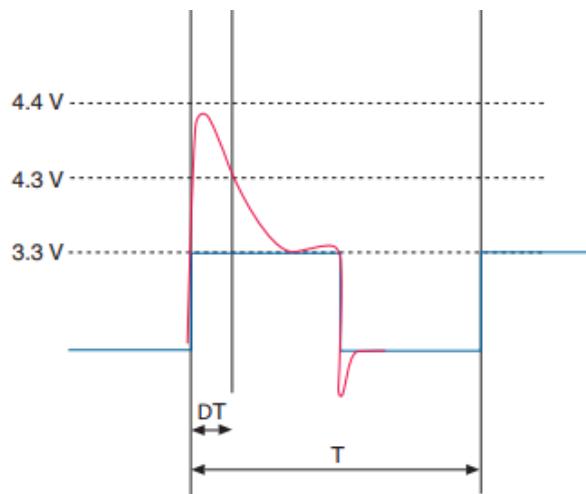


Figure 3-1 Input Signal Overshoot/ Undershoot

Table 3-2 Overshoot and Undershoot Duration As Percentage of High Time over 10-Year Life Time

Parameter	Condition(V)	Under/Overshoot Duration as % of High Time	Unit
VI AC Input Voltage	-0.3	100	%
	-0.4	100	%
	-0.5	86	%
	-0.6	49	%
	-0.7	28	%
	-0.8	16	%
	-0.9	9.23	%
	-1	5.27	%
	-1.1	3	%
	3.7	100	%
	3.8	86	%
	3.9	49	%
	4	28	%



Parameter	Condition(V)	Under/Overshoot Duration as % of High Time	Unit
	4. 1	16	%
	4. 2	9. 23	%
	4. 3	5. 27	%
	4. 4	3	%

3.1.2 Recommended Operation Condition

Table 3-3 Recommended Operation Condition

Symbol	Parameters		Min	Typ	Max	Unit
V _{CCINT}	Supply Voltage for core		1. 14	1. 2	1. 26	V
V _{CCAUX}	Auxiliary Supply Voltage		2. 375	2. 5/3. 3	3. 63	V
V _{CCIO³}	Supply Voltage for I/O @ 3. 3V		3. 135	3. 3	3. 465	V
	Supply Voltage for I/O @ 2. 5V		2. 375	2. 5	2. 625	V
	Supply Voltage for I/O @ 1. 8V		1. 71	1. 8	1. 89	V
	Supply Voltage for I/O @ 1. 5V		1. 425	1. 5	1. 575	V
	Supply Voltage for I/O @ 1. 2V		1. 14	1. 2	1. 26	V
V _{I³}	DC input voltage		-0. 5	—	3. 6	V
V _O	Output voltage		0	—	V _{CCIO}	V
T _J	Operating Junction Temperature	Commercial	0	—	85	°C
		Industrial	-40	—	100	°C
T _{RAMP}	Power supply ramp ratio		0. 05	—	100	V/ms
I _{Diode}	DC current across PCI-clamp		—	—	10	mA



Symbol	Parameters	Min	Typ	Max	Unit
	diode				

Note:

1. V_{CCIO} for I/O banks must be powered up during device operation
2. All input buffer must be powered by V_{CCIO}
3. If true differential pair pin is used as single-ended I/O, the minimum input voltage should not lower than -0.3V or another pin of true differential pair remains unused.
4. I/O interface cannot directly connect to ground or V_{CCIO} , if connecting to applications, a resistor is required.

3.1.3 Basic Power Supply Requirements

Table 3-4 Minimum Power Supply for EG4A20BG256

Symbol	Basic Power Supply ³	Note
VCCAUX	$\geq 2.5V$	Ripple peak-to-peak value should lower than 100mV, must supply power
VCCIO1	\geq Supply Voltage for Downloader	JTAG used for download. Voltage should same as for downloader
VCCIO2	$\geq 1.2V$	Required ²
VCCIO3	$\geq 1.2V$	Required ²
VCCIO4	$\geq 1.2V$	Required ²
VCCIO5	$\geq 1.2V$	Required ²
VCCIO6	$\geq 1.2V$	Required ²
VCCIO7	$\geq 1.2V$	Required ²
VCCIO8	$\geq 1.2V$	Required ²
VCCINT	$= 1.2V$	Must supply

1. In MSPI mode, voltage for V_{CCIO1} should not lower than regulated operational voltage for FLASH



2. V_{CCIO} should be powered up when unused
3. ADC used or not, voltage for ADC_VDDA and VCC108(ADC_VDDD) should be same, and voltage for ADC_VREF should not greater than that of ADC_VDDA. ADC_VDDA and VCC108(ADC_VDDD) should connect to device maximum voltage by recommendation.

Table 3-5 Minimum Power Supply for EG4X20BG256

Symbols	Basic Voltage Supply ³	Note
VCCAUX	$\geq 2.5V$	Peak-to-peak ripple should lower than 100mV, must supply
VCC100	\geq Supply Voltage for Downloader	If use JTAG mode. VCC100 should same as download voltage.
VCC101	\geq Supply Voltage for Downloader	If use JTAG mode. VCC100 should same as download voltage.
VCC102 ¹	$\geq 1.5V$ (Must Supply)	Required ²
VCC103	$\geq 1.2V$	Required ²
VCCINT	$= 1.2V$	Must supply

1. In MSPI mode, voltage for VCC102 should not lower than regulated operational voltage for FLASH
2. VCC10 must be powered up when unused
3. ADC used or not, voltage for ADC_VDDA and ACC102(ADC_VDDD) should be same, and voltage for ADC_VREF should not greater than ADC_VDDA. ADC_VDDA and VCC102(ADC_VDDD) should connect to maximum voltage for device.

Table 3-6 Minimum Power Supply for EG4A20NG88

Symbols	Basic Voltage Supply	Note
VCCAUX	$\geq 2.5V$	Peak-to-peak value should lower than 100Mv, must supply power



VCCIO1	$\geq 1.2V$	Must supply voltage when VCCIO unused
VCCIO2	$=3.3V$	Must supply voltage when VCCIO unused
VCCIO3	$=3.3V$	Must supply voltage when VCCIO unused When using JTAG download, voltage for JTAG should same as downloader voltage for downloader should be same.
VCCIO4	$=3.3V$	Must supply voltage when VCCIO unused
VCCIO5	$\geq 1.2V$	Must supply voltage when VCCIO unused
VCCIO6	$\geq 1.2V$	Must supply voltage when VCCIO unused
VCCIO7	$=3.3V$	Must supply voltage when VCCIO unused
VCCIO8	$\geq 1.2V$	Must supply voltage when VCCIO unused
VCCINT	$=1.2V$	Must supply voltage

1. In MSPI mode, voltage for VCCIO8 should not lower than Flash regulated work voltage
2. EG4A20NG88 BANK2, BANK3, BANK4, BANK7 must be supplied with 3.3V IO voltage.

Table 3-7 Minimum Power Supply for EG4X20LG144

Symbol	Basic Power Supply	Note
VCCAUX	$\geq 2.5V$	Waveform peak-to-peak value should lower than 100mV, must supply power
VCCIO1	$\geq 1.2V$	VCCIO should be supplied with power when unused
VCCIO2	\geq voltage supplied for downloader	VCCIO should be supplied with power when unused; when using JTAG download, voltage supply should same as downloader
VCCIO3	\geq voltage supplied for downloader	VCCIO should be supplied with power when unused; when using JTAG download, voltage supply should same as downloader
VCCIO4	$\geq 1.2V$	VCCIO should be supplied with power when unused
VCCIO5	$\geq 1.2V$	VCCIO should be supplied with power when unused
VCCIO6	$\geq 1.2V$	VCCIO should be supplied with power when unused



VCCIO7	=3. 3V	VCCIO should be supplied with power when unused
VCCIO8	=3. 3V	VCCIO should be supplied with power when unused
VCCINT	=1. 2V	Must supply

3.1.4 Static Supply Current^{1,2}

Table 3-8 Current of Static Power

Symbol	Parameter	Device	Typical	Unit
I_{VCCINT}	Supply voltage for core	EAGLEA_10	3	mA
		EAGLEA_20	5	mA
I_{VCCIO}	I/O Bank Supply Voltage, $@V_{CCIO}=2.5V$	EAGLEA_10	0.4	mA
		EAGLEA_20	0.6	mA
I_{VCCAUX}	Auxiliary Power Supply	EAGLEA_10	2	mA
		EAGLEA_20	2.5	mA

1. Conditions listed above table based on generic recommended operational conditions, test in $TJ= 25^{\circ}\text{C}$ by model device.
2. Model value is tested all static power current fed by I/O from blank device without output current loading, in high impedance and all pull-up/pull-down resistor forbidden in I/O pin.

3.1.5 Hot Socketing

Table 3-9 Hot Socketing parameters

Symbol	Parameters	Max	Unit
$I_{IOPIN(DC)}$	DC current, each I/O	1	mA
$I_{IOPIN(AC)}$	AC current, each I/O	8 ¹	mA

1. Signal rising time is equal or greater than 10us
2. B4, A4, A3, B3, E2, B5, A2, C3, D3 of EG4A20BG256 do not support hot socketing, user should avoid these pins when requires hot socketing.
3. L10, M10, P11, N11, L11, N12, P12, M11, M12 of EG4X20BG256 do not support hot



socketing, user should avoid these pin when require hot socketing.

4. EG4A20NG88 84, 87, 86 do not support hot socketing, user should avoid these pins when requires hot socketing.
5. EG4X20LG144 137, 140, 141, 142, 143 do not support hot socketing, user should avoid these pins when requiring hot socketing.

3.1.6 Voltage Threshold for Power-on Reset

Table 3-10 Voltage threshold for power-on reset

Symbol	Parameters	Min	Typical	Max	Unit
V_{CC_PORUP}	Test threshold voltage for V_{CC} Power-on	0.95	1	1.05	V
V_{CCAUX_PORUP}	Test threshold voltage for V_{CCAUX} power-on	2	2.1	2.2	V
V_{CC_PORDN}	Test threshold voltage for V_{CC} power-down	—	—	0.9	V
V_{CCAUX_PORDN}	Test threshold voltage for V_{CCAUX} power-down	—	—	1.9	V
V_{SRAM_PORDN}	SRAM Test threshold voltage for supply power-down	—	—	0.85	V

3.1.7 I/O DC Electrical Specifications

Table 3-11 Recommended basic operation conditions

Symbol	Parameters	Test Condition	Min	Typical	Max	Unit
I_{IL}, I_{IH}	Input leakage current	$0 \leq V_I \leq V_{CCIO} - 0.5V$	-15	—	15	uA
I_{IH}	Input leakage current	$V_{CCIO} - 0.5V \leq V_I \leq V_{IH_MAX}$	—	—	150	uA
I_{PU}	I/O Weak pull-up current	—	35	—	250	uA
I_{PD}	I/O Weak pull-down current	—	35	—	250	uA



I_{BHLS}	Bus-hold low sustaining current	—	40	—	—	uA
I_{BHHS}	Bus-hold high sustaining current	—	40	—	—	uA
I_{BHLO}	Bus-hold low overdrive current	$0 \leq V_I \leq V_{CCIO}$	—	—	350	uA
I_{BHHO}	Bus-hold high overdrive current	$0 \leq V_I \leq V_{CCIO}$	—	—	350	uA
V_{BHT}	Bus-hold trigger voltage	—	V_{IL_max}	—	V_{IH_min}	V



3.1.8 I/O Pin Capacitance

Table 3-12 EAGLE devices pin capacitance

Symbol	Parameter	QFP	FBGA	Unit
C_{IOTB}	Input capacitance on top/bottom I/O pins	7	6	pF
C_{IOLR}	Input capacitance on left/right I/O pins	8	7	pF

3.1.9 Single-ended I/O DC Electrical Specifications

Table 3-13 Single-ended I/O standards specifications for EAGLE Devices

I/O Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} Max	V_{OH} Min	I_{OL}	I_{OH}
	Min	Max	Min	Max	(V)	(V)	(mA)	(mA)
LVTTL33	-0.3	0.8	1.9	$V_{CCIO}+0.3$	0.4	V_{CCIO} -0.4	4	-4
							8	-8
							12	-12
							16	-16
							20	-20
LVCMOS25	-0.3	0.7	1.7	$V_{CCIO}+0.3$	0.4	V_{CCIO} -0.4	4	-4
							8	-8
							12	-12
							16	-16
							20	-20
LVCMOS18	-0.3	$0.35*V_{CCIO}$	$0.65*V_{CCIO}$	$V_{CCIO}+0.3$	0.4	V_{CCIO} -0.4	4	-4
							8	-8
							12	-12
LVCMOS15	-0.3	$0.35*V_{CCIO}$	$0.65*V_{CCIO}$	$V_{CCIO}+0.3$	0.4	V_{CCIO} -0.4	4	-4
							8	-8
LVCMOS12	-	$0.35*V_{CCIO}$	$0.65*V_{CCIO}$	$V_{CCIO}+0.3$	0.4	V_{CCIO} -	-3	4



I/O Standard	V _{IL} (V)		V _{IH} (V)		V _{OL} Max	V _{OH} Min	I _{OL}	I _{OH}
	Min	Max	Min	Max	(V)	(V)	(mA)	(mA)
	0. 3					0. 4	-6	8
PCI33	- 0. 3	0. 3*V _{CCIO}	0. 5*V _{CCIO}	V _{CCIO} +0. 3	0. 1*V _{CCIO}	0. 9*V _{CCIO}	1. 5	-0. 5

1. As compatible with 5V input, the maximum value of V_{IH} is 5.5V

Table 3-14 Single-ended level standard feeding relation

Input Standard	V _{CCIO} (Typ.)				
	3. 3V	2. 5 V	1. 8V	1. 5V	1. 2V
LVTTL33	√	√ ²	√ ²	√ ²	√ ²
LVCMOS33	√	√ ²	√ ²	√ ²	√ ²
LVCMOS25	√ ¹	√	√ ²	√ ²	√ ²
LVCMOS18		√ ¹	√	√ ²	√ ²
LVCMOS15			√ ¹	√	√ ²
LVCMOS12				√ ¹	√

- When input high level, if input voltage lower than requirements, high leakage current occurs
- PCI-clamp and OverDriven should turn off to avoid leakage current.

3.1.10 Differential I/O Electrical Characteristics

Table 3-15 Recommended Operational Conditions for EAGLE LVDS

Parameters	Description	Test Conditions	Min	Typical	Max	Unit
V _{IP} , V _{IN}	Input voltage	V _{CCIO} =2. 5	0	—	2. 4	V
		V _{CCIO} =3. 3	0. 45	—	3. 2	V
V _{ID}	Input differential swing	V _{IP} -V _{IN} RT = 100 Ω V _{CCIO} =3. 3/2. 5	150	350	800	mV
V _{ICM}	Input common-	V _{CCIO} =2. 5	0. 05	—	2. 35	V



Parameters	Description	Test Conditions	Min	Typical	Max	Unit
	mode voltage	$V_{CCIO}=3.3$	0.6	—	3.15	V
I_{IN}	Input current	Power-on process	—	—	± 15	uA
R_T	On-chip differential termination resistor	—	80	100	120	Ω
V_{OD}	Standard differential output swing	$ V_{OP} - V_{ON} , R_T = 100\Omega$	150	250	350	mV
V_{OD}	Differential output large swing	$ V_{OP} - V_{ON} , R_T = 100\Omega$	450	480	550	mV
ΔV_{OD}	Differential output swing deviation	—	—	—	50	mV
V_{OCM}	Output common mode voltage	$(V_{OP} + V_{ON})/2, R_T = 100\Omega$ $V_{CCIO}=2.5V$	0.6	—	1.4	V
		$(V_{OP} + V_{ON})/2, R_T = 100\Omega$ $V_{CCIO}=3.3V$	0.6	—	1.4	V
ΔV_{OCM}	Output common mode voltage deviation	—	—	—	50	mV

- When differential input swing is greater than 500mV, only external 100Ω differential resistor can be used.



Table 3-16 Recommended operational conditions for EAGLE LVPECL33

Parameters	Description	Test condition	Min	Typical	Max	Unit
V_{IP} , V_{IN}	Input Voltage	—	0	—	2.95	V
V_{ID}	Input differential swing	$ V_{IP}-V_{IN} $	100	—	1600	mV
V_{ICM}	Input common mode voltage	—	0.3	—	2.9	V

1. LVPECL receiver can only use external 100Ω resistor

3.2 AC Electrical Characteristics

This chapter provides EAGLE core and periphery blocks performance characteristics. The timing parameters and its typical value are important for general design. These parameters reflect the actual performance of devices on the worst conditions.

3.2.1 Clock Performance

Table 3-17 Recommended Maximum Clock Operation Frequency

Device	Speed	Unit
EAGLEA_10	440	MHz
EAGLEA_20	440	MHz

3.2.2 PLL Specifications

Table 3-18 PLL Specifications for EAGLE Devices

Parameter	Description	Min	Typical	Max	Unit
f_{IN}	Input clock frequency	10	—	400	MHz
f_{PFD}	Phase Frequency Detector (PFD) input frequency	10	—	400	MHz
f_{VCO}	PLL internal oscillator frequency range	300	—	1200	MHz
f_{OUT}	Output clock frequency	—	—	400	MHz
AC Characteristic					
t_{IN_H}	Input clock high level duration (90% to 90%)	0.5	—	—	ns
t_{IN_L}	Input clock low level duration (10% to 10%)	0.5	—	—	ns
f_{INDUTY}	Duty cycle for clock input	40	—	60	%
f_{RISE}	Input clock rising edge slope	1	—	3	V/ns
f_{FALL}	Input clock falling edge slope	1	—	3	V/ns



$t_{INJITTER}^1$	Input clock jitter, $f_{PFD} \geq 20$ MHz	—	—	800	ps p-p
	Input clock jitter, $f_{PFD} < 20$ MHz	—	—	0.02	UI
$t_{OUTDUTY}$	Duty cycle for clock output	45	50	55	%
$t_{OUTJITTER}^2$	Output clock period jitter, $f_{OUT} > 100$ MHz, $f_{VCO} > 400$ Mhz	—	—	160	ps p-p
	Output clock cycle-to-cycle jitter, $f_{OUT} > 100$ MHz, $f_{VCO} > 400$ Mhz	—	—	200	ps p-p
	Output clock Phase Jitter, $f_{OUT} > 100$ MHz, $f_{VCO} > 400$ Mhz	—	—	180	ps p-p
t_{LOCK}^3	PLL lock time	—	—	15	ms
t_{DLOCK}	Dynamic locked time (After switch and reset)	—	—	15	ms
t_{PLL_PS}	Accuracy of PLL phase	—	—	\pm 125	ps
t_{RST}	Minimum reset pulse width	1	—	—	ns
t_{RSTREC}	Recovery time for reset	1	—	—	ns
$t_{CONFIGPLL}$	Time required to dynamically configure for PLL phase	—	3.5	—	cycles
$f_{SCANCLK}$	SCANCLK frequency	—	—	100	MHz

1. The allowed maximum input jitter of reference clock. To have the output clock with low jitter, you must provide a quality reference clock. PLL cannot filter low-frequency noise. PLL filters parts of high-frequency input noise.
2. Period jitter is tested through sampling PLL output for 10,000 times. Cycle-to-cycle jitter through sampling PLL output for 1,000 times. Phase shift jitter through sampling PLL output for 2,000 times. Reference clock jitter 30ps.
3. After t_{LOCK} , have a stable clock at output.

3.2.3 Embedded DSP Specifications

Table 3-19 EAGLE Embedded DSP Specifications

Mode	Performance	Unit
M9×9 (All registers)	350	MHz
M18×18 (All registers)	350	MHz

3.2.4 Memory Block (ERAM) Specifications

Table 3-20 EAGLE Memory Block Specifications

Memory	Mode	Performance	Unit
M9K	FIFO 512 × 18	220	MHz
	Single port 512 × 18	220	MHz
	Simple dual-port 512 × 18	220	MHz
	True dual-port 1024 × 9	220	MHz

3.2.5 High-speed I/O Interface Performance

Table 3-21 High-speed I/O Interface Performance

I/O Standard	Description	Max	Unit
Maximum Input Frequency			
LVDS25	LVDS, VCCIO = 2.5V	400	MHz
LVDS33	LVDS, VCCIO = 3.3V	400	MHz
LVPECL33	LVPECL, VCCIO = 3.3V	400	MHz
LVTTL33	LVTTL, VCCIO = 3.3V	166	MHz
LVCMOS33	LVCMOS, VCCIO = 3.3V	166	MHz
LVCMOS25	LVCMOS, VCCIO = 2.5V	166	MHz
LVCMOS18	LVCMOS, VCCIO = 1.8V	166	MHz
LVCMOS15	LVCMOS, VCCIO = 1.5V	166	MHz



LVCMOS12	LVCMOS, VCCIO = 1.2V	166	MHz
PCI33		133	MHz
Maximum Output Frequency			
LVDS25	LVDS, VCCIO = 2.5V	400	MHz
LVDS33	LVDS, VCCIO = 3.3V	400	MHz
LVDS25E	LVDS, Emulated, VCCIO = 2.5V	166	MHz
LVPECL33E	LVPECL, Emulated, VCCIO = 3.3V	166	MHz
LVTTL33	LVTTL, VCCIO = 3.3V	166	MHz
LVCMOS33	LVCMOS, VCCIO = 3.3V	166	MHz
LVCMOS25	LVCMOS, VCCIO = 2.5V	166	MHz
LVCMOS18	LVCMOS, VCCIO = 1.8V	166	MHz
LVCMOS15	LVCMOS, VCCIO = 1.5V	166	MHz
LVCMOS12	LVCMOS, VCCIO = 1.2V	100	MHz
PCI33		133	MHz

3.2.6 Configuration Block and JTAG Specifications

Table 3-22 EAGLE Devices Configuration Mode Timing Specifications

Download Mode	Min	Typ	Max	Unit
Master Serial PROM (MS)	2.5	—	24	MHz
Master Serial (MS) SPI (MSPI)	2.5	—	16	MHz
Master Parallel (MP) x8	2.5	—	24	MHz
Slave Serial (SS)	—	—	30	MHz
Slave Parallel (SP) x8	—	—	30	MHz

Note:

1. In master loading mode, EG4 device maximum loading frequency should take OSC accuracy deviation into consideration. EG4 OSC central frequency is 290MHz, the maximum deviation should $\pm 30\%$.

3.2.7 ADC Performance

Table 3-23 ADC Performance

Parameters	Performance
Operational voltage	3.3V Analog Voltage (VDDA) and 3.3V Digital Voltage (VDDD)
ADC Reference voltage (VREF)	0.5~1.0xVDDA
Maximum sampling rate	1MHz
Channel number	8
Sampling range	0.1*VREF ~ 0.9*VREF
ADC output digital width	12 bits
ADC accuracy	8 bits
Dynamic performance	>50dB SFDR >45dB SINAD
Linearity performance	INL<1 LSB, DNL<1 LSB (8bits accuracy)
Maximum clock frequency	16MHz

1. ADC accuracy is highly dependent on reference voltage. You must provide a specific and reliable VREF, and the accuracy should be controlled within VDDA +/-0.2%.
2. The acceptable range of VREF is 0.5x VDDA~1.0x VDDA. As input signal range also be decided by VREF, to get a wider input signal range, set VREF as 1.0x VDDA by suggestion.
3. When using ADC, you should avoid using digital I/O of ADC I/O same BANK to reduce noise interruption.

4 Pin and Package

4.1 Pin Definition and Rules

Table 4-1 Pin Definition and Rule

Pin Name	Direction	Description
General Purpose I/O		
NC	—	No connection
GND	—	Ground
VCC	—	Voltage supply for core
VCCIOx	—	Voltage supply for I/O Bank
VCCAUX	—	Auxiliary voltage
VCC_PLLX	—	PLL voltage
GND_PLLx	—	PLL Ground
JTAG Dedicated pin		
TCK	Input	TCK input boundary scan clock
TDI	Input	Boundary scan data input
TDO	Output	Boundary scan data output
TMS	Input	Boundary scan mode select
Dedicated pin for configuration		
CSN ¹	Input	chipselect signal, low active
CSI_B ²	Input	Parallel mode chipselect signal, low active
MSEL[2:0] ¹ /M[1:0] ²	Input	Download mode selection
PROGRAMN	Input	Global reset input, low active
CCLK	I/O	Dedicated configuration pin
DONE	I/O	Dedicated configuration status pin, output high after configuration

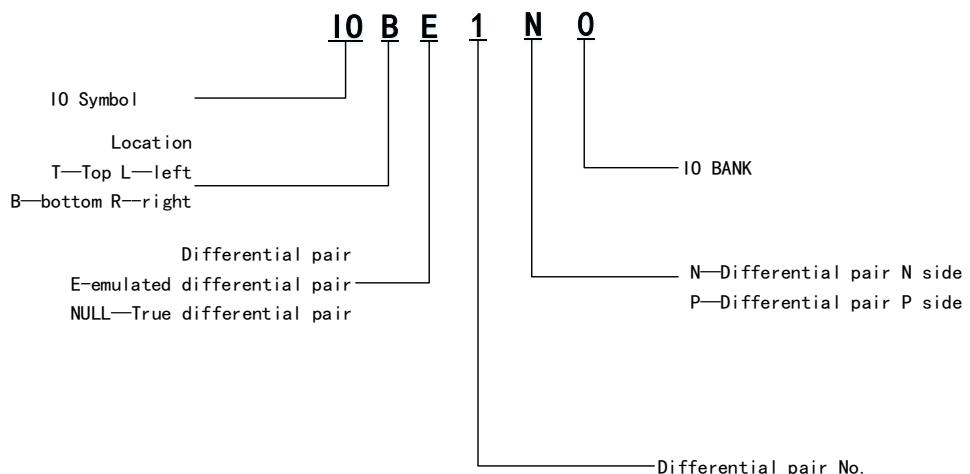


INITN	I/O	Dedicated configuration pin, output high indicates FPGA configuration ready
SPICSN ¹ /CSO_B ²	Input	MSPI mode Flash chipselect pin
MISO	Input	MSPI mode data input pin
ADC Functional pin		
ADC_CHx	Input	ADC analog signal input
ADC_VREF	Input	ADC reference voltage
ADC_VDDA	Input	ADC analog voltage
ADC_VDDD	Input	ADC digital voltage

Note:

1. CSN, SPICSN, MSEL [2:0] pins are used for EG4A20BG256 configuration.
2. CSI_B, CSO_B, M [1:0] pins are used for EG4X20BG256, EG4A20NG88, EG4X20LG144 configuration.

4.2 IO Naming Rule



4.3 EG4X20BG256 Pin Description¹

No.	BANK	EG4X20BG256	No.	BANK	EG4X20BG256
C4	0	IO_BE1P_HSWAPEN_0	F9	0	IO_BE15P_0
A4	0	IO_BE1N_VREF_0	D9	0	IO_BE15N_0
B5	0	IO_BE2P_0	B12	0	IO_BE16P_0
A5	0	IO_BE2N_0	A12	0	IO_BE16N_VREF_0
D5	0	IO_BE3P_GPLL3_OUTP_0	C13	0	IO_BE17P_0
C5	0	IO_BE3N_GPLL3_OUTN_0	A13	0	IO_BE17N_0
B6	0	IO_BE4P_0	F10	0	IO_BE18P_0
A6	0	IO_BE4N_0	E11	0	IO_BE18N_0
F7	0	IO_BE5P_0	B14	0	IO_BE19P_GPLL0_CLKIN0_0
E6	0	IO_BE5N_0	A14	0	IO_BE19N_GPLL0_CLKIN1_0
C7	0	IO_BE6P_0	D11	0	IO_BE20P_GPLL0_OUTP_0
A7	0	IO_BE6N_0	D12	0	IO_BE20N_GPLL0_OUTN_0
D6	0	IO_BE7P_0			
C6	0	IO_BE7N_0			
B8	0	IO_BE8P_0			
A8	0	IO_BE8N_0			
C9	0	IO_BE9P_GCLK10B_7_0			
A9	0	IO_BE9N_GCLK10B_6_0			
B10	0	IO_BE10P_GCLK10B_5_0			
A10	0	IO_BE10N_GCLK10B_4_0			
E7	0	IO_BE11P_GCLK10B_3_0			
E8	0	IO_BE11N_GCLK10B_2_0			
E10	0	IO_BE12P_GCLK10B_1_0			
C10	0	IO_BE12N_GCLK10B_0_0			
D8	0	IO_BE13P_0			
C8	0	IO_BE13N_VREF_0			
C11	0	IO_BE14P_0			
A11	0	IO_BE14N_0			



No.	BANK	EG4X20BG256	No.	BANK	EG4X20BG256
E13	1	I0_L1P_1	K14	1	I0_L14N_GCLK10L_4_1
E12	1	I0_L1N_VREF_1	K12	1	I0_L15P_GCLK10L_3_1
B15	1	I0_L2P_1	K11	1	I0_L15N_GCLK10L_2_1
B16	1	I0_L2N_1	J14	1	I0_L16P_GCLK10L_1_1
F12	1	I0_L3P_1	J16	1	I0_L16N_GCLK10L_0_1
G11	1	I0_L3N_1	K15	1	I0_L17P_1
D14	1	I0_L4P_1	K16	1	I0_L17N_1
D16	1	I0_L4N_1	N14	1	I0_L18P_1
F13	1	I0_L5P_1	N16	1	I0_L18N_1
F14	1	I0_L5N_1	M15	1	I0_L19P_1
C15	1	I0_L6P_1	M16	1	I0_L19N_1
C16	1	I0_L6N_1	L14	1	I0_L20P_1
E15	1	I0_L7P_1	L16	1	I0_L20N_1
E16	1	I0_L7N_1	P15	1	I0_L21P_1
F15	1	I0_L8P_1	P16	1	I0_L21N_1
F16	1	I0_L8N_1	R15	1	I0_L22P_1
G14	1	I0_L9P_1	R16	1	I0_L22N_1
G16	1	I0_L9N_1	R14	1	I0_L23P_1
H15	1	I0_L10P_1	T15	1	I0_L23N_1
H16	1	I0_L10N_1	T14	1	I0_L24P_1
G12	1	I0_L11P_1	T13	1	I0_L24N_1
H11	1	I0_L11N_1	R12	1	I0_L25P_1
H13	1	I0_L12P_1	T12	1	I0_L25N_1
H14	1	I0_L12N_1	L12	1	I0_L26P_1
J11	1	I0_L13P_GCLK10L_7_1	L13	1	I0_L26N_VREF_1
J12	1	I0_L13N_GCLK10L_6_1	M13	1	I0_L0_1
J13	1	I0_L14P_GCLK10L_5_1	M14	1	I0_DOUT_1



No.	BANK	EG4X20BG256	No.	BANK	EG4X20BG256
R11	2	IO_CCLK_2	R5	2	IO_TE14P_D7_2
T11	2	IO_M0_2	T5	2	IO_TE14N_VREF_2
M12	2	IO_TE2P_GPLL1_CLKIN0_ADC_CH4_2	N5	2	IO_TE15P_D3_2
M11	2	IO_TE2N_GPLL1_CLKIN1_ADC_CH7_2	P5	2	IO_TE15N_D4_2
P10	2	IO_DO_DIN_MISO_2	L8	2	IO_TE16P_D5_2
T10	2	IO_MOSI_CS1_B_2	L7	2	IO_TE16N_D6_2
N12	2	IO_TE4P_ADC_CH5_D1_2	P4	2	IO_TE17P_2
P12	2	IO_TE4N_ADC_CH6_D2_2	T4	2	IO_TE17N_2
N11	2	IO_TE5P_M1_ADC_CH0_2	M6	2	IO_TE18P_2
P11	2	IO_TE5N_ADC_CH2_VERF_2	N6	2	IO_TE18N_2
N9	2	IO_TE6P_2	R3	2	IO_INIT_B_2
P9	2	IO_TE6N_2	T3	2	IO_CS0_B_2
L10	2	IO_TE7P_ADC_CH1_2			
M10	2	IO_TE7N_ADC_CH3_2			
R9	2	IO_TE8P_2			
T9	2	IO_TE8N_2			
M9	2	IO_TE9P_GCLK10T_3_2			
N8	2	IO_TE9N_GCLK10T_2_2			
P8	2	IO_TE10P_GCLK10T_1_2			
T8	2	IO_TE10N_GCLK10T_0_2			
P7	2	IO_TE11P_GCLK10T_7_2			
M7	2	IO_TE11N_GCLK10T_6_2			
R7	2	IO_TE12P_GCLK10T_5_2			
T7	2	IO_TE12N_GCLK10T_4_2			
P6	2	IO_TE13P_2			
T6	2	IO_TE13N_2			



No.	BANK	EG4X20BG256	No.	BANK	EG4X20BG256
M4	3	IO_R1P_3	H5	3	IO_R14N_GCLKIOR_2_3
M3	3	IO_R1N_VREF_3	H4	3	IO_R15P_GCLKIOR_1_3
M5	3	IO_R2P_3	H3	3	IO_R15N_GCLKIOR_0_3
N4	3	IO_R2N_3	L4	3	IO_R16P_3
R2	3	IO_R3P_GPLL2_CLKIN0_3	L5	3	IO_R16N_3
R1	3	IO_R3N_GPLL2_CLKIN1_3	E2	3	IO_R17P_3
P2	3	IO_R4P_3	E1	3	IO_R17N_3
P1	3	IO_R4N_3	K5	3	IO_R18P_3
N3	3	IO_R5P_3	K6	3	IO_R18N_3
N1	3	IO_R5N_3	C3	3	IO_R19P_3
M2	3	IO_R6P_3	C2	3	IO_R19N_3
M1	3	IO_R6N_3	D3	3	IO_R20P_3
L3	3	IO_R7P_3	D1	3	IO_R20N_3
L1	3	IO_R7N_3	C1	3	IO_R21P_3
K2	3	IO_R8P_3	B1	3	IO_R21N_3
K1	3	IO_R8N_3	G6	3	IO_R22P_3
J3	3	IO_R9P_3	G5	3	IO_R22N_3
J1	3	IO_R9N_3	B2	3	IO_R23P_3
H2	3	IO_R10P_3	A2	3	IO_R23N_3
H1	3	IO_R10N_3	F4	3	IO_R24P_3
G3	3	IO_R11P_3	F3	3	IO_R24N_3
G1	3	IO_R11N_3	E4	3	IO_R25P_3
F2	3	IO_R12P_GCLKIOR_7_3	E3	3	IO_R25N_3
F1	3	IO_R12N_GCLKIOR_6_3	F6	3	IO_R26P_3
K3	3	IO_R13P_GCLKIOR_5_3	F5	3	IO_R26N_3
J4	3	IO_R13N_GCLKIOR_4_3	B3	3	IO_R27P_3
J6	3	IO_R14P_GCLKIOR_3_3	A3	3	IO_R27N_3



No.	BANK	EG4X20BG256	No.	BANK	EG4X20BG256
P13	1	IO_DONE_1	L9	-	VCCAUX
T2	2	IO_PROGRAM_B_2	G7	-	VCCINT
P14	1	IO_L1_1	G9	-	VCCINT
C14	0	IO_TCK_0	H10	-	VCCINT
C12	0	IO_TDI_0	H8	-	VCCINT
E14	1	IO_TDO_1	J7	-	VCCINT
A15	1	IO_TMS_1	J9	-	VCCINT
L11	2	ADC_VREF	K10	-	VCCINT
B13	-	VCCO_0	K8	-	VCCINT
B4	-	VCCO_0	A1	-	GND
B9	-	VCCO_0	A16	-	GND
D10	-	VCCO_0	B11	-	GND
D7	-	VCCO_0	B7	-	GND
D15	-	VCCO_1	D13	-	GND
G13	-	VCCO_1	D4	-	GND
J15	-	VCCO_1	E9	-	GND
K13	-	VCCO_1	G15	-	GND
N15	-	VCCO_1	G2	-	GND
R13	-	ADC_VDDA	G8	-	GND
N10	-	VCCO_2	H12	-	GND
N7	-	VCCO_2	H7	-	GND
R4	-	VCCO_2	H9	-	GND
R8	-	VCCO_2	J5	-	GND
D2	-	VCCO_3	J8	-	GND
G4	-	VCCO_3	K7	-	GND
J2	-	VCCO_3	K9	-	GND
K4	-	VCCO_3	L15	-	GND
N2	-	VCCO_3	L2	-	GND
E5	-	VCCAUX	M8	-	GND
F11	-	VCCAUX	N13	-	GND



No.	BANK	EG4X20BG256	No.	BANK	EG4X20BG256
F8	-	VCCAUX	P3	-	GND
G10	-	VCCAUX	R10	-	GND
H6	-	VCCAUX	R6	-	GND
J10	-	VCCAUX	T1	-	GND
L6	-	VCCAUX	T16	-	GND

Note:

1. ADC_VDDD is fixedly connected to VCCIO2 on chip, when using ADC, the voltage supply for BANK2 should not lower than that of ADC analog voltage.

4.4 EG4A20BG256 Pin Description¹

No.	BANK	EG4A20BG256	No.	BANK	EG4A20BG256
D4	1	IO_L1P_1	M2	2	IO_L1P_GCLKIOL_5_2
B1	1	IO_L1N_1	M1	2	IO_L1N_GCLKIOL_4_2
C1	1	IO_L5_1, MOSI, D1	J1	2	IO_L2N_GCLKIOL_6_2
C2	1	IO_L1_1	J2	2	IO_L2P_GCLKIOL_7_2
E5	1	IO_L3P_1	K1	2	IO_L3N_2
F5	1	IO_L3N_1	K2	2	IO_L3P_2
D1	1	IO_L2_1	J6	2	IO_L1_2
D2	1	IO_L4_SPICSN_1	L1	2	IO_L4N_2
G5	1	IO_L5P_1	L2	2	IO_L4P_2
G4	1	IO_L5N_1	L3	2	IO_L5N_VREF_2
F4	1	IO_L6_1, INITN	R1	2	IO_L5P_2
F3	1	IO_VREF_1	K5	2	IO_L6N_2
F2	1	IO_L7P_1	L4	2	IO_L6P_2
F1	1	IO_L7N_1	N1	2	IO_L7N_2
H3	1	IO_L8P_1, TCK	N2	2	IO_L7P_2
H4	1	IO_L8N_1, TDI	L6	2	IO_L8N_2
H5	1	IO_L9N_1, PROGRAMN	K6	2	IO_L8P_2
J5	1	IO_L9P_1, TMS	N4	2	IO_L2_2
H2	1	IO_L3_1, MISO, D0	P2	2	IO_L9P_2
H1	1	IO_L8_1, CCLK	P1	2	IO_L9N_2
J3	1	IO_L11N_1, CSN			
J4	1	IO_L11P_1, TDO			
G2	1	IO_L12P_GCLKIOL_3_1			
G1	1	IO_L12N_GCLKIOL_2_1			
E1	1	IO_L7_GCLKIOL_0_1			



No.	BANK	EG4A20BG256	No.	BANK	EG4A20BG256
P3	3	I0_BE1N_GPLL0_CLKIN1_3	R8	4	I0_BE1P_GCLK1OB_7_4
N3	3	I0_BE1P_GPLL0_CLKIN0_3	T8	4	I0_BE1N_GCLK1OB_6_4
M6	3	I0_BE2P_3	T9	4	I0_BE2N_GCLK1OB_2_4
L7	3	I0_BE2N_3	R9	4	I0_BE2P_GCLK1OB_3_4
P6	3	I0_BE3N_3	R10	4	I0_BE3P_4
T2	3	I0_BE3P_3	T10	4	I0_BE3N_4
R3	3	I0_BE4P_3	P9	4	I0_BE4N_4
T3	3	I0_BE4N_3	P11	4	I0_BE4P_4
T4	3	I0_BE5N_GPLL0_OUTN_3	M9	4	I0_BE5P_4
R4	3	I0_BE5P_GPLL0_OUTP_3	N9	4	I0_BE5N_4
N6	3	I0_BE6N_3	L9	4	I0_BE6N_4
N5	3	I0_BE6P_3	K9	4	I0_BE6P_4
R5	3	I0_BE7P_3	T11	4	I0_BE7N_4
T5	3	I0_BE7N_3	R11	4	I0_BE7P_4
T6	3	I0_BE8N_3	M10	4	I0_BE8P_4
R6	3	I0_BE8P_3	N11	4	I0_BE8N_4
R7	3	I0_BE9P_3	L10	4	I0_BE9N_4
T7	3	I0_BE9N_3	K10	4	I0_BE9P_4
K8	3	I0_BE10N_3	T12	4	I0_BE10N_GPLL3_OUTN_4
M7	3	I0_BE10P_3	R12	4	I0_BE10P_GPLL3_OUTP_4
N8	3	I0_BE11P_GCLK1OB_1_3	R13	4	I0_BE11P_4
P8	3	I0_BE11N_GCLK1OB_0_3	T13	4	I0_BE11N_4
M8	3	I0_BE12N_GCLK1OB_4_3	N12	4	I0_BE12N_4
L8	3	I0_BE12P_GCLK1OB_5_3	M11	4	I0_BE12P_4
			T14	4	I0_BE13P_4
			T15	4	I0_BE13N_4
			L11	4	I0_BE14N_4
			P14	4	I0_BE14P_4



No.	BANK	EG4A20BG256	No.	BANK	EG4A20BG256
R14	5	I0_R1N_GPLL3_CLKIN1_5	H15	6	I0_R1P_GCLKIOR_3_6
P15	5	I0_R1P_GPLL3_CLKIN0_5	H16	6	I0_R1N_GCLKIOR_2_6
R16	5	I0_R2P_5	E16	6	I0_R2N_GCLKIOR_4_6
P16	5	I0_R2N_5	E15	6	I0_R2P_GCLKIOR_5_6
N13	5	I0_R3P_5	G15	6	I0_R3P_6
N14	5	I0_R3N_5	G16	6	I0_R3N_6
N15	5	I0_R4P_5	H13	6	I0_R4_MSEL0_6
N16	5	I0_R4N_5	H14	6	I0_R5_6, DONE
M12	5	I0_R5P_5	G12	6	I0_R5P_MSEL2_6
L12	5	I0_R5N_5	H12	6	I0_R5N_MSEL1_6
L13	5	I0_R6P_5	F15	6	I0_R1_6, USRCLK
L14	5	I0_R6N_5	F16	6	I0_R3_6, CS0N, DOUT
L15	5	I0_R7P_5	F13	6	I0_R7P_6
L16	5	I0_R7N_5	G11	6	I0_R7N_6
K15	5	I0_R8P_5	D16	6	I0_R8N_6
K16	5	I0_R8N_5	D15	6	I0_R8P_6
J11	5	I0_R9P_5	C16	6	I0_R9N_6
K11	5	I0_R9N_5	C15	6	I0_R9P_6
K12	5	I0_R10P_5	B16	6	I0_R10N_6
J13	5	I0_R10N_5	F14	6	I0_R10P_VREF_6
J12	5	I0_R11P_5	D13	6	I0_R2_6
J14	5	I0_R11N_5	A15	6	I0_R11P_GPLL2_CLKIN0_6
J15	5	I0_R12P_GCLKIOR_7_5	F11	6	I0_R11N_GPLL2_CLKIN1_6
J16	5	I0_R12N_GCLKIOR_6_5			
M16	5	I0_R13N_GCLKIOR_0_5			
M15	5	I0_R13P_GCLKIOR_1_5			



No.	BANK	EG4A20BG256	No.	BANK	EG4A20BG256
D14	7	I0_TE1P_7	A9	7	I0_TE14N_GCLKIOT_6_7
C14	7	I0_TE1N_7	A8	7	I0_TE15N_GCLKIOT_4_7
A14	7	I0_TE2N_GPLL2_OUTN_7	B8	7	I0_TE15P_GCLKIOT_5_7
B14	7	I0_TE2P_GPLL2_OUTP_7	B6	7	I0_TE16P_GCLKIOT_1_7
B13	7	I0_TE3P_7	A6	7	I0_TE16N_GCLKIOT_0_7
A13	7	I0_TE3N_7	E8	7	I0_TE17N_GCLKIOT_2_7, D2
D11	7	I0_TE4N_7	F8	7	I0_TE17P_GCLKIOT_3_7, D3
D12	7	I0_TE4P_7	A5	8	I0_TE1P_8, D7
B12	7	I0_TE5P_7	C6	8	I0_TE1N_8
A12	7	I0_TE5N_7	E7	8	I0_TE2N_8, D5
C11	7	I0_TE6P_VREF_7	E6	8	I0_TE2P_8, D6
E11	7	I0_TE6N_7	D6	8	I0_TE3P_8
A11	7	I0_TE7N_7	D5	8	I0_TE3N_8
B11	7	I0_TE7P_7	F6	8	I0_TE4N_GPLL1_OUTN_8
B10	7	I0_TE8P_7	F7	8	I0_TE4P_GPLL1_OUTP_8
A10	7	I0_TE8N_7	B4	8	I0_TE5P_ADC_CH1_8
F10	7	I0_TE9N_7	A4	8	I0_TE5N_ADC_CH3_8
F9	7	I0_TE9P_7	A3	8	I0_TE6N_ADC_CH2_8
E10	7	I0_TE10P_7	B3	8	I0_TE6P_ADC_CHO_8
E9	7	I0_TE10N_7	E2	8	ADC_VREF
C9	7	I0_TE11N_7	B5	8	I0_TE7P_ADC_CH5_8
D9	7	I0_TE11P_7	A2	8	I0_TE7N_ADC_CH7_8
B7	7	I0_TE12P_7, D4	C3	8	I0_TE8N_GPLL1_CLKIN1_ADC_CH6_8
A7	7	I0_TE12N_7	D3	8	I0_TE8P_GPLL1_CLKIN0_ADC_CH4_8
C8	7	I0_TE13N_7			
D8	7	I0_TE13P_7			
B9	7	I0_TE14P_GCLKIOT_7_7			



No.	BANK	EG4A20BG256	No.	BANK	EG4A20BG256
B2	-	GND	F12	-	VCCAUX
B15	-	GND	L5	-	VCCAUX
C12	-	GND	G6	-	VCCINT
D7	-	ADC_VSSA	G7	-	VCCINT
D10	-	GND	G8	-	VCCINT
E4	-	GND	G9	-	VCCINT
E13	-	GND	G10	-	VCCINT
G13	-	GND	H6	-	VCCINT
H7	-	GND	H11	-	VCCINT
H8	-	GND	K7		VCCINT
H9	-	GND	E3	-	VCCI01
H10	-	GND	G3	-	VCCI01
J7	-	GND	K3	-	VCCI02
J8	-	GND	M3	-	VCCI02
J9	-	GND	P4	-	VCCI03
J10	-	GND	P7	-	VCCI03
K4	-	GND	T1	-	VCCI03
K13	-	GND	P10	-	VCCI04
M4	-	GND	P13	-	VCCI04
N7	-	GND	T16	-	VCCI04
N10	-	GND	K14	-	VCCI05
P5	-	GND	M14	-	VCCI05
P12	-	GND	E14	-	VCCI06
R2	-	GND	G14	-	VCCI06
R15	-	GND	A16	-	VCCI07
M5	-	GND_PLLA0	C10	-	VCCI07
E12	-	GND_PLLA2	C13	-	VCCI07
C5		GND_PLLA1	C4	-	VCCI08
M13		GND_PLLA3	C7	-	VCCI08
	-		A1	-	ADC_VDDA

Note:

- ADC_VDDD is fixedly connected to VCCI08, when using ADC, the voltage for



BANK8 should not be lower than that of ADC analog voltage.



4.5 EG4A20NG88 Pin Description¹

No.	BANK	EG4A20NG88	No.	BANK	EG4A20NG88
1	-	VCC	23	3	IO_B1_3
2	1	IO_L1_1	24	3	VCCI03
3	1	IO_L2_1	25	3	IO_B2_3, TDI
4	1	IO_L1N_1	26	3	IO_B3_3, TCK
5	1	IO_L1P_1	27	3	IO_B4_3
6	1	GND	28	3	IO_BE1N_3
7	1	VCCI01	29	3	IO_BE1P_3
8	1	IO_L3_1, DONE	30	3	IO_B5_3
9	1	VCCI01	31	3	IO_B6_3
10	1	IO_L2P_1, GCLK10L_3	32	3	IO_BE2P_3
11	1	IO_L2N_1, GCLK10L_2	33	3	IO_BE2N_3
12	2	IO_L2P_2, GCLK10L_5	34	3	IO_B7_3, GCLK10B_5
13	2	IO_L2N_2, GCLK10L_4	35	4	IO_B1_4, GCLK10B_2
14	2	IO_L5_2	36	-	VCC
15	2	VCCI02	37	4	IO_BE1P_4
16	2	IO_L1N_2	38	4	IO_BE1N_4
17	2	IO_L1P_2	39	4	IO_B2_4
18	2	IO_L1_2	40	4	IO_BE2N_4
19	2	IO_L2_2	41	4	IO_BE2P_4
20	2	VCCI02	42	4	IO_B3_4
21	2	IO_L3_2, TDO	43	4	VCCI04
22	2	IO_L4_2, TMS	44	4	IO_B4_4, HSWAPEN

Note:

1. EG4A20NG88 VCC indicates internal core voltage, which symbolizes same function with other devices' VCCINT.



No.	BANK	EG4A20NG88	No.	BANK	EG4A20NG88
45	5	IO_R1_5	67	7	IO_T1_7, PROGRAM_B
46	5	VCCI05	68	7	IO_T2_7, INIT_N
47	5	IO_R1P_5	69	7	IO_T3_7, CS0_B
48	5	IO_R1N_5	70	7	IO_TE1P_7, D3
49	5	IO_R2P_5	71	7	IO_TE1N_7, D4
50	5	IO_R2N_5	72	7	IO_T4_7, D7
51	5	IO_R2_5	73	7	VCCI07
52	5	IO_R3_5	74	7	IO_TE2N_7, D6
53	5	VCCI05	75	7	IO_T5_7, GCLK10T_7
54	5	IO_R3N_5, GCLK10R_0	76	7	IO_TE2P_7, D5
55	5	IO_R3P_5, GCLK10R_1	77	7	IO_TE3N_7, GCLK10T_4
56	-	VCC	78	7	IO_TE3P_7, GCLK10T_5
57	6	IO_R1_6, GCLK10R_4	79	7	IO_T6_7, GCLK10B_0
58	6	VCCI06	80	8	IO_T1_8, DO_DIN_MISO
59	6	IO_R2_6	81	8	IO_T2_8, MOSI_CSI_B
60	6	IO_R1N_6	82	8	IO_T3_8, CCLK
61	6	IO_R1P_6	83	8	IO_T4_8, M0
62	6	IO_R3_6	84	8	IO_T5_8, M1
63	6	IO_R2N_6	85	8	VCCI08
64	6	IO_R2P_6	86	8	IO_TE1P_8, D1
65	6	VCCI06	87	8	IO_TE1N_8, D2
66	6	IO_R4_6	88	-	VCCAUX
			89	-	GND_EPAD

4.6 EG4X20LG144 Pin Description

No.	BANK	EG4X20LG144	No.	BANK	EG4X20LG144
8	1	IO_L0_1	44	3	IO_B0_3
18	1	IO_L1P_1, GCLK10L_3	50	3	IO_BE1P_3
19	1	IO_L1N_1, GCLK10L_2	51	3	IO_BE1N_3
21	1	IO_L2P_1, GCLK10L_1	53	3	IO_BE2P_3, GCLK10B_1
20	1	IO_L2N_1, GCLK10L_0	54	3	IO_BE2N_3, GCLK10B_0
12	1	IO_L3P_1	56	3	IO_BE3P_3, GCLK10B_5
13	1	IO_L3N_1	55	3	IO_BE3N_3, GCLK10B_4
15	1	IO_L4P_1	41	3	IO_BE4P_3, GPLLO_CLKIN0
14	1	IO_L4N_1, DOUT	40	3	IO_BE4N_3, GPLLO_CLKIN1
10	1	IO_L5P_1, DONE	42	3	IO_BE5P_3, TDI
11	1	IO_L5N_1	43	3	IO_BE5N_3, TCK
7	1	IO_L6P_1	46	3	IO_BE6P_3, GPLLO_OUTP
6	1	IO_L6N_1	45	3	IO_BE6N_3, GPLLO_OUTN
3	1	IO_L7P_1	49	3	IO_BE7P_3
4	1	IO_L7N_1	48	3	IO_BE7N_3, VREF0_2
5	1	IO_L8_1	47	3	IO_B8_3
29	2	IO_L0_2	57	4	IO_B0_4, GCLK10B_6
30	2	IO_L1P_2	59	4	IO_BE1P_4, GCLK10B_3
31	2	IO_L1N_2, VREF1_0	58	4	IO_BE1N_4, GCLK10B_2
28	2	IO_L2P_2	62	4	IO_BE2P_4
27	2	IO_L2N_2	63	4	IO_BE2N_4
25	2	IO_L3P_2	66	4	IO_BE3P_4, GPLL3_OUTP
24	2	IO_L3N_2	65	4	IO_BE3N_4, GPLL3_OUTN
34	2	IO_L4P_2, TDO	64	4	IO_B4_4
35	2	IO_L4N_2, TMS	67	4	IO_B5_4
22	2	IO_L5P_2, GCLK10L_5	72	4	IO_B6_4, HSWAPEN
23	2	IO_L5N_2, GCLK10L_4	71	4	IO_B7_4, VREF0_0



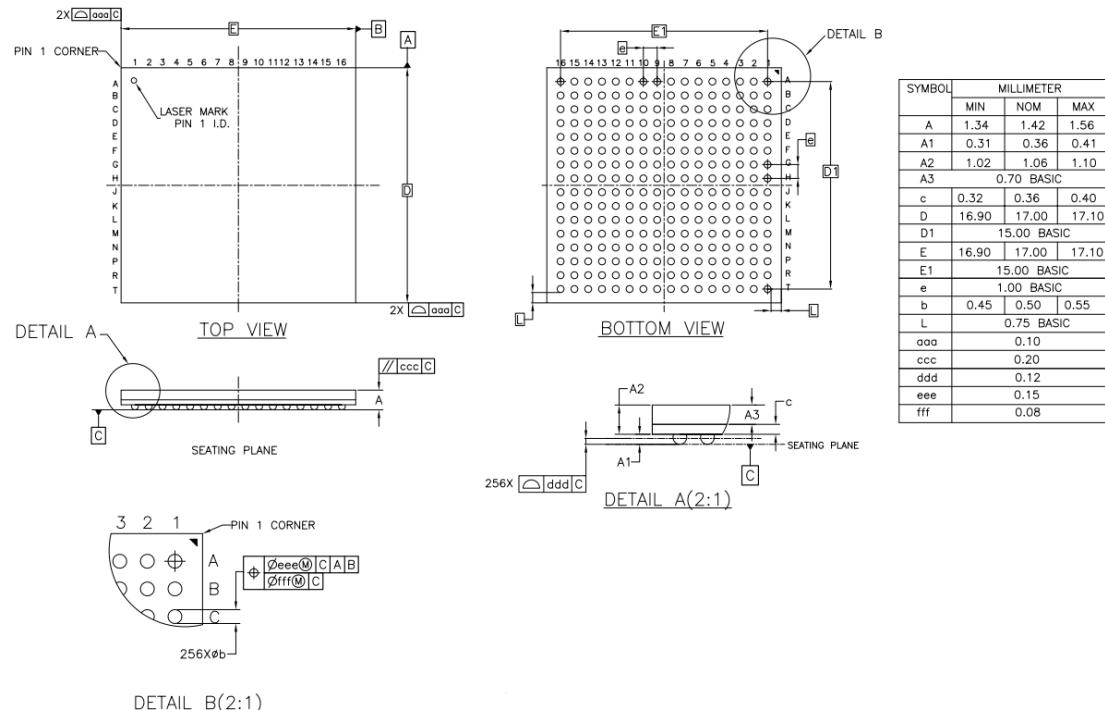
No.	BANK	EG4X20LG144	No.	BANK	EG4X20LG144
77	5	I0_R0P_5	128	7	I0_TE0P_7, GCLKIOT_1
78	5	I0_R0N_5	129	7	I0_TE0N_7, GCLKIOT_0
79	5	I0_R1P_5	127	7	I0_TE1P_7, GCLKIOT_5
80	5	I0_R1N_5	126	7	I0_TE1N_7, GCLKIOT_4
81	5	I0_R2P_5	124	7	I0_TE2P_7, GCLKIOT_7
82	5	I0_R2N_5	125	7	I0_TE2N_7, GCLKIOT_6
84	5	I0_R3P_5	123	7	I0_TE3P_7, D5
83	5	I0_R3N_5	122	7	I0_TE3N_7, D6
75	5	I0_R4P_5, GPLL3_CLKIN0	117	7	I0_TE4P_7, D7
74	5	I0_R4N_5, GPLL3_CLKIN1	118	7	I0_TE4N_7, VREF2_1
88	5	I0_R5P_5, GCLKI0R_1	115	7	I0_TE5P_7, D3
87	5	I0_R5N_5, GCLKI0R_0	116	7	I0_TE5N_7, D4
106	6	I0_R0_6	113	7	I0_TE6P_7, INIT_B
93	6	I0_R1P_6, GCLKI0R_5	114	7	I0_TE6N_7, CS0_B
92	6	I0_R1N_6, GCLKI0R_4	109	7	I0_TE7P_7
90	6	I0_R2P_6, GCLKI0R_3	110	7	I0_TE7N_7, PROGRAM_B
91	6	I0_R2N_6, GCLKI0R_2	137	8	I0_T0_8, M1
97	6	I0_R3P_6	142	8	I0_TE1P_8, GPLL1_CLKIN0
96	6	I0_R3N_6	143	8	I0_TE1N_8, GPLL1_CLKIN1
99	6	I0_R4P_6	140	8	I0_TE2P_8, D1
98	6	I0_R4N_6	141	8	I0_TE2N_8, D2
102	6	I0_R5P_6	135	8	I0_TE3P_8, CCLK
103	6	I0_R5N_6	136	8	I0_TE3N_8, M0
100	6	I0_R6P_6	132	8	I0_TE4P_8, DO_DIN_MISO
101	6	I0_R6N_6	133	8	I0_TE4N_8, MOSI_CSI_B
107	6	I0_R7P_6, GPLL2_CLKIN0	134	8	I0_T5_8
108	6	I0_R7N_6, GPLL2_CLKIN1			



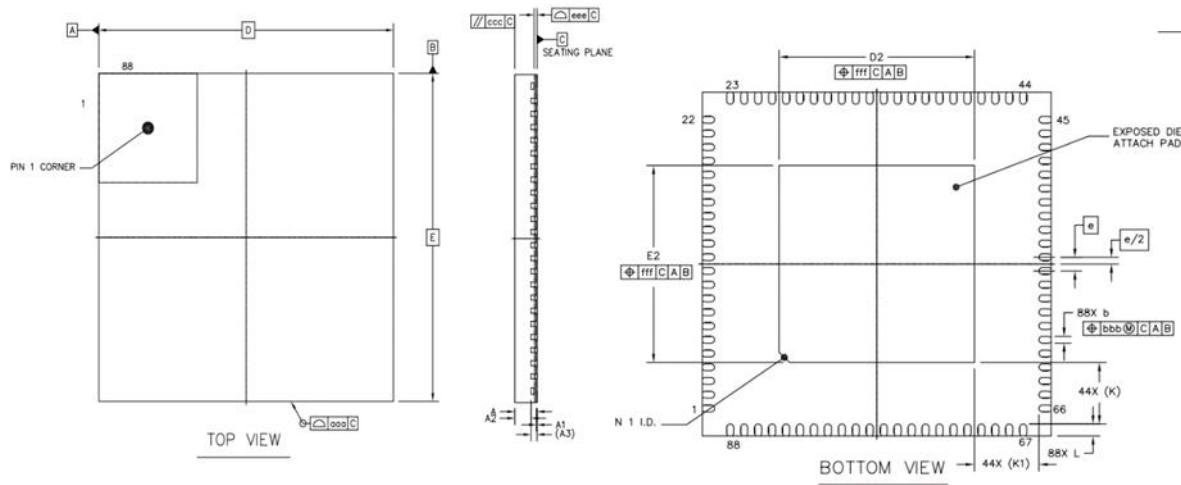
No.	BANK	EG4X20LG144	No.	BANK	EG4X20LG144
2	-	VCCINT	9	1	VCCI01
36	-	VCCINT	16	1	VCCI01
61	-	VCCINT	26	2	VCCI02
73	-	VCCINT	32	2	VCCI02
89	-	VCCINT	39	3	VCCI03
111	-	VCCINT	52	3	VCCI03
37	-	VCCAUX	68	4	VCCI04
70	-	VCCAUX	76	5	VCCI05
121	-	VCCAUX	86	5	VCCI05
144	-	VCCAUX	94	6	VCCI06
1	-	GND	104	6	VCCI06
17	-	GND	119	7	VCCI07
33	-	GND	130	7	VCCI07
38	-	GND	139	8	VCCI08
60	-	GND			
69	-	GND			
85	-	GND			
95	-	GND			
105	-	GND			
112	-	GND			
120	-	GND			
131	-	GND			
138	-	GND			

4.7 Package Information

4.7.1 BG256 Package Specifications

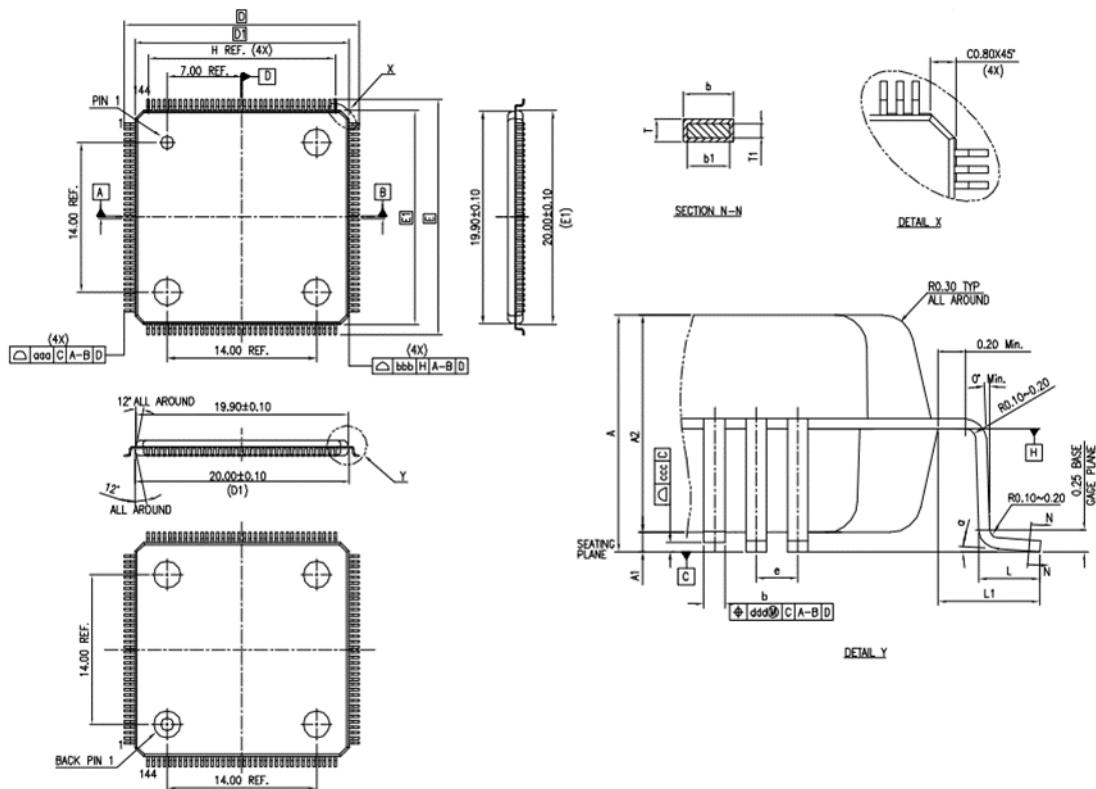


4.7.2 NG88 Package Specification



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.7	0.75	0.8
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.55	---
L/F THICKNESS	A3		0.203 REF	
LEAD WIDTH	b	0.15	0.2	0.25
BODY SIZE	X	D	10 BSC	
	Y	E	10 BSC	
LEAD PITCH	e		0.4 BSC	
EP SIZE	X	D2	5.5	5.6
	Y	E2	5.63	5.73
LEAD LENGTH	L	0.25	0.35	0.45
LEAD TIP TO EXPOSED PAD EDGE	K		1.785 REF	
	K1		1.85 REF	
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	ccc		0.1	
COPLANARITY	eee		0.08	
LEAD OFFSET	bbb		0.07	
EXPOSED PAD OFFSET	fff		0.1	

4.7.3 LG144 Package Specification



DIMENSION LIST (FOOTPRINT: 2.00)

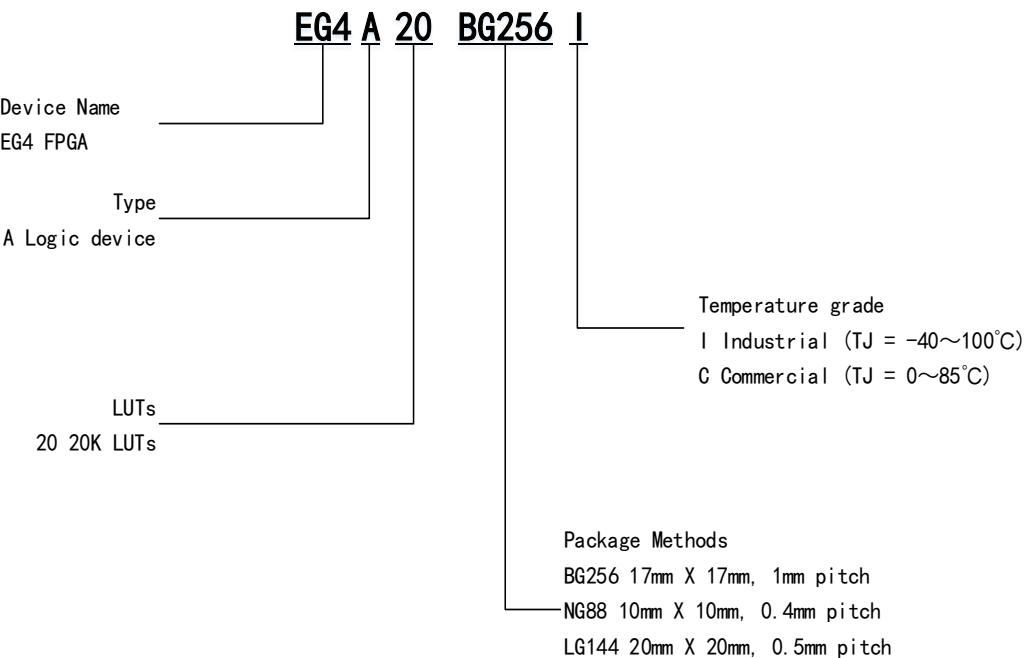
S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.60	OVERALL HEIGHT
2	A1	0.10±0.05	STANDOFF
3	A2	1.40±0.05	PKG THICKNESS
4	D	22.00±0.20	LEAD TIP TO TIP
5	D1	20.00±0.10	PKG LENGTH
6	E	22.00±0.20	LEAD TIP TO TIP
7	E1	20.00±0.10	PKG WIDTH
8	L	0.60±0.15	FOOT LENGTH
9	L1	1.00 REF.	LEAD LENGTH
10	T	$0.15^{+0.05}_{-0.06}$	LEAD THICKNESS
11	T1	0.127±0.03	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.22±0.05	LEAD WIDTH
14	b1	0.20±0.03	LEAD BASE METAL WIDTH
15	e	0.50 BASE	LEAD PITCH
16	H (REF.)	(17.50)	CUM. LEAD PITCH
17	ooo	0.20	PROFILE OF LEAD TIPS
18	bbb	0.20	PROFILE OF MOLD SURFACE
19	ccc	0.08	FOOT COPLANARITY
20	ddd	0.08	FOOT POSITION

5 Ordering Information

Table 5-1 Device Abbreviation

Device Name	Type	LUTs	Package type	Temperature grade
EG4	A	20	BG256	-

- Device Family
 - ✧ EAGLE family
- Type
 - ✧ A Type A 10 array
 - ✧ X Type X 10 array
- LUTs
 - ✧ 20 20K LUTs
- Package Type: <Type><#>
 - ✧ BG FBGA
 - ✧ NG QFN
 - ✧ LG LQFP
 - ✧ # Pin number (256 refers to 256 pins)
- Temperature grade
 - ✧ C Commercial ($T_J = 0 - 85^\circ\text{C}$)
 - ✧ I Industrial ($T_J = -40 - 100^\circ\text{C}$)



Note

1. This device silk printed without temperature symbol, such as EG4A20BG256, EG4X20BG256, EG4X20LG144 are industrial, the other are all commercial.
2. The symbol of "I", "I7" and "I8" on inner box indicate the same type of symbol.



Revision History

Date	Version	Changes
2024/6/26	3. 9. 4	<ol style="list-style-type: none">1. Delete #NHP on Table 4-1, add MISO2. Update EG4X20BG256, EG4A20BG256, EG4A20NG88 and EG4X20LG144 pin descriptions.3. Delete Bypass configuration mode relevant description.4. Update JTAG relevant parameters and timing sequence of Table 2-28 and Figure 2-795. Add USRCLK and note 4 on Table 2-296. Update temperature grade on chapter 5, add note 2
2024/2/22	3. 9. 3	<ol style="list-style-type: none">1. Add OSC accuracy note under Table 3-222. Add test condition on Table 3-15 and Table 3-163. Update chapter 4. 5, EG4A20NG88 pin information4. Add JTAG configuration mode switch to user mode restrictions on chapter 2. 8. 85. Add LVDS33 voltage standard performance on Table 3-216. Update NG88 package specifications
2023/9/10	3. 9. 2	<ol style="list-style-type: none">1. Add note in chapter 5
2023/08/01	3. 9. 1	<ol style="list-style-type: none">1. Delete device EAGLE_10 on chapter 1. 12. Add package LQFP144 on Table 1-2; add EG4X20LG144 on chapter 2. 8; update package on chapter 53. Update chapter 2. 8 configuration mode relevant table, figure name. update CS0_B pin description4. Add EG4X20LG144 does not support ADC function on chapter 2. 95. Add Table 3-76. Update hot socketing restriction on device EG4X20LG1447. Update configuration dedicated pins on Table 4-1Add note after Table 4-18. Add chapter 4. 69. Add chapter 4. 7. 3 LG144 package specification
2023/06/15	3. 9	<ol style="list-style-type: none">1. Add device EG4A20NG88, Update section 1. 1; add package type QFN88 and modify package type 256ftBGA



		<p>to 256FBGA; update package type in section 5.</p> <ol style="list-style-type: none">2. Update description about dynamic phase shift; Update Table 2-15 and Table 2-163. Update Table 2-314. Update section 2.95. Add Table 3-66. Add note 4 after Table 3-97. Add section 4.58. Add package specification on section 09. Add “#NHP” pin description on Table 4-1
2023/05/23	3. 8. 9	<ol style="list-style-type: none">1. Update Figure 2-30 and Table 2-142. Update section 2.8.143. Update Table 2-29 Table 2-30 name and relevant notes4. Update Table 3-15. Update Table 3-36. Update Table 3-87. Add Vccint on Table 3-4 Table 3-58. Update section 4.49. Update Table 2-910. Update port name “wbyte_ena” to “bytewea” , “wbyte_enb” to “byteweb” on Table 2-2-12 and Figure 2-22,11. Update package type to FBGA in section 112. Update Table 1-1 Table 1-213. Add description about chip internal resistance is 20 ohms. Update Figure 2-6114. Update Table 3-22



		<ol style="list-style-type: none">15. Update section 4.316. Update section 4.5.117. Update package type in section 518. Update Table 2-1319. Modify signal multi_bootn=0 to rebootn=0
2022/10/13	3.8.8	<ol style="list-style-type: none">1. Update Table 3-32. Update Table 2-283. Update Table 2-26 and Table 2-254. Update Table 2-295. Update Table 2-306. Update Table 3-137. Update Table 3-58. Update disclaimer



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