

### Homework 3

Questions are equal weights

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#### **Question 1**

Instruction	Clock Cycles																	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
LD R1, 0(R2)	IF	ID	EX	M	W													
DADDI R1, R1, #1																		
SD 0(R2), R1																		
DADDI R2, R2, #4																		
DSUB R4, R3, R2																		
BNEZ R4, Loop																		

Complete the above timing sequence.

A. Assume no forwarding unit

B. assume forwarding unit

## **Question 2**

Suppose that in 1000 memory references there are 40 misses in the first-level cache and 20 misses in the second-level cache.

Assume the miss penalty from the L2 cache to memory is 200 clock cycles, the hit time of the L2 cache is 10 clock cycles, the hit time of L1 is 1 clock cycle. What is the average memory access time.