# Simulation of Electrical Circuit in Semiconductor Design Process using Xschem and Ngspice

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# **ACTIVITY DETAILS**

## I. Background

In semiconductor device design process, many tools and software are used to make the circuit design and verify its behavior extensively. The software, especially the one used for simulation, is useful to verify the design before it goes to layout process and fabrication, since mistakes in circuit level may render the fabricated silicon unusable and, therefore, useless. It is important that the designer is able to use and understand their software and tools completely, in order to produce a functional, verified design that can be brought for further processing.

#### **II. Simulation Detail**

In this simulation, a simple inverter circuit is used for testing purposes. The circuit will be created with Xschem and run using ngspice simulation engine. The library used in this simulation is the default Xschem library and sky130 library that corresponds to Skywater 130 process used by efabless in the Tiny Tapeout program. The inverter consist of two MOSFETs, one being an N-Channel 1.8V Gate and the other is P-Channel 1.8V Gate. It is wired as in the following figure:

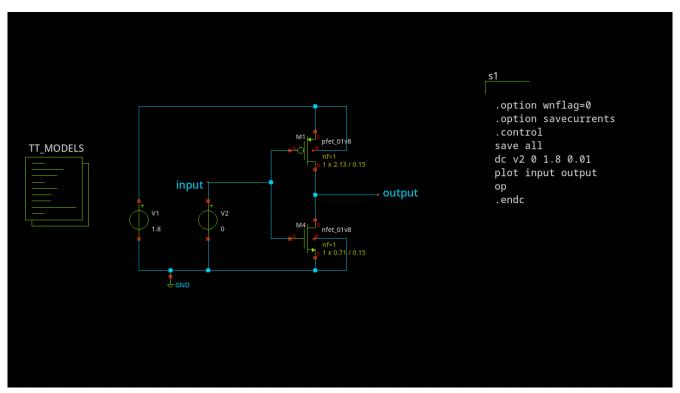


figure 1. The inverter circuit used in this simulation

A script is added in order to enable the simulation and to find the required SPICE model for the components. The simulation is a DC sweep simulation, varying source V2 voltage that connected to the MOSFETs gate pin. The voltage in "input" and "output" label is then graphed. In theory, this should allow us to find the voltage required for the transistors to be fully on. For the sake of curiosity, the simulation is also run with an entirely different transistor (the 20V gate PMOS and NMOS) with the circuit as follows:

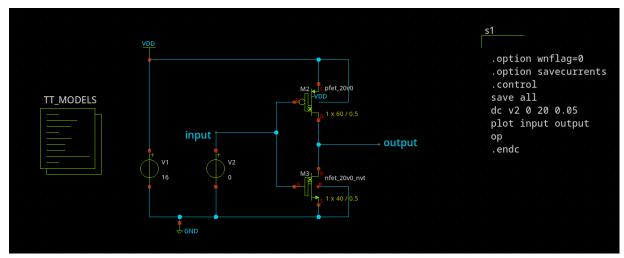


figure 4. the 20V gate MOSFET inverter circuit

The script is also slightly modified to use higher DC voltage at the MOSFETs gate pin, the cause of which will be explained later in this document.

# **SIMULATION ACTIVITY**

# **I. Simulation Results**

The result with default settings (Width = 1 micron, L = 0.15 micron) is as follows:

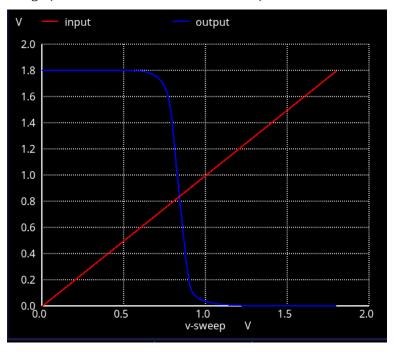


Figure 2. Result of the simulation with default transistor parameters

Changing the width of the transistor to 0.71 micron for NMOS and 2.13 micron for PMOS yield the following result :

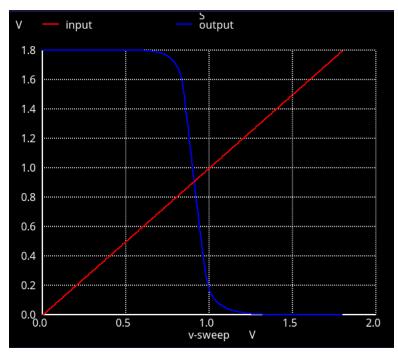


Figure 3. Result of the simulation with modified transistor parameters  $% \left( 1\right) =\left( 1\right) \left( 1\right) \left($ 

The results for inverter with 20V gate MOSFET is as follows:

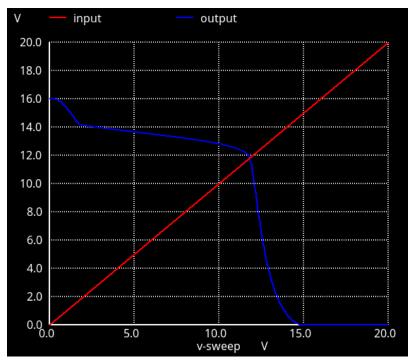


Figure 5. Simulation result with 20V gate MOSFETs

## **II. Discussion**

As seen in the simulation data section, it is observed that the inverter behaves normally, as the voltage sweep introduced at the transistor gates will gradually turn off the PMOS and turn on the NMOS transistor. There is no noticeable difference between transistor settings, as modifying the MOSFET width with last 2 digit of NRP number (which means W = 0.71 micron for NMOS and W = 3x0.71 = 2.13 for PMOS) doesn't make any meaningful change to the graph. It might be caused by the nature of MOSFET itself, which only require voltage in its gate pin in order to be turned on/off. Since the gate virtually doesn't pull any current and is isolated from source and drain, its DC steady state will become similar to a capacitor and its voltage will follow the voltage supplied to it. A different outcome might be expected when the AC analysis is used instead or the MOSFET is used to modulate/amplify an analog signal. Meanwhile, with 20V gate MOSFET, the 1.8V supplied to gates is not enough to fully turn on/off the MOSFETs. As an initial result, the simulation gave the following graph:

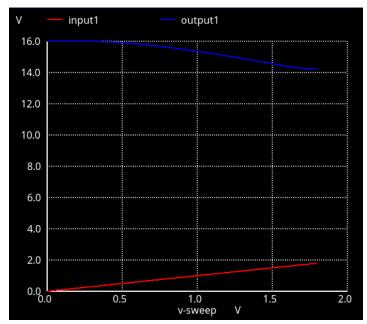


Figure 6. Simulation of 20V gate MOSFETs with 1.8V sweep voltage

The graph means that the MOSFET has begun to turn on/off, but not fully on/off. The output voltage only drop slightly which means that there's some sort of voltage divider that present before the output. By increasing the voltage sweep to 20V, the expected graph is produced, which can be seen in the data section. All of this means that the software has, and can be run smoothly. It also successfully produce the simulation data in the expected fotmat (graph). Accuracy of this simulation is, of course, depends on the SPICE model used, the simulation engine, and the simulation configuration. The file used for simulation can be accessed at <a href="https://github.com/radityankn/dsrt2024">https://github.com/radityankn/dsrt2024</a> raditya 5022211071

### **III. Conclusion**

The simulation software (namely Xschem and ngspice) has been successfully run and is able to give the expected simulation data. The simulation accuracy, however, depends on the accuracy of SPICE model used, the simulation engine itself, and the configuration of the simulation before runtime. This software can be a helpful tool to evaluate electrical design before being processed further to become a single, integrated circuit.