D20 : VoidWalkers

Post Mortem Slides

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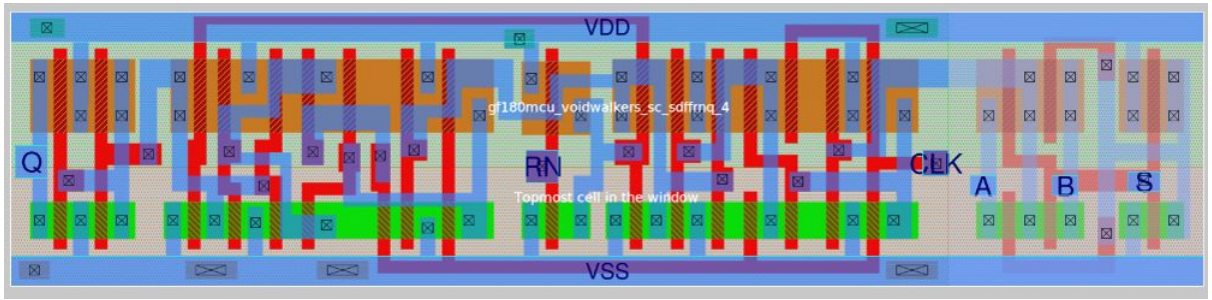
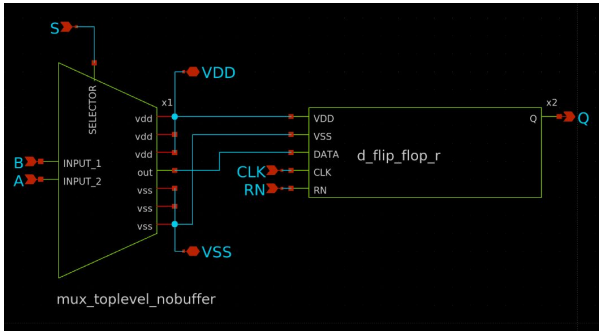
What We Build

- Scan DFF with Negative Edge Reset. we intended to build something useful but combining our (limited) expertise and aspiration
- Status : Tape Out (integrated to Digital Blocks Padframe)





What We Learned

Working :

- Hierarchical layout is a very helpful approach, though it must be done with good tools too. We did have some instance in Magic where hierarchical layout failed to be simulated whereas the flatten one run just fine 😅 (the hierarchical one is kept for guidance and conformity, at least we know it works)
- We did learned some hotkeys and pin arrangements, as well as forcing ourselves to read the NGSpice manual and figuring out how components inside spice files work
- Floorplanning and layouting needs good strategy, otherwise you'll end up with messy knots of connection in metal layer (this happened in integration phase with other teams)
- Now we know that it is surprisingly similar with PCB Design, only difference is that it is done at 180 um (much smaller than a PCB)

What We Learned

Not Working :

- Netgen LVS just freezes midway when running LVS for the whole padframe (We didn't know what's inside a padframe back then. It turned out to be more than just pads 😶)
- Charlib doesn't work for our block. We didn't dig deeper to that problem and proceed to eyeball the manual simulation for characterization (if it looks fine, proceed)
- Parasitic extraction can be improved if ext2sim and associated tools have the ability to simply change the file extension and not simply adding theirs on top of the existing file name (my_circuit.ext will be my_circuit.ext.sim, instead of my_circuit.sim)
- Our flow is largely manual process, tools work albeit with little hacks here and there, but we wish we have more time to learn about the tools to actually fixed it

Reflection / Feedback

- Most favorite part : Schematic and Design Review -> everyone gathering and presenting their layout, each with their own consideration, very different approach can be seen in undergrad vs masters and pros
- LLM? We didn’t use LLM except for consultation, and we always be wary about its output (making sure it is at least sane and reasonable). Provided tools helped immensely, and most of them working as expected
- Suggestion -> It might be better for digital teams to be able to build something useful but coordinated, mixing digital signal with traditional floorplanning, maybe trying to make an IP for RV32?

Reflection / Feedback

- Chipathon 2025 really tested our teamwork, especially across country and universities, and for 3 months with weekly pace (most of us are final year student, still doing our thesis back then and preparing for graduation, as well as job seeking, while also managing the team workload)
- It encourages exploration, knowing more about our computers and systems. W
- We wish we could understand every program we've come across that fast (fully understanding a piece of code might take us 2-3 days for python script, modifying it while not breaking other things is another matter, not mentioning if we need to learn new language like Tcl)
- We need to find motivation when working on projects like this, especially with other tight deadlines and schedule (personal projects can be postponed indefinitely, but not if it involves another person)

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LVS Result

```
Subcircuit summary:
Circuit 1: sdffrnq                      |Circuit 2: sdffrnq
----------------------------------------|----------------------------------------
pfet_03v3 (20)                          |pfet_03v3 (20)
nfet_03v3 (20)                          |nfet_03v3 (20)
Number of devices: 40                   |Number of devices: 40
Number of nets: 28                      |Number of nets: 28
----------------------------------------------------------------------------------
Netlists match uniquely.

Subcircuit pins:
Circuit 1: sdffrnq                      |Circuit 2: sdffrnq
----------------------------------------|----------------------------------------
S                                       |S
CLK                                     |CLK
A                                       |A
B                                       |B
RN                                      |RN
Q                                       |Q
VSS                                     |VSS
VDD                                     |VDD
----------------------------------------------------------------------------------
Cell pin lists are equivalent.
Device classes sdffrnq and sdffrnq are equivalent.

Final result: Circuits match uniquely.
```

- Passed LVS
- Using flattened layout because of some difficulties regarding extraction in hierarchical mode
- Command :
  - extract all
  - ext2spice lvs
  - ext2spice

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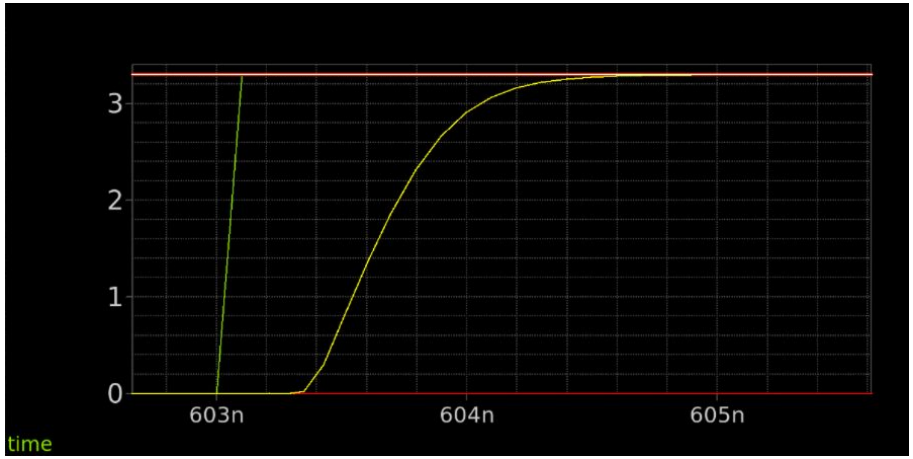
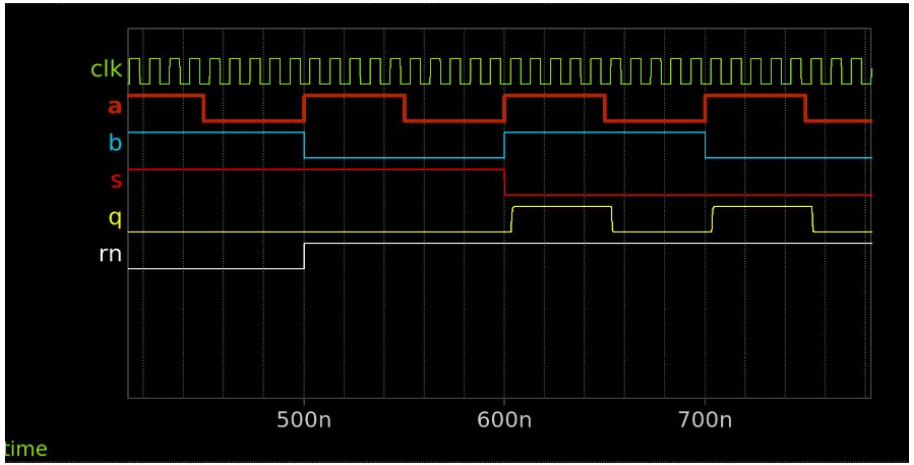
Prelayout simulation





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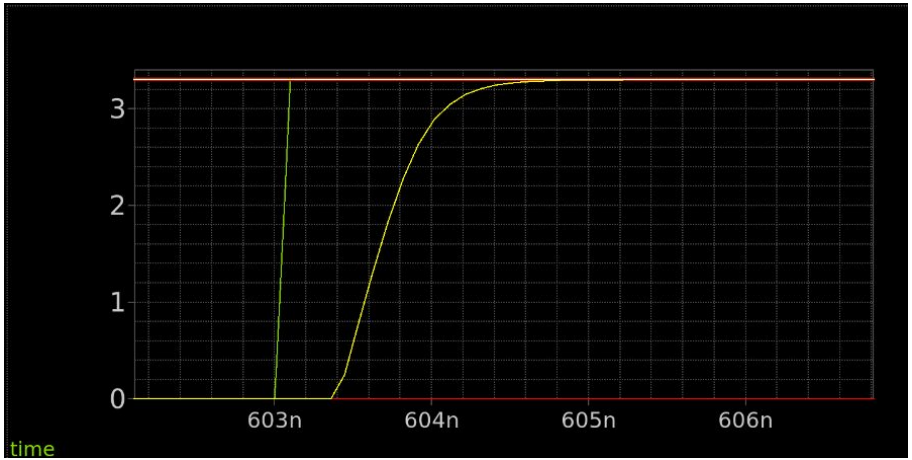
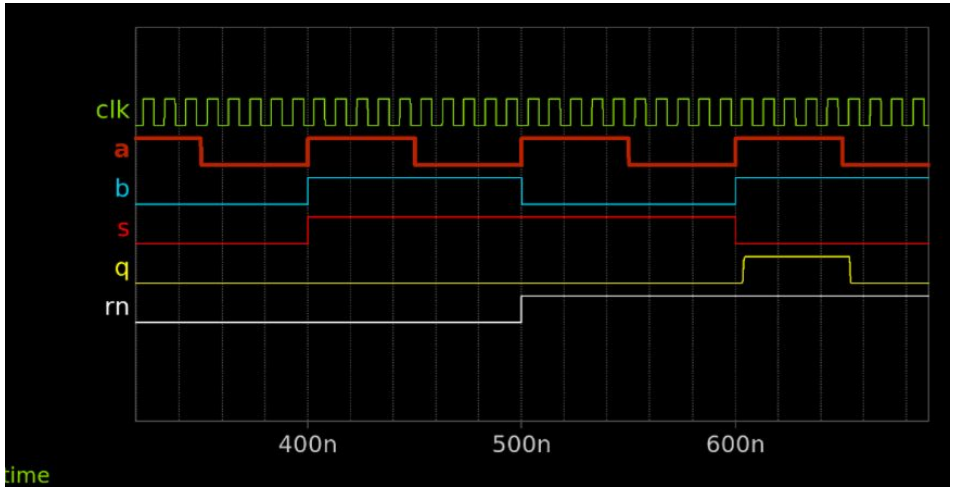
Postlayout simulation





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Progress Tracker

Weekly Progress Tracker

Task	Assigned To	Start Date	End Date	Dur	Phase Activity	Status
Team Formation & Idea	Every Member	25/06/2025	02/07/2025	7	Proposal	Complet...
Tools installation & setup	Every Member	03/07/2025	05/07/2025	2	Proposal	Complet...
Github Repo & Proposal Creation	Every Member	06/07/2025	10/07/2025	4	Proposal	Complet...
Mux 2:1 Schematic Design	Sarah	10/07/2025	24/07/2025	14	Schematic	Complet...
DFF Schematic Design	Aji	10/07/2025	24/07/2025	14	Schematic	Complet...
Mux 2:1 Schematic Simulation	Sarah	21/07/2025	30/07/2025	9	Pre-Sim	Complet...
DFF Schematic Simulation	Aji	21/07/2025	30/07/2025	9	Pre-Sim	Complet...
DFF & Mux Integration & Simulation	Every Member	30/07/2025	07/08/2025	8	Pre-Sim	Complet...
Pre-sim Charlib characterization	Every Member	08/08/2025	15/08/2025	7	Pre-Sim	Complet...
MUX and DFF Layout	Every Member	17/08/2025	30/08/2025	13	Layout	Complet...
Layout Integration	Every Member	31/08/2025	03/09/2025	3	Layout	Complet...
Post Layout Simulation	Every Member	02/09/2025	03/09/2025	1	Post-Sim	Complet...
STD Cell Characterization	Every Member	04/09/2025	12/09/2025	8	Post-Sim	In Progr...
Github Repo Documentation	Every Member	13/09/2025	15/09/2025	2	Documentation	Not Star...
		dd/mm/yyyy	dd/mm/yyyy	##		
		dd/mm/yyyy	dd/mm/yyyy	##