NATIONAL UNIVERSITY OF SINGAPORE

EG3601

INDUSTRIAL ATTACHMENT

Final-Term Report

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Acknowledgements

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1 Introduction

This report will attempt to articulate more on the interpersonal aspects of the industrial attachment. This first segment will give a brief description of the technical work done and the rest of the report will be more reflective in nature. The appendix will contain more technical concepts which apply to my project but do not fit into my main report.

2 Internship Project Progress

Over the second half of my internship, I carried on with the prototyping of the visible light communication system. The image below shows the typical communication system.

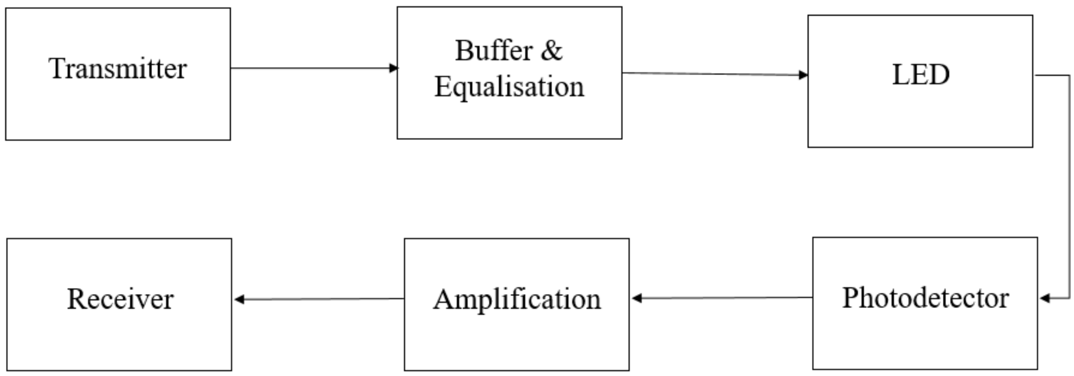

Figure 1: Communication system block diagram

At the end of the first half, I had completed the transmitter portion of the LiFi communication pathway. During the second half, my focus was geared toward the receiver portion. Once the receiver was complete, we could then build two full setups for two devices to communicate with.
For the receiver, we were following the design in this study[10], which used the Maxim 3766 limiting amplifiers and the AD8015 transimpedance amplifiers. This specific limiting amplifier allows for up to 600Mbps transfer speeds as it functioned using Positive Emitter Coupled Logic. The lower voltage level variation of that logic (0.8V) allows for faster transmission of data. However, for 10BASE-T communication standard. We had strict guidelines to follow which mandated we use voltage levels of ± 2.5V. This is vastly different from the PECL levels of 5.0V and 4.2V. The reason we had to adhere to the standard religiously is because of the autonegotiation mechanism.

2.1 Autonegotiation

We found that every ethernet driver was consistently sending out link pulses. The following is an image of said link pulses.

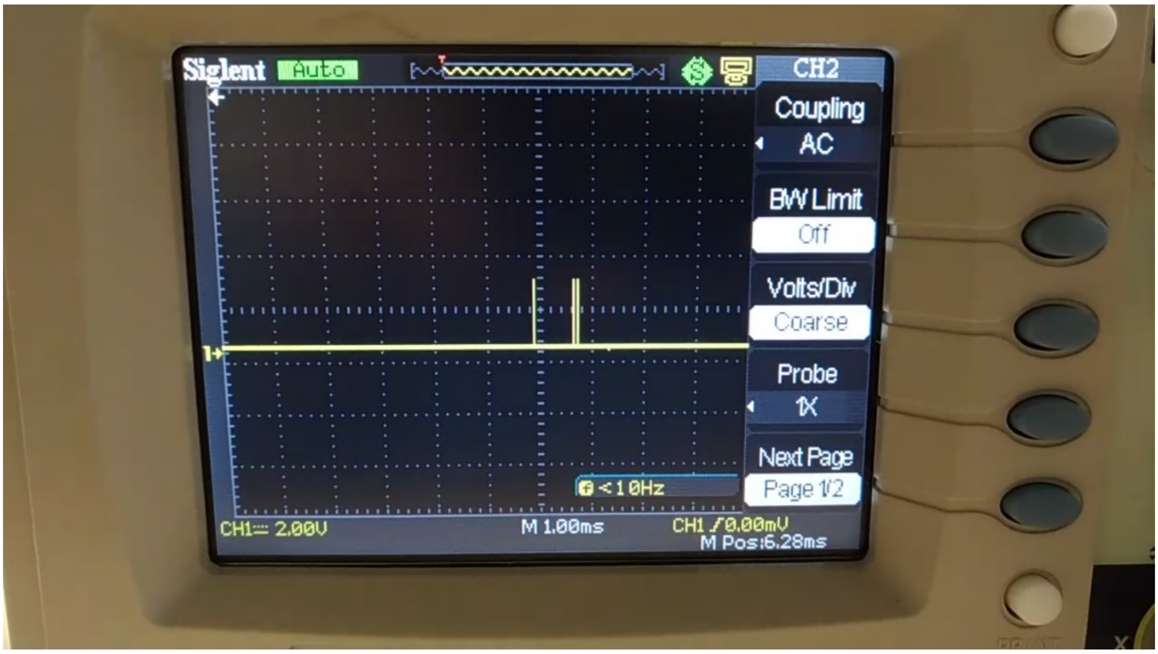

Figure 2: Link pulses from my laptop seen in an oscilloscope

The link pulses are a stream of bits which declare the capabilities of a device using the IEEE ethernet standard which allows it to negotiate a common standard with another device so successful communication can be established[14]. Regardless of whether, it is connected to another device or not, most ethernet cards are constantly sending and listening for these link pulses. Only when it receives a compatible stream, will it establish a communication channel to transmit data through. The priority for the communication standard is as follows[6]:

1. 10GBASE-T full duplex
2. 1000BASE-T full duplex
3. 1000BASE-T half duplex
4. 100BASE-T2 full duplex
5. 100BASE-TX full duplex
6. 100BASE-T2 half duplex
7. 100BASE-T4 half duplex
8. 100BASE-TX half duplex
9. 10BASE-T full duplex
10. 10BASE-T half duplex

The standard that both devices can support will be selected from the top down. Thus, the fastest standard compatible with both devices will be chosen. As we can see, we cannot use any arbitrary voltge levels to communicate. To be compatible with multiple devices, we had to adhere to the already established IEEE802.3 standard.

2.2 The Circuit

In order to be compatible with the 10BASE-T standard, we decided to use more operational amplifiers to amplify the signals from the Maxim chip to the required levels of ± 2.5V. A simulation of the circuit was done and tested to prove the concept.

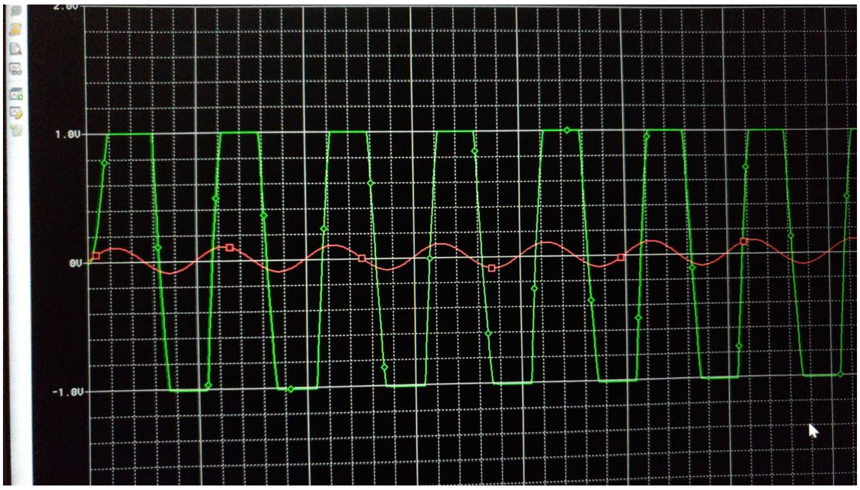

Figure 3: Simulation shows the amplification and shaping capabilities of the circuit

However, when doing breadboard testing, there was a very large amount of noise in the output signal. We realised that this could be due to poor contacts within the breadboard and poor manufacturing of breadboard (one of the breadboards had a manufacturing fault where two rails which were supposed to be independent were shorted). As a result, we decided to go ahead and design a PCB to test the circuit. The design was to be modular so that troubleshooting would be easier. We split the design into three modules:

Transimpedance Module: Convert current signal to voltage signal

Limiting Amplifier Module: Preliminary shaping of signal

Main Amplifier Module: Final amplification to $\pm$2.5V

The following shows the transimpedance module which I designed to be manufactured. I chose to use only surface-mount components as they can be smaller than through-hole components and have less noise overall[12].

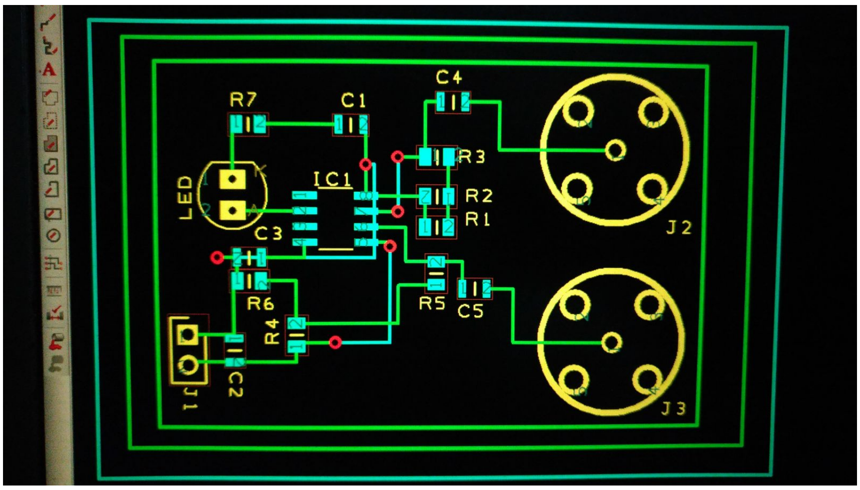

Figure 4: PCB design of Transimpedance Module

As of writing this report, the PCB is still in production.

2.3 Way Forward

At the current state, we have managed to get the transmission of basic sine and square wave signals with very low Signal-to-Noise Ratio (SNR). The way to proceed is to test with the PCBs and if successful, connect the PCB modules to RJ45 ethernet jacks and test again. After it is able to funtion with the RJ45 connectors, we can redesign the PCB into one complete transceiver module. This would allow us to minimize the size of the full circuit as we won't need the BNC connecters anymore for intermodule connectivity.

3 Challenges & Solutions

Since the start of the second half of my internship. There were quite a few unexpected hindrances to my progress. This, as my supervisor later told me, was part and parcel of research life. The main goal for me was to build a 10Mbps visible light communication system.

3.1 Procurement Delays

As of the start of the second term, the transmitter portion was complete and I was waiting for components to arrive to begin work on the receiver. We had bought limiting amplifiers which would act as the main amplification unit for our receiver. Limiting amplifiers have the characteristic of clipping the signal at the programmed voltage level. The behaviour is shown below.

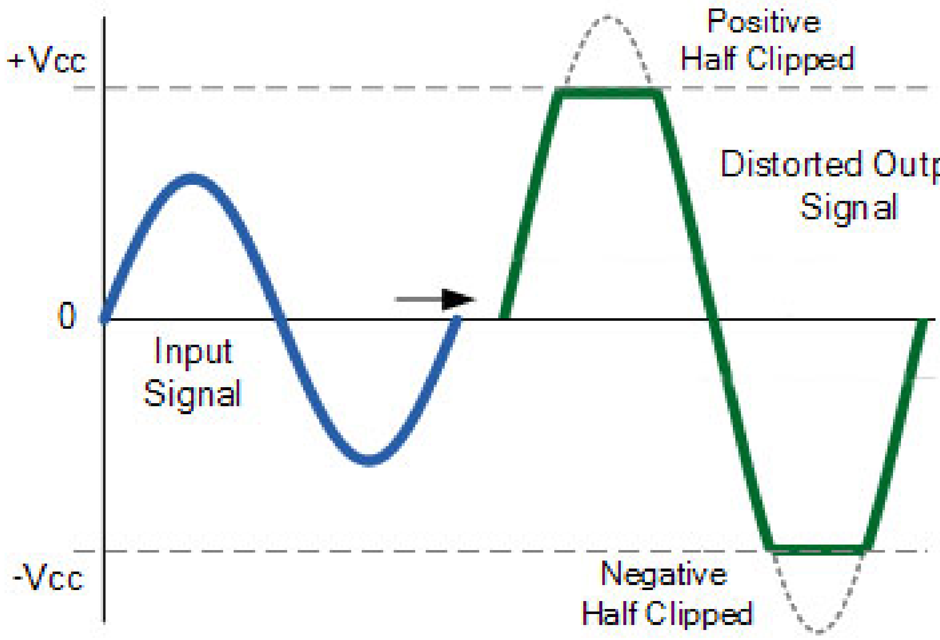

Figure 5: Limiting amplifier boosts and clips signal [3]

This special characteristic would allow us to convert the incoming signal to a nice square wave of $\pm$2.5V; which are the signal levels for 10BASE-T communication. However, when testing the limiting amplifiers, quite a few tended to be faulty. That is when I learnt the important principle of buying small components in bulk. One big setback that stemmed from long delivery times is that, in the interim period, the momentum gained is lost. Thus, important concepts become foggy and require some jogging of the memory. Since a researcher has little control over delivery times, it is his/her imperative to ensure as little time as possible is spent waiting for deliveries. This can be done by

1. Ordering components in bulk; insures against faulty components
2. Doing sufficient simulation in software before ordering; prevents ordering of incompatible or unnecessary components
3. Aggregating as many required components as possible into one order; reduces total number of orders

3.2 Lack of Expertise

Another big challenge was the fact that neither of us working on the project was experienced in analysing and designing circuits. I undertook this project in spite of that fact and was prepared to face the problems that might arise. However, because of the fact that both of us were not trained electrical engineers, we had to learn the fundamentals the hard way.

Numerous times, we would get perplexing results and we would spend hours trying to troubleshoot only to realize that the problem lay in something we had not even thought about; for example, the way in which we were probing the circuit for analysis. In school, there would always be an expert around the corner able and willing to help. However, here there was no easy solution providence. We had to learn on our own, many times having to resort to trial and error.

The good thing was that it became easier and easier the more we did it as we learned the theoretical concepts behind what gave rise to those errors. This meant that we were better-equipped with the knowledge to properly analyse the circuits and troubleshoot errors.

4 Reflection

The internship, on the whole, has been a very enjoyable and enriching experience for me. As I mentioned previously, I was thrown into the deep end as I was not familiar with the subject matter. However, I found company in the uncertainty. This uncertainty, I realized, is something that comes part and parcel with the field of research. Be it a topic in which you are already an expert, or one in which you are completely new, research is in its very nature a process of discovering the unknown. As such, my co-worker was struggling through the same struggles I was and both of us learnt through the successes and failures of one another. It has honed my skills in finding and applying relevant information. Learning how to learn is the one most important takeaway from this experience. After consistently dwelling in uncertainty, I emerge, feeling more certain in my own capabilities.

I have learnt through this internship that working together may The internship has answered numerous questions and at the same time brought up many more to be answered. I have learnt more about the research sector in Singapore and have experienced the working life in the sector but I still have ways to go before I can decide on my preferred field.

This experience has been a great starting point as it exposed me to numerous areas which have truly captivated my interests and inspired me to take action. Feeling motivated to learn more, I am confident that I have taken steps in the right direction.

Whatever project or employment opportunity awaits me, I am sure that I am now much better equipped to rise to the challenge.

5 A*STAR

As its name suggests, the agencyFLs mission is to advance scientific knowledge and technology.It was founded in 1991 as the National Science and Technology Board (NSTB) and is a statutory board under the Ministry of Trade and Industry. The organisation follows a hierarchical structure and is stratified as shown in the following image.

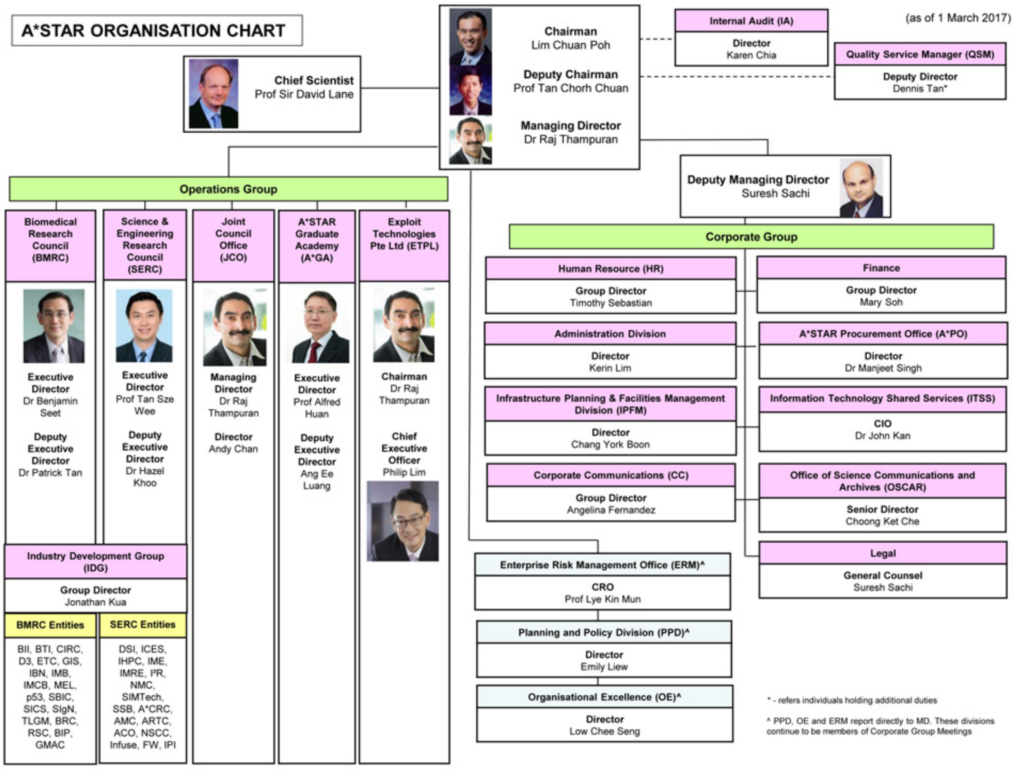

Figure 6: A*STAR Organisational Chart as of Mar 2017 [2]

As evident above, the agencyFLs operations group consists of 5 divisions. Two of them, BMRC and SERC, form the research wing dealing with the biomedical science and the physical sciences and engineering fields respectively. They are further divided into smaller institutes, each specialising in different areas. My workplace is in one of these institutes from SERC called the Institute for Materials Research and Engineering (IMRE).

The Joint Council Office is in charge of collaborating research between A*STAR and other organisations. This includes organisations based outside of Singapore.

A*STAR Graduate Academy (A*GA) is in charge of identifying and nurturing scientifically talented individuals through scholarships and youth outreach programs. They give scholarships for every level of tertiary education and also sponsor overseas study. They ensure A*STAR always has a new pool of talented researchers to take the reign.

ETPL is the commercialisation arm at A*STAR. It deals with patenting and licensing the research done by the agency. This generates additional revenue for A*STAR to fund its numerous projects. In recent times, ETPL has been gearing towards product co-development instead of just gap funding for start-ups. Thus, instead of just providing technology for start-ups and SMEs, ETPL is intent on nurturing them so that they don't fail. The following illustration shows the change in direction followed by ETPL.

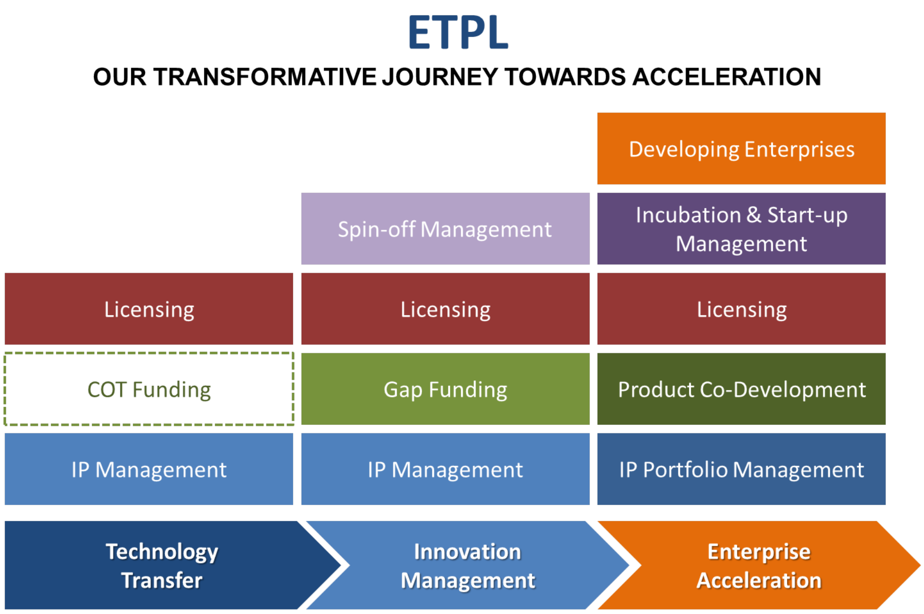

Figure 7: ETPL progression towards enterprise management [1]

A*STAR mostly conducts problem-solving for the numerous industries in Singapore. My project itself was part of a project for the Aerospace sector. The reason for this trend is that Scientists have to source external funding for their research topics and in the process usually end up having to take up projects which benefit the investors. Given that A*STAR is a government funded institution, it is usually the first resort for problem-solving in government run organisations. One downside to this is that research topics which do not have immediate applications and rewards do not receive the funding to proceed. As a result, the local research scene will not be at the forefront of science and technology.

6 Possible Career Paths

At this point after the internship, I still feel very uncertain as to what I actually want to pursue as a career. I am very inclined towards working in the science and technology sector as I really like learning and enjoyed the work experience during my attachment with A*STAR. If I were to narrow down the work opportunities as a *research engineer* in fields I like, I would look at the following research institutes[13].

A*STAR

Institute of High Performance Computing: Deals with research, development and application of modelling, simulation and visualisation techniques

Institute for Infocomm Research: Deals with communication technology research (very similar to my internship project)

Singapore Institute of Manufacturing Technology: Research includes numerous manufacturing methods and technology to aid in them

Institute of Bioengineering and Nanotechnology: Deals with nanotechnology applications in medicine

CREATE

Singapore-MIT Alliance for Research and Technology Centre (SMART): MIT's research centre in Singapore. Deals in multiple areas; Future Mobility would be my main interest

TUM-CREATE Centre on Electromobility in Megacities: Deals with future transport systems

There are also many opportunities available in universities to work in research related positions.

References

[1] A*STAR. *ETPL (Commercialisation and Technology Transfer)*. 2017. URL: https://www.a-star.edu.sg/About-A-STAR/ETPL-Commercialisation-and-Technology-Transfer.aspx (visited on 04/16/2017).

[2] A*STAR. *Organisation Structure*. 2017. URL: https://www.a-star.edu.sg/About-A-STAR/Corporate-Profile/Organisation-Structure.aspx (visited on 04/16/2017).

[3] MTX Audio. *Clipped Signal*. 2017. URL: http://international.mtx.com/ (visited on 04/16/2017).

[4] Lloyd Butler. *Waveform Analysis*. 1989. URL: http://users.tpg.com.au/users/ldbutler/Waveforms.htm (visited on 04/16/2017).

[5] Engineers Garage. *Difference between AM and FM*. 2016. URL: https://www.engineersgarage.com/contribution/difference-between-am-and-fm-modulation (visited on 04/16/2017).

[6] IEEE. *IEEE Std 802.3-2002 - 8023.pdf*. 2017. URL: http://people.ee.duke.edu/~mbrooke/EE164.02/Spring_2004/group_2/index_files/8023.pdf (visited on 07/22/2017).

[7] Alan Kaminsky. *Digital Signal Analysis*. Rochester Institute of Technology, 2014.

[8] Pulse Research Lab. *NECL/PECL FAQs – Pulse Research Lab*. 2017. URL: https://www.pulseresearchlab.com/pages/necl-pecl-faqs (visited on 07/22/2017).

[9] Ralf Neuhaus. "A Beginner's Guide to Ethernet 802.3". In: *Engineer-to-Engineer Note EE-269-Analog Devices* (2005).

[10] Rupak Paudel et al. "Investigation of FSO ground-to-train communications in a laboratory environment". In: *Internet (AH-ICI), 2011 Second Asian Himalayas International Conference on*. IEEE. 2011, pp. 1–5.

[11] Paolo Prandoni and Martin Vetterli. *Digital Signal Processing*. École Polytechnique Fédérale de Lausanne, 2017.

[12] JR Reed. *Through-Hole vs. Surface Mount*. 2017. URL: http://blog.optimumdesign.com/through-hole-vs-surface-mount (visited on 07/22/2017).

[13] SNAS. *Research*. 2017. URL: https://snas.org.sg/research/ (visited on 07/22/2017).

[14] Wikipedia. *Autonegotiation - Wikipedia*. 2017. URL: https://en.wikipedia.org/wiki/Autonegotiation (visited on 07/22/2017).

[15] Wikipedia. *Quadrature amplitude modulation - Wikipedia*. 2017. URL: https://en.wikipedia.org/wiki/Quadrature_amplitude_modulation (visited on 04/16/2017).

Appendices

A ECL, PECL, LVPECL

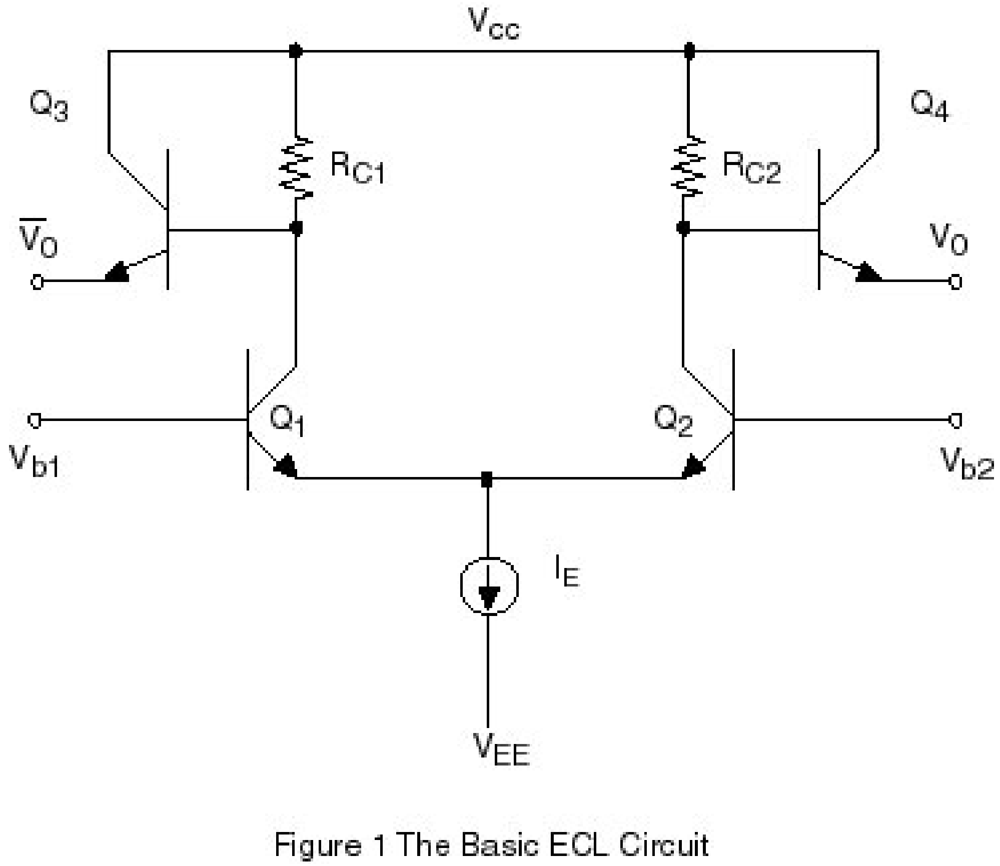

Figure 8: A basic ECL circuit [8]

ECL stands for Emitter Coupled Logic. The basic circuit configuration consists of a pair of NPN transistors with their emitters connected together and fed by a current source. The table below shows the logic levels for different ECL standards.

	ECL	**LVECL**	**PECL**	**LVPECL**
V_{CC}	0 V	0 V	+5.0 V	+3.3 V
V_{EE}	-5.2 V	-3.3 V	0 V	0 V
V_{OH}	-0.8 V	-0.8 V	+4.2 V	+2.5 V
V_{OL}	-1.6 V	-1.6 V	+3.4 V	+1.7 V
V_{BB}	-1.3 V	-1.3 V	+3.7 V	+2.0 V
V_{TT}	-2 V	-2 V	+3 V	+1.3 V
V_{OHPG}	+0.4 V	+0.4 V	+5.4 V	+3.7 V
V_{OLPG}	-1.2 V	-1.2 V	+3.8 V	+2.1 V

Figure 9: Table comparing the logic levels of different ECL standards[8]

As you can see, all ECL standards have inter-logic-level voltage difference of only 0.8V. This allows for higher data rates as it is easier to alternate between low voltage differences.

B 4B/5B

Code type	4B Code	Name	5B Symbol
data	0000	0	11110
data	0001	1	01001
data	0010	2	10100
data	0011	3	10101
data	0100	4	01010
data	0101	5	01011
data	0110	6	01110
data	0111	7	01111
data	1000	8	10010
data	1001	9	10011
data	1010	A	10110
data	1011	B	10111
data	1100	C	11010
data	1101	D	11011
data	1110	E	11100
data	1111	F	11101
Idle	undefined	I	11111
Start of stream	0101	J	11000
Start of stream	0101	K	10001
End of stream	undefined	T	01101
End of stream	undefined	R	00111
Transmit error	undefined	H	00111
Invalid code	undefined	V	00000
Invalid code	undefined	V	00001
Invalid code	undefined	V	00010
Invalid code	undefined	V	00011
Invalid code	undefined	V	00100
Invalid code	undefined	V	00101
Invalid code	undefined	V	00110
Invalid code	undefined	V	01000
Invalid code	undefined	V	10000
Invalid code	undefined	V	11001

Figure 10: Encoding of 4-bit data into 5-bit symbols [9]

C Digital vs Analog

Analog: Signal is continuous in time and amplitude. It is called analog as the signal is usually analogous to another naturally occurring signal. An example would be a microphone which picks up the sound of someone's voice. The voltage leaving the microphone would be analogous to the sound waves entering the microphone.

Digital: Signal is discrete in time and amplitude. It is called digital as it represents information as a finite number of integers (binary digits). There are two advantages to the digital signal. First, because it is discrete in time, it only has a finite number of samples. This would mean that if we were to perform some computations on the signal such as taking its average, it would no longer require integration as it is not continuous. It would instead require just a simple summation.

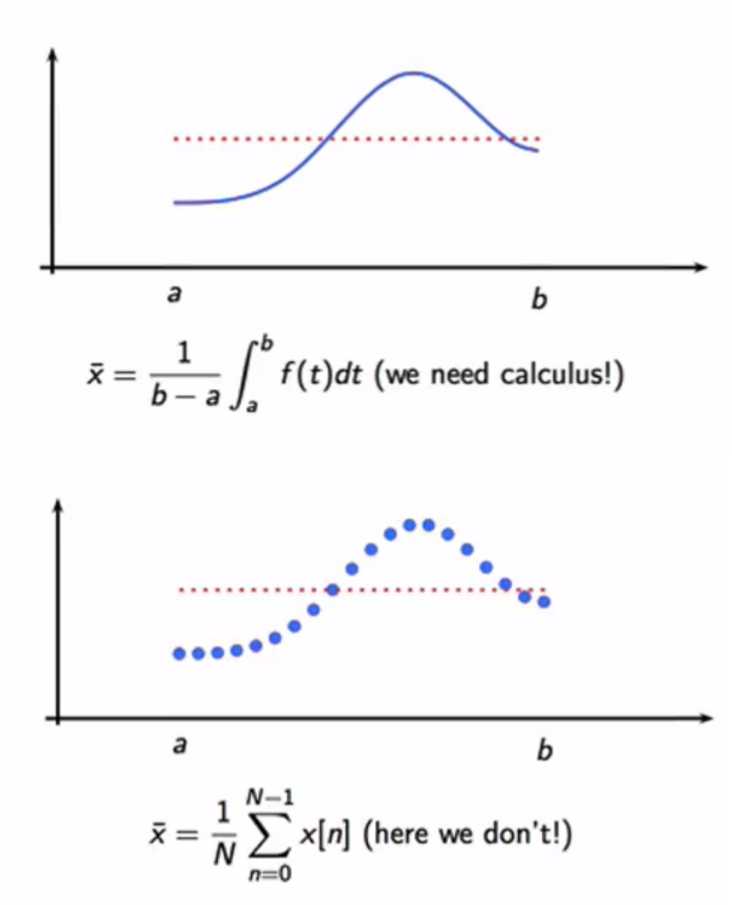

Figure 11: Comparison between calculations on continuous and discrete signals [11]

Thus, it is computationally much simpler to work with. Secondly, because it is also discrete in amplitude, meaning it can only take on a finite set of possible values, the information becomes completely abstract and general. This is very important as this means that storage is a lot simpler. Any memory that can store integers can store signals; unlike analog storage, which was very dependant on the application and the kind of signal. Another significant impact is on transmission of the signals.

Whenever we transmit signals over a line, the signal attenuates and some noise is added to the signal. With analog signals the problem of noise is significant and difficult to overcome. Since the signal can take on an infinite set of values, there is no way to retrieve it once it has a significant level of noise. Digital signals on the other hand, are a bit more robust. Because we transmit only integers with a finite set of possible values, we can retrieve the correct information despite the noise.

D Modulation

Modulation converts a digital signal into an analog one and demodulation does the opposite. This is done to change the bandwidth of the signal so that it can be transmitted on a band-limited channel without much distortion. It can be achieved by varying a sinusoidal signal with a bit stream. There are 3 fundamental ways to modulate a signal.

D.1 Bits vs Symbols

Bit: Digital value ”0” or ”1”

Symbol: Modulated analog waveform. A symbol can encode more than one bit as you can see later in QAM. Symbol rate is also known as Baudrate and if a symbol encodes n bits, $baudrate = \frac{bitrate}{n}$.

D.2 Amplitude Modulation (AM)

AM varies the amplitude of the sinusoidal signal to encode the bits. For example, a higher amplitude could signify a "1" while a lower amplitude could be "0".

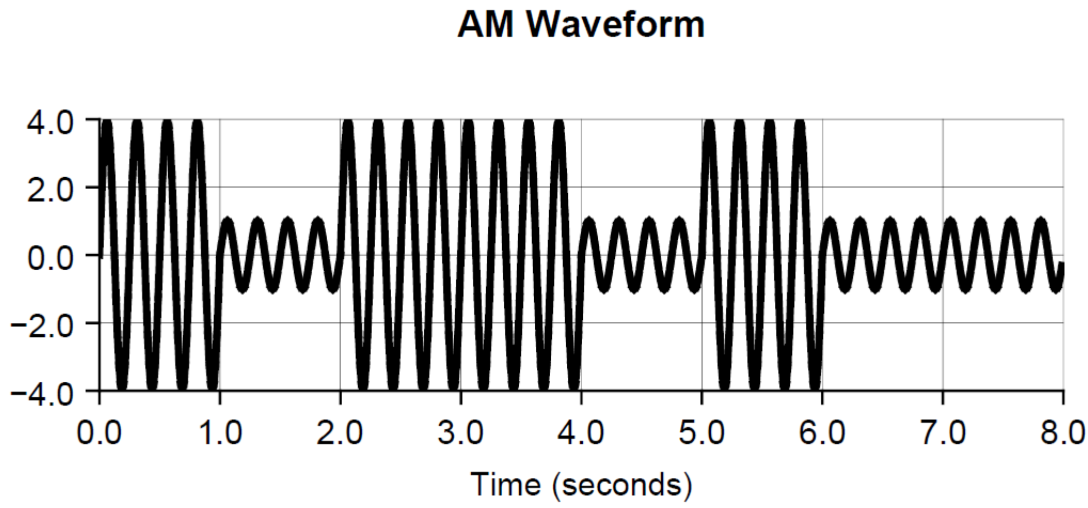

Figure 12: AM wave for bit stream 10110100 [7]

$$bitrate = 1bps, f = 4Hz, a_0 = 1, a_1 = 4$$

D.3 Frequency Modulation (FM)

Same idea as AM but varying frequency instead. FM requires a higher bandwidth than AM but is less prone to interference and thus, results in much better signal quality upon reception [5].

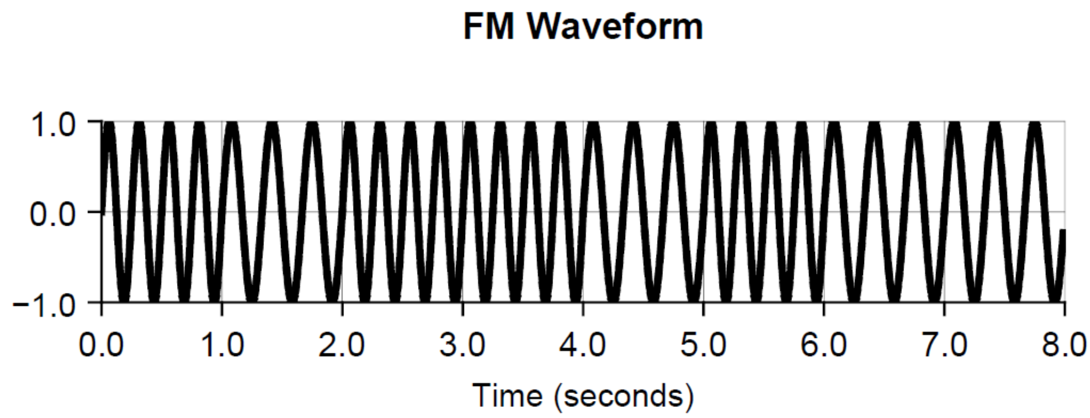

Figure 13: FM wave for bit stream 10110100 [7]

$$bitrate = 1bps, a = 1, f_0 = 3Hz, f_1 = 4Hz$$

D.4 Phase Modulation (PM)

Phase modulation is sometimes referred to as indirect frequency modulation as changing phase produces a change in frequency and thus, has the same advantage of FM as being more robust to noise. However, it does require more complex circuitry to produce.

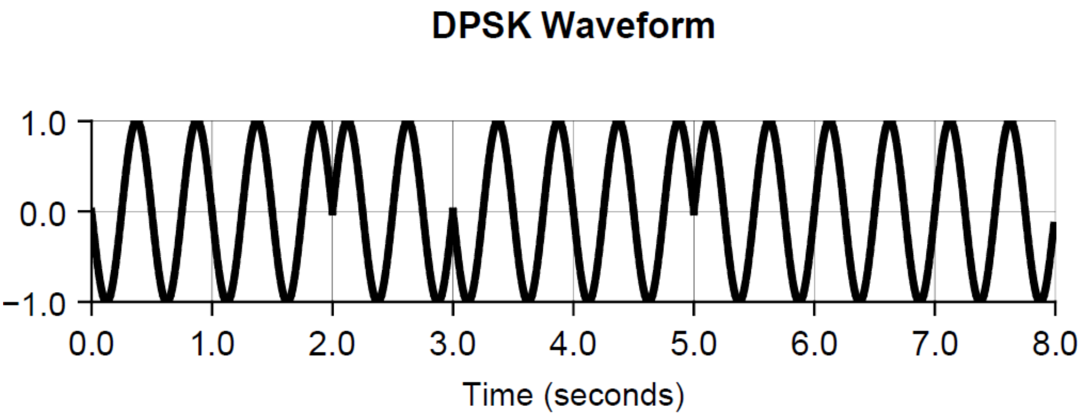

Figure 14: Differential Phase Shift Keyed waveform for bit stream 10110100 [7]

$$bitrate = 1bps, a = 1, f = 2Hz, \Delta\phi_0 = 0, \Delta\phi_1 = \pi$$

D.5 Quadrature Amplitude Modulation (QAM)

QAM is a multibit/symbol signalling scheme which is composed of two carrier waves of the same frequency. The carrier waves are $90\deg$ out-of-phase (a sine and a cosine wave) and thus, are called quadrature carriers; lending to the name of the modulation. The amplitude of the carriers are modulated with the digital data stream. For example, even bits could encode the sin component while the odd bits encode the cosine component. The modulated carriers are then summed up resulting in a waveform that is modulated in both *amplitude and phase* [15].

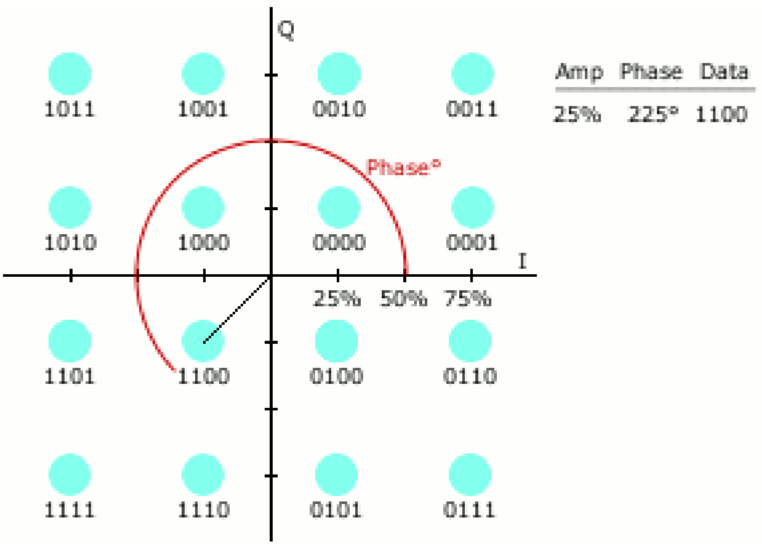

Figure 15: Constellation diagram of a 16QAM signal showing amplitude and phase encoding of data

D.6 Frequency Domain

Unlike what it may seem, any periodic signal can actually be synthesised by adding together sinusoids of different frequencies and amplitudes. This forms the basis of Fourier analysis; decomposition of signals into their constituent parts. This decomposition is done by Fourier Transform given below.

$$H(f) = \int_{-\infty}^{+\infty} h(t)e^{2\pi ift}dt$$

The reverse can be achieved using the inverse Fourier Transform:

$$h(t) = \int_{-\infty}^{+\infty} H(f)e^{-2\pi ift}df$$

In practice, we obtain a time series from the signal by sampling it at regular intervals Δt. Then we perform *Discreet* Fourier Transform (DFT) to obtain a frequency series.

$$H(f) = \sum_{j=0}^{N-1} h(t)e^{2\pi ijk/N}, k = 0, 1, 2, ...N-1$$

Inverse DFT: $h(j) = \frac{1}{N}\sum_{k=0}^{N-1} H(k)e^{2\pi ijk/N}, j = 0, 1, 2, ...N-1$

N = number of samples

Analysis of Frequency Domain:
Frequency component: $\Delta f = \frac{1}{N\Delta t}$
$|H_k|$ = Amplitude of frequency component at $f = \Delta fk$
Power of frequency component at $(f = \Delta fk) = |H_k|^2$
Therefore, Spectrum analysis = Plot of $|H_k|^2$ against $k\Delta f$
When doing spectrum analysis, one will realise that even a signal which seems to only consist of a single frequency (e.g. an AM modulated signal), has constituents from other frequencies, called sidebands, as shown below and thus, have a bandwidth.

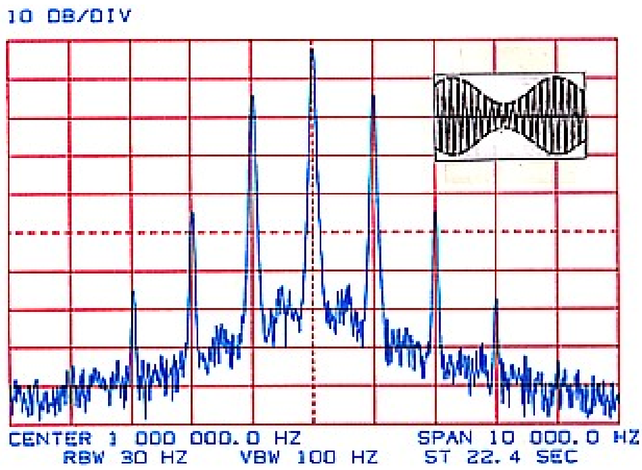

Figure 16: Spectrum analysis of an AM signal [4]

D.6.1 Bandwidth

Spectrum analysis is the tool with which we can ascertain the bandwidth required by a certain signal. Bandwidth is the range of frequencies where most of the energy in the signal is located [7].

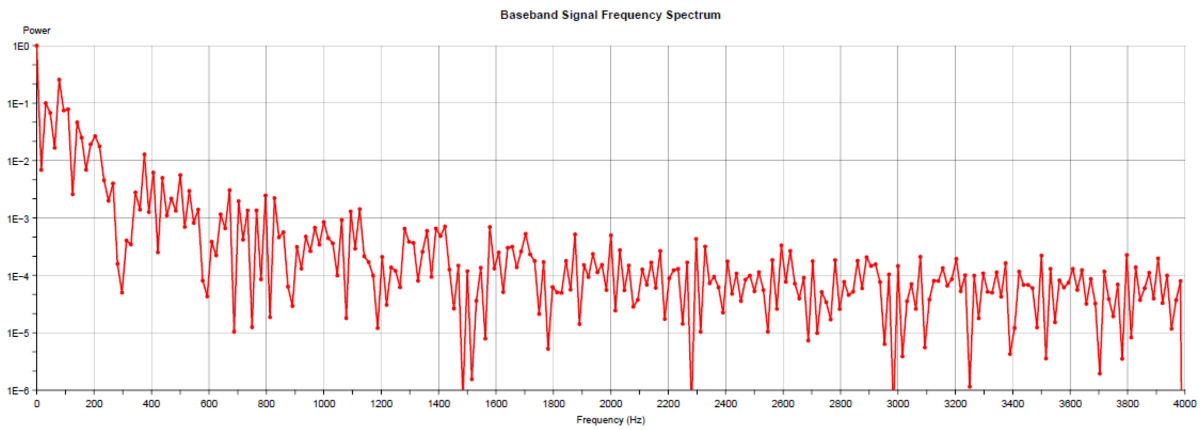

Figure 17: Spectrum analysis of unmodulated digital signal at 300bps [7]

The bandwidth is the range of frequencies which are above a set threshold value (e.g 0.01); from the smallest frequency component to the largest frequency component above the threshold. So in the above scenario, it would be roughly 0Hz - 400Hz.

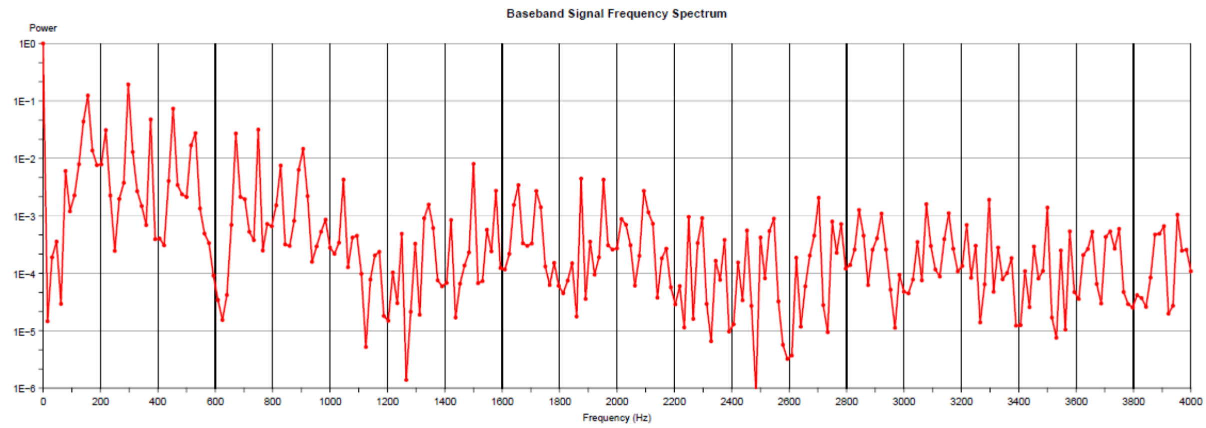

Figure 18: Spectrum analysis of unmodulated digital signal at 300bps [7]

With a 1200bps signal, we can see that the bandwidth would be roughly 0Hz - 1500Hz. Thus, we can see that larger data rates require a larger bandwidth and ergo, the hunt for ever more bandwidth to play with.

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Student Information

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Department	Mechanical Engineering
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IA Report	Mid-Term / End-Term

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Name of Supervisor	Teo Ee Jin
Designation	Scientist III
Email / Telephone	teoej@imre.a-star.edu.sg

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