Hardware:

The change from last lab to this current lab was the change in use from the internal ADC to the external ADC. The connections made from the external adc included the ref198 which generates a 5V reference voltage for the external ADC, max144 chip. This chip generates a 12 bit value rather than a 10 bit value, so this external voltage should give a more accurate result than the 10 bit one.

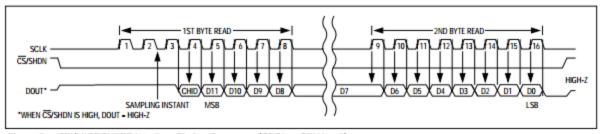


Figure 8c. SPI/MICROWIRE Interface Timing Sequence (CPOL = CPHA = 0)

The max144 chip is a analog voltage to digital converter. The advantage of using this chip is that there is a 12 bit digital output, which means more accuracy in the measurements. With this external adc, the constantly changing Isb during last Iab could be avoided. The max144 chip uses spi protocol to transfer the data between the MCU and chip. The chip is used as a slave and MCU as the master. The max144 will be clocked by the master. The ref pin of the chip will be connected to ref198 chip which will provide 4.096V voltage as the reference voltage. Thus the maximum voltage that can be measured will be 4.096v. The max144 has a accuracy of +-1 Isb, which means up to a 11 bits will be exact thus output will be more accurate. The program used will implement a sck frequency of fck/4, for every clock cycle 4 bits of data will be transferred. The specified max frequency for this chip is 2.17Mhz, the frequency used is 0.25Mhz, wake

¹ courtesy - max144 datasheet

up time of this chip is 2.5 microseconds or approximately three MCU clock cycles.

Although there are two different channels which has the ability to measure two different voltage, both are connected together for this lab. When cs is high the chip will be powered down. The MCU will start receiving data when the System clock is on and when CS is low. When a dummy value from the MCU is sent, the max144 will start sending data. Since there are 12 bits of data to be transferred. First 8 msb will be transferred within the first 8 scks and next 8 will be sent after the spdr register has been cleared.

The REF198 chip is used as a voltage reference. The chip as specified by the datasheet has a accuracy of +-2mV. The chip will provide an output voltage of maximum 4.096V. when the chip is placed on a sleep mode, it will require only 15 microamps of currents, thus an ideal chip to be used with battery powered systems. The sleep pin for this lab will be connected to power. Two capacitors with 10uf and 0.1 uf respectively are connected to dout, to reduce noise and sudden spikes.

A pull down resistor is added to the ch0 and ch1 of max144. The pull down is required for the third task of the lab. Attaching a pull down resistor guarantees that when a voltage source is not connected the chip will read 0v. This helps in coding, as it is easier to check for an exact value of 0 and perform the capture function.

Software:

The change in this code involves only the change in which the r9 and r8 values are obtained. In this lab the change would be that since the values obtained come from an outside source, a serial port is used to connect the output of the ADC to the input of the port MISO pin. Everything in portB is set as output except for the second to last pin. In the spcf the spi, and master is enabled, thus making the SPI run at fck/4. As a result the SPI register is used to transmit the data from the slave into the master. In order to obtain the the 12 bit data register, the value must be obtained a byte at a time totalling two byte transfers. Through this MISO is set as an input and an 8 bit dummy value is sent out where the high byte of the ADC value is shifted in. Because the lcd was disabled before the dummy value was set and the ADC enabled, then only the ADC will be affected due to the SCK clock cycles from sending the dummy values. Thus only 8 bits will be obtained, which is 1 byte. Then the program will prompt for the low byte after storing the high byte into r9 and when the low byte is completely transferred it will be stored in r8. Everything else will be the same as the last lab.

The initialisation of the spi ports is given in the below picture.
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