SG2300X
Board Bring Up Guide

Version: 1.0

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Document Revision History

Revision	Date	Author	Description
1.0			Draft version

Table of Contents

1 overview

The guidance only makes some explanations on the minimum system of SG2300X bring Up. According to users ' requirements, it introduces some other functional interfaces, such as PCIE,RGMII,UART,I2C, etc., which can be used to bring up according to the actual situation.

2 Check Items

1. Check before power on
2. Power on Check
3. Check configuration information
4. Check serial port information
5, Uboot burning
6. Kernal burned

3 Check before power on

3.1 Appearance defect Inspection

Check whether the veneer has obvious defects:
1. Whether the solder pad is connected with tin or has missed welding and virtual welding
2. Is there any wrong part, missing part or damaged part
3. Whether the pin of device 1 corresponds correctly
4. Whether the polarity of capacitor, diode and connector is correct

3.2 Impedance Check

Check the ground impedance of each power source
1. Whether each power field has short circuit or open circuit to the ground;
2. Short circuit between each power domain
As the design of each single board circuit is different, the impedance of the power source to the ground is different. The figure shows the impedance measured by the development board, which can be used for reference.

Table 1 Impedance

POWER	Impedance（Ω）		
	max	typical	min
VDDIO18	1K	305	100
VDDC	10	0.9	0.5
VDDIO33	20M	15K	1K
VDD_PHY	10	3.9	2
VDD_PCIE	10	4.1	2
VDD_TPU	10	0.3	0.1
DDR_VDDQ	10	4.7	2
DDR_VDDQLP	20M	10K	1K
VQPS18	20M	10k	1K

4 Power on Check

4.1 Power field Check

Check whether the voltage in each voltage domain of the single board meets the requirements of spec.

4.2 Power domain

- Check that all SG2300X device power supply pins are connected to their required voltages.
- Ensure that selected power regulators meet operating voltage range requirements and meet operating current requirements.
- Check that all VSSC pins are properly connected to ground.

Table 2 Power field

Power domain	Voltage (V)	varation	Power Ball	Power(W) worst
VDDC	0.926/0.85	-10%~+10%	VDDC	9
VDD_TPU	0.62/0.585	-10%~+10%	VDD_TPU	12.5
VDDIO18	1.8	-7% ~ +10%	VDDIO_RGM_33	0.466
			VDDIO_RGM_18	0.022
			VDDIO	0.02
			DDR0A_DDR_VAA	0.03012
			DDR0B_DDR_VAA	
			DDR1_DDR_VAA	
			DDR2_DDR_VAA	
			VDDIO_EMMC_18	0.022
			VDDIO_SENSOR	0.045
			VDDIO_OSC_DDR0	0.045
			VDDIO_OSC_DDR1	0.045
			VPH0	0.702
			VPH1	0.702
VQPS18	1.8	-5%~+5%	VQPS	0.148
VDDIO33	3.3	-10%~+10%	VDDIO_EMMC_33	0.466
			VDDIO_PCIE_PAD_33	0.1
VDD_PHY	0.84	-7%~+5%	VDD_EFUSE	0.028
			VDD_DDR	1.6
			PLL_VDD	0.012
			PLL_VSS	
			PLL_VDD_DDR	
			PLL_VSS_DDR	
VDD_PCIE	0.84	-7%~+10%	VP0	0.794

			VP1	0.794
			VDD_PCIE	0.9
DDR_VDDQ	1.1	-5%~+5%	DDR_VDDQ	1.86
DDR_VDDQLP	0.6	-5%~+5%	DDR_VDDQLP	0.49
GND	0		VSSC	

5 Clock Check

After the power on Check is OK, Check whether the clock output of each clock domain is normal

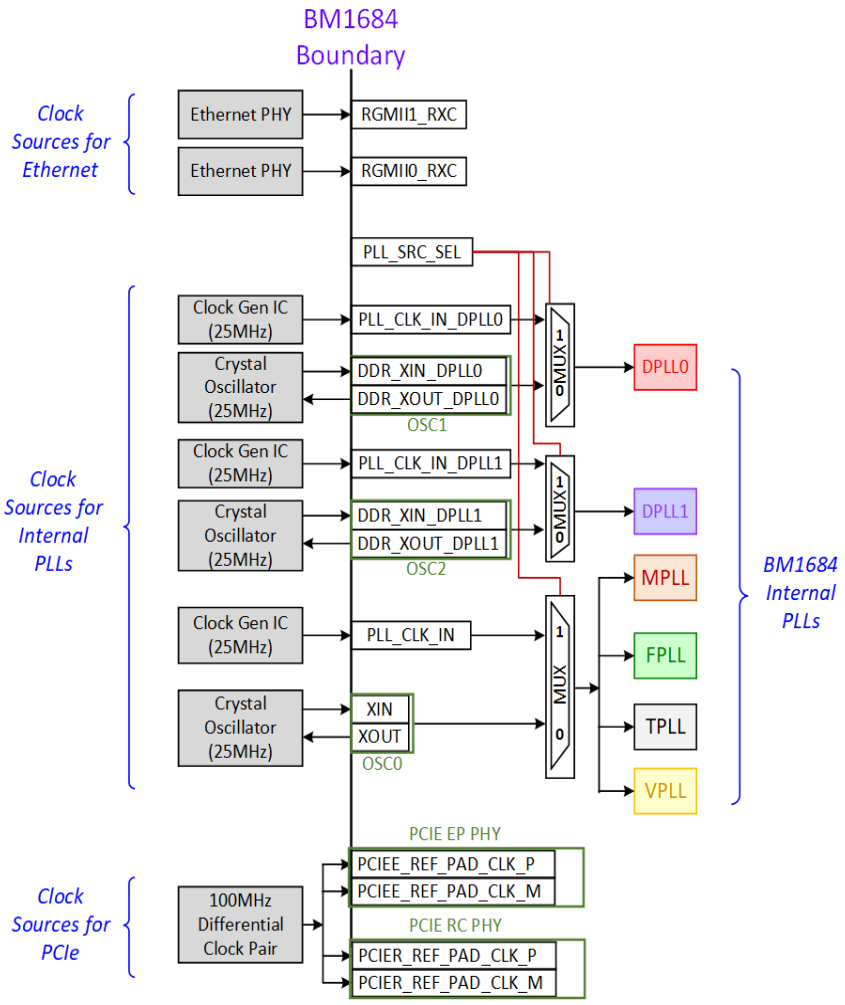

Figure 1 *clock tree*

5.1 Board level clock

- Three 25MHz crystal oscillators are required to provide clock source for SG2300X internal PLLs. They should be connected to PLL_CLK_IN, PLL_CLK_IN_DPLL0 and PLL_CLK_IN_DPLL1.
- PLL_SRC_SEL must be pull down to use crystal oscillators.
- To cost down and save the area,suggest use the clk generator.

5.2 RGMII Ethernet Clock

- For ethernet, gigabit Ethernet PHY provides RX clock to the gigabit Ethernet MAC inside SG2300Xchip.

5.3 PCIE Clock

- For PCIE, PCIe PHY needs 2 100MHz reference clock inputs. One is for phy0, the other is for phy1.GPIO 14（PCIE_REFCLK_SEL）is to control phy1 used repeat clk or ref clk.
  0:disable repeat clk,phy1 used refclk
  1:enable repeat clk,phy1 used repeat clk,phy1 refclk tie 0.
  Advise to use refclk.

6 Power on time series Check

Check whether the power-on timing meets spec requirements.

6.1 Power sequence

- Check all power on sequence meet the list of figure 2-1.
- SG2300X have 5 PG input pin,net name: P08_PWR_GOOD,PCIE_PG2,TPU_PG3, TPUMEM_PG1,DDR_PG,check PG input pin meet the power on sequence.

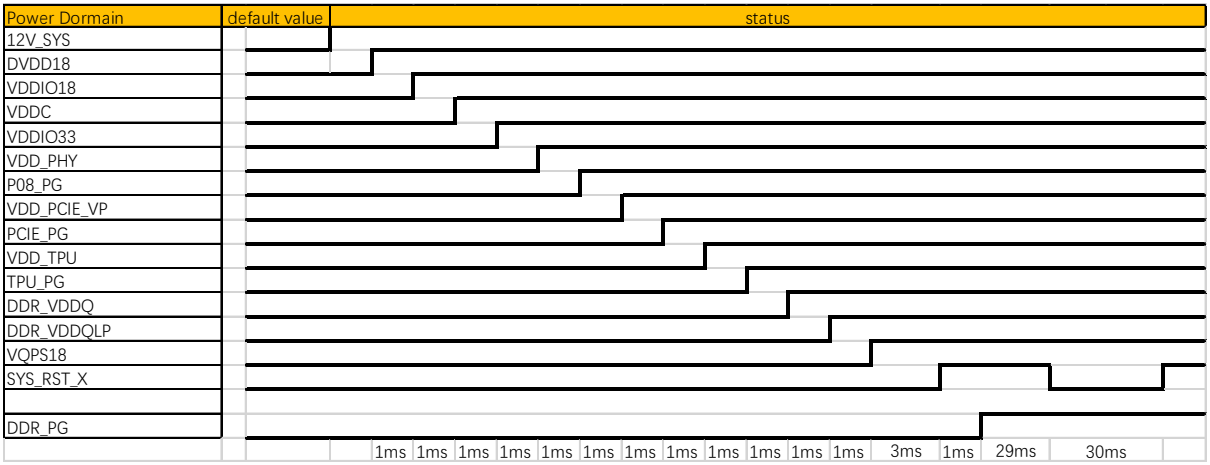

Figure 2 power on sequence

- The power off sequence is reversed of power on sequence.
- If the feature of PCIE used,the power up of VDD_PHY and VDD_PCIE can be synchronize.
- For normal mode ,VQPS18 could be power off,when programme effuse,it must be power on.
- We suggest the power on and power off sequence controlled by MCU.

7 Reset

7.1 SYS Reset

- The SG2300X has an active-low asynchronous device rst pin.The SG2300X rst timing requires the rst signal must be asserted for a minimum of 30ms.
- At initial device power-on,the rst signal must be held low for 30ms after all power supplies,and next be held high for 30ms,and then rst again ,the signal be held low for 30ms again,after rst twice,release the rst signal,as shown in figure 1
- Sys rst pin is 1.8V tolerant.

7.2 PCIE Reset

- When SG2300X in SOC mode,PCIE rst signal must be pull up.
- When SG2300X in PCIE mode,PCIE rst connected to the host p_rst,when host P_rst asserted,the SG2300X sys rst must be asserted.
- PCIE rst pin is 3.3V tolerant.
- For timing control,we suggest tie the P_rst pin to MCU,when P_rst low,MCU asserted SG2300X sys_rst.

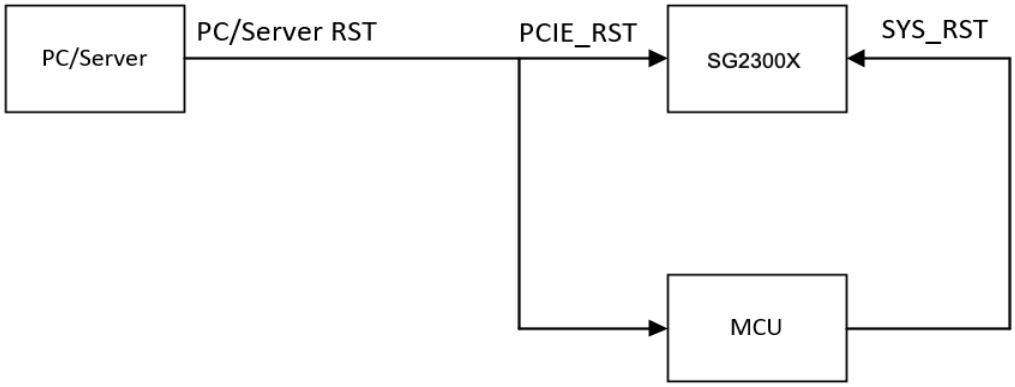

***Figure 3 PCIE_RST** sequence*

8 Configuration information check

Check if the configuration information is correct:
SG2300X support lots of working mode ,boot mode & clk sourc mode,you can set the config pin 1 or 0 by pull-up to VDDIO18 or pull-down to GND with 4.7K ohm resister.The design of EVB used toggle switch to pull-up or pull-down.

8.1 Boot Mode

SG2300X boot sequence have two stages.
First stage, A53 fetch the 1st instruction from off-chip SPI NOR Flash or ONFI NAND Flash or on-chip ROM.
BOOT_SEL[3] = 1'b0: boot from internal ROM. A53 fetch the 1st instruction from internal ROM. The boot loader code is embedded in the ROM. After ROM boot, corresponding device will be ready for linux kernel loading.
BOOT_SEL[3] = 1'b1: boot from SPI NOR FLASH. This is mainly for debug purpose.
A53 fetch the 1st instruction from the off-chip SPI nor Flash with address 0x0600_0000. The main code will be later loaded to AXI SRAM or DDR. Flash is read only, write to Flash will lead to unexpected error.
After Flash boot, corresponding device will be ready for Linux kernel loading.
Second stage, A53 loading Linux kernel
BOOT_SEL[2:0] = 3'b000: loading next bootloader from SPI NOR Flash, but try SD boot first (note1)
BOOT_SEL[2:0] = 3'b001: loading next bootloader from eMMC's boot0 partition, but try SD boot first (note1)
BOOT_SEL[2:0] = 3'b010: loading next bootloader from AXI SRAM, loaded by dbg_I2C/PCIe/JTAG, but try SD boot first (note1)
BOOT_SEL[2:0] = 3'b011: this is not used.
BOOT_SEL[2:0] = 3'b100: loading next bootloader from SPI NOR Flash, without trying SD boot first
BOOT_SEL[2:0] = 3'b101: loading next bootloader from eMMC's boot0 partition, without trying SD boot first
BOOT_SEL[2:0] = 3'b110: loading next bootloader from AXI SRAM, loaded by dbg_I2C/PCIe/JTAG, without trying SD boot first
BOOT_SEL[2:0] = 3'b111: A53 will enter WFI directly, do nothing else.
Note
1 If BOOT_SEL[2] = 1'b0, the software will check whether there is SD card inserted and whether there is firmware image in the SD card first. if trure, it will use this firmware in SD card to boot up, otherwise it will check BOOT_SEL[1:0] for firmware source.
2 When boot from SPI Flash, SPIF_CLK_SEL1 is used to determine clock of SPI interface as shown in this table.

SPIF_CLK_SEL1	SPI Flash Clock Freq
0	0.5M
1	10M

8.2 Chip Mode

*SG2300X*chip mode can be selected by set specific IO into different constant vaule as shown in this table.

In function mode, there are two extra IOs to control chip mode.
MODE_SEL3 should be tied to constant value according top power voltage in function mode.
1'b0 : top power at 0.8V
1'b1 : top power at 0.7V
MODE_SEL2 is used to control whether or not enable fast reset mode in function mode.
1'b0 : disable fast reset mode
1'b1 : enable fast reset mode
In fast reset mode, *SG2300X* will bypass reset debounce stage. And disable fast reset mode is only used for debug.

8.3 Clk source select

Three 25MHz crystal oscillators are required to provide clock source for *SG2300X* internal PLLs.As a backup option, three 25MHz clock gen chips are suggested to be deployed on Check board. They should be connected to PLL_CLK_IN, PLL_CLK_IN_DPLL0 and PLL_CLK_IN_DPLL1.
PLL_SRC_SEL is used to select the source are crystal oscillators or clock gen chips.
0: used crystal oscillators
1: used clock gen chips
For ethernet, gigabit Ethernet PHY provides RX clock to the gigabit Ethernet MAC inside *SG2300X* chip.
For PCIE, PCIe PHY needs 2 100MHz reference clock inputs. One is for phy0, the other is for phy1.GPIO 14（PCIE_REFCLK_SEL） is to control phy1 used repeat clk or ref clk.
0:discable repeat clk,phy1 used refclk
1:enable repeat clk,phy1 used repeat clk,phy1 refclk tie0.

8.4 Debug&GPIO

These pins should be set 0 in most case. Pull-down to gnd with 4.7k ohm resister.
GPIO0(UART_CLI)= 1'b0: boot ROM will wait 1 second for the UART to resume automatically if there is no input.
GPIO0(UART_CLI)= 1'b1: boot ROM will be forced into command line mode.
GPIO12(DISABLE_MMU)= 1'b0: boot ROM enable MMU.
GPIO12(DISABLE_MMU)= 1'b1: boot ROM disable MMU.
GPIO13(EFUSE_PATCH)= 1'b0: boot ROM will not check efuse to see if patch table exists.
GPIO13(EFUSE_PATCH)= 1'b1: boot ROM will check efuse to see if patch table exists.
GPIO16(PCIe_RC_RST)= Used to drive the EP RST of this chip and its downstream neighboring chips in multi-chip scenarios.

9 Serial port information view

After the Check is completed in Chapter 1-5, the printing information can be viewed through UART0, serial port rate: 115200

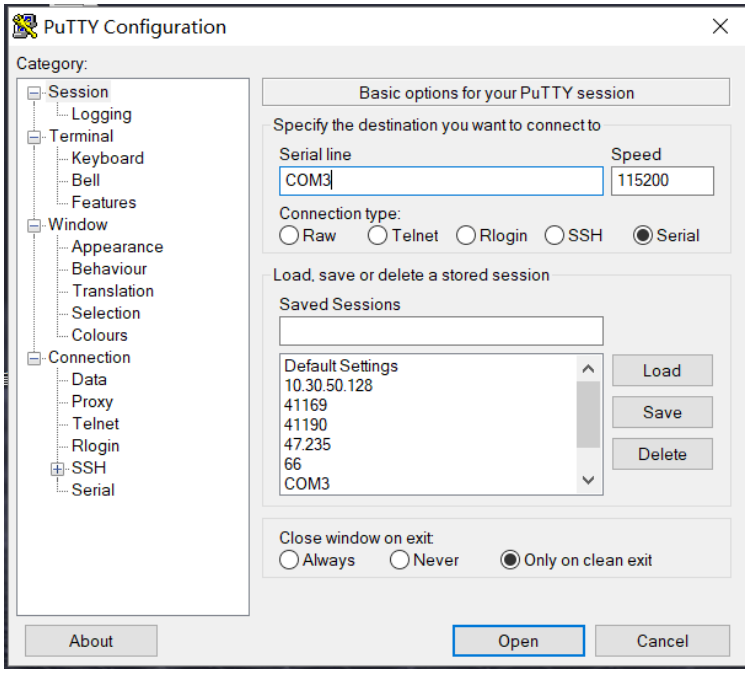

Figure 4 serial port config

You can see the following information:

NOTICE: GPIO0: 600
PCIe 115314
NOTICE: BOOT: 7000000/1/0
NOTICE: Booting Trusted Firmware
NOTICE: BL1: v2.5(release):bm1686_rom_v6
NOTICE: BL1: Built : 19:08:47, Jan 24 2022
INFO: BL1: RAM 0x10002000 - 0x1000d000
INFO: BL1: Loading BL2