SG2300X
Hardware Design Guide

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Version history

版本	日期	作者	更新描述
1.0	2022-07-15	Xinwen Xu	First Release
1.1	2023-4-13	Xinwen Xu	Add GMAC

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Schematic design considerations

This document provides a summary of all schematic design consideration for hardware designers to ensure that all requirements are met. The proceeding sections provide additional detail to clarify each requirement.

Additionally we provided the SG2300X Critical Schematic Review Checklist Application Note, contains a table that provides a high-level checklist of each requirement in this document. Using this Application Note Checklist is recommended when creating or reviewing a design.

Users that have reviewed the reference schematics and the respective BOM will note that a number of devices in those documents are not mandatory for device operation. To help users understand the minimum set of devices, each row in the Schematic Review Checklist Application Note is tagged as mandatory (M), recommended (R) or as-needed for your specific design (D).

Catalogue

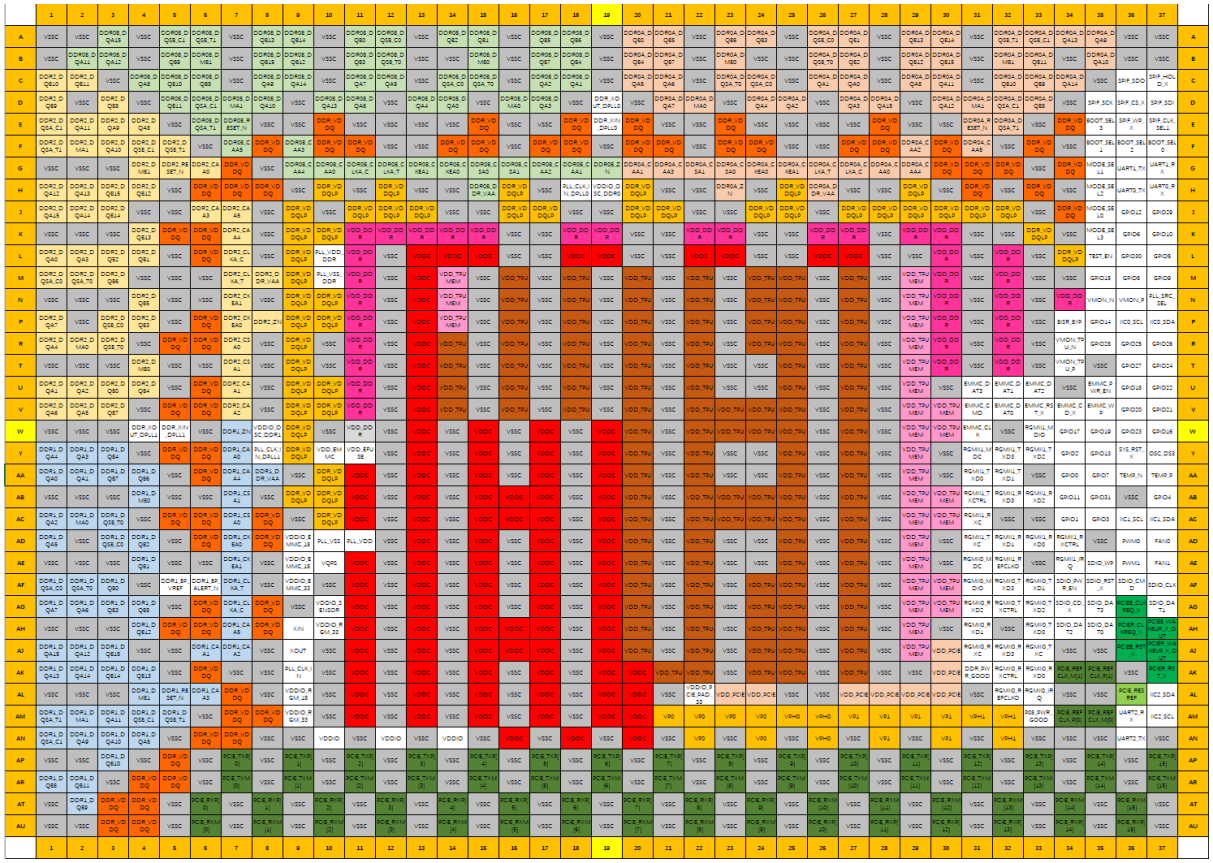
1 Ball Map

Using the latest release of the ball map document for the respective SG2300X device:

• Check that all SG2300X nets in the schematic match their respective ball map definitions.

This critical check will help ensure that all SG2300X device pins are properly connected in your design.

1.1 Signal Map



2 Power

2.1 Power domain & requirement

- Check that all SG2300X device power supply pins are connected to their required voltages.
- Check that all VSSC pins are properly connected to ground.

Table 2-1:

Power domain	Supply Voltage	operating Voltage（V）	operating voltage varation	Power Ball
VDDC	0.8Vcore supply	0.94	±3%	VDDC
VDD_TPU	0.65Vtpu supply	0.78	±2.5%	VDD_TPU
VDDIO18	1.8V IO supply	1.8	±5%	VDDIO_RGM_33
				VDDIO_RGM_18
				VDDIO
				DDR0_DDR_VAA
				DDR1_DDR_VAA
				DDR2_DDR_VAA
				DDR3_DDR_VAA
				VDDIO_SENSOR
				VDDIO_OSC_DDR0
				VDDIO_OSC_DDR1
				VPH0
				VPH1
VQPS18	1.8V VQPS supply	1.8	±5%	VQPS
VDDIO33	3.3V IO supply	3.3	±5%	VDDIO_EMMC_33
				VDDIO_PCIE_PAD_33
VDD_PHY	0.8V phy supply	0.8	±2.5%	VDD_EFUSE
				VDD_DDR
				PLL_VDD
				PLL_VSS
				PLL_VDD_DDR
				PLL_VSS_DDR
VDD_PCIE	0.8V PCIE supply	0.8	±2.5%	VP0
				VP1
DDR_VDDQ	1.1V DDR supply	1.1	±2.5%	DDR_VDDQ
DDR_VDDQLP	0.6V DDR suppluy	0.6	±2.5%	DDR_VDDQLP
GND	0	0		VSSC

2.2 Power consumption

- Ensure that selected power regulators meet operating voltage range requirements and

meet operating current requirements.

- The worst Power：CVS10 model，Junction Temperature 85℃，TPU frequency 1GHz

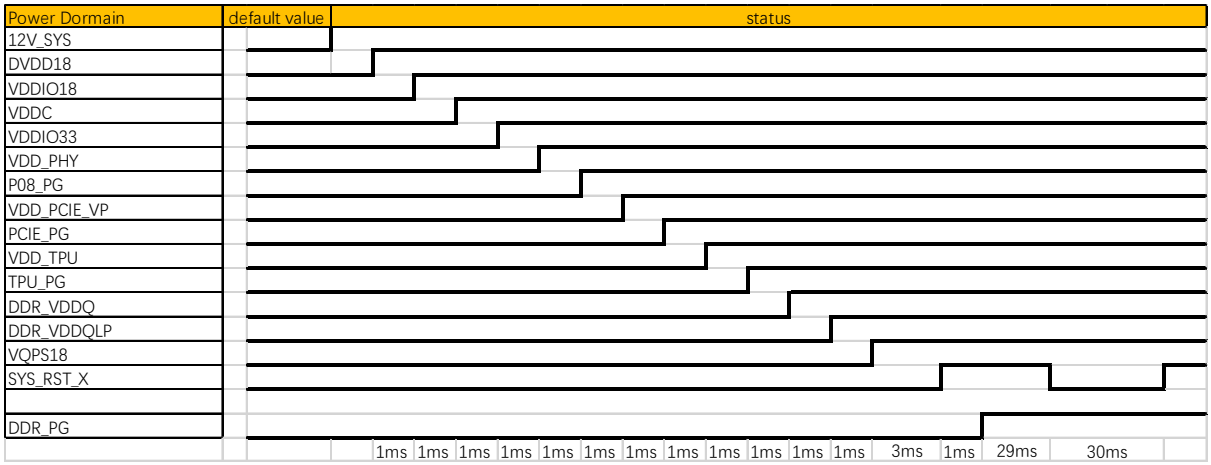
Table 2-1：

Power domain	Power Ball	Power(W) worst	Description
VDDC	VDDC	9	
VDD_TPU	VDD_TPU	12.5	
VDDIO18	VDDIO_RGM_33	0.466	Reference to EVB Schematic
	VDDIO_RGM_18	0.022	
	VDDIO	0.02	
	DDR0_DDR_VAA	0.0301	
	DDR1_DDR_VAA		
	DDR2_DDR_VAA		
	DDR3_DDR_VAA		
	VDDIO_EMMC_18	0.014	
	VDDIO_SENSOR	0.045	
	VDDIO_OSC_DDR0	0.045	
	VDDIO_OSC_DDR1	0.045	
	VPH0	0.702	
	VPH1	0.702	
VQPS18	VQPS	0.148	default power off
VDDIO33	VDDIO_EMMC_33	0.466	
	VDDIO_PCIE_PAD_33	0.1	
VDD_PHY	VDD_EFUSE	0.028	Recommended LDO for PLL
	VDD_DDR	1.6	
	PLL_VDD	0.022	
	PLL_VSS		
	PLL_VDD_DDR		
	PLL_VSS_DDR		
VDD_PCIE	VP0	0.292	
	VP1	0.292	
DDR_VDDQ	DDR_VDDQ	1.86	
DDR_VDDQLP	DDR_VDDQLP	0.49	
GND	VSSC		

2.3 Power sequence

- Check all power on sequence meet the list of figure 2-1.
- SG2300X have 4 PG input pin, net name: P08_PWR_GOOD, PCIE_PG2, TPU_PG3,DDR_PG, check PG input pin meet the power on sequence.

Figure 2-1:



- The power off sequence is reversed of power on sequence.
- If the feature of PCIE used, the power up of VDD_PHY and VDD_PCIE can be synchronize.
- For normal mode ,VQPS18 could be power off, when programme effuse, it must be power on.
- We suggest the power on and power off sequence controlled by MCU.

3 Reset

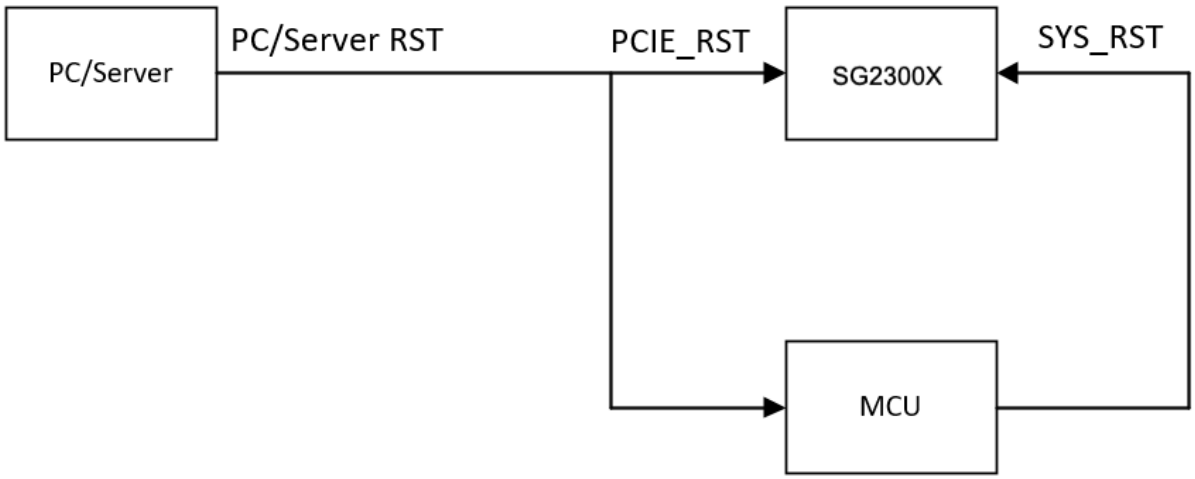
3.1 SYS Reset

- The SG2300X has an active-low asynchronous device rst pin. The SG2300X rst timing requires the rst signal must be asserted for a minimum of 30ms.
- At initial device power-on, the rst signal must be held low for 30ms after all power supplies, and next be held high for 30ms, and then rst again, the signal be held low for 30ms again, after rst twice, release the rst signal, as shown in figure 2-1.
- Sys rst pin is 1.8V tolerant.

3.2 PCIE Reset

- When SG2300X in SOC mode, PCIE rst signal must be pull up.
- When SG2300X in PCIE mode, PCIE rst connected to the host p_rst, when host P_rst asserted, the SG2300X sys rst must be asserted.
- PCIE rst pin is 3.3V tolerant.
- For timing control, we suggest tie the P_rst pin to MCU, when P_rst low, MCU asserted SG2300X sys_rst.

Figure 3-1:



4 Clock

4.1 Board level clock

- Three 25MHz crystal oscillators are required to provide clock source for SG2300X internal PLLs. They should be connected to PLL_CLK_IN, PLL_CLK_IN_DPLL0 and PLL_CLK_IN_DPLL1.Recommend clock specification is in Table 4-1.
- PLL_SRC_SEL must be pull down to use crystal oscillators.
- To cost down and save the area, suggest use the clk generator.

Table4-1：

Parameter	Symbol	Min	Type	Max	Units
Frequency	f	-	25	-	MHz
Logic Levels	VIH	-	1.8	-	V
	VIL	-	0	0.36	V
Rise Time/Fall Time	t_R/t_F		1.2	2	ns
Duty Cycle	SYM	45	50	55	%
Period Jitter,RMS	J_{PER}	-	20	-	ps
Period Jitter, Peak-to-Peak	J_{PER}	-	170	-	ps
Cycle-to-Cycle Jitter, Peak	J_{CY-CY}	-	150	-	ps

4.2 RGMII Ethernet Clock

- For Ethernet, gigabit Ethernet PHY provides RX clock to the gigabit Ethernet MAC inside SG2300X chip.

4.3 PCIE Clock

- For PCIE, PCIE PHY needs 2 100MHz reference clock inputs. One is for phy0, the other is for phy1.GPIO 14（PCIE_REFCLK_SEL）is to control phy1 used repeat clk or ref clk.
  0:disable repeat clk,phy1 used refclk
  1:enable repeat clk,phy1 used repeat clk,phy1 refclk tie 0.
- Advise to use refclk.

5 Config

5.1 Boot mode

SG2300X boot sequence have two stages.

First stage, A53 fetch the 1st instruction from off-chip SPI NOR Flash or ONFI NAND Flash or on-chip ROM. After Flash boot, corresponding device will be ready for Linux kernel loading.

Second stage, A53 loading Linux kernel

- Utilize 4.7k ohm resistors for all bootstrapping pins
- Pull up resistors must go up to 1.8V. Boot-strapping pins are only 1.8V tolerant.
- We advise both of two stages boot from SPI NOR FLASH.
- Use toggle switch for better control or pull up and pull down resistors.

Table5-1：

BOOT_SEL	b'	boot mode
3	0	BL1 boot from internal ROM
	1	BL1 boot from internal SPI NOR FLASH
2	0	try SD boot first. the software will check whether there is SD card inserted and whether there is firmware image in the SD card first. if true, it will use this firmware in SD card to boot up
	1	it will check BOOT_SEL[1:0] for firmware source, without trying SD boot first
10	00	loading next bootloader from SPI NOR Flash
	01	loading next bootloader from EMMC's boot0 partition
	10	loading next bootloader from AXI SRAM
	11	A53 will enter WFI directly
note: BOOT_SEL[2:0] = 3'b011: this is not used.		

5.2 Chip mode

- Utilize 4.7k ohm resistors for all chip select pins
- Pull up resistors must go up to 1.8V. Chip select pins are only 1.8V tolerant.
- We advise MODE_SEL=b'0001.
- Use toggle switch for better control or pull up and pull down resistors.

Table 5-2：

CHIP_SEL	b'	chip mode
3	0	top power （VDDC） at 0.8V

	1	top power （VDDC）at 0.7V
2	0	disable fast reset mode
	1	enable fast reset mode
10	00	normal speed function mode
	01	fast speed function mode
	10	safe speed function mode
	11	bypass speed function mode
note: TSET_EN = 0		

5.3 Debug & GPIO

- These pins should be set 0 in most case. Pull-down to gnd with 4.7k ohm resister.
- These pins are only 1.8V tolerant. Pull-up to 1.8V with 4.7k ohm resister.
- Check GPIO pin default status as table 5-3.

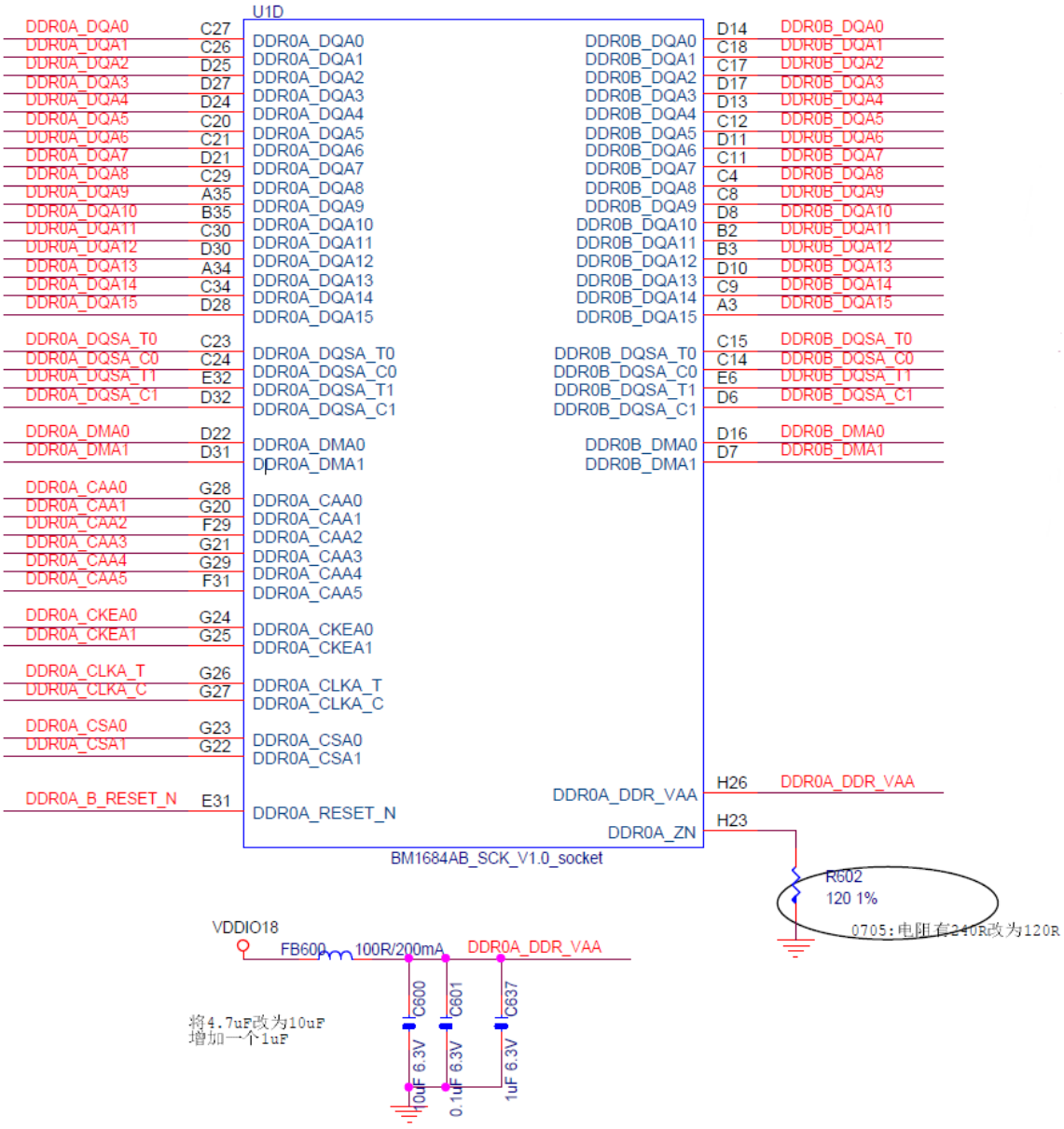
Table 5-3：

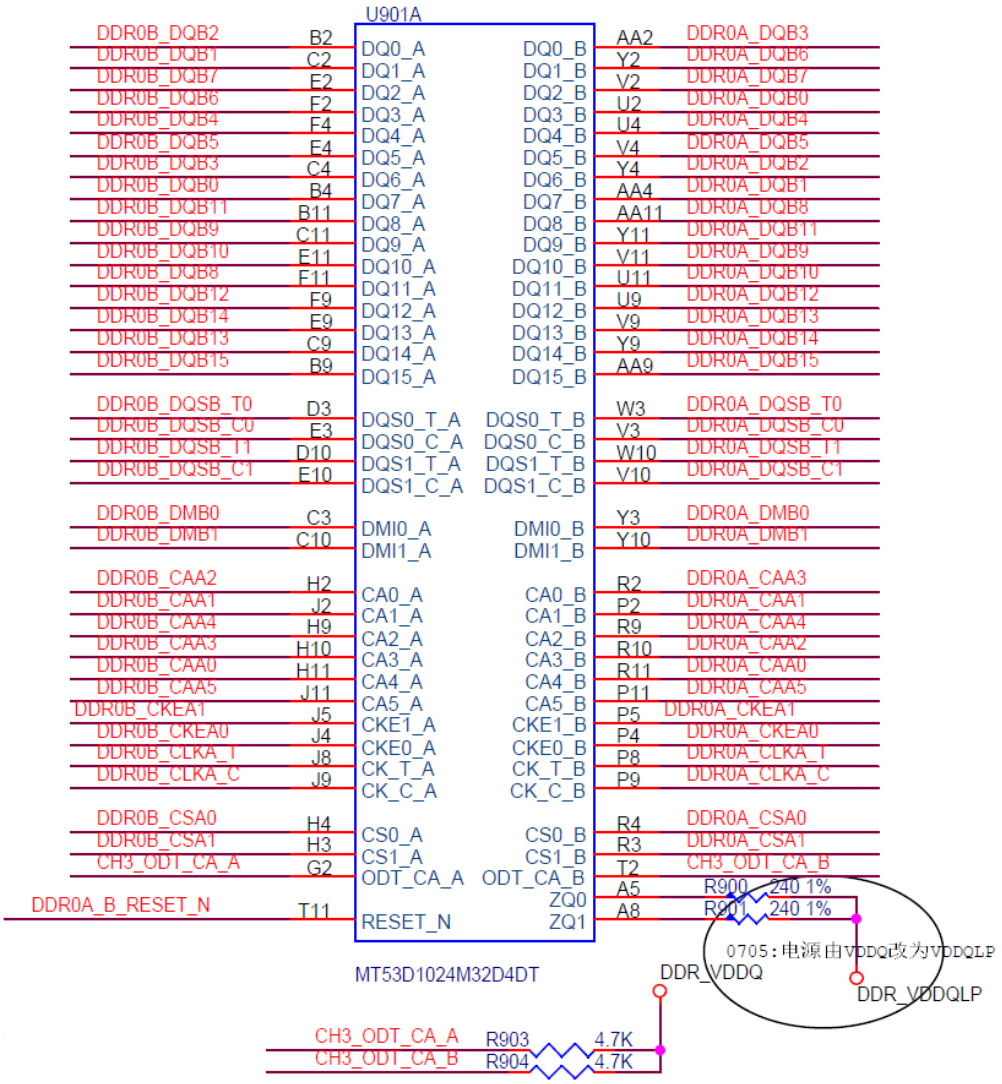
GPIO	pin name	I/O	Description	default
GPIO0	GPIO0/UART_CLI	input	high enter command line mode	0
GPIO1	GPIO1	input	GPIO	0
GPIO2	GPIO2/PCIE_PG	input	detect VDD_PCIE power good	0
GPIO3	GPIO3/TPU_PG	input	detect VDD_TPU power good	0
GPIO4	GPIO4/PLL_LOCKO	output	high mean PLL is OK	0
GPIO5	GPIO5/IIC_ADDR0	input	distinguish different SG2300X locations	0
GPIO6	GPIO6/IIC_ADDR1	input		0
GPIO7	GPIO7/IIC_ADDR2	input		0
GPIO8	GPIO8/IIC_ADDR3	input		0
GPIO9	GPIO9/PCIE_EP_RC[0]	input	distinguish EP mode or EP+RC mode detail description in chapter 7(PCIE)	0
GPIO10	GPIO10/PCIE_EP_RC[1]	input		0
GPIO11	GPIO11/PCIE_EP_RC[2]	input		1
GPIO12	GPIO12/DISABLE_MMU	input	0:enable MMU 1：disable MMU	0
GPIO13	GPIO13/UART0_RST /EFUSE_PATCH	input	0:skip patch table 1:always check EFUSE patch table	0
GPIO14	GPIO14/UART0_CTS /PCIE_REFCLK_SEL	input	0:disale PCIE repeat CLK 1:enable repeat CLK,phy1 use repeat CLK	0
GPIO15	GPIO15/JTAG_1_2_SEL	input	0: JTAG1 1: JTAG2	0
GPIO16	GPIO16/PCIE_RC_RST	output	used for multi-chip card scenarios to drive next chip EP RST	0
GPIO17	GPIO17/JTAG0_TDO	output		0
GPIO18	GPIO18/JTAG0_TCK	I/O		0

GPIO	pin name	I/O	Description	default
GPIO19	GPIO19/JTAG0_TDI	input	JTAG0 for A53 JTAG1 for AMR9 JTAG2 for RISC	0
GPIO20	GPIO20/JTAG0_TMS	I/O		0
GPIO21	GPIO21/JTAG0_TRST	I/O		0
GPIO22	GPIO22/JTAG0_SRST	I/O		0
GPIO23	GPIO23/JTAG_1_2_TDO	output		0
GPIO24	GPIO24/JTAG_1_2_TCK	I/O		0
GPIO25	GPIO25/JTAG_1_2_TDI	input		0
GPIO26	GPIO26/JTAG_1_2_TMS	I/O		0
GPIO27	GPIO27/JTAG_1_2_TRST	I/O		0
GPIO28	GPIO28/JTAG_1_2_SRST	I/O		0
GPIO29	GPIO29/DBG_IIC_SCL	I/O	Boot from I2C	1
GPIO30	GPIO30/DBG_IIC_SDA	I/O		1
note: I/0 and description is GPIO pin in the case of reuse				

6 DDR

- Ensure DDR SDRAM support LPDDR4X.
- We recommend Micron SDRAM: MT53D512M32D4 or MT53D1024M32D4.
- Ensure SG2300X DDR0A_ZN (DDR0B_ZN/ DDR1_ZN/ DDR2_ZN) connect 120 ohm 1% resister to gnd.
- Ensure DDR SDRAM ZQ0 and ZQ1 are connect 240 ohm 1% resister to DDR_VDDQLP.CH[0:3]_ODT_CA_A and CH[0:3]_ODT_CA_B are connect 4.7k ohm resister to DDR_VDDQ.

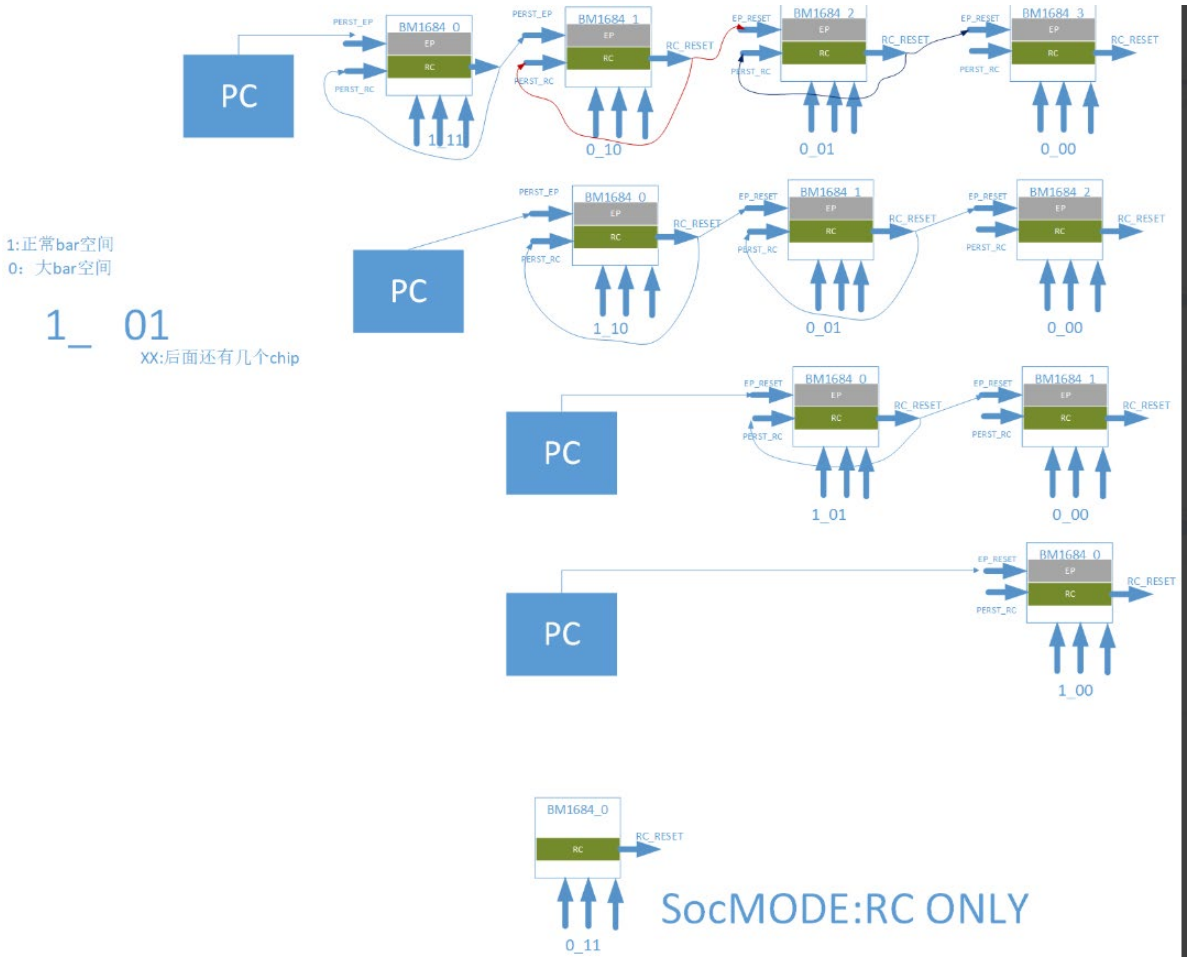




7 PCIE

7.1 PCIE mode

SG2300X has two PCIE phy,phy0 and phy1. SG2300X support three different PCIE mode, such as:x16 EP only, x8 RC+EP, and RC only.SG2300X select different PCIE mode by pull up or pull down GPIO11,GPO10 and GPIO9 .



- The number from left to right means GPIO11, GPIO10 andGPIO9.
- BOOT_SEL[11:9] = 3’b011 not just configurate RC only ,but also EP+RC, the different is RC only mode must floating EP reference CLK, and PERST tie high.
- GPIO[11:9]=3’b100 configurate x16 EP only.

7.2 PCIE interface

- Ensure PCIE_REFCLK_ P/N is connected to a low jitter free-running 100MHz clock.
- Ensure any required host or drive side clocks are connected as needed for common clock use cases.
- Ensure all used PCIE transmitter (Tx) lanes have 0.22µF inline AC coupling caps

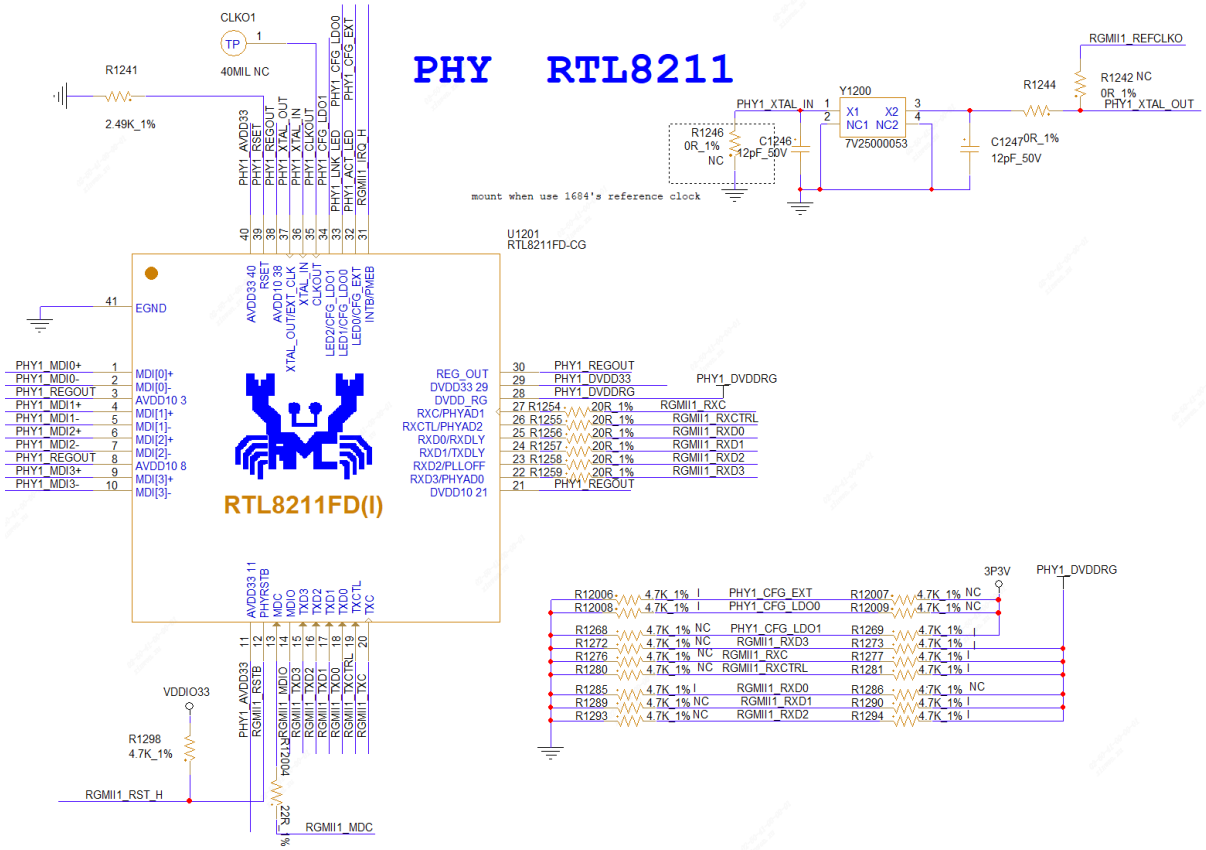
- AC coupling caps for PCIE are part of the PCIE SIG Base Spec
- Inverted polarity of the PCIE transmitter or receiver (Tx_P/N or Rx_P/N) lanes are supported and handled automatically by the device.
- Used ports must utilize lanes in sequential order. Lane reversal within a port is allowed.
- Unused PCIE transmitters/receivers should be left unconnected

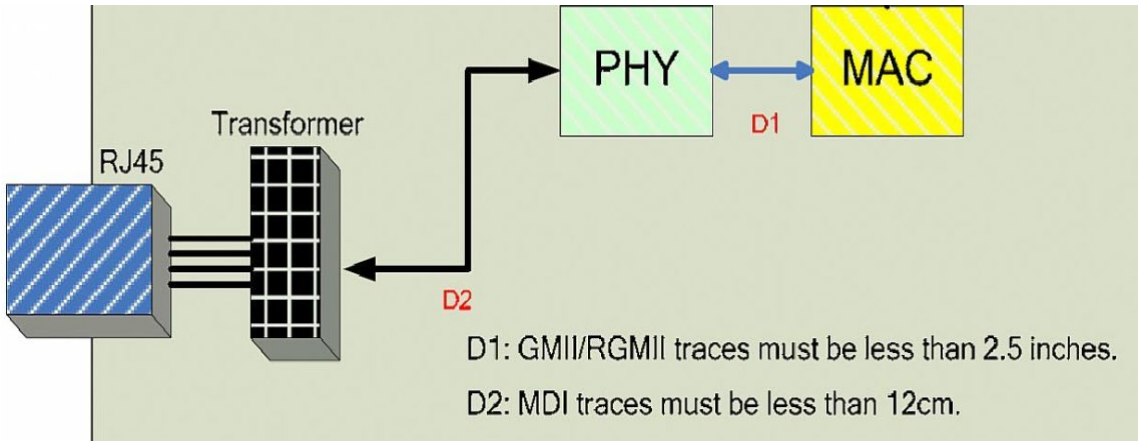
8 Ethernet

- *SG***2300X** has two integrated GMAC, both supporting the RGMII.
- RGMII interface pins are 1.8V tolerant
- Advise use the Ethernet transceiver RTL8211FDI covert RGMII interface to MDI interface.
- RTL8211FDI must follow schematic design as below，the configuration pins must not be changed，the strapping pins according to the table

Pin Name	Strapping
PHY1_CFG_EXT	Pull down
PHY1_CFG_LDO0	Pull down
PHY1_CFG_LDO1	Pull up
RGMII1_RXD3	Pull up
RGMII1_RXC	Pull up
RGMII1_RXCTRL	Pull up
RGMII1_RXD0	Pull down
RGMII1_RXD1	Pull up
RGMII1_RXD2	Pull up

- RGMII interface needs equal length constraints.




PHY
MAC
D1
Transformer
RJ45
D2
D1: GMII/RGMII traces must be less than 2.5 inches.
D2: MDI traces must be less than 12cm.

9 SDIO

SG2300X has two SDIO IP, one for EMMC, the other for SD card.

9.1 EMMC

- Ensure a 4.7kohm resister to pull up EMMC_CMD to VDDIO18.
- EMMC Support HS200 4bit mode.

9.2 SD

- Ensure a 4.7kohm resister to pull up SDIO_CMD to VDDIO18.
- Ensure add a series resister 22ohm in SDIO data and clk trace.

10 MISC

10.1 SPI flash

- SPI clock support HCLK frequency 10M and CLK frequency 0.5M by set SPIF_CLK_SEL1 1 or 0.
- Advise SPIF_CLK_SEL1 pull up to 1.8V with 4.7k ohm resister.
- We suggest to add a series resister 22ohm in clk and data trace, the resister should be placed near SG2300X or SPI slave device(GD25LQ128DSIG).
- Ensure 1.8V flash part is used as all SPI pins are only 1.8V tolerant.

10.2 I2C

- These pins are only 1.8V tolerant.
- Ensure all I2C pins pull-up to 1.8V with 4.7k ohm resister.

10.3 FAN & PWM

- These pins are only 1.8V tolerant.
- Advise pull-up these pins to 1.8V with 4.7k ohm resister.

10.4 UART

UART is utilized by the firmware command server providing a command line user interface. The CLI is used for debugging and diagnosing.

- These pins are only 1.8V tolerant.
- Advise pull-up RX to 1.8V with 4.7k ohm resister.

10.5 JTAG

- These pins are only 1.8V tolerant.

11 V/T/P Monitor

11.1 Voltage monitor

- TPU_SENSE_P and TPU_SENSE_N are use as remote sense pin for VDD_TPU in multiphase power supply;
- VDD_SENSE_P and VDDC_SENSE_N are use as remote sense pin for VDDC in multiphase power supply;
- VMON_P and VMON_N are used as voltage monitor pins.
- By setting different register value of 0x5001_0014 bit[12:8], there are total 19 points in SG2300X chip can be monitored.

11.2 Temperature monitor

- TEMP_P and TEMP_N are used as temperature monitor pins.
- By setting different register value of 0x5001_0014 bit[4:0], there are total 12 points in SG2300X chip can be monitored
- Requires a remote temperature monitor device.

11.3 Process monitor

- There are process monitors in SG2300X .
- Configure reg_pm_select（0x5001_0018 bit[2:1]）to select VT

  2'd0 for lvt；2'd1 for svt；2'd2 for ulvt

12 Reference design document

SG2300X design reference document，include：

1、 SG2300X_EVB_Schematic.DSN

2、 SG2300X EVB MCU 使用说明文档 V1.0.xlsx

SG2300X_Refrence_Design.7z