

SG2300X

Signal & Power Integrity

Design Guide

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SIPI design considerations

This document provides a summary of all high speed design consideration for hardware&sipli designers to ensure that all requirements are met. The proceeding sections provide additional detail to clarify each requirement.

1 LPDDR4/4X Signal Integrity Design Guide

1.1 LPDDR4/4X Features and Benefits

The most significant difference between LPDDR4 and LPDDR4X is the reduction of the data (DQ) IO voltage to 0.6V for additional power savings. Beyond this, there is no difference.

These interfaces operating up to 4266Mbps. They strive to reduce power and improve signal integrity by implementing a lower voltage IO power rail, employing ODT on the Command Address bus and reducing the overall width of the Command/Address bus among other features.

1.1.1 1.1V LVSTL Signaling

The signaling level for LPDDR4 is 1.1V+/- 5% for the I/O voltage. Termination for the data lanes and the Command/Address lane is a pull-down resistor to VSS. Final swing of the received signal will be determined by the termination value at the target device and the pull-up termination value of the driver. The advantage of this is that only a “1” toggle will burn termination power, “0s” can be signaled without burning any termination power. A very low signal swing can be implemented to control simultaneous switching noise as well as reduce the amplitude of the crosstalk. VREF is determined through a training algorithm.

1.1.2 0.6V Signaling for LPDDR4X

LPDDR4X uses a nominal voltage supply of 0.6V with a tolerance of -30mV and +50mV. To power the data lanes during Write and Read operations. The CA bus continues to operate at 1.1V for LPDDR4X.

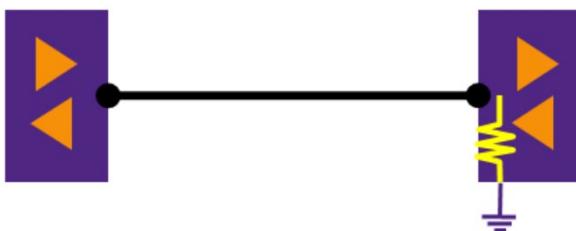


Figure 1 Data lanes and Command/Address signals implement a pull-down termination to VSS

1.1.3 Command/Address Features

1.1.3.1 Narrow Bus

To reduce power, the width of the CA bus has been reduced to 6 bits. Though there are two of these 6 bit busses on the dual channel interface, many of the operational configurations only require a single set of CA signals to be driven from the SOC.

1.1.3.2 On Die Termination

LPDDR4 is the first JEDEC memory standard to offer ODT on the unidirectional CA bus. This will improve signal integrity and allow support for longer routed lengths such as would be encountered in side by side implementations.

1.1.3.3 Single Data Rate Signaling

Unlike LPDDR3, LPDDR4/4x implements single data rate signaling for the Command/Address bus. This will allow for better signal integrity and/or heavier loading on the CA busses, depending on the configuration.

1.1.4 VREF Training for DQ and CA

Because the VREF level for DQ and CA can vary by ODT level as described in Figure 1, VREF must be able to be trained to the correct level. The LPDDR4/4x SDRAMs have internally generated VREF for both DQ and CA signals. Additionally, loading conditions will impact the available signal swing through

inter-symbol interference effects. The VREF training algorithm will allow the placement to be done within 0.5% of VDDQ accuracy. Training will settle to the average calculated Vref level across the byte lane. Since signal channel configurations can vary from lane to lane, training for different VREF levels between byte lanes is supported (Figure2)

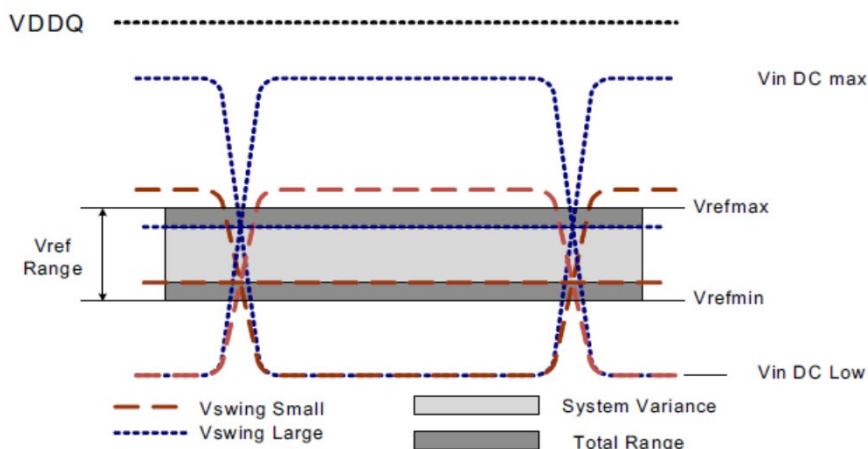


Figure 2 Vref Training optimizes the centering of VREF in the vertical scale for both DQ and DMI

1.1.5 Data Bus Inversion

Data Bus Inversion allows the LPDDR4/4X data interface to conserve termination by inverting busses that signal a greater number of “1”s than “0”s. Since LPDDR4/4X is terminated to VSS, signaling a 0 draws no termination current, as opposed to signaling a 1. This has the added benefit of reducing simultaneous switching noise and, to a certain extent, crosstalk.

1.1.6 Eye Characterization Techniques for LPDDR4/4x

As DDR bit rates have been increasing, the impact of random jitter has become a more significant component in timing closure. The LPDDR4/4x standard is written to accommodate Bit Error Rate techniques by defining the DQ receive parameters in terms of a data window instead of set up and hold specifications. Figure 3 illustrates this new window. For DQ, the window, 0.25UI in width and 120mV in height for 3200Mbps operation represents the needed window to support a BER of 1E-16. The CA timing also uses a rectangular window, but since this is single data rate, there is no provision for random jitter in the form of a target bit error rate. The assumption is that at the lower signaling rate, the BER contribution is small.

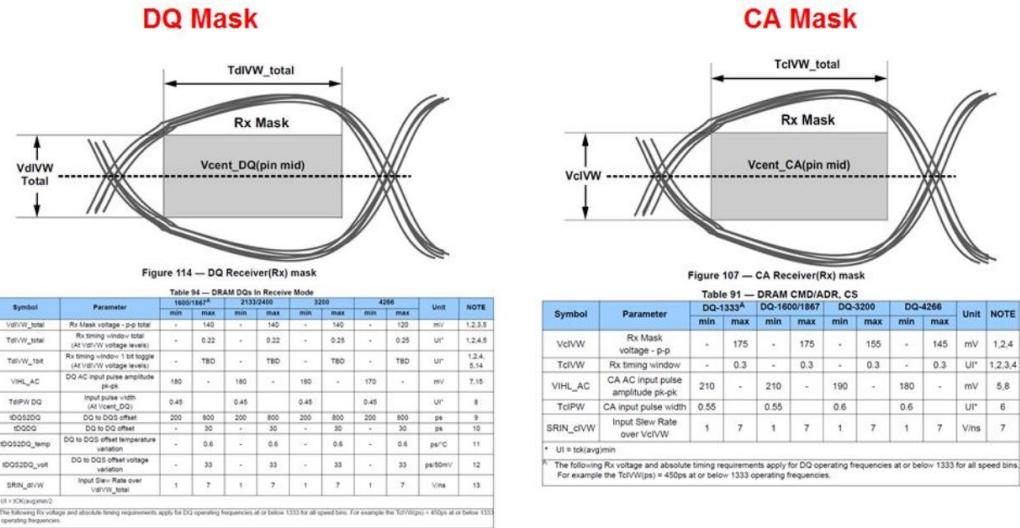


Figure 3 DQ and CA Receiver data input valid windows

1.1.7 tDQS2DQ

LPDDR4/4x implements an un-matched DQS to DQ path. This reduces the latching power consumed by the SDRAM. This introduces a skew between DQS and DQ of as much as 800ps. 800ps equates to ~3.4UI at 4267Mbps. To this amount of skew reduces the amount of beneficial jitter tracking between DQS and DQ. The impact of this is to increase the amount of relative jitter between DQS and DQ during Write operations. To close timing, the power rail noise specifications must be reduced for LPDDR4 to +/-2% on the VDD and +/-5% on the VDDQ. Implementing data bus inversion will make these levels easier to achieve.

Note: For LPDDR4X, the +/-5% guidance applies to the 0.6V supply.

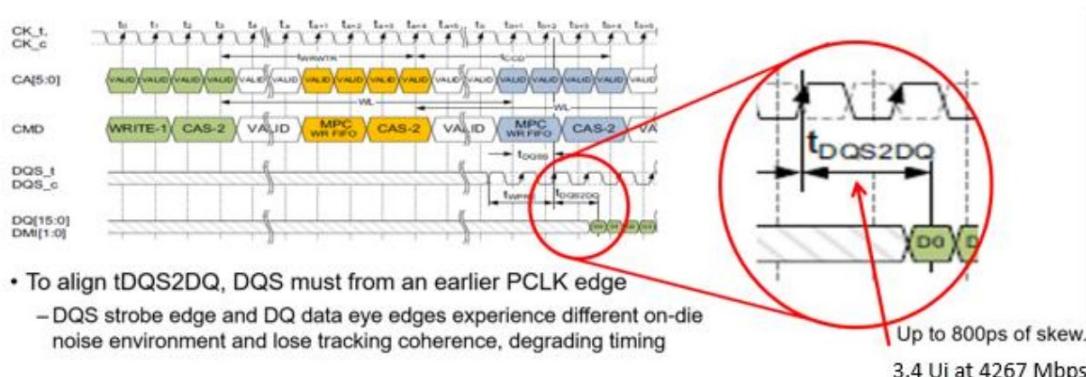


Figure 4 Illustration of tDQS2DQ specification.

1.1.8 Multichannel Architecture

Dual channels in the LPDDR4/4X device give the user many choices for connectivity compared to a single channel device. Each of these configurations have pros and cons in terms of pin usage, bandwidth and ease of implementation. Please refer to Figure 5 though Figure 7 below for connectivity options offered with a single dual channel device.

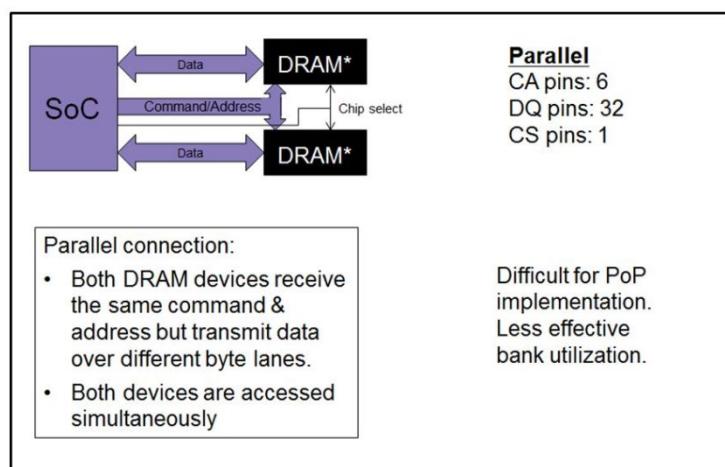


Figure 5 Parallel Configuration.

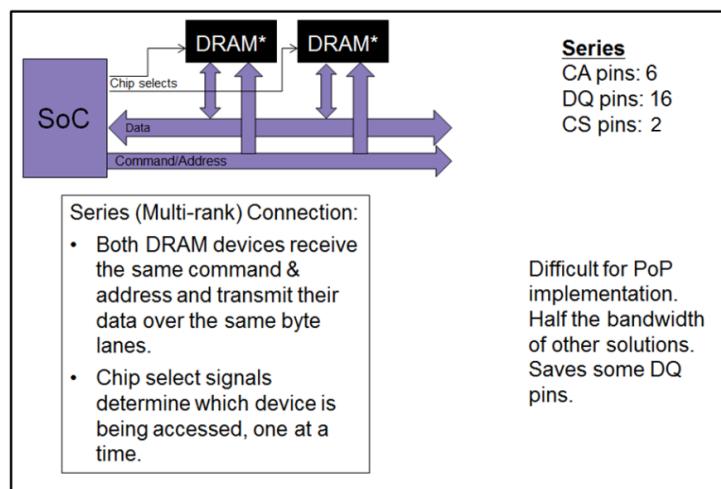


Figure 6 Series Configuration.

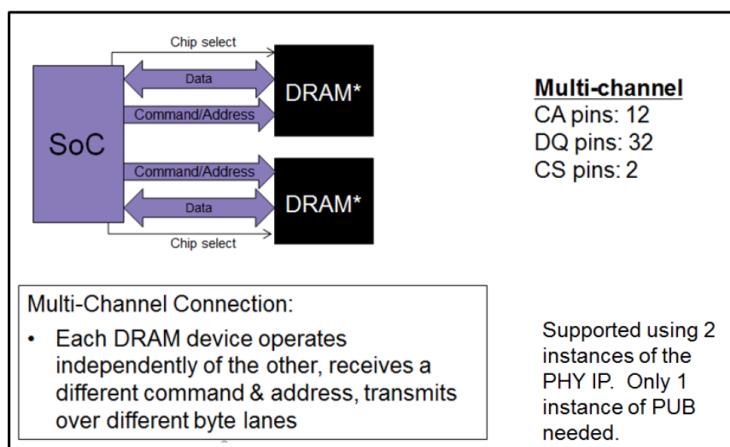


Figure 7 Multichannel Configuration.

1.2 LPDDR4/4X Specific Routing and Implementation Guidelines

1.2.1 Crosstalk Control

Crosstalk and characteristic impedance of an array of traces are interrelated. To minimize crosstalk, the characteristic impedance of a trace should be determined predominantly by the distance to the reference plane and not the distance to the neighboring traces. To achieve this, the space between traces should be 2X to 3X the height of the trace above the ground plane. Longer routed parallel lengths should have wider spacing.

Figure 8 shows three cases that depict this relationship. Case 1 depicts a typical routing scheme with equal lines and spaces. While the Z_0 of these lines looks good at 49.9Ω , much of this impedance is determined by the proximity of the neighboring lines. Consequently, there is very high near end crosstalk from multiple aggressors of 30.8%. For a 1.8V signal, this is 473 mV. For Case 2, where the space is doubled, the Z_0 rises to 54.8Ω and the multi-active crosstalk is cut in half to 15.1%, a more manageable number. In this case, the Z_0 is determined more by the proximity of the reference plane instead the neighboring traces. Further isolation, shown in Case 3, decreases crosstalk with only a 1Ω increase in Z_0 . When increasing spacing has no effect on Z_0 , the traces are said to be isolated.

Note that stripline applications can tolerate narrower spacing within signal groups. Because the fields from all signals are captured within the same dielectric constant substrate, there are no differences in the mode velocities from different switching patterns. If necessary, spacing can be cut to 1.5X to 2X the height to the nearest reference plane in stripline applications.

While this tighter spacing can be used if necessary in stripline, wider spacing is always preferred.

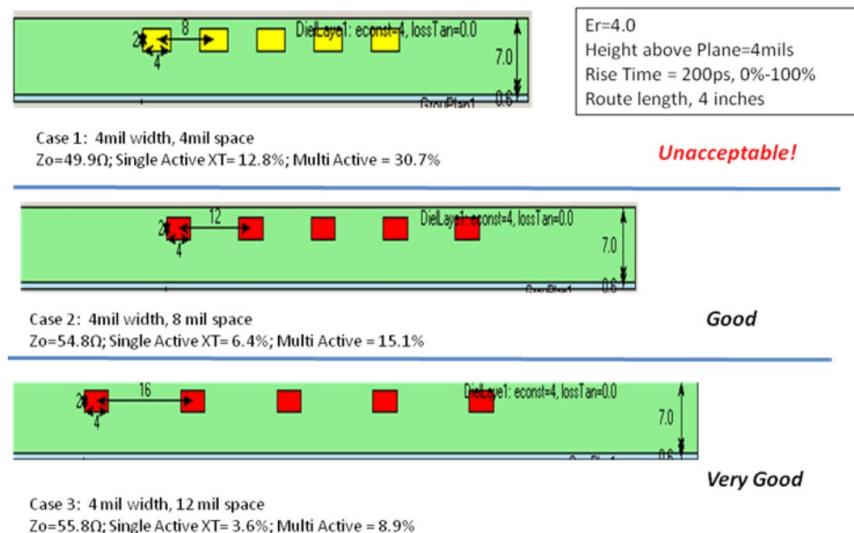


Figure 8 Relationship between Characteristic Impedance and Crosstalk

1.2.2 Stripline vs. Microstrip.

For applications that exceed 1866Mbps, Be careful to use microstrip line. Because of the mixed dielectric materials in a microstrip configuration, different coupled modes will travel at different velocities causing temporal dispersion at the target device. This increases with routed length. Since signals traveling in stripline see a uniform dielectric, the dispersion is greatly reduced. At high bit rates, timing budgets cannot tolerate the margin loss to this modal dispersion. If Microstrip must be used, it should be confined to short lengths with spacing that is greater than 3X the height to the reference plane.

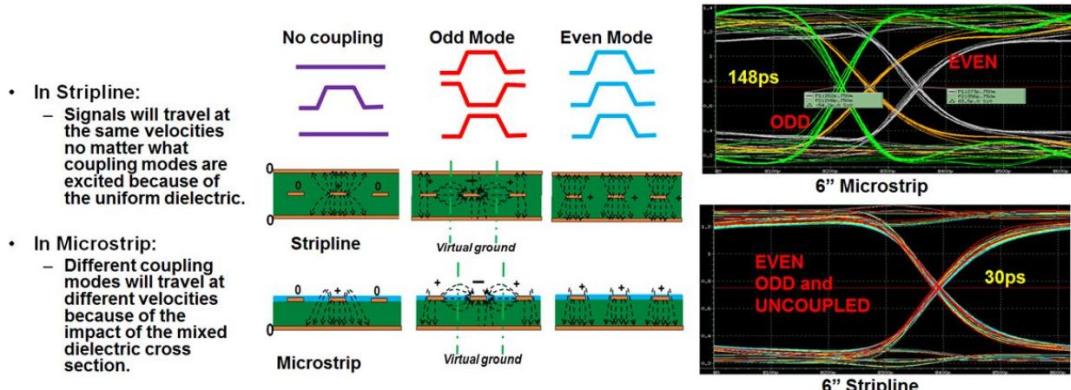


Figure 9 Signal dispersion in microstrip vs. Stripline.

1.2.3 Routing Skew for LPDDR4/4X – Summary and Discussion

There are many trainings available for the LPDDR4/4X interface that can remove skew. The implementer should make every effort to control skews as tightly as possible in order to improve overall operating margins when the interface is trained. This is sound engineering practice and can simplify debugging. Table 1 lists recommended skew targets for LPDDR4/4X. A further discussion of these is found below.

System Routing requirements for LPDDR4/4X 4267 operation			
Constraints	Available Deskew Range	Recommended Routed Skew Limits	Notes
DQ to DQ arrival time mismatch within a byte or nibble	<200ps	<20ps	It is highly recommended that flight times across the data lanes be tightly matched in order to preserve operating margin and reduce vertical eye collapse that can occur from crosstalk between unaligned DQ signals.
DQ to DQS domain	DQS position +/-100ps.	DQS position +/-10ps.	
CS, ODT, CKE, Cmd, Add to CK/CK#	Not applicable	CK position +/-25ps	PHY can be programmed to add delay to 4 bit groups of AC signals to address potential skew violations
DQS to CK domain	-0.5 to +5.47 Clock Cycles	CK edge position +/-60ps. (without Write Leveling)	Write Leveling training can compensate for delay differences that extend over multiple clock cycles.

Table 1 Summary of outing skew requirements for LPDDR4/4X

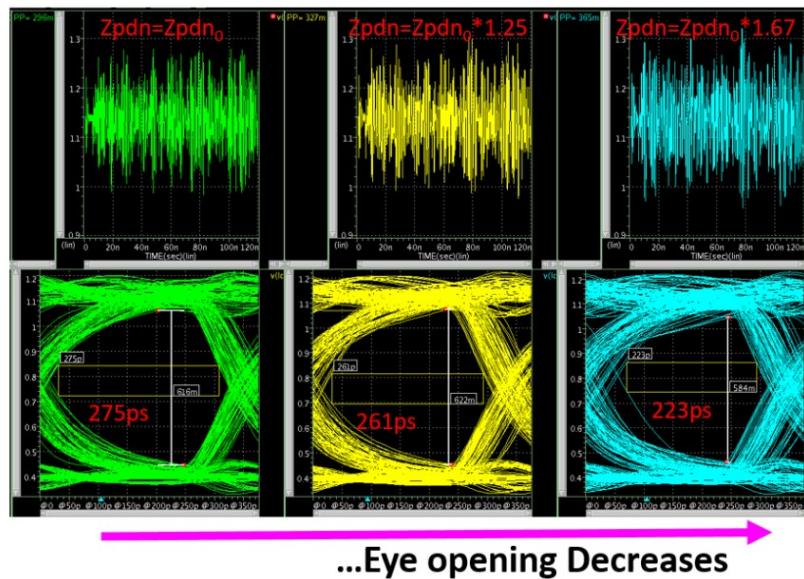
- **DQ and DQS.** For the LPDDR4X MultiPHY , the deskew range is limited to a total of 200ps across the byte lane. At high data rates, skew must be kept to a minimum to avoid center-eye cross-talk. Strongly advocates designing an interconnect with very tight skew control, even with per bit training, +/-10ps skew between the DQ and DQS signals for 2133Mbps and This can be relaxed below this bit rate.
- **Command/Address/Control vs. Clock.** Delay on the command/address bus can be adjusted in 4bit wide groups to reduce the overall skew penalty. A routing tolerance of +/-25ps of all of the signals relative to the CK/CK# should be observed. This can be relaxed if the timing budget and simulation results indicate that there is adequate margin.
- **DQS/DQS# vs. CK/CK#.** For LPDDR4/4X, the specification requirement is that the DQS/DQS# arrive within 0.25 of a clock cycle from CK/CK#. At 3200Mbps, this is +/- 156ps. At the high bit rates associated with LPDDR4, this is usually managed with Write Leveling. If a user chooses to try to operate without Write Leveling, it is recommended that the routed skew between any DQS pair and the clock pair be kept to ½ of the tDQSS budget.

2 LPDDR4/4X Power Integrity Design Guide

2.1 The Scope of Power Integrity

Power integrity as a topic covers the ability of a particular system to maintain its voltage rail as close to ideal DC as possible. Failing that, power integrity is about evaluating the timing impact of any divergence from the ideal voltage level. Figure 10 illustrates how the eye opening at a given bit rate will close as the supply impedance increases. Higher supply impedance means the drawn current will result in more power rail voltage noise. The increased voltage noise will yield increased Power Supply Induced Jitter, PSIJ, that will lead to greater deterioration of the eye opening.

Supply Impedance Increases...



...Eye opening Decreases

Figure 10 supply impedance and the size of the eye opening

Transient variations from the nominal supply voltage will cause signal edges to be delayed with decreases in voltage and arrive early with increases in voltage (Figure 11). This leads to jitter as shown in the figure. Jitter will erode the timing of the memory interface. Jitter related to variations in the supply voltage is described as Power Supply Induced Jitter (PSIJ).

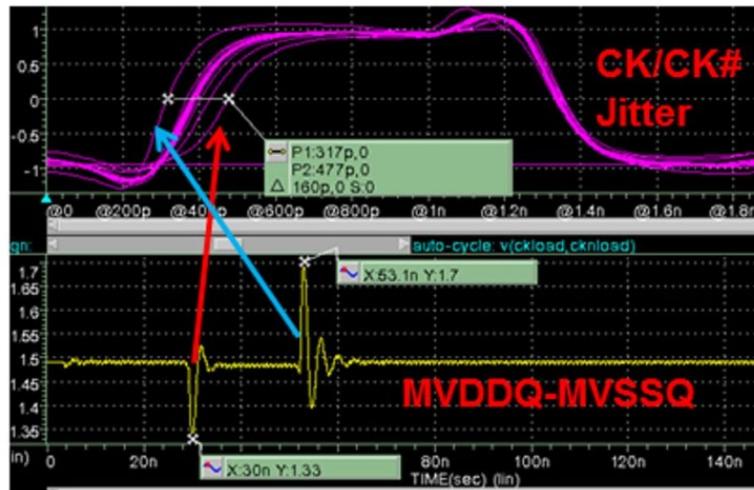


Figure 11 Transient changes in supply voltage lead to clock jitter

To minimize PSIJ, the supply impedance must be kept low to reduce the change in voltage associated with the transient current. Table 1 is a list of memory interface variables that must be considered when determining supply impedance requirements. Starting from a baseline system with power supply induced jitter, of +/- N ps, the table lists the relative change in a particular

interface parameter and the change in supply impedance needed to maintain the PSIJ performance at the same level as the baseline system. Note that Anything that increases currents will require a lower supply impedance. Anything that increases jitter sensitivity will also require a lower supply impedance.

Interface Parameter Impact on Supply Impedance (Zpdn) Requirements			
Parameter Name	Relative Change in Parameter	Change in Zpdn to Maintain Jitter Performance	Comments
Bit Rate	Increase	Decreases	Tighter jitter specs
DC Voltage	Increase	Increases	Lower PSIJ sensitivity outweighs greater current
Interface Width	Increase	Decreases	Greater current. A 72 bit interface will require a proportionally lower Zpdn than a 32 bit interface.
ODT at Target Device	Increase	Decreases	Higher ODT will result in larger signal swing and higher switching currents.
Zsource	Increase	Increases	Higher Source Impedance will generate a lower signal swing with lower switching currents.
Host Silicon Process	Slower	Decreases	Greater PSIJ sensitivity in slower process.
Capacitive Load	increase	Decreases	Greater current draw
Slew Rate	Increase	Decreases	Faster current draw.

Table 2 Parameters that influence supply impedance requirements.

2.2 Supply Noise Requirements.

To control power supply induced jitter effects, the power rail noise of LPDDR4X should adhere to the following conditions:

- VDD: - +/- 2.0% noise
- VDDQ_LP (0.6V): +/- 5% noise
- VDDQ (1.1V): +/- 5% noise

Because of the skew between DQ and DQS defined by tDQS2DQ by the JEDEC standard, power rail noise must be additionally constrained to reduce the resulting jitter.

2.3 Components of the Power Delivery Network

The components of the power delivery network are broken up into five categories that correspond to the frequency range each category impacts. Reference Figure 12 Voltage Regulator Module (VRM) – DC to KHz range.

Bulk Decoupling Capacitors- KHz-MHz range.

- Includes Bulk capacitors in 10uF to 100's uF range and high frequency ceramic capacitors in the 1nF to 10Uf range.

Surface Mount Capacitors (package substrate) - 10KHz to low 100MHz range
 Package Impedance – 100MHz to 200MHz range. The inductance sets the cut

off frequency.

On Die Decoupling – Supplies all of the current in the frequency range above the cutoff frequency determined by the package.

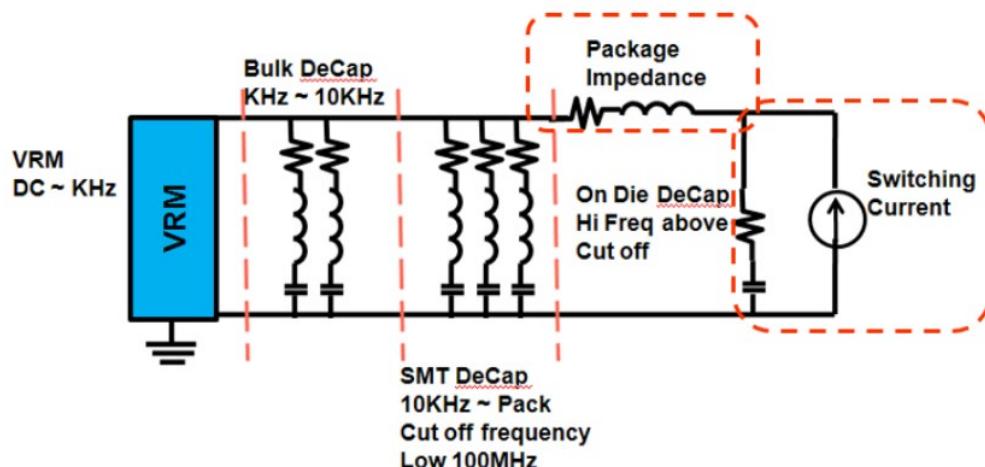


Figure 12 The supply impedance network.

Figure 12 illustrates a typical power distribution network. Each of the components has a different frequency range of effectiveness. It is important that the power distribution network provides low impedance power delivery across the frequency spectrum to control power noise. When impedance is low, large changes in current will only result in small changes in noise. Figure 13 illustrate how the various components of the PDN influence supply impedance at different frequencies. The light blue curve labeled "ALL" is the composite impedance magnitude (Ohms) of all the elements combined vs. frequency. The other curves represent impedance plots of contributions of different power supply network elements vs. frequency. Note that inductive elements like the package only impedance (dark blue curve) increase with increasing frequency. Capacitive elements like on die decoupling caps (or Diecap, green curve) decrease with increasing frequency. The components of the power supply network have different frequency ranges of effectiveness and can be modeled electrically as shown in Figure 14. The next three sections describe the main elements of the power supply network, the voltage regulator, the supply interconnect path, and the decoupling capacitors, and their influences on the overall power impedance.

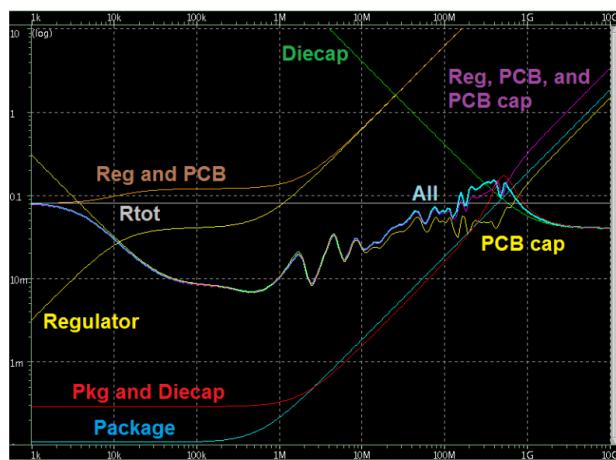


Figure 13 Power network impedance plot.

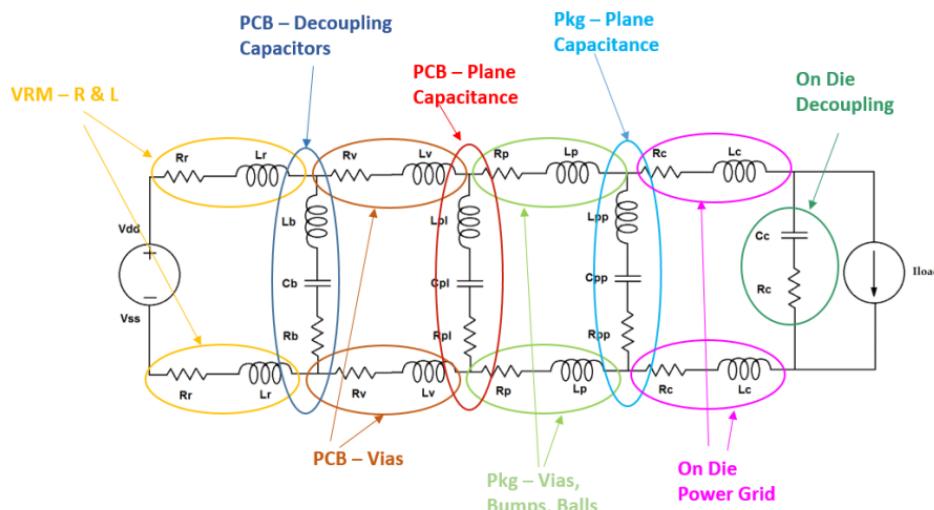


Figure 14 Electrical model of power supply network.

2.3.1 Voltage Regulator

The VRM (Voltage Regulator Module) is typically a brick type module component or integrated circuit on the PCB providing current and regulated voltage for the DDR IO, termination voltage VTT, and Vref voltage of the DDR interface. The VRM circuit is the L_r inductance and R_r resistor (and VDD DC supply) shown on the left side of Figure 15. The VRM will provide low impedance from DC to the low kHz range (Yellow curve labeled “Regulator” in Figure 14). Beyond this frequency, the VRM cannot respond quickly enough to meet the current demands. The regulator and PCB vias cause the low frequency impedance to increase as seen by the brown curve on the impedance

plot labeled “Reg and PCB”. The power supply is typically distributed from the VRM with the use of power and ground plane layers in the PCB. PCB vias are required to connect the VRM to the power and ground balls of the DDR host and SDRAM devices.

2.3.2 PCB Parasitics

Power and ground PCB planes internal to the PCB are used to supply power from the regulator to the device package pins. This is labeled as Lpl, Cpl, and Rpl in Figure 18. In multi-layer PCBs power, ground, and signal vias are used to bring nets from layers other than the top layer to the device balls. These vias need clear-out spaces from the power and ground planes to avoid shorting. These clear-outs (if too big) combined with small power net plane area fills in the pin field region of a high-density chip can increase power plane impedance by reducing the metal available to carry the power supply current. Figure 16 shows an example of a good PCB power plane layout. The power net connections from PCB vias to power plane are shown as green circles and traces to the green power plane. The power vias are well supplied from the power plane metal fill and the clear-outs from other signal vias does not cut off the flow of current from the power plane to the power vias.

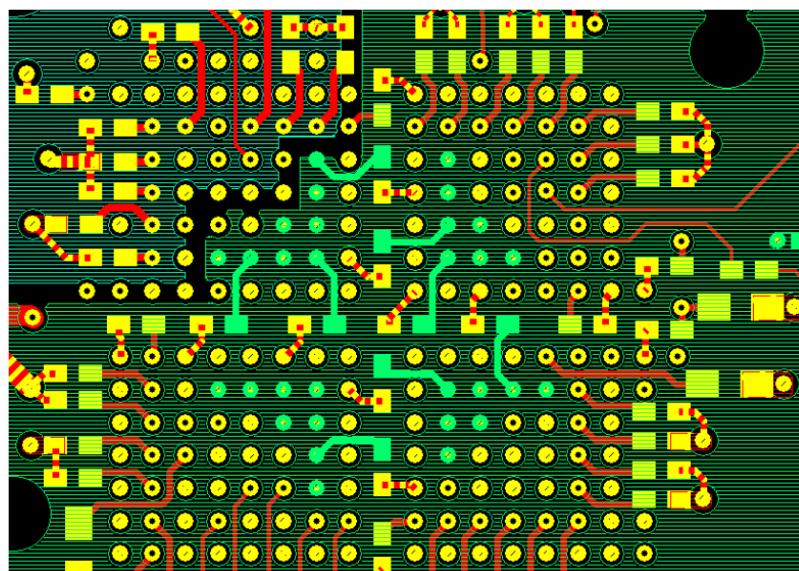


Figure 16 Device Power Plane Connections

The power and ground planes also form a parallel plate capacitor (assuming power and ground planes are adjacent to each other) which can be useful at much higher frequencies than the PCB mounted decoupling caps. The only

drawbacks are the capacitance is small since the size of the plane area is quite small (typical plane cap = 322pF per square inch power plane cap area for a typical board) and the loop inductance of the power and ground vias connecting the planes to the package balls will limit their high frequency effectiveness. The equation for PCB power plane cap is roughly:

$$\text{Power Plane Capacitance} = \frac{8.854 \times 10^{-12} \cdot \epsilon_r \cdot A}{d}$$

where ϵ_r is the relative dielectric constant of the dielectric between the planes, A is the area of the planes in square meters, d is the distance in meters between the planes. A few ways to maximize this capacitance is to keep the distance d between power and ground planes small (use thinner dielectric), use higher dielectric material between the power and ground planes, and increase the A, or area of the planes. One way to maximize plane area is to fill unused plane areas on adjacent routing layers with power and ground plane fill and connect with stitching vias.

3 PCIE GEN3 Signal & Power Integrity Design Guide

3.1 SERDES Differential Channel Guidelines

You must design the package and board with signal integrity (SI) in mind. This chapter details guidelines for the SERDES differential signals. These guidelines are meant to be generic for multiple SERDES products.

3.1.1 Board Guidelines

Check all routes through simulation or measurement for impedance matching, discontinuity, insertion loss, and crosstalk using your specific board interconnect model. The PMA RX and TX s-parameter model is also provided to check for return loss compliance to the given specification.

Important board routing guidelines are listed below:

- In general, use high-speed differential routing guidelines as indicated by the protocol specification.
- Use AC coupling capacitors of 220 nF or as specified by the standard. Some important board guidelines are listed below:
- Route the TX and RX signal routes on different signal layers to avoid Near-End Crosstalk from the TX into the RX lane. If routed on the same layer, make sure that the spacing is more than 6 times the PCB dielectric height, or meet the -30 dB crosstalk requirement.
- Return path should be ground plane and continuous.
- Minimize the crosstalk and accumulated total with all aggressors in phase < -30 dB until Nyquist frequency.
- Length Variation within differential pair should be less than 5 mil.
- Choose trace width and spacing of 90 Ω differential (+/-10%) impedance.
- Choose proper spacing between differential pairs in Stripline and Microstrip to reduce crosstalk.
- Do not route trace over plane void or antipads.
- PCB via transitions can introduce large impedance discontinuity and crosstalk. Differential signal via spacing, antipad size and GND reference via location should be carefully tuned to minimize reflection and crosstalk. Use ground return vias adjacent to the differential pair vias to minimize crosstalk between lanes.
- BGA ball pad, AC coupling cap pad, and large connector finger pads generally introduce large capacitive discontinuities. You can minimize this by voiding the planes below the BGA pads.
- Minimize the PCB via stub by choosing proper routing layer, using blind via or back drilling of via stubs.
- For long channels, take care to minimize insertion loss of trace due to copper loss and dielectric loss. Careful choice of trace geometry, board material, copper roughness are essential to help reduce insertion loss for long route, and maximize signal to noise ratio at receiver.

3.2 Supply Routing for Boards

You must route the power supplies with the following guidelines in mind:

- When possible, put power supply on power planes adjacent to GND reference to minimize PDN impedance
- Ensure that SERDES power is well shielded from other noisy source on PCB to minimize any capacitive or inductive noise coupling.

3.2.1 Board Bypass Capacitors

Supply bypass capacitors are recommended to minimize power supply noise. Simulation of the power delivery network is required to determine the actual values. Depending on their size, each capacitor has a different equivalent series resistance (ESR) and equivalent series inductance (ESL) that determines the given capacitor's effectiveness over a frequency range. In general, several low-value capacitors should be placed as close as possible to the package pins. Larger-value capacitors can be placed farther away.

Connect the supply bypass capacitors as close as possible to the package pins to ensure a tight return path and maximize their effectiveness. When connecting from the package pin to the bypass capacitors, use as wide a plane as possible to reduce both inductive as well as resistive losses. Typical capacitor placement can be under the package in BGA pin field using low inductance attachment, or placed close at the peripheral of BGA on the same side.

The key to get proper PCB decoupling is to have low mounting inductance with proper layout practice, have power plane and closely spaced GND plane for low spread inductance. Capacitor choices are made to suppress resonance in the low/mid frequency range and get as flat and low impedance curve as possible.

3.3 Impact of PCB material loss

This section describes how the PCB loss affects the channel insertion loss and link performance. Channel insertion loss is mainly driven by total etch length and dB/inch loss due to dielectric loss and skin effect. Many factors affect the loss from traces, for example, trace width, copper roughness, and dielectric loss (Df). For high frequency applications, dielectric loss of material has a significant impact. In the following example, a worst case PCB trace length of 12" on the Motherboard and 4" on the add-on card are assumed. Two PCB materials are considered, standard FR4 and Megtron 6, which is a known low-loss material, with a Dk of 3.4 and a Df of 0.004 at 1 GHz. Figure 17 compares the differential insertion loss of the two channels assuming the same interconnect for different PCB materials.

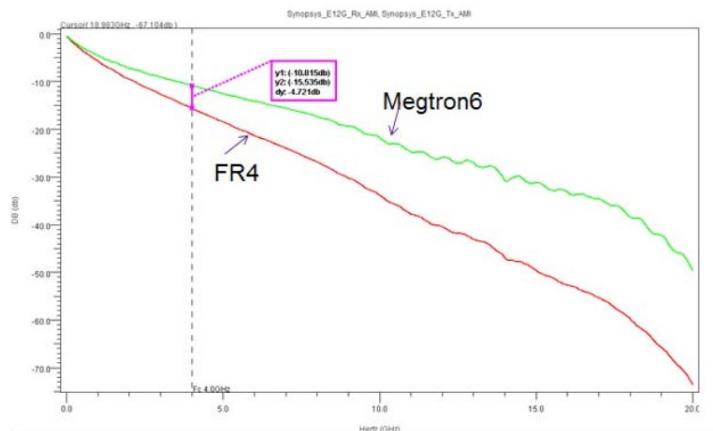


Figure 17 Channel Insertion Loss Comparing FR4 and Megtron 6

There is a difference of approximately 4.7 dB at a Nyquist frequency of 4 GHz. Note that there is not much ripple in the insertion loss curve up to about 15 GHz, which indicates that the return loss is properly managed.

To examine the impact of loss in time domain, an ideal unit interval (UI) pulse is used at the input of the channel or Tx end; Figure 18 shows the output of the channel or Rx end.

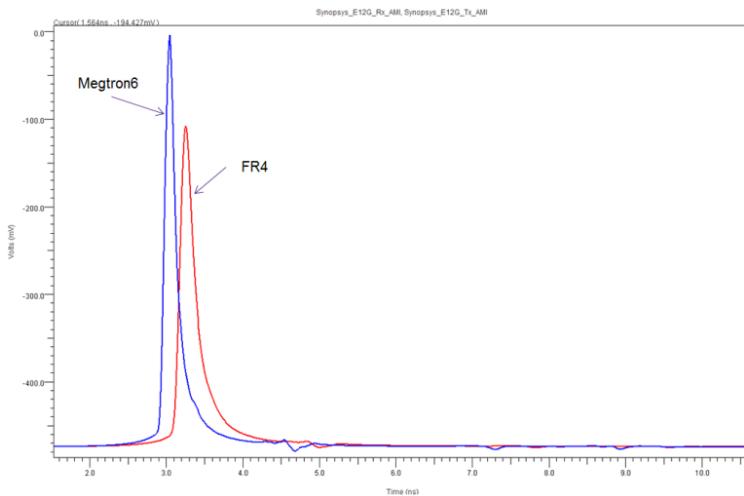


Figure 18 Pulse Response of Passive Channel

This example shows that the FR4 channel has more attenuation with less peak amplitude and also a wider spread of pulse, especially, post cursor or the tail of falling edge which generates inter-symbol interference (ISI) and causes eye closure at the receiver end if not properly compensated. Channel BER simulation with an IBIS AMI model is run with above channel, as shown in Figure 19, with an eye probe both at the input and output of Rx after the AFE/DFE equalization circuit.

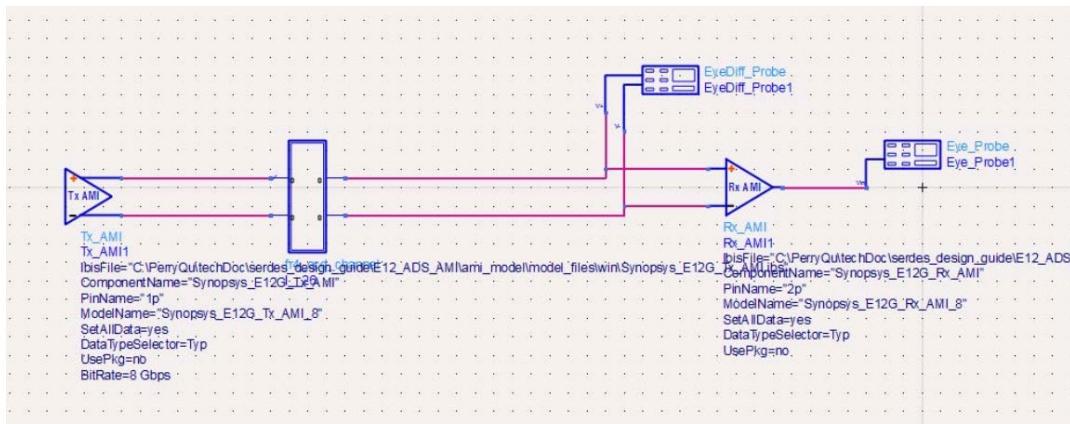


Figure 19 Eye Probe at Input of Rx before Equalization and Output of Rx after Equalization

Figure20 shows the eye plot at the input of Rx receiver assuming that there is no Tx/Rx equalization.

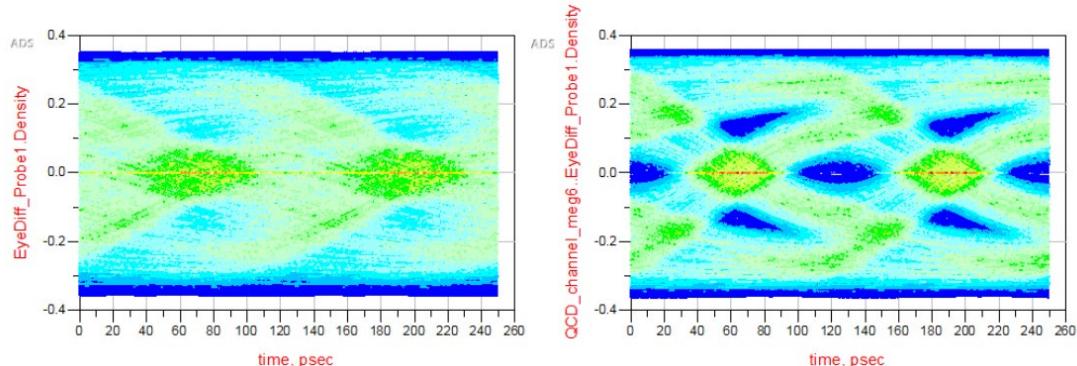


Figure 20 Eye Density Plot at Input of Rx Assuming no Tx/Rx Equalization: Left FR4 Right Megtron 6

Figure20 shows that the eye is completely closed for FR4 channel and better, but still closed for Megtron 6 channel if no Tx/Rx equalization is applied.

If Tx pre and post cursor equalization is turned on with some amount of compensation, an open eye at the input of Rx can be observed (Rx equalization is not in effect at this point), as shown in Figure21.

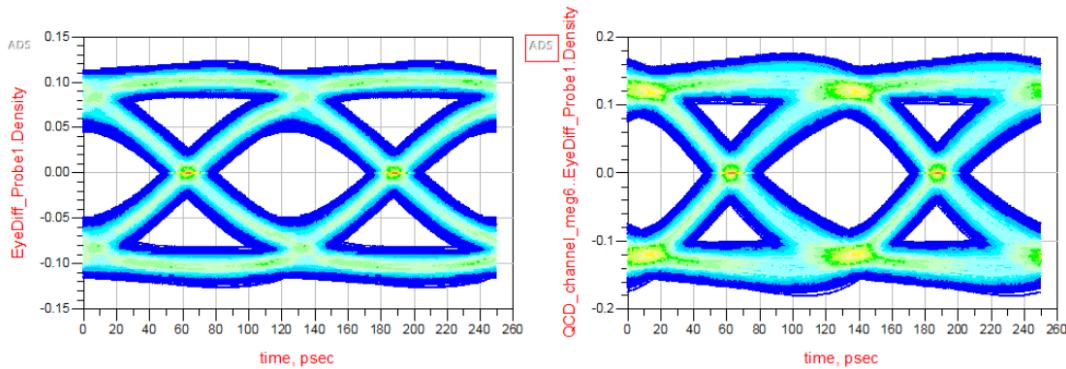


Figure 21 Eye Density at Input of Rx with Tx Pre/Post Cursor Equalization: Left FR4 Right Megtron 6
 As shown in Figure21, Megtron 6 channels show better eye height in comparison, so, Tx equalization can be helpful in dealing with ISI generated by interconnect loss.

In large systems, particularly backplane applications, the total PCB trace length can increase significantly resulting in an increased insertion loss. For those applications, the benefits of low loss material can be critical in ensuring low BER, as signal to noise ratio is reduced due to high loss. To demonstrate the effect of material loss for long channel, the trace length in the PCIe channel was increased so a -30 dB loss at Nyquist frequency for FR4 channel was observed. The channel loss of Megtron 6 channel was derived for the same length as shown in Figure 22. There is a gain of about 9.5 dB using a low loss material assuming same trace geometry and same trace length.

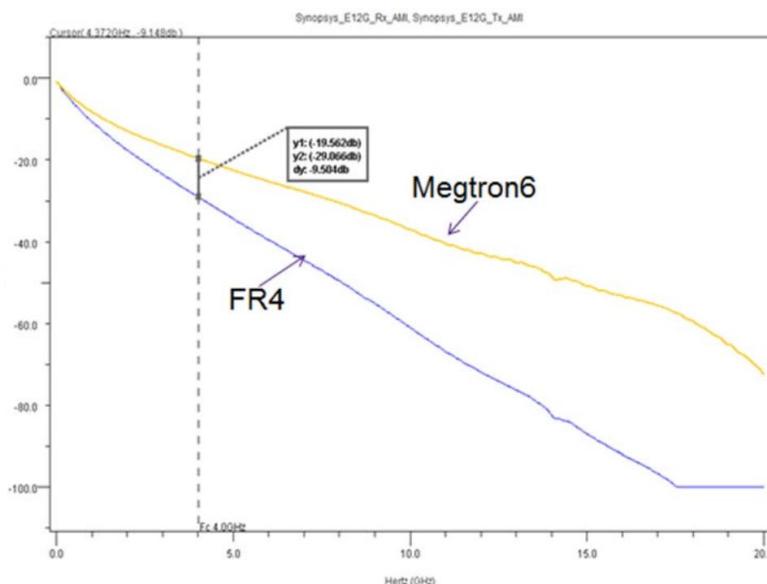


Figure 22 Hypothetical Loss Channel FR4 versus Megtron 6

Optimized BER 1E-12 contours with Tx/Rx equalization are shown in Figure 23.

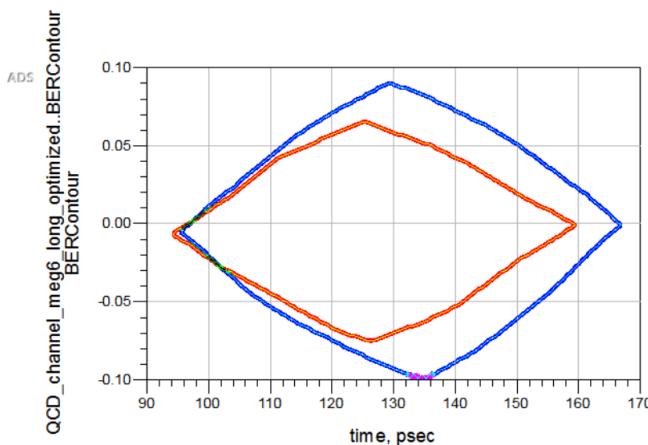


Figure 23 BER 1E-12 Contour at DFE Output FR4 (Red) versus Megtron 6 (Blue)

This shows the advantage of having low loss material with better signal to noise ratio at receiver.

Note the following additional factors that also affect PCB trace loss:

- Copper roughness: An increased copper surface can have a significant effect on loss per inch. This is because the additional skin effect loss due to increased copper surface can negate the benefit of low loss material and significantly affect the loss per inch. To get accurate estimates of trace loss, copper roughness must be taken into account and verified with PCB vendors.
- Trace width and spacing: A wider trace generally improves loss to a certain extent. Proper design has to balance trace loss with routing density, as wider trace means more routing space needed. Optimization should be done to get the best tradeoff between loss and routing density.
- Transmission line type Microstrip versus Stripline: A Microstrip line with trace on the surface without solder mask has less loss per inch compared to a Stripline with similar dimension and material, as Microstrip is surrounded by non-uniform dielectrics which is partially air with no dielectric loss. However, solder mask coating on top of the Microstrip, which is widely used in production PCB, significantly increases the loss, especially for the low loss material, because solder mask coating has high tangent loss.

3.4 Impact of Interconnect Discontinuity

An important factor for SERDES interconnect design is the discontinuity when a signal travels from the transmitter through packaging, via, connector, and arrives at the receiver. Impedance discontinuity usually occurs when there is a change of trace impedance, or when there is a disruption of the return path such

as a transition from trace to via. A reflected pulse causes additional ISI and eye closure which cannot be compensated by Tx/Rx equalization circuit. For a successful link design, it is crucial to have reflection and return loss under control. In the following sections, common causes of reflection and its impact on the link performance is analyzed.

3.4.1 Via Stub

To demonstrate the impact of discontinuity, this example uses the topology used the PCB trace on the motherboard and add-on card to 6" and 2", respectively. The AC coupling cap is added with two more vias, to emulate the scenario where the AC coupling caps are placed about 1" away from Tx, and Stripline routing/vias are required from the TX BGA breakout to the AC capacitor, as shown in Figure 24.

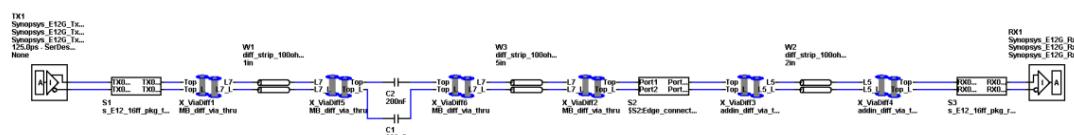


Figure 24 Schematic Topology of Shorter PCIe Link with AC Coupling Capacitor

To examine the impact of reflection on the link performance, two scenarios are compared:

- A topology built with the same interconnect elements, except a via with long stubs is present on both the motherboard and the add-on card, as shown in Figure 25. There is a through hole via from the top to the bottom layer but the signal exit layer is on layer 2 with a long stub between layer 2 and the bottom side, as opposed to layer 7 with a minimum via stub in the previous via model.

1	Dielectric	1.0
2	Top	Signal 0.6
3	Dielectric	5.0
4	P1	Plane 0.6
5	Dielectric	5.0
6	L2	Signal 0.6
7	Dielectric	5.0
8	P2	Plane 0.6
9	Dielectric	5.0
10	L3	Signal 0.6
11	Dielectric	5.0
12	P3	Plane 0.6
13	Dielectric	5.0
14	L4	Signal 0.6
15	Dielectric	5.0
16	P4	Plane 0.6
17	Dielectric	38.0
18	P5	Plane 0.6
19	Dielectric	5.0
20	L5	Signal 0.6
21	Dielectric	5.0
22	P6	Plane 0.6
23	Dielectric	5.0
24	L6	Signal 0.6
25	Dielectric	5.0
26	P7	Plane 0.6
27	Dielectric	5.0
28	L7	Signal 0.6
29	Dielectric	5.0
30	P8	Plane 0.6
31	Dielectric	5.0
32	Bottom	Signal 0.6
33	Dielectric	1.0

Figure 25 Long Via Stub on Mother Board

Figure 26 shows the channel differential insertion loss and return loss comparing a short stub via with a long stub.

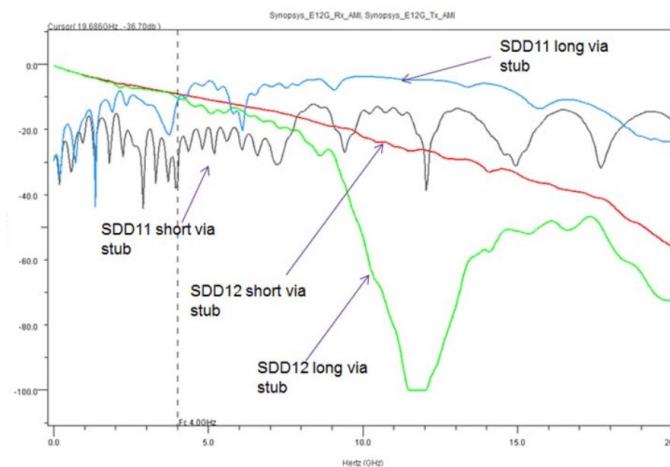


Figure 26 Comparing Channel Insertion Loss and Return Loss for Through Hole Via with Long and Short Stub

Figure 26 shows that the long via stub caused significant reflection and resonance in the insertion loss that resulted in a large dip. This resonance frequency is directly linked to the length of the stub, so the layer where the signal exits and total PCB thickness affects the resonance frequency. For a thick board, for example a backplane, this resonance frequency shifts to the lower end and causes a worse degradation of insertion loss close to the fundamental frequency of the link and its harmonics.

Figure 27 shows the response at the receiving side of the time domain response

of the channel with an ideal unit interval pulse.

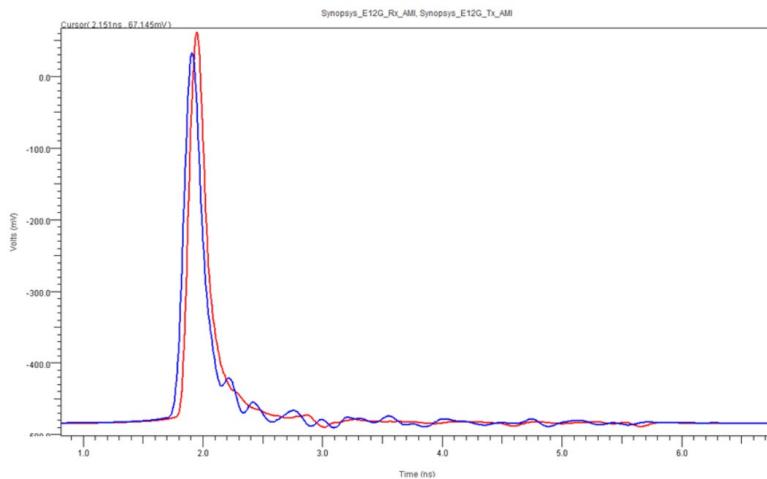


Figure 27 Pulse Response of Long Stub Via Channel (Blue) versus Short Stub Via Channel (Red)

There is a slight amplitude degradation of the main cursor for the long via stub channel. There are more small ripples in the long stub channel response due to multiple reflections from long stub vias in the link.

These ripples can add or subtract from main cursor depending on the data pattern, and generate ISI and eye closure at the receiving side. These reflections cannot be compensated by an equalization circuit. The final simulation in this section shows the eye contour degradation at BER 1E-12, as shown in Figure 28:

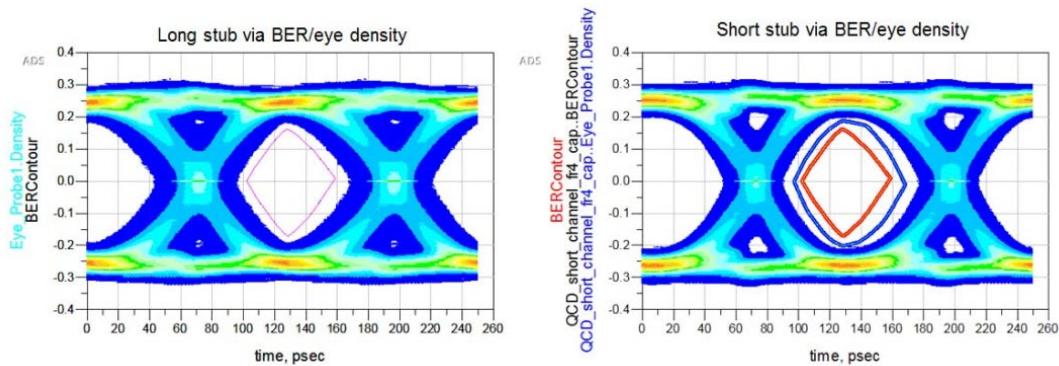


Figure 28 BER Contour and Eye Density of Short Stub Via Channel versus Long Stub Via Channel

On the right side of the plot, the eye contour of BER 1E-12 of both long stub via channel (red) and short stub via channel (blue) are shown for comparison. The degradation of eye height and width is significant and reduces the operation margin in presence of other noise source.

In practical design, there are situations where escape on upper layers of PCB not avoidable due to routing density. In such a case, backdrilling of via is a

viable option to minimize the via stub and maintain good signal integrity.

3.4.2 Via Antipad

Cutout on ground and power planes around signal vias (antipad) are other factors that can affect reflection. Capacitive coupling between the via pad and the cylinder wall and copper planes results in excessive capacitance and lowers equivalent impedance of vias which results in reflection. When the antipad diameter increases, both the capacitive coupling and reflection are reduced. Beyond a threshold of antipad dimension, the benefit tapers off. Long vias in a thick PCB or large vias, for example, a plated through hole via for backplane connector pins, benefit more from antipad optimization. It is advised to use a 3D full wave electromagnetic field solver to simulate and to choose the proper antipad dimension taking into account the via discontinuity, reference plane continuity, and power integrity due to Swiss cheese effect.

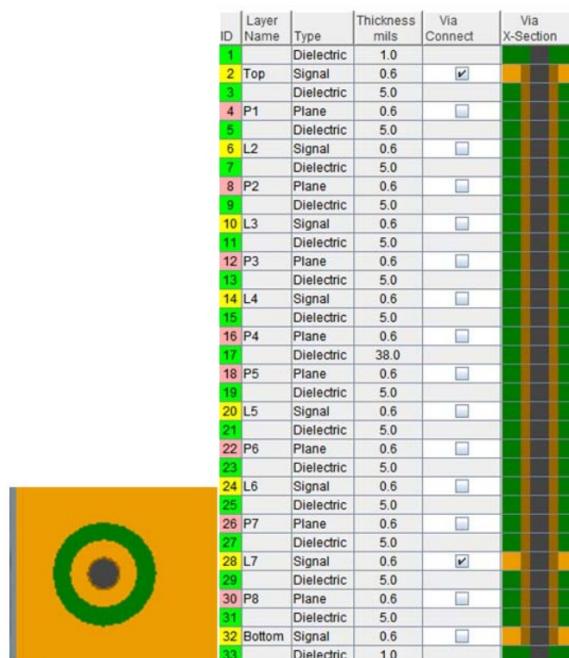


Figure 29 Single-Ended Via with Default Antipad Clearance

Figure 30 shows the circuit topology with a single-ended via with default antipad clearance.

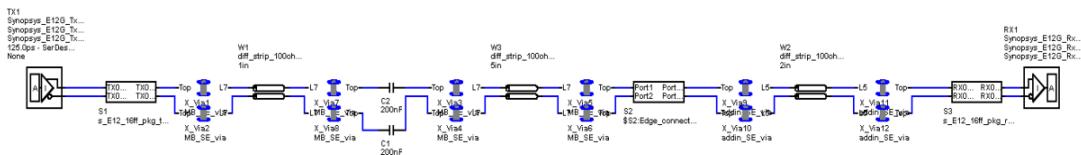


Figure 30 Circuit Topology with Single-Ended Via

Figure 31 shows the insertion loss and the return loss of topology using optimized via versus a single ended via.

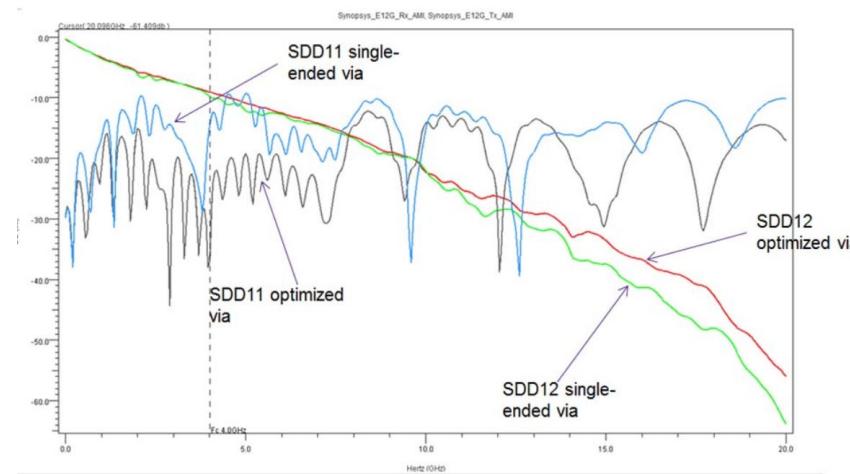


Figure 31 Differential Insertion Loss of Channel with Optimized Via versus Single-Ended Via

Figure 31 shows that the return loss of a channel using a single-ended via is worse compared to a channel with an optimized via. The ripples in its insertion loss curve as a result of the reflections.

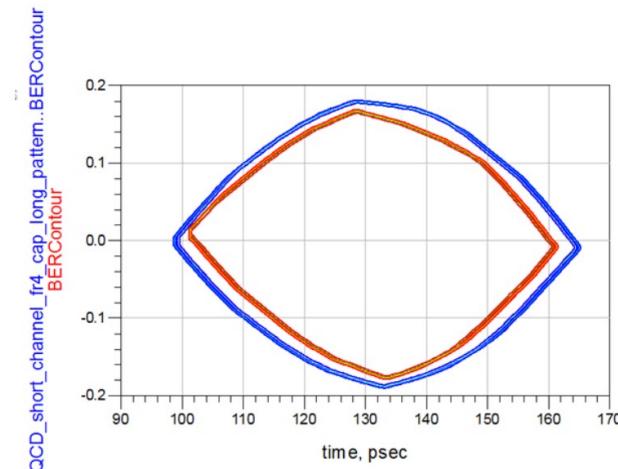


Figure 32 BER Contour at 1E-12 Comparing Optimized Via (Blue) versus Single-Ended Via (Red)

The eye opening is reduced for the case with a single-ended via and reduces the operation margin. The impact is significant as speed is increased and again the degradation is not compensated by a Tx/Rx equalization circuit.

3.4.3 Additional aspects of reflection control on PCB

The following optimizations are needed for additional cases:

- Cutout under AC coupling capacitor pads and large connector finger pads: When an AC coupling capacitor is used, there is capacitive coupling between the GND plane underneath, the pads/capacitor body, among others. This excessive capacitance degrades the channel return loss similar to what is referred for via channel degradation. The cutout underneath the pads should be optimized to improve reflection as shown in Figure 33. The same principle applies to a connector footprint with a large finger pad, as for example, a PCIe edge connector.

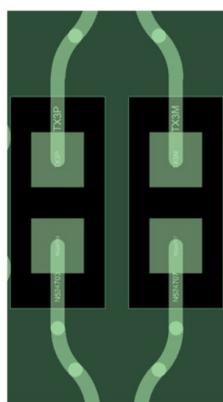


Figure 33 Cutout of GND Planes under AC Coupling Cap Pads

3.5 Crosstalk

Crosstalk is an important design consideration for SERDES implementation. It is common to have multiple Tx and Rx lanes on a packaging substrate and a PCB concentrated in a limited space, and therefore, proper care must be taken to minimize the crosstalk from the interconnect in order to achieve good signal integrity performance.

Crosstalk exists on several interconnect elements such as:

- Packaging substrate
- PCB breakout
- Vias
- Traces

■ Connectors

3.5.1 Far End and Near End Crosstalk

Far end crosstalk refers to SERDES pairs that travel in the same direction, and crosstalk from the Tx of an adjacent aggressor pair to the Rx of a victim pair. For example, assume Tx1/Rx1 is the victim pair in Figure 34. FEXT refers to crosstalk from Tx2 and Tx3 to Rx1. Near end crosstalk refers to the SERDES pair that travels in the opposite directions, and the Tx of the aggressor pair coupled to a nearby SERDES pair Rx, as shown in Figure 35.

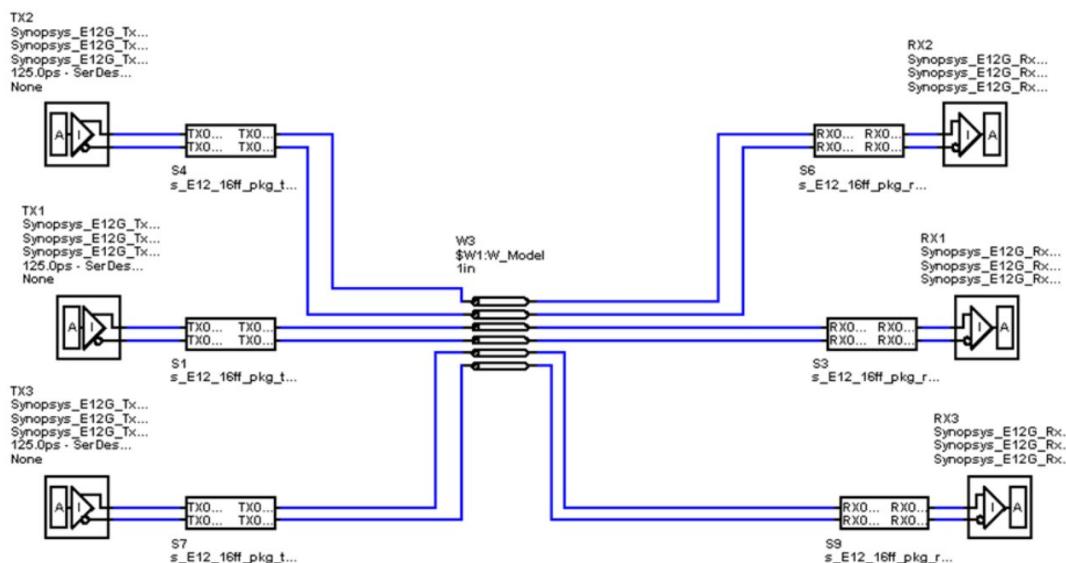


Figure 34 Far End Crosstalk (FEXT)

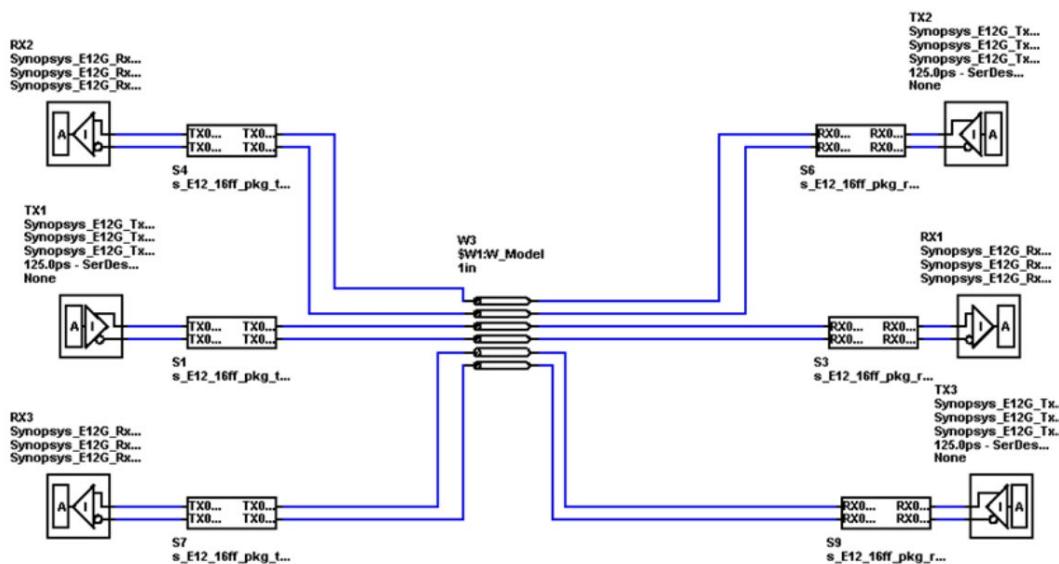


Figure 35 Near End Crosstalk (NEXT)

In general, near end crosstalk is a particular concern for long lossy channels because when a strong Tx signal is coupled to a weak victim Rx signal after channel attenuation, the signal to noise ratio at Rx of the victim pair may drop significantly making it impossible to achieve an open eye.

3.5.2 Crosstalk due to PCB Traces

The following factors that must be considered regarding crosstalk due to PCB traces:

- Far end and near end crosstalk (FEXT or NEXT) are as explained in 3.5.1 "Far End and Near End Crosstalk"
- Microstrip versus Stripline: As shown in Figure 36, a Microstrip refers to traces on outer layers of the PCB, with a reference plane underneath and surrounded by mixed dielectrics (air on top and dielectric material below). In most applications, there is also a thin layer of solder mask on top of the trace (not shown in this example), which impact its impedance and loss. Stripline refers to traces sandwiched by the two reference planes, and submerged in the dielectric material that has very similar dielectric properties. Given the difference in constructions, Microstrip and stripline have very different electrical characteristics in terms of loss and crosstalk. For a stripline, assuming dielectric constant for layers involved are identical, far end crosstalk is very small. For a Microstrip, far end crosstalk is a concern as it is affected by both spacing and coupled length. A Microstrip also has a worse near end crosstalk compared to a stripline. The following section examines the difference through some

simulations.

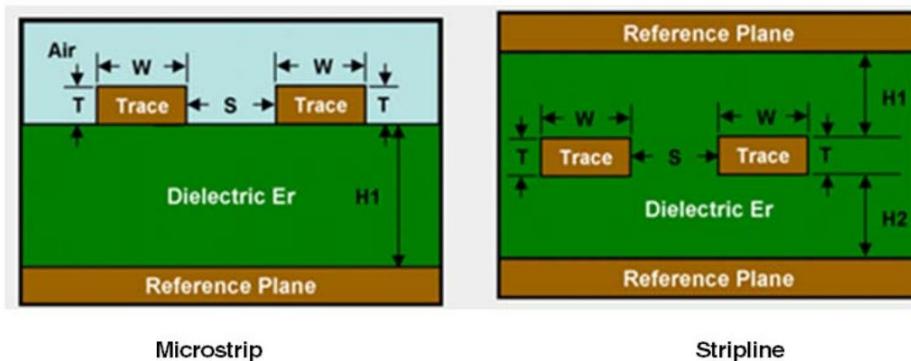


Figure 36 Illustration of Microstrip and Stripline

3.5.3 Far End Crosstalk Stripline and Microstrip

Figure 37 examines the impact of FEXT from a Stripline and a Microstrip line, and includes two aggressors and a coupled transmission line. The Tx1 to Rx1 link is the victim pair, two symmetrical aggressor links Tx2/Rx2 and Tx3/Rx3 sandwich the victim pair, and exercise crosstalk through PCB traces. Traces on the motherboard from Tx to AC decoupling capacitor and from capacitor to connector are coupled to the transmission line where crosstalk happens. The spacing between pairs is about 15 mil or three times the dielectric height, and both the Microstrip and the Stripline are simulated to observe the far end crosstalk at Rx side.

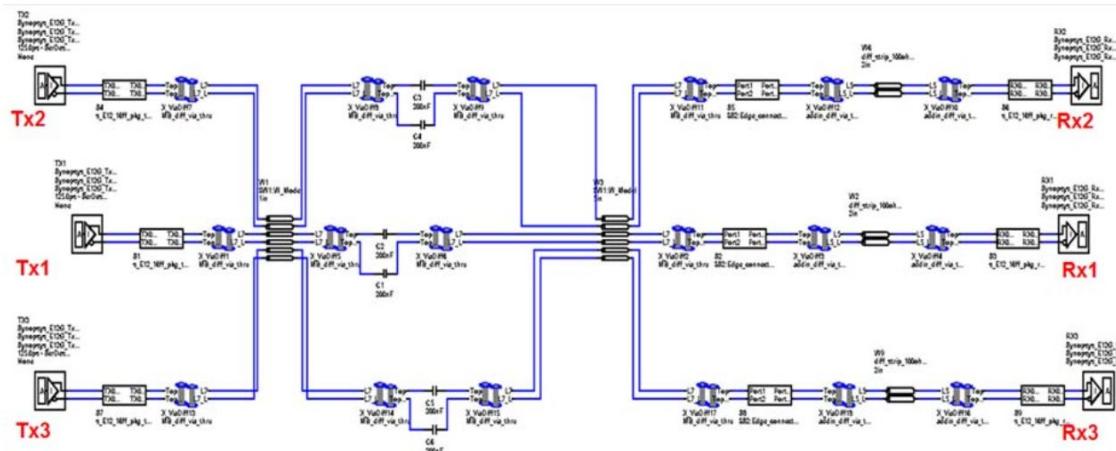


Figure 37 FEXT Example Stripline and Microstrip

Figure 38 shows the differential mode crosstalk in frequency domain from Tx2 to Rx1, which is FEXT as explained in “Far End and Near End Crosstalk”.

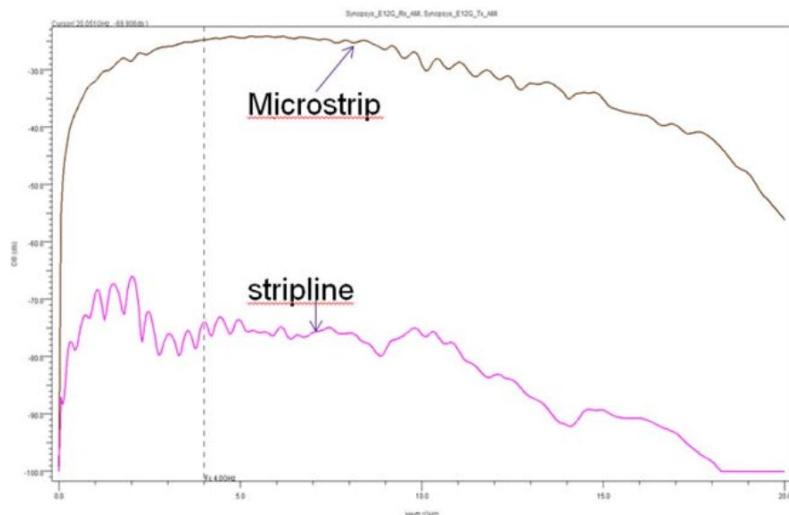


Figure 38 FEXT Microstrip vs stripline frequency domain

Figure 38 shows that the FEXT crosstalk for a Stripline is very small but for Microstrip it is not negligible. Note that, in the case of Microstrip, FEXT depends on both spacing between pairs and the length of parallel running.

Figure 39 shows a channel simulation using an IBIS AMI model with aggressors, using the channel model that includes crosstalk coupling from traces.

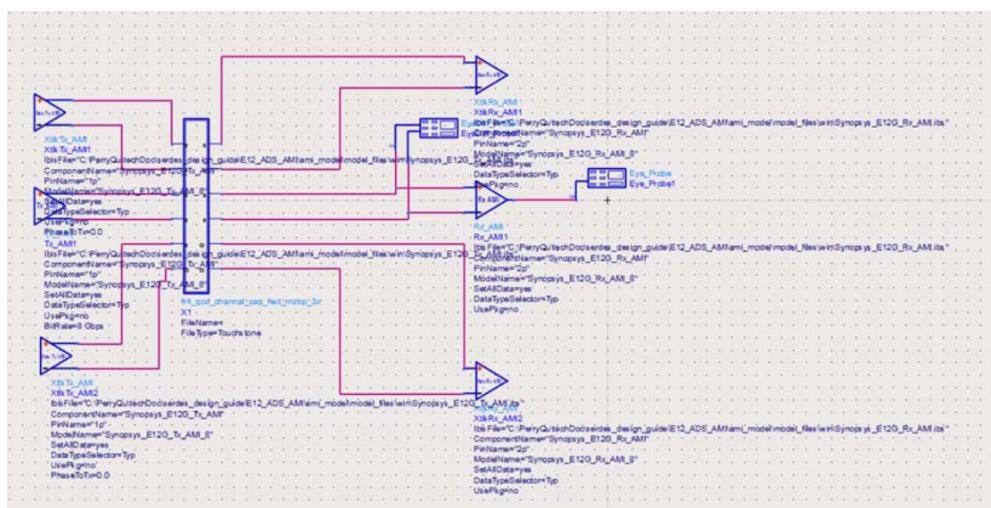


Figure 39 FEXT Simulation in ADS using IBIS AMI Model

Figure 40 shows the BER contour at 1E-12 with and without FEXT for a Microstrip (right) and a Stripline (left). The BER of the link without the crosstalk is shown in red for comparison. Figure 40 shows a visible degradation of the horizontal eye opening in the case of FEXT from a Microstrip, while in the case of a Stripline, the impact of FEXT is negligible. It shows that, three time spacing and 6" parallel run of a Microstrip results in significant FEXT. So, to reduce the

crosstalk to acceptable level, it is necessary to increase pair to pair spacing and/or decrease parallel run length.

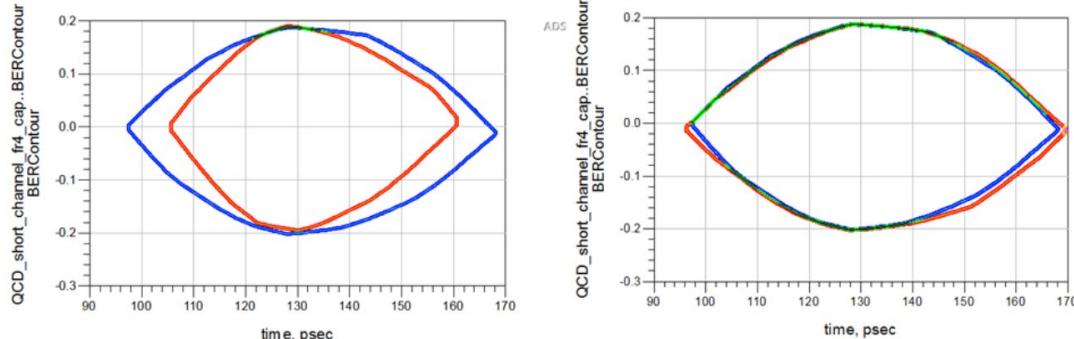


Figure 40 Eye contour at BER 1E-12 with and without FEXT

3.5.4 Near End Crosstalk Example

Figure 41 shows the topology for NEXT simulation. The traces on add-on card have two near end aggressors with coupling to the center victim pair. Both the Microstrip and the Stripline models are explored in this example to analyze the NEXT from TX2/3 to Rx1.

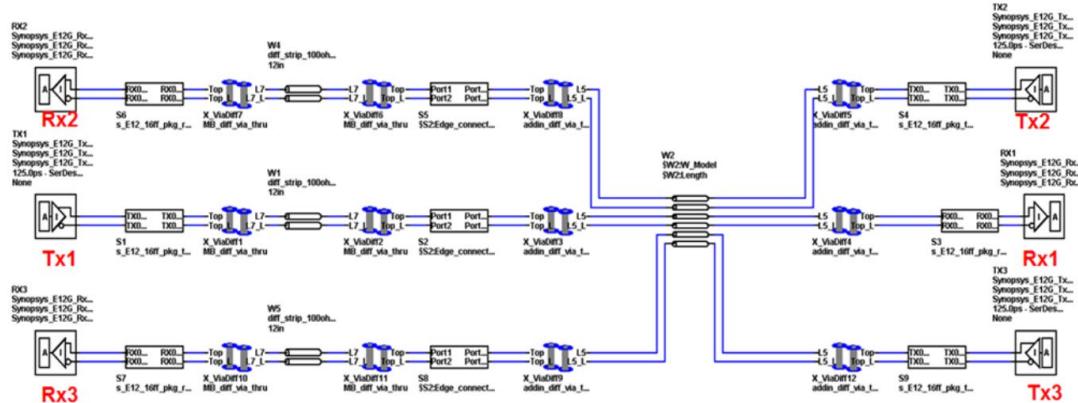


Figure 41 NEXT Topology

Figure 42 shows the NEXT from Tx2/3 to Rx1 in frequency domain.

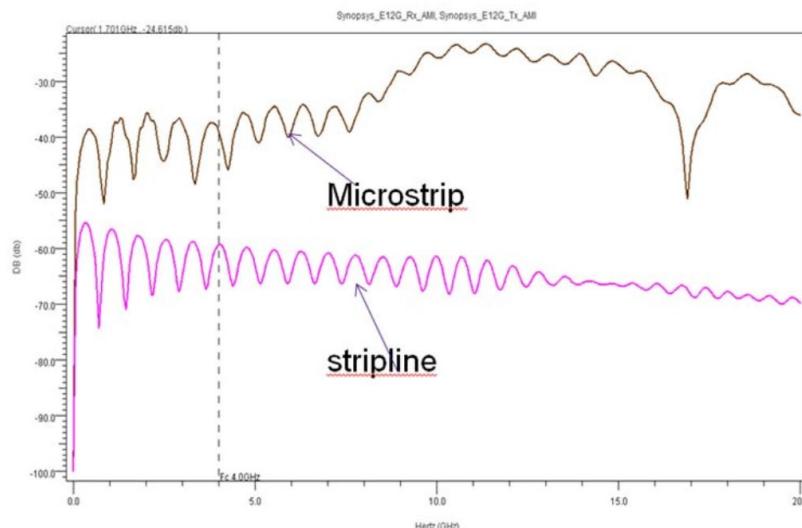


Figure 42 NEXT in Frequency Domain Microstrip versus Stripline

Channel BER simulation is also run with NEXT included, as shown in the following topology in ADS.

Figure 43 shows BER with and without NEXT for Microstrip (right) and Stripline (left). In both, plot BER without crosstalk is shown in red.

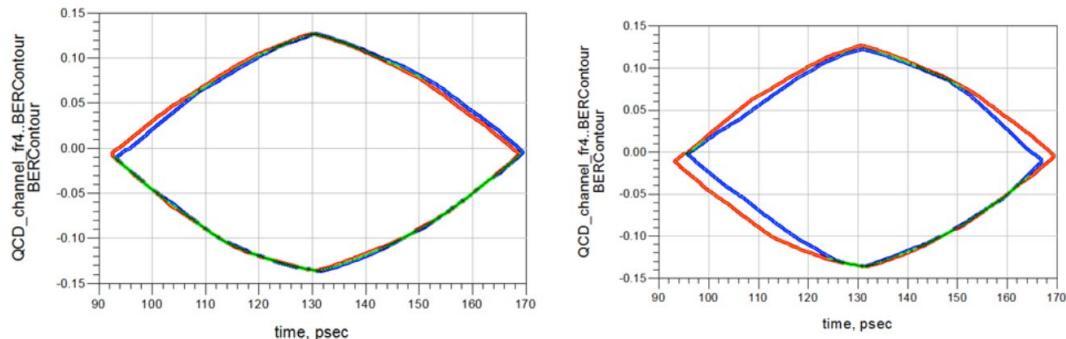


Figure 43 BER 1E-12 Contour with and without NEXT Microstrip versus Stripline

In this example, the Microstrip shows some eye degradation due to NEXT but the Stripline does not. In practical design, care must be exercised to minimize NEXT and proper design rules must be checked taking into account the data bit rate and insertion loss to crosstalk ratio as a longer channel requires more stringent crosstalk control.

3.5.5 Crosstalk of Vertical Interconnect

When a signal differential pair has to transit to another layer, discontinuity is

introduced on the signal return path and, as a result, both near end and far end crosstalk can be induced at these vertical transitions. These transitions can be seen on:

- PCB from the BGA ball of one device to the BGA ball of another device
- One PCB to another PCB through a connector

If not properly designed, these vertical transitions can cause significant near end or far end crosstalk compared to signal traces.

Note the following guidelines on designing transitions:

- Maintain proper GND reference, for example, GND vias besides signal vias.
- Proper isolation and spacing of the Tx vias and the Rx vias are critical to achieve low NEXT.
- Crosstalk is proportional to the length of vias, so, shorter vias have better performance.

Figure 44 shows an example of a well-planned via pattern to minimize the crosstalk from vias associated with a PCIe connector. Here, blue vias are GND, red vias are Rx pairs, and green vias are Tx pairs. By placing GND vias between Tx pairs and between Rx pairs, far end crosstalk is minimized. A Tx via pair and an Rx via pair are almost orthogonal to each other, which helps to reduce magnetic coupling and minimizes near end crosstalk. Similar principles can be applied on a BGA ball out pattern or substrate core via pattern.

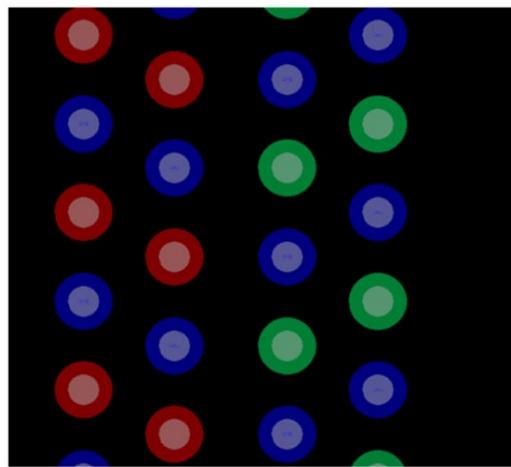


Figure 44 Via Pattern of a Generic PCIe Connector