

# **SG2300X Layout Design Guide**

**Version:** 1.0

**Release date:** 2022-07-13

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## Document Revision History

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Revision	Date	Author	Description
1.0	2022/07/13	Luoping	First Version
1.1	2023/04/13	Xuxinwen	Add RGMII

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# 1 PCB Layout Design Guide

## 1.1 PCB Stackup Design Considerations

The PCB stackup design plays a central part in the overall system performance, especially with high-performance ICs. The PCB stackup is the substrate upon which all design components are assembled. A poorly designed PCB stackup with inappropriately selected materials can degrade the electrical performance of signal transmission, power delivery, manufacturability, and long term reliability of the finished product. To successfully design PCB stackups for IC designs, you must have a good understanding of both PCB construction and the factors that influence material selection and cost.

### 1.1.1 PCB Stackup and Via Description

A typical PCB stackup is constructed from multiple alternating layers of core, prepreg, and copper foil materials heat-pressed and glued together. Recommend stackup is illustrated in Figure1.

	Layer Stack up	Thickness (mil)
	Silk Top	Default
	Solder Top	
TOP		1/3oz+plating
PREPREG		3.00
ART02		1/3oz+plating
PREPREG		2.10
ART03		1/3oz+plating
PREPREG		2.10
ART04		1/3oz+plating
PREPREG		2.10
ART05		1/3oz+plating
PREPREG		2.10
ART06		1/3oz+plating
PREPREG		1.95
ART07		1/3oz+plating
CORE		21.00
ART08		1/3oz+plating
PREPREG		1.95
ART09		1/3oz+plating
PREPREG		2.10
ART10		1/3oz+plating
PREPREG		2.10
ART11		1/3oz+plating
PREPREG		2.10
ART12		1/3oz+plating
PREPREG		2.10
ART13		1/3oz+plating
PREPREG		3.00
BOTTOM		1/3oz+plating
	Solder Bot	Default
	Silk Bot	
		Total Thickness: 1.60mm

Figure 1 PCB Stackup

Via description is shown in table1.

**Table 1 Via Description**

Via Parameter	Micro Laser Via	Buired Mechanical Via	Plated Through Via
Via name(start layer to end layer)	VIA1-2, VIA1-3 etc.	VIA7-8	VIA1-14
Drill diameter	4mil	8mil	8mil
Capture pad diameter	10mil	16mil	16mil

### 1.1.2 Material Selection

There are LPDDR4 and PCIE high speed data in chip . Material loss becomes very important and controlled dielectric construction must be considered during the design process. To mitigate loss caused by the material, the following material parameters must be considered during the material selection process:

- Relative Dielectric Constant
- Loss Tangent
- Fiberglass Weave Composition
- Skin Effect

These material parameters have significant impact on the electrical properties. Therefore, you should consider them as critical parameters during the stackup design.

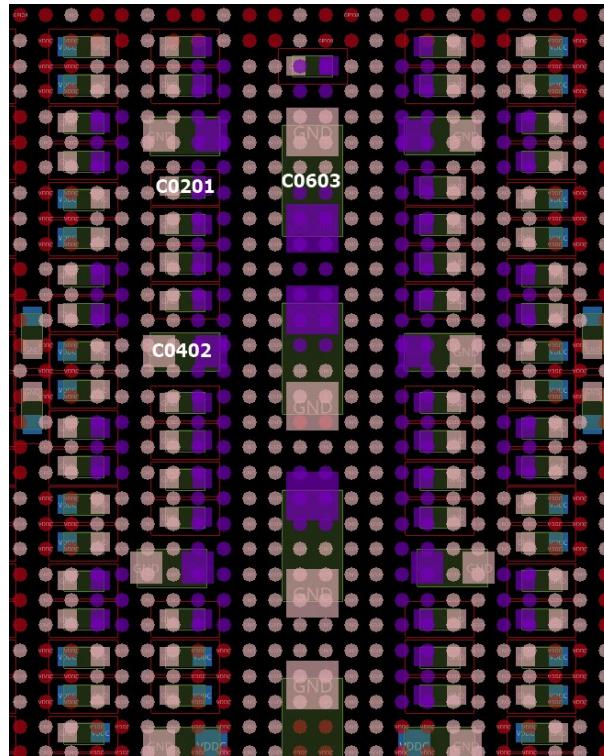
It is recommend that middle loss material EM-370(Z) is used for SG2300X stackup constration. It is avoid to use 106 woven glass style material for high speed trace layers.

## 1.2 Core Power Design and Capacitor Placement

### 1.2.1 VDD\_TPU

#### 1.2.1.1 VDD\_TPU Capacitor Placement

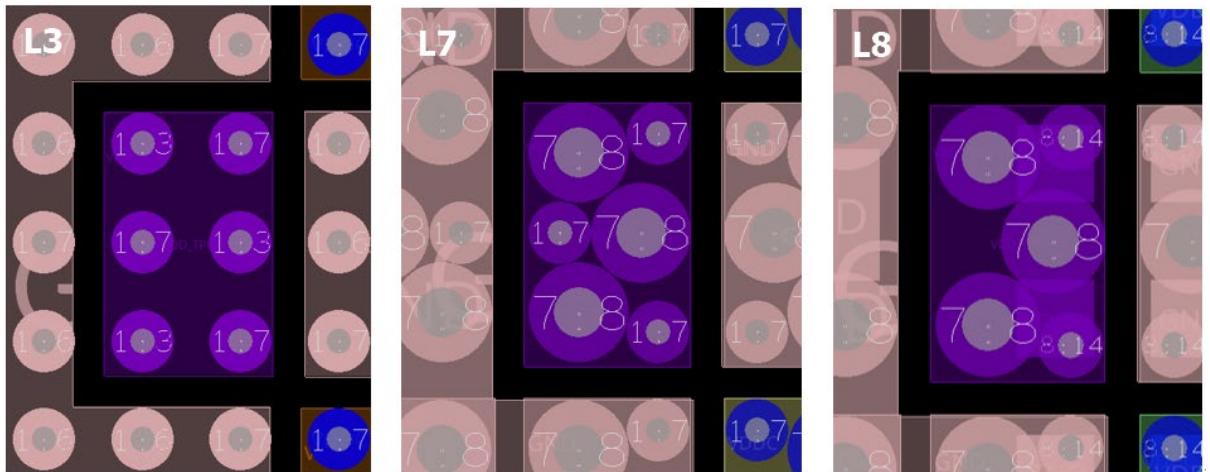
VDD\_TPU ballmap and capacitor placement is depicted in Figure2. It can be seen that the power pin and gnd pin of the capacitor is just below the power and gnd ball of the VDD\_TPU power.



*Figure 2 VDD\_TPU Capacitor Placement*

#### 1.2.1.2 VDD\_TPU Via Design

VDD\_TPU Via design for capacitors are depicted in Figure3 .

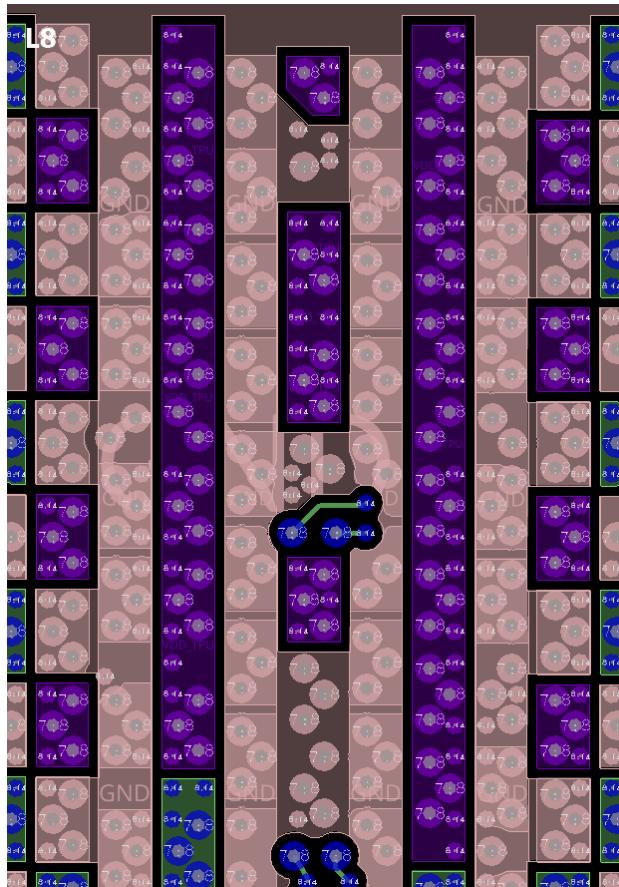


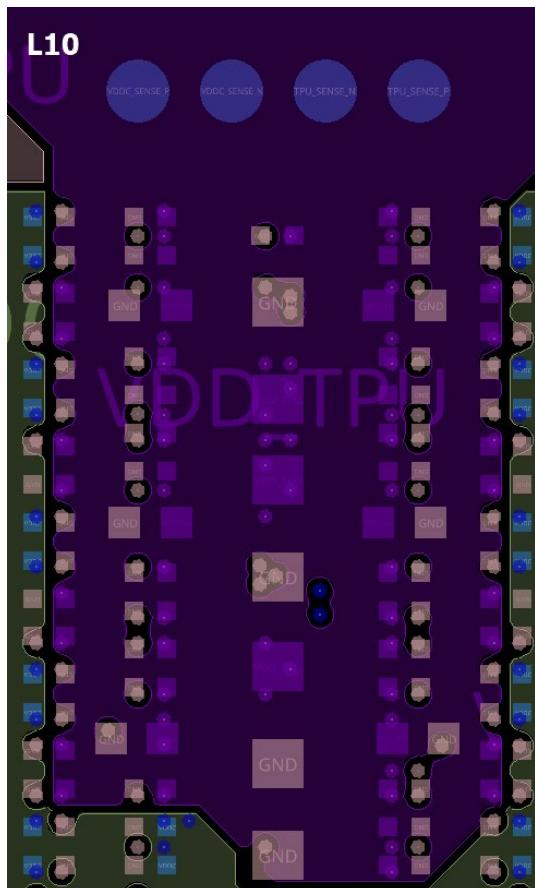
*Figure 3 VDD\_TPU Via Design*

#### 1.2.1.3 VDD\_TPU Power Plane Design

At least two POWER planes for VDD\_TPU are needed to meet IR drop specification. Power plane design of L3, L7, L8 and L10, L12 are depicted in Figure4.

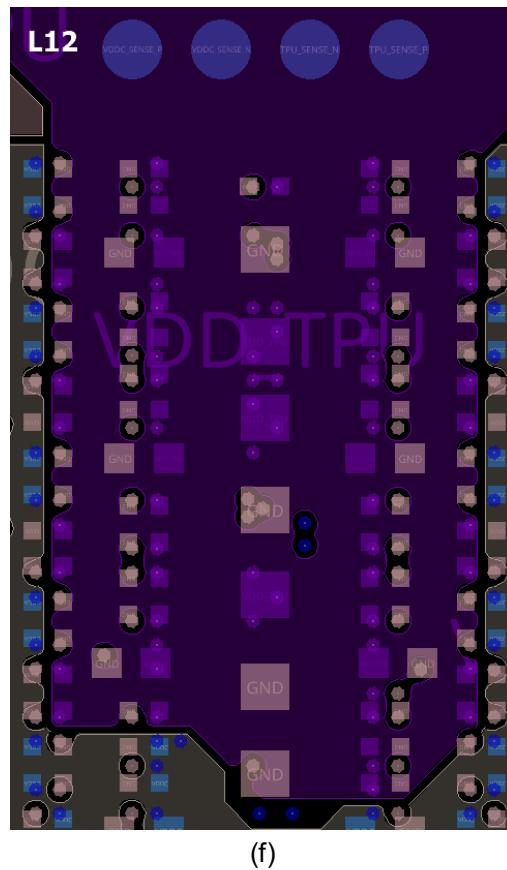






(c)

(d)



**Figure 4 VDD\_TPU Power Plane Design**

## 1.2.2 VDDC

### 1.2.2.1 VDDC Capacitor Placement

Figure 5 illustrates capacitor placement of VDDC power. It can be seen that the power pin and gnd pin of the capacitor is just below the power and gnd ball of the VDDC power.

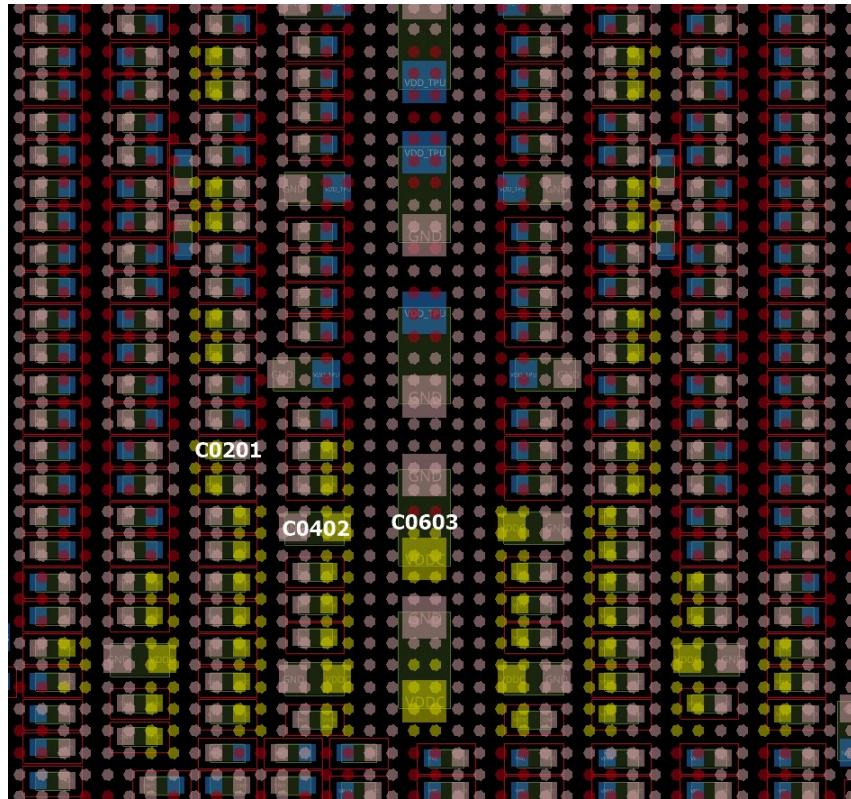


Figure 5 VDDC Capacitor Placement

#### 1.2.2.1 VDDC Via Design

VDDC design for capacitors are depicted in Figure6 .

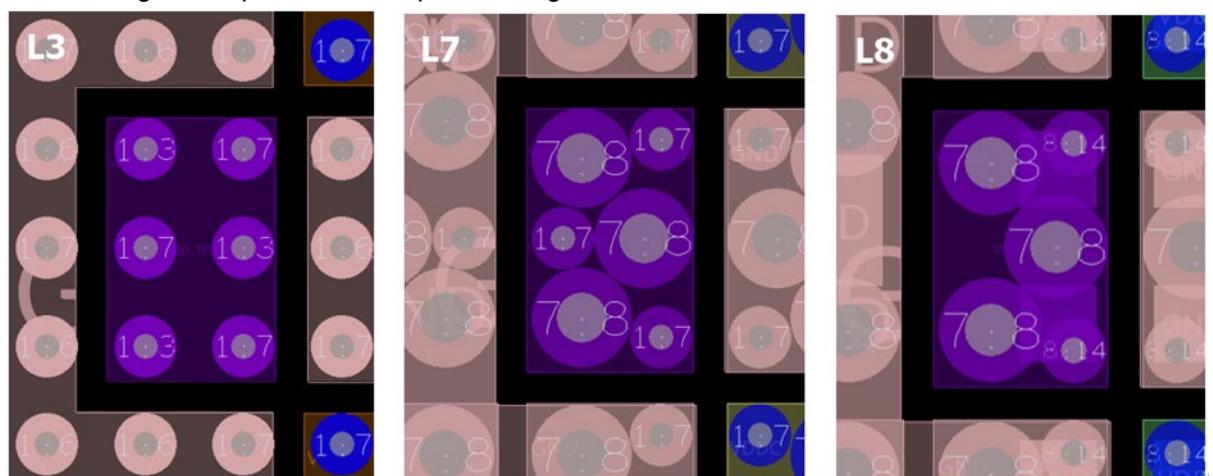
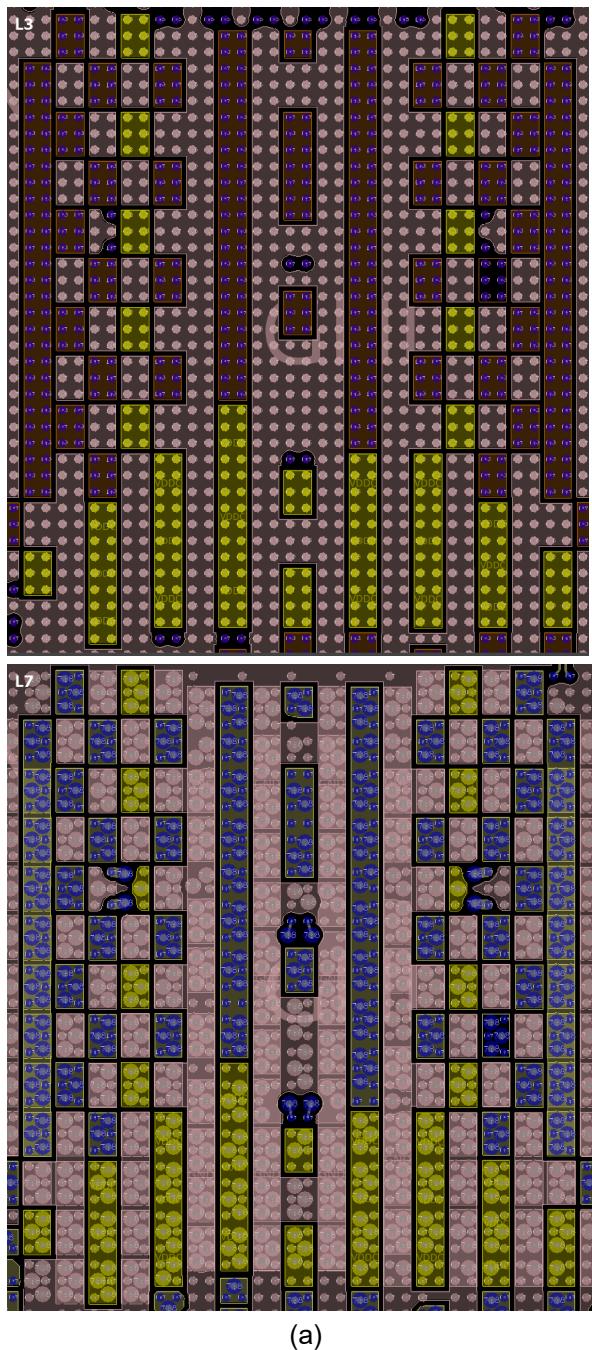


Figure 6 VDDC Via Design

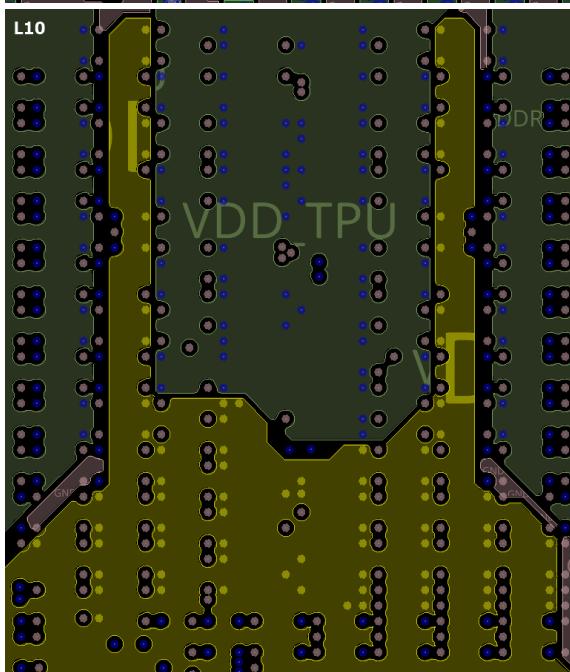
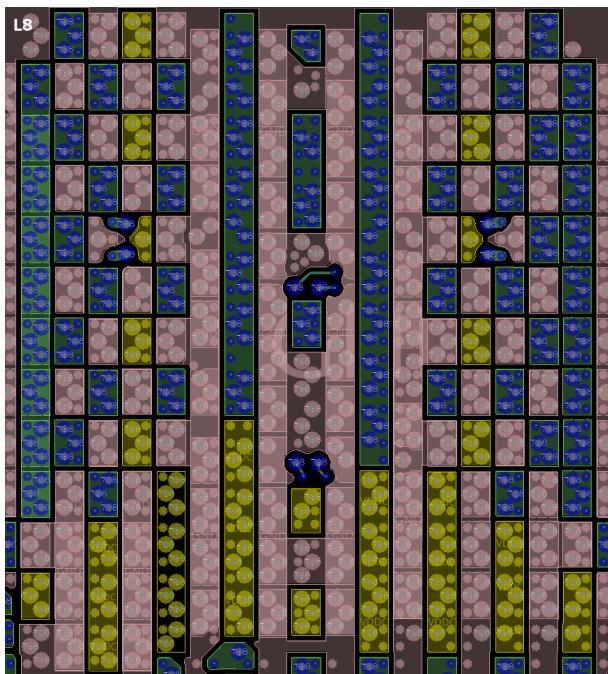
### 1.2.2.2 VDDC Power Plane Design

At least two POWER planes for VDDC are needed to meet IR drop specification. Power plane design of L3, L12, L7, L8, L10 and L12 are depicted in Figure7.



(a)

(b)



(c)

(d)

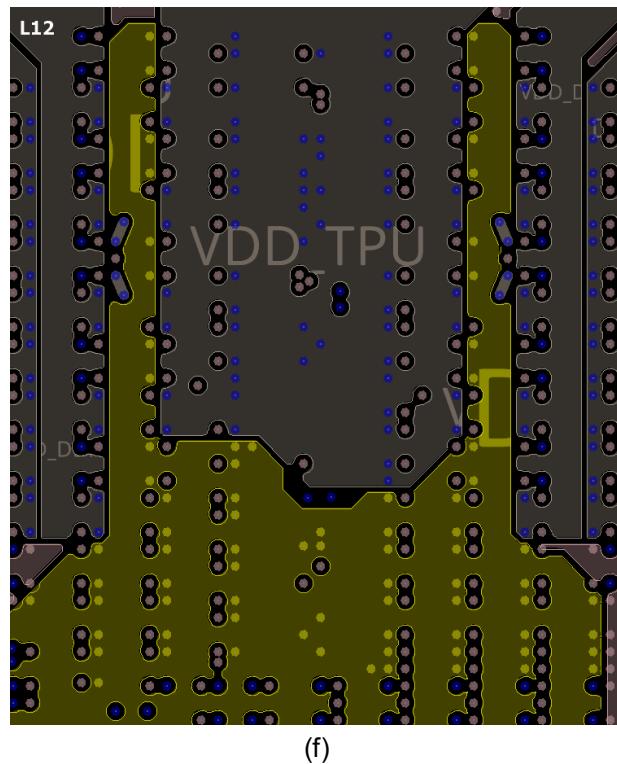


Figure 7 VDDC Power Plane Design

## 1.3 LPDDR4/4X Specific Routing and Implementation Guidelines

### 1.3.1 LPDDR4/4X Topology

S G 2 3 0 0 X LPDDR4/4X dual channel topology is illustrate in Figure8.

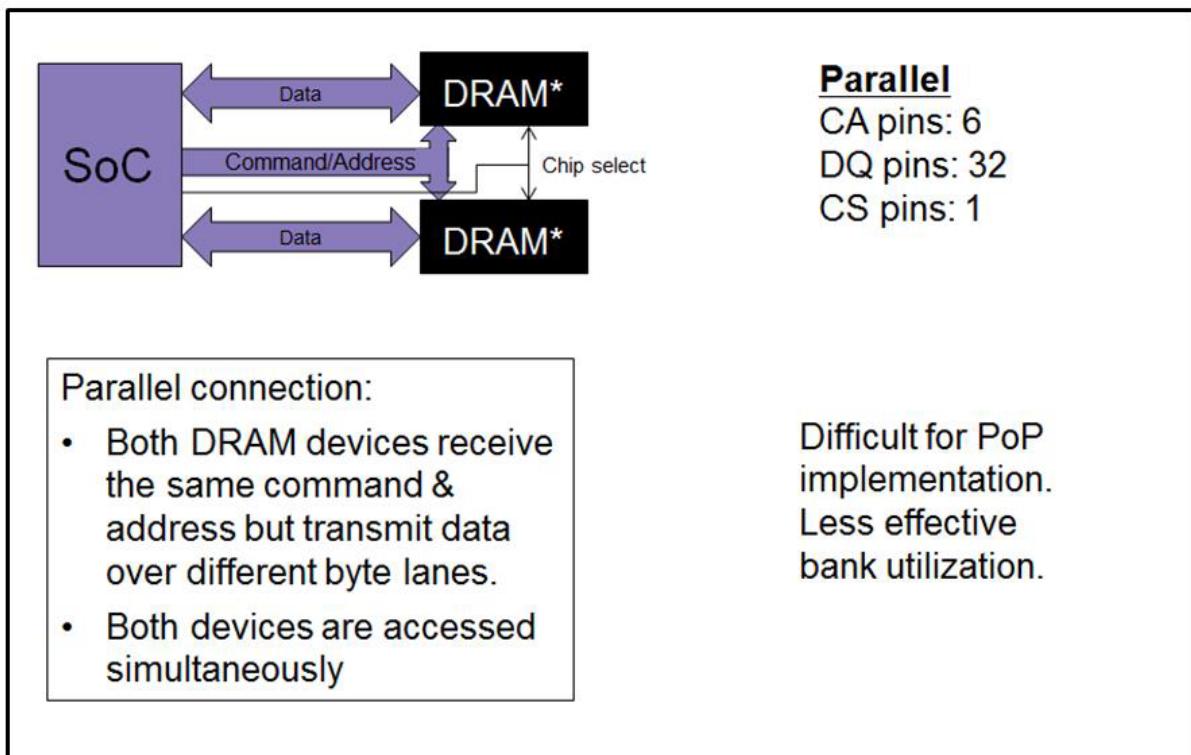


Figure 8 SG2300X LPDDR4/4X topology

### 1.3.2 LPDDR4/4X Impedance requirements

LPDDR4/4X Signal impedance control requirements are illustrated in Table2.

Table 2 LPDDR4/4X Impedance requirements

Single Impedance Control				
Signals	Route Layer	Width(mil)	Impedance( $\Omega$ )	Reference Layer
DQ/DM	L3	2.8	40	L2&L4
	L5	2.8	40	L4&L6
CA	L7	6.8	30	L6&L8
Differential Impedance Control				
Signals	Route Layer	Width/Spacing(mil)	Impedance( $\Omega$ )	Reference Layer
DQS	L3	2.8/9.0	80	L2&L4
	L5	2.8/9.0	80	L4&L6
CLK	L7	4.4/6.2	70	L6&L8

### 1.3.3 LPDDR4/4X Routing Skew

There are many trainings available for the LPDDR4/4X interface that can remove skew. The implementer should make every effort to control skews as tightly as possible in order to improve overall operating margins when the interface is trained. This is sound engineering practice and can simplify debugging. Table3 lists recommended skew targets for LPDDR4/4X. A further discussion of these is found below.

**Table 3 LPDDR4/4X Routing Skew**

System Routing requirements for LPDDR4/4X 4267 operation			
Constraints	Available Deskew Range	Recommended Routed Skew Limits	Notes
DQ to DQ arrival time mismatch within a byte or nibble	<200ps	<20ps	It is highly recommended that flight times across the data lanes be tightly matched in order to preserve operating margin and reduce vertical eye collapse that can occur from crosstalk between unaligned DQ signals.
DQ to DQS domain	DQS position +/-100ps.	DQS position +/-10ps.	
CS, ODT, CKE, Cmd, Add to CK/CK#	Not applicable	CK position +/-10ps	PHY can be programmed to add delay to 4 bit groups of AC signals to address potential skew violations
DQS to CK domain	-0.5 to +5.47 Clock Cycles	CK edge position +/-0ps. (without Write Leveling)	Write Leveling training can compensate for delay differences that extend over multiple clock cycles.

**DQ and DQS.** For the LPDDR4X MultiPHY , the deskew range is limited to a total of 200ps across the byte lane. At high data rates, skew must be kept to a minimum to avoid center-eye cross-talk. Synopsys strongly advocates designing an interconnect with very tight skew control, even with per bit training, +/-10ps skew between the DQ and DQS signals for 2133Mbps and This can be relaxed below this bit rate. This will allow margins for on die skews and on chip process variation.

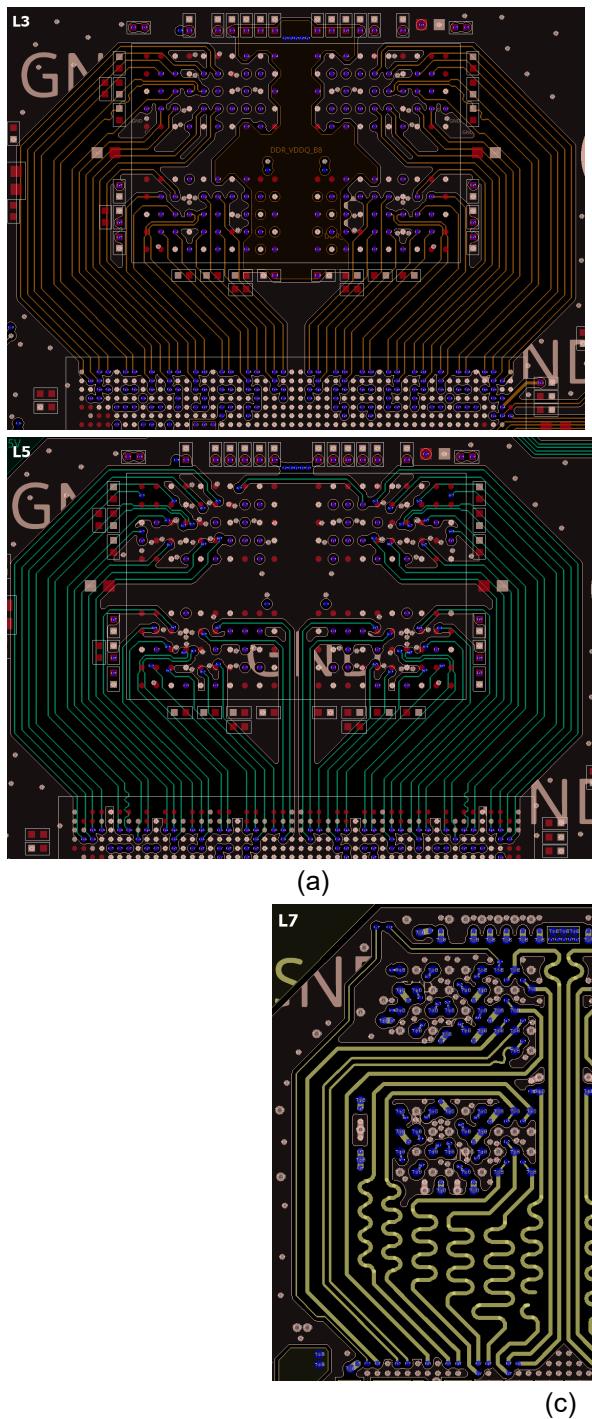
**Command/Address/Control vs. Clock.** Delay on the command/address bus can be ad-justed in 4bit wide groups to reduce the overall skew penalty. A routing tolerance of +/-10ps of all of the signals relative to the CK/CK# should be observed. This can be relaxed if the timing budget and simulation results indicate that there is adequate margin.

**DQS/DQS# vs. CK/CK#.** For LPDDR4/4X, the specification requirement is that the DQS/DQS# arrive within 0.25 of a clock cycle from CK/CK#. At 3200Mbps, this is +/-156ps. At the high bit rates associated with LPDDR4, this is usually managed with Write Leveling. If a user chooses to try to operate without Write Leveling, it is recommended that the routed skew between any DQS pair and the clock pair be kept to ½ of the tDQSS budget.

### 1.3.4 LPDDR4/ LPDDR4X Routing Example

LPDDR4 route example is illustrated in Figure9. DQ and DQS of DDR on top layer are mainly routing on L3. DQ and DQS of DDR on bottom layer are mainly routing on L5. Shared CA traces are routing on L7.

It is highly recommended that routing CA traces on the middle layer of the PCB to ensure the flight time of the two DDRs to be tightly matched.

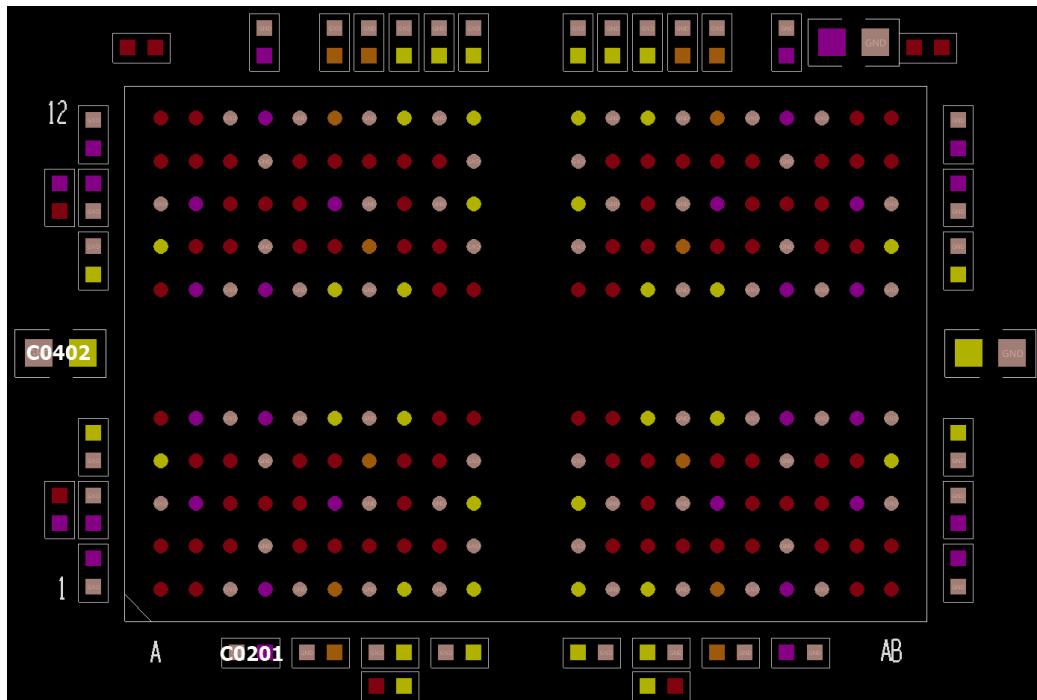


*Figure 9 LPDDR4/ LPDDR4X Routing Example*

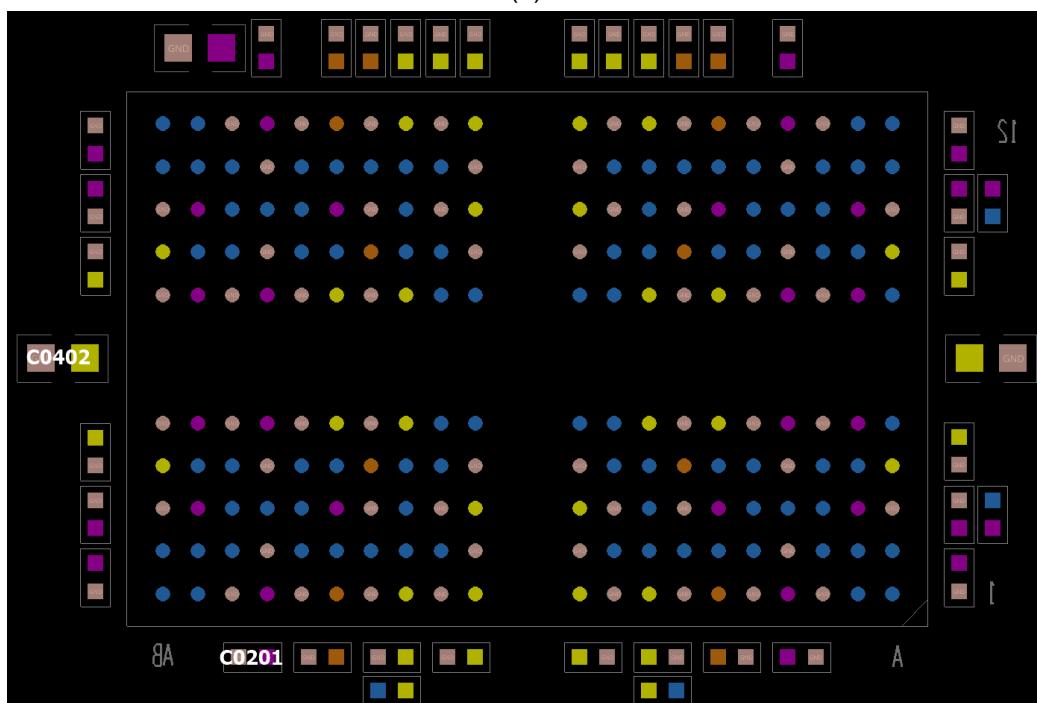
### 1.3.5 LPDDR4/4X Capacitor Placement

#### 1.3.5.1 DDR Side Capacitor Placement

Capacitor placement for DDR powers is illustrated in Figure10. Capacitors with size of 0201 on top and bottom layers are at same location to share the VIA7-8 of power and gnd.



(a)

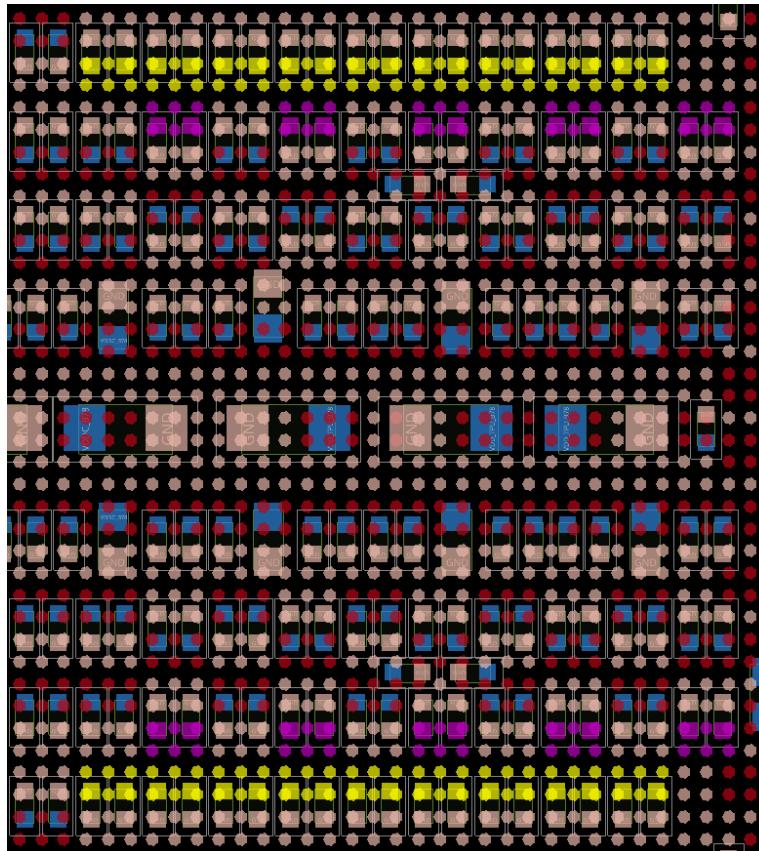


(b)

*Figure 10 DDR Side Capacitor Placement*

### 1.3.5.2 S G 2 3 0 0 X Side Capacitor Placement

Capacitor placement for SG2300X DDR powers is illustrated in Figure11.

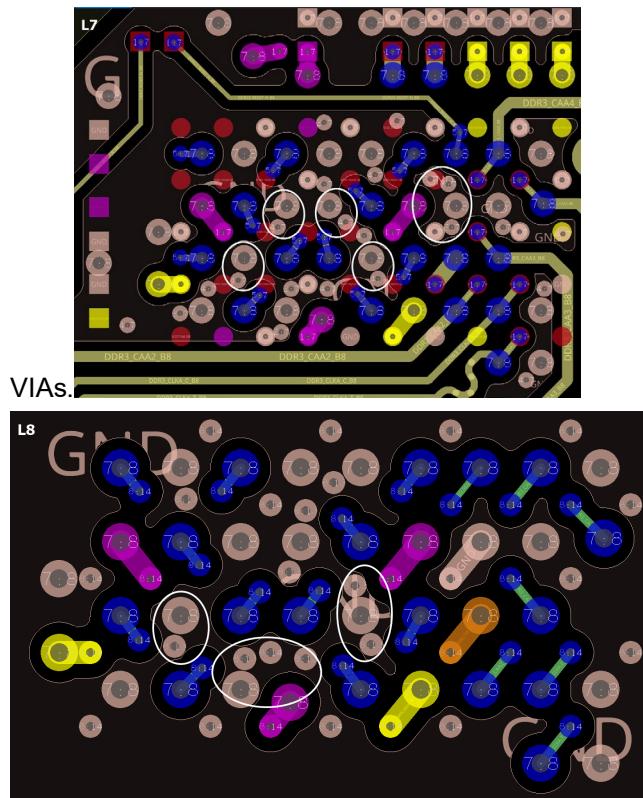


*Figure 11 S G 2 3 0 0 X Side Capacitor Placement*

### 1.3.6 LPDDR4/4X Power Via Design

#### 1.3.6.1 DDR Side Via Design

LPDDR4/4X Power via design is illustrated in Figure12. Notice that capacitor with size of 0201 on top and bottom layers share the same VIA7-8 of power and gnd. Make sure VIA1-7, VIA7-8 and VIA8-14 are connected on Layer7 and Layer8 to suppress crosstalk between DQ

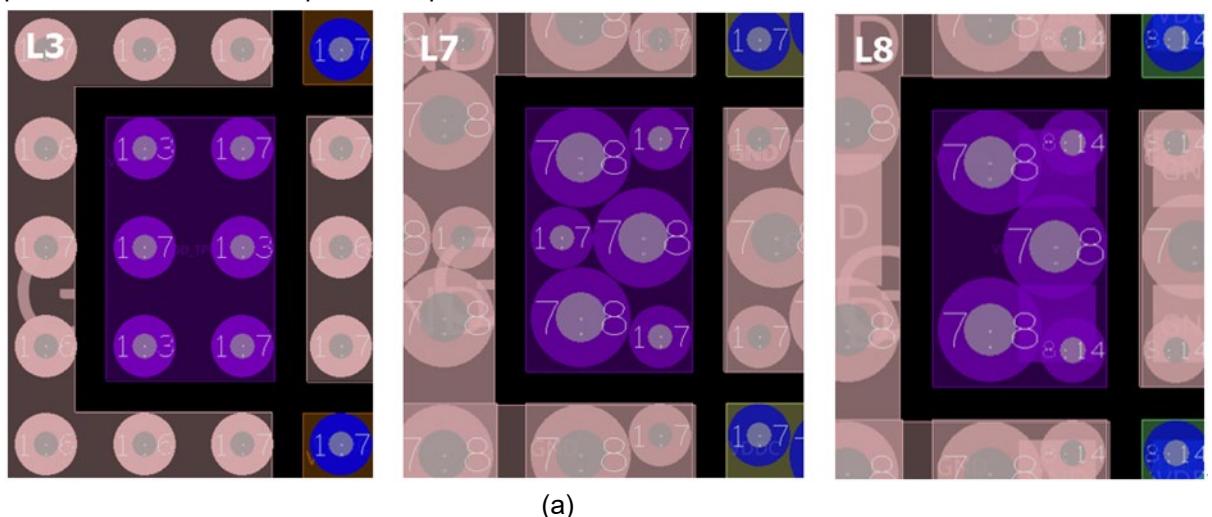


**Figure 12 DDR Side Via Design**

### 1.3.6.2 S G 2 3 0 0 X Side Via Design

DDR power via design of SG2300X side is illustrated in Figure13.

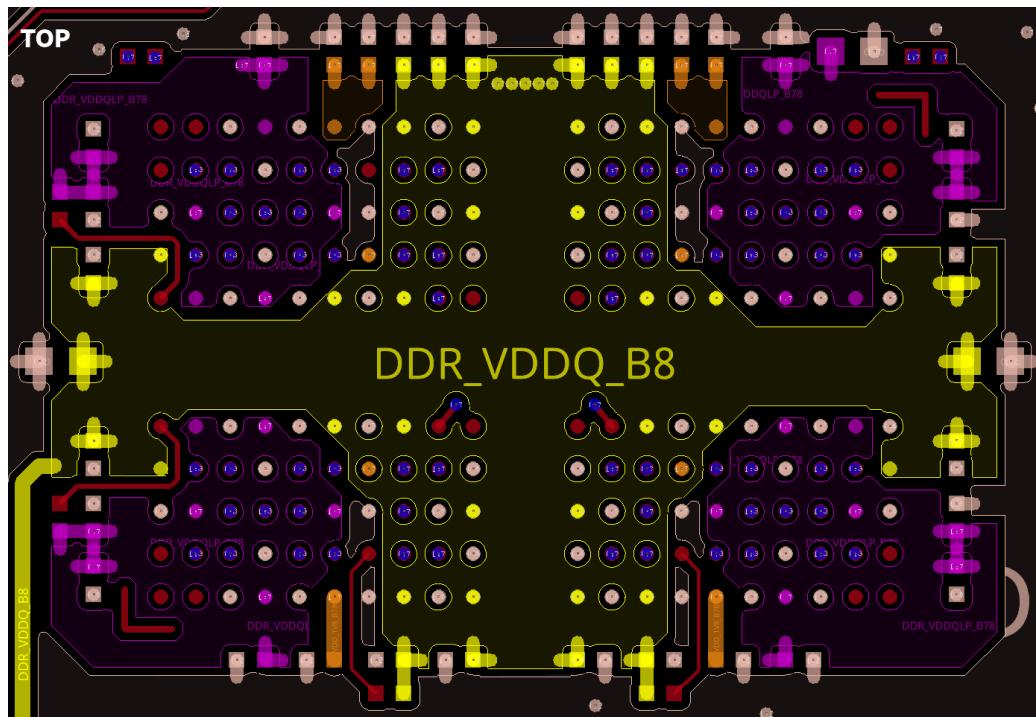
It is highly recommended that three VIA7-8 are used to connect VIA1-7 to VDDQLP power plane to achieve lower capacitor loop inductance.



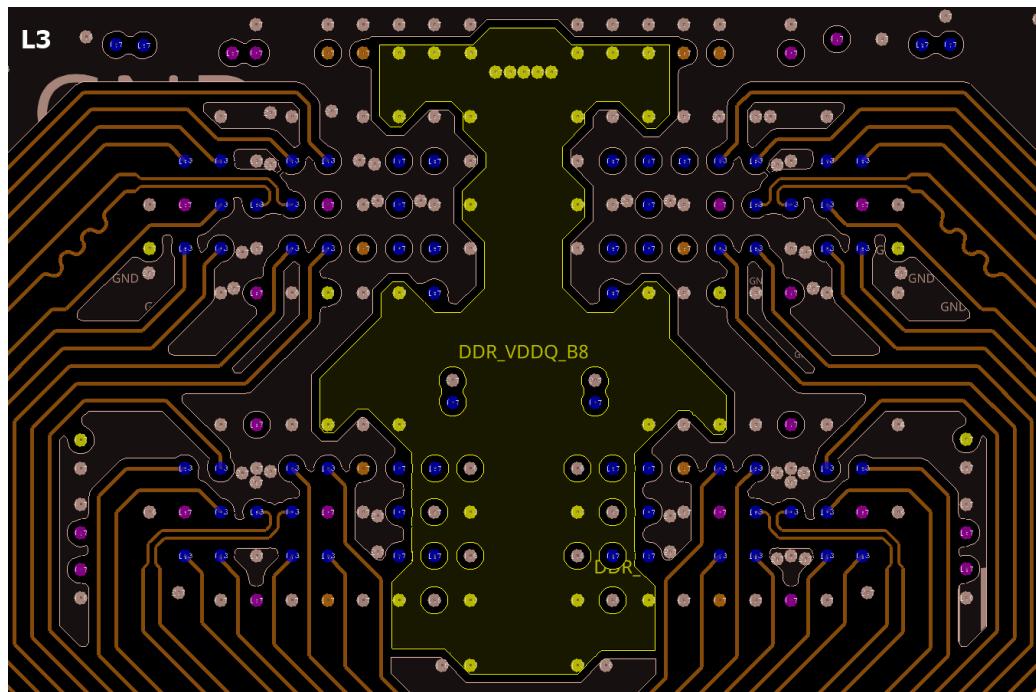
**Figure 13 SG2300X Side Via Design**

### 1.3.7 LPDDR4/4X Power Plane Design

LPDDR power plane design from top layer to bottom layer are illustrated in Figure14.

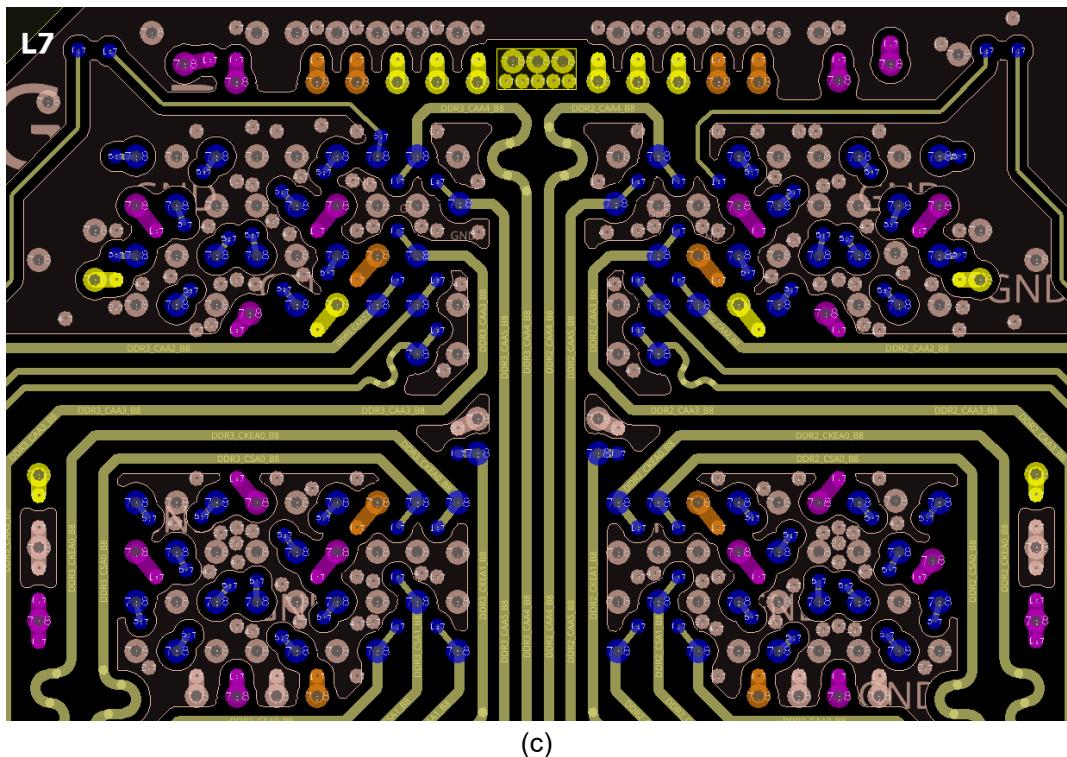


(a)

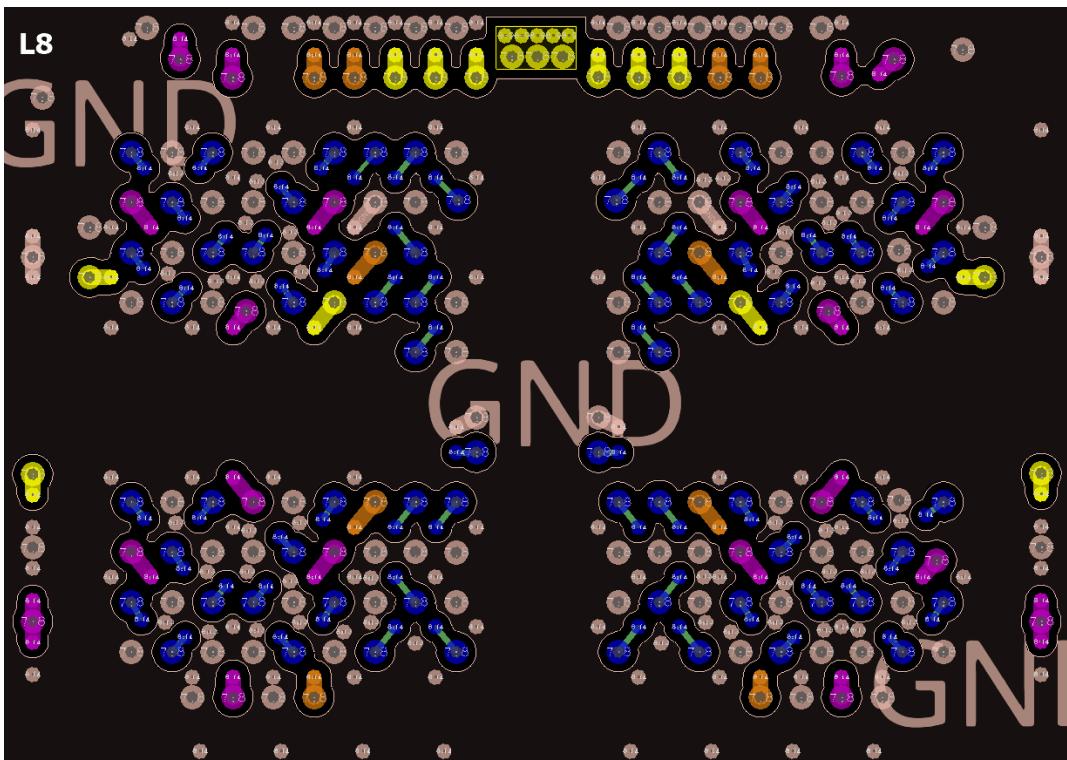


(b)

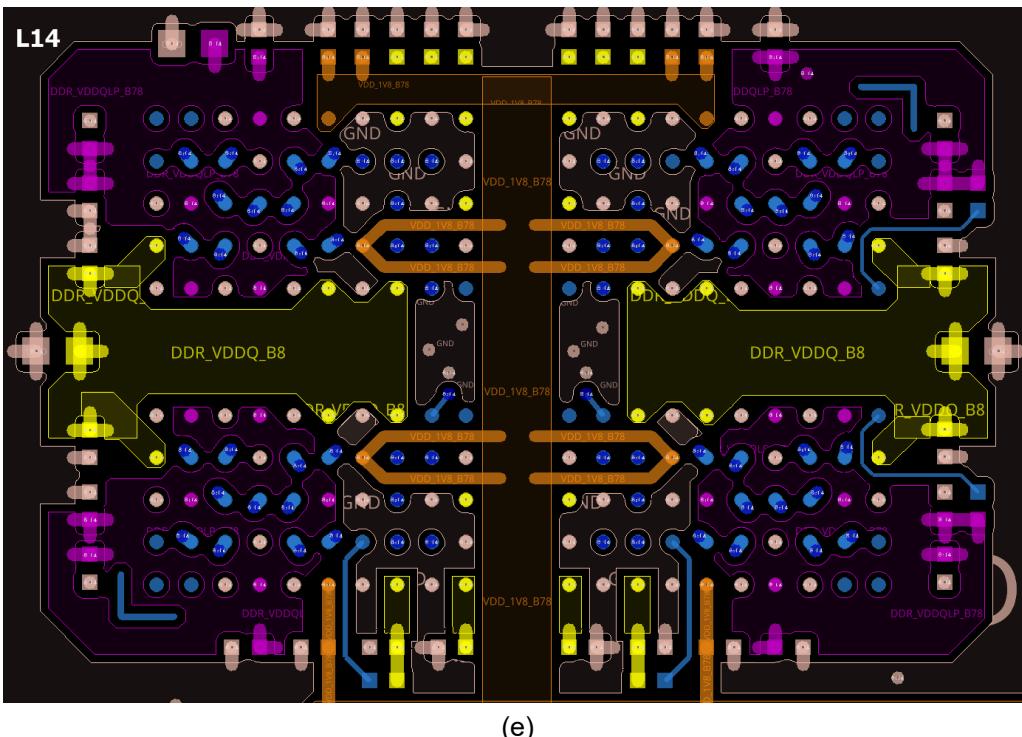
Specifications are subject to change without notice



(c)



(d)



**Figure 14 LPDDR4/4X Power Plane Design**

## 1.4 PCIE Implementation Guidelines

#### 1.4.1 PCIE Impedance Requirements

The PCB trace pair differential impedance is shown in Table 4. These limits apply to both the add-in card and the system board. Motherboards with long (high loss) channels may need to have tighter impedance control. This requirement does not apply to vias, the connectors, package traces, cables, and other similar structures. Designs should still attempt to minimize the impedance discontinuities from vias, the connectors, package traces, cables, and other similar structures.

**Table 4 PCIE Impedance Requirements**

<b>Signal</b>	<b>Differential Impedance</b>
PCIE DATA	90 Ω
PCIE CLK	100 Ω

#### 1.4.2 PCIE Skew Requirement

The skew within the differential pair gives rise to a common-mode signal component, which can, in turn, increase Electromagnetic Interference (EMI). The differential pair shall be routed such that the skew within differential pairs is less than 5 mils.

**Table 5 PCIE Skew Requirement**

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Signal	Skew within differential pair
PCIE DATA	5 mil
PCIE CLK	5 mil

### 1.4.3 PCIE Capacitor Placement and Power Design

SG2300X PCIE capacitor placement is illustrated in Figure15. Capacitor with size of 0201 is placed under the power ball. Via and power plane design is shown in Figure16. It is highly recommended that at least two VIA7-8 are used to connect power ball with capacitors for each PCIE power net.

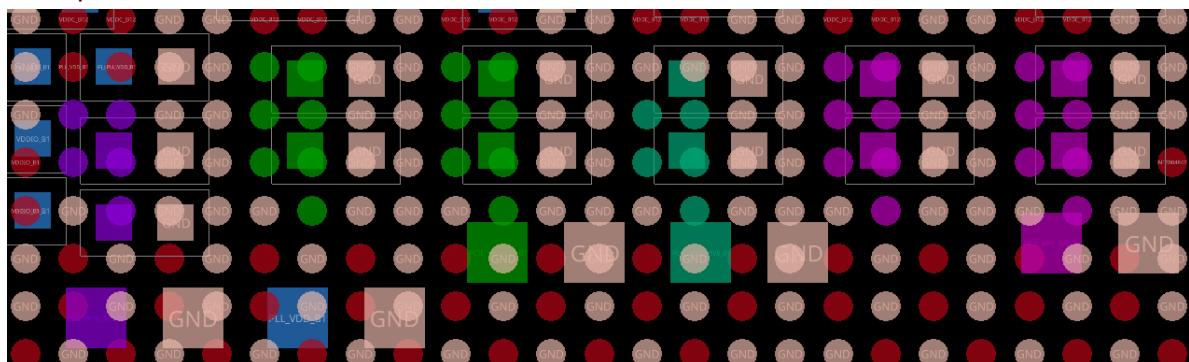
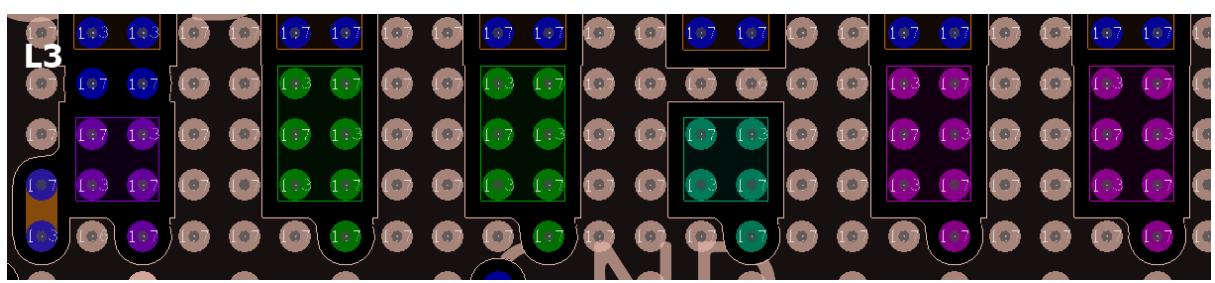
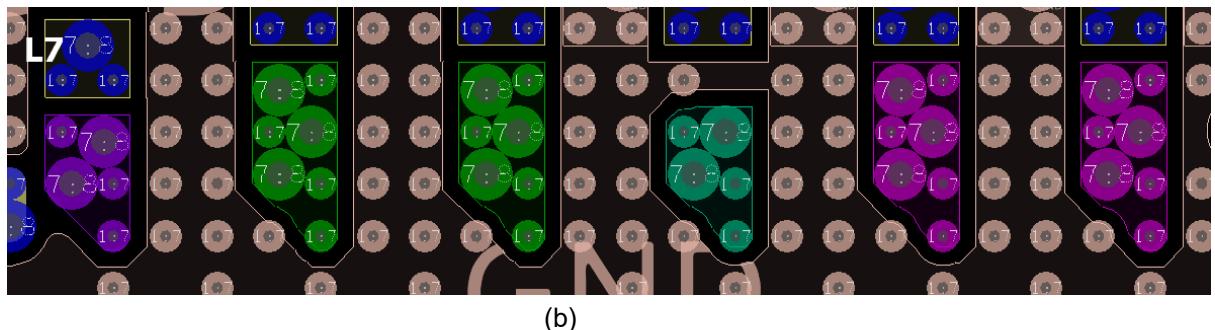


Figure 15 PCIE Capacitor Placement.

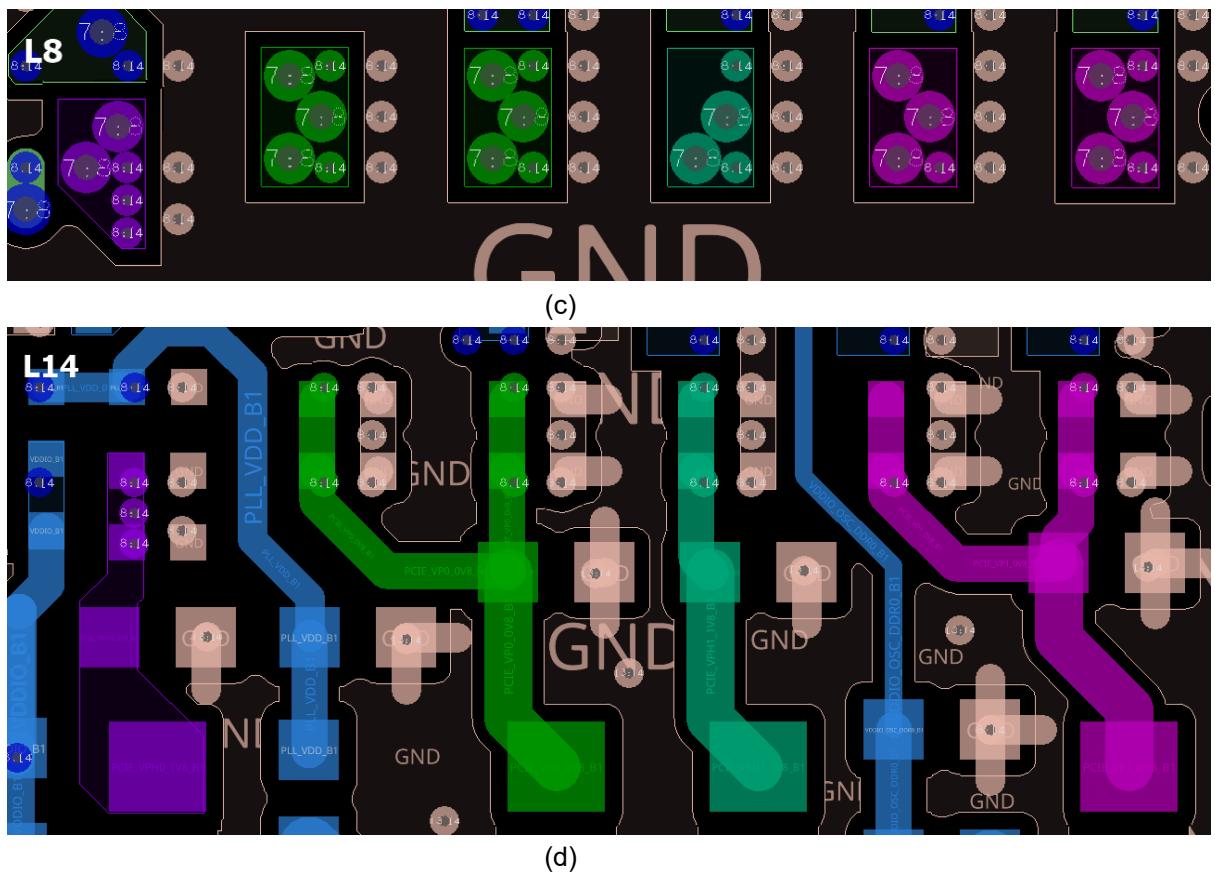


(a)



(b)

Specifications are subject to change without notice



*Figure 16 PCIE Via and power plane design.*

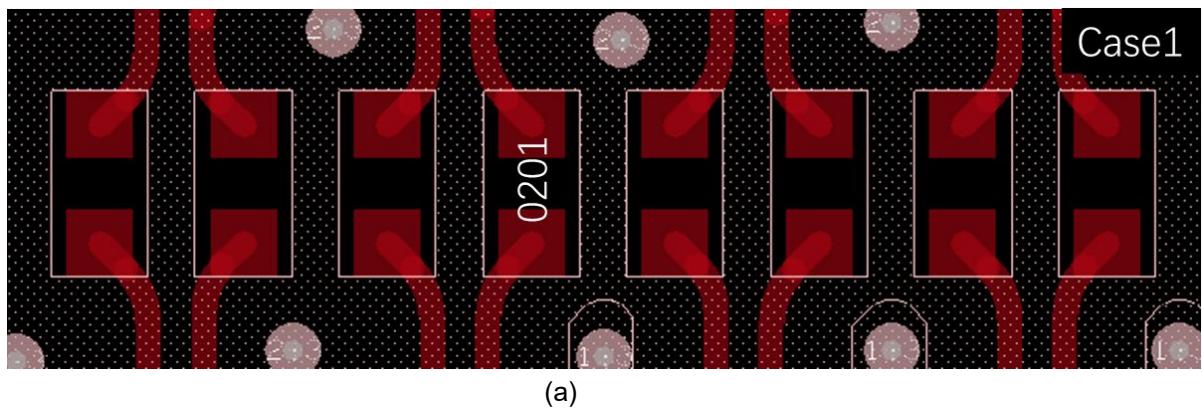
#### 1.4.4 AC Coupling Capacitors and Via design considerations

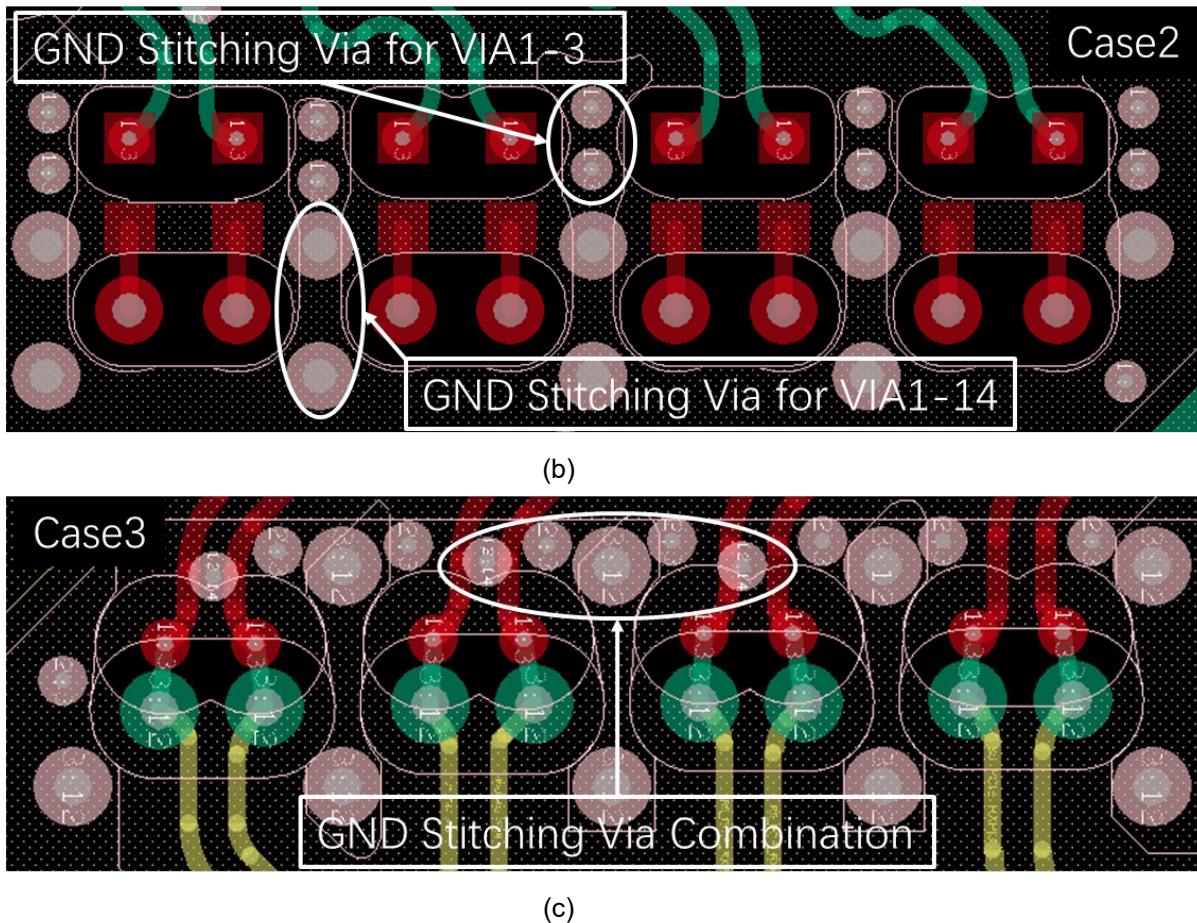
AC Coupling capacitor and different via design is illustrated in Figure17.

Case1 & Case2: It is recommend that void the area of adjacent layer under the capacitor pads.

Case2: Place GND stitching via for each signal VIA1-3 and close to it.

Case3: Place GND stitching via combination(VIA2-7, VIA7-8 and VIA8-14) to connect signal reference layers.





**Figure 17 AC Coupling Capacitors and Via design considerations**

## 1.5 RGMII Implementation Guidelines

### 1.5.1 RGMII Definition

The RGMII interface reduces the number of traces between the MAC and the PHY, which is achieved by simultaneous sampling and signal multiplexing on the rising/falling edges of the reference clock.

RGMII pin definition as below.

Signal Name	RGMII	Description
TXC	MAC	The transmit reference clock will be 125MHz, 25MHz, or 2.5MHz $\pm$ 50ppm depending on speed.

Signal Name	RGMII	Description
TXD[3:0]	MAC	bits 3:0 on rising edge of TXC, bits 7:4 on falling edge of TXC.
TX_CTL	MAC	TXEN on rising edge of TXC, and a logical derivative of TXEN and TXERR on falling edge of TXC.
RXC	PHY	The continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz $\pm 50\text{ppm}$ , and shall be derived from the received data stream.
RXD[3:0]	PHY	bits 3:0 on rising edge of RXC, bits 7:4 on falling edge of RXC.
RXC_CTL	PHY	RXDV on rising edge of RXC, and a logical derivative of RXDV and RXERR on falling edge of RXC.

### 1.5.2 RGMII layout considerations

The rule of RGMII Layout is mainly the following:

- 1、The data and clock trace must be less than 2.5 inches; Create 2 equal-length groups, refer to TXC and RXC respectively, The difference in trace length within a group does not exceed 20mil;
- 2、In SG2300X RGMII design, TXC delay have added inside PHY and RXC delay have added inside MAC. So in pcb layout, there is no need to delay clock line.

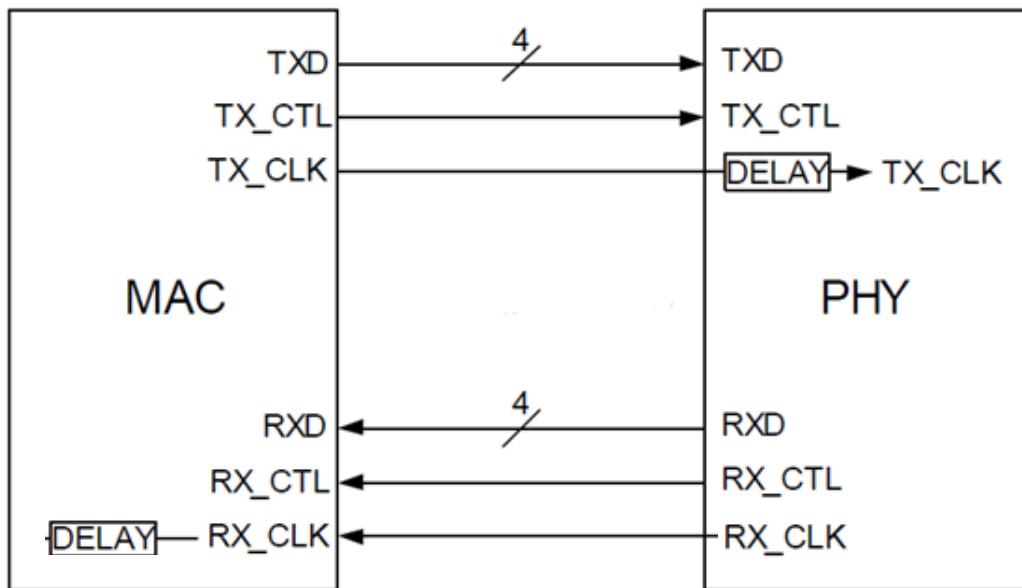


Figure 18 SG2300X TXC and RXC delay topology

The clock frequency of RGMII at 1 Gbit/s rate can reach 125MHz. It is conceivable that RGMII Layout also needs to comply with the basic principles of high-speed digital circuit layout:

- 1、Impedance control;
- 2、2W/3W principle.

Note that in the design where RF and high-speed digital circuits exist at the same time, it is impossible to control the impedance of RF traces and high-speed digital traces at the same time. At this time, please be sure to add series matching resistors on all RGMII traces, and place them in accordance with the source end matching principle.