Elec Eng 2EI5
Design Project #4

Problem Statement
Design and simulate a MOSFET based exclusive OR gate.

Report Requirements
This project does not have a hardware component. It is only design and simulation based. Therefore there are some very specific requirements. The report should include:

1. A maximum of 2 pages showing your hand analysis and discussing design considerations;
2. A maximum of 2 page showing figures (circuit diagram, simulation results, etc.); and
3. A maximum of 2 page describing your simulations, discussing circuit functionality, and comparing hand calculations with simulation.

Your report should address the following areas and constraints:

1. Circuit topology:
    a. For power supplies use V- = 0 and V+ = 5V.
    b. You may use as many MOSFETs and/or resistors as you choose but see below for discussion of circuit performance.
    c. Your MOSFETs should be the N- and P-MOSFETs from the ALD1115 (the chip you have in the lab), and both hand calculations and simulations should be based on the specified parameters for these devices as discussed below.
    d. You should discuss the reasons you chose a particular topology and discuss at least one alternate design that you decided against.
2. Device modeling:
    a. You will need to extract a VT and K for your MOSFETs from the specification sheet.
    b. You should assume (not true but works as a guide for design) that the value of K you extract is K' and that for the devices specified $W = L = L_{\min}$. You may then choose sizes for transistors you include in your design and use them to scale device parameters.
    c. You should assume that a resistor with $W = L = L_{\min}$ has a resistance of 100 Ω.
3. Device modeling in PSpice:
    a. Ensure that you have entered a complete model specification for your device (including capacitance).
    b. Ensure that you enter the value of *K* you extract as K' and the appropriate W/L for each device.
4. Functional and timing simulation:
    a. You need to simulate the basic operation and timing of the circuit.
    b. One simple way to do this (if you do something different please explain it) is to have a square wave at some moderate frequency (e.g. 500 Hz) to represent input A, and a second square wave at double the frequency (e.g. 1 kHz) to represent input B. This then gives you the data 00, 01, 10, 11 in sequence at a rate (in this example) of 2 kb/sec. The

output waveform would then demonstrate whether your circuit produces the correct truth table.

c. You may use the output waveform to determine rise time, fall time, and propagation delay. Use a capacitive load that equals the estimated input capacitance of your gate.

5. Static level simulation:
    a. Set one of the inputs to be logic-1 and sweep the other input from V- to V+ for your circuit. The circuit should now work as an inverter so you should be able to simulate the voltage transfer characteristic (vout as a function of vin).
    b. Use the VTC to estimate the noise margins for your circuit.
6. Circuit properties:
    a. Use the size of the capacitor and the voltage levels obtained to estimate the dynamic power dissipation.
    b. Use the results of your static level simulation to estimate the static power dissipation for the different logic states.
    c. Estimate the total area of your design given the assumptions stated above under the heading “Circuit Topology”.
    d. Redo the timing analysis at different frequencies to estimate when the circuit output begins to degrade – that’s the speed of your circuit.

Marking

The rubric for this project will closely follow the items outlined above.

Further Information

If you need any clarification on this project please email as soon as possible.

Deadline

This project is due April 18, 2015 at 5:00 p.m.