

ELECENG 3EJ4 Lab 4

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Part 1

- Q1.**
1. Based on the simulation data obtained in Step 1.2, the low-frequency voltage gains in dB are: $A_{d1} = 7.38$, $A_{d2} = 70.05$, and $A_{d3} = 0$.
 2. Based on the simulation data obtained in Step 1.2, the overall voltage gain for the differential-mode signal is $A_d = 77.43$ dB or $A_d = 7437.8$ (real magnitude).
 3. The non-inverting input of the operational amplifier is V_2 , as the simulated phase of the output voltage V_o is in phase with the phase offset of V_2 at low-frequency.
 4. The upper 3-dB frequency f_H of the operational amplifier is approximately 6.4 kHz, and this value was determined the frequency when the phase drops by 45 degrees from its initial value.
- Q2.**
- The differential-mode gain A_{d1} in Q1, 7.38 dB, is around one-tenth of the differential-mode gain A_d in Lab 3, 70.07 dB. The difference is due to the feedback received by the emitters of the PNPs in the current mirror, affecting the collector current at the output of the differential amplifier (likely an increase in emitter currents causing a decrease in voltage gain).
- Q3.**
- Based on the simulated results obtained in Step 1.2 and 1.3, the input resistance $R_{in} = 81.757$ k Ω and the output resistance $R_o = 461$ Ω . This matches the expected resistances for an operational amplifier, a high input resistance and a low output resistance.

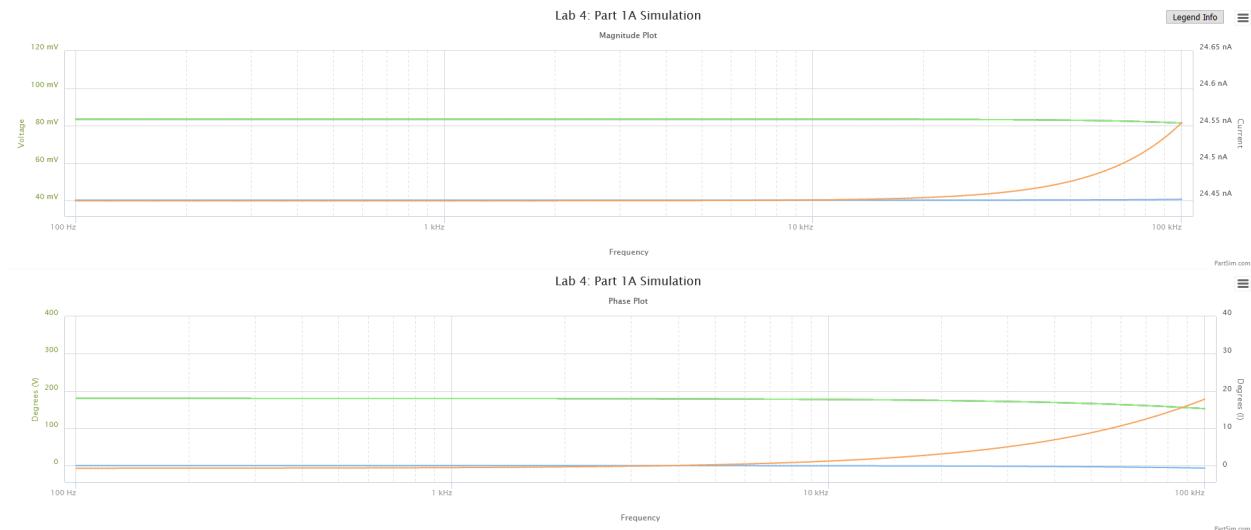


Figure 1: Bode plots for Step 1.2 (Green/Black: V_o/V_{o2} , Orange: i_{b1} , Blue: V_{o1})

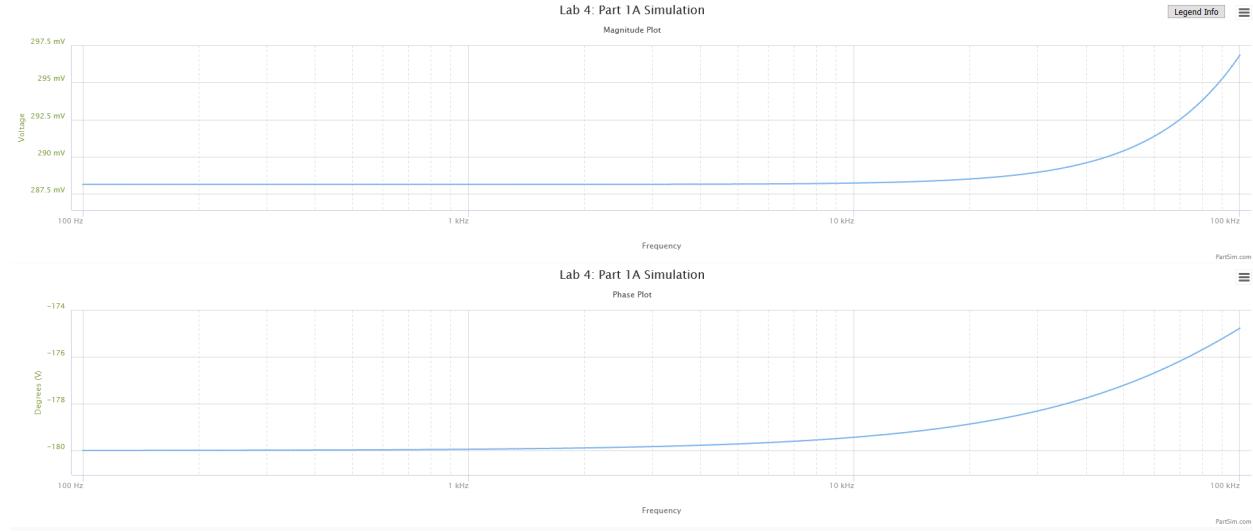
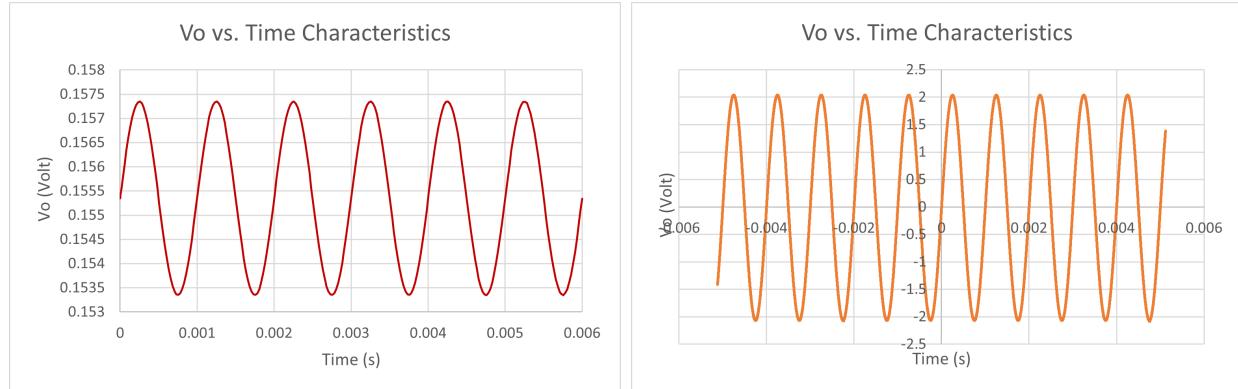


Figure 2: Bode plots for Step 1.3

- Q4.** 1. The plots for the simulated and measured results from Steps 1.6 and 1.11 for the output voltage V_o vs. the time characteristics at 1 KHz are shown in Figure 3.



(a) Step 1.6 (Simulated) Plot

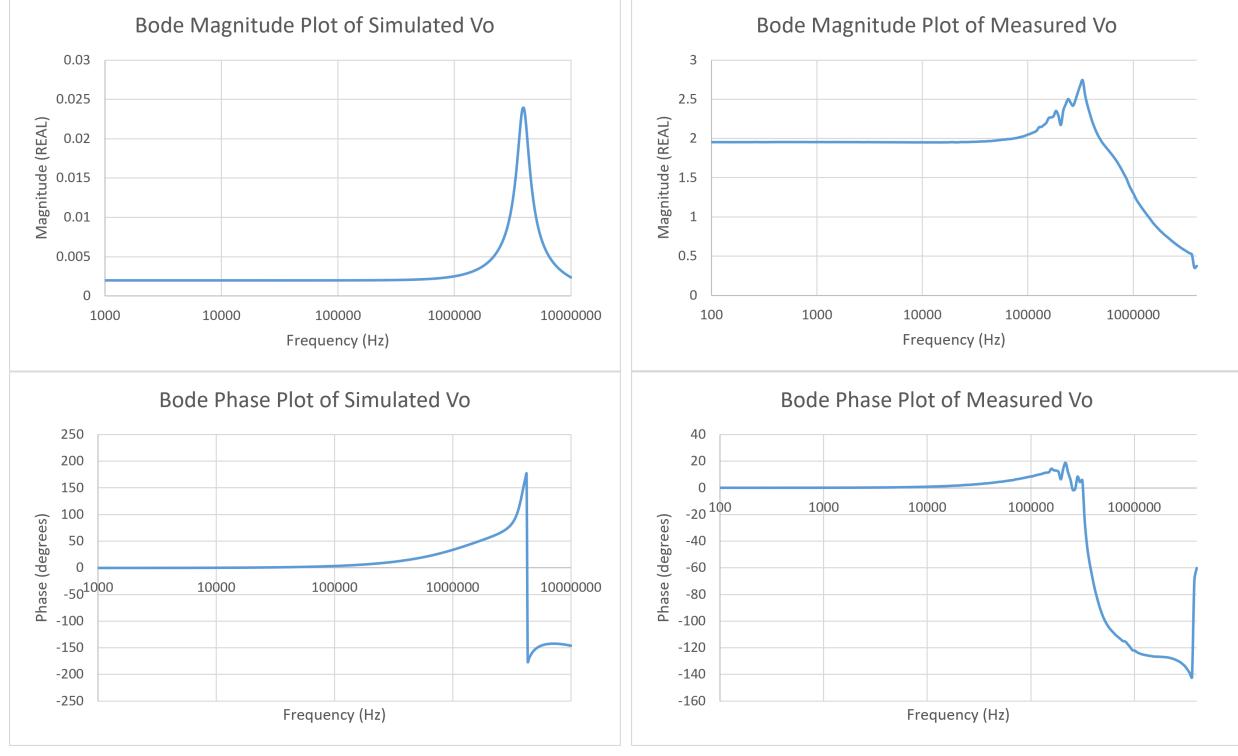
(b) Step 1.11 (Measured) Plot

Figure 3: Output voltage V_o vs. time characteristics at 1 kHz

2. The peak to peak voltage, V_{pp} for the simulated results is 40 mV, while the peak to peak voltage, V_{pp} , for the measured results is around 4 V. The AC amplitude, V_p and DC voltages, V_{dc} for the simulated results are 20 mV and 155 mV, while V_p and V_{dc} for the measured results are 2 V and -15 mV. The differences in V_{pp} and V_p voltages are explained by the different input AC voltages at V_1 , the input for the measurement is 1000 times greater than the input for the simulation, therefore the measured peak to peak voltage and AC voltage are 1000 times greater than the simulated peak to peak voltage and AC voltage. Otherwise, both sets of data have the same frequency/period and exhibit the same behaviour.

- Q5.** 1. The plots for the simulated and measured results from Steps 1.7 and 1.12 for

the voltage gain magnitude and phase vs. frequency characteristics are shown in Figure 4.



(a) Step 1.7 (Simulated) Plot

(b) Step 1.12 (Measured) Plot

Figure 4: Bode plots for Step 1.7 and 1.12

2. Similar to Q4, the bode magnitude plots display similar behaviour (albeit at much lower frequencies), but have different very different scales due to the 1 mV input AC voltage in simulation, causing the magnitude gain to be 1000 times smaller in the simulated results. If the simulation is done with the same input AC voltage (1 V), the resulting bode magnitude plot has the same behaviour as before, but matches the scale of the magnitude gain seen in the measured bode magnitude plot. The bode phase plot also displays the same general behaviour, beginning to increase at a certain frequency before having a steep drop in the phase. The behaviour towards the end of the plot begins to slightly differ. This due to a number of factors such as the internal capacitances in all of the BJTs affecting the phase at higher frequencies, or other components of the physical circuit behaving differently than expected in simulation at higher frequencies (breadboard, wires, AD2 board) despite behaving the same at lower frequencies.

Q6. The circuit uses a series-shunt feedback configuration. The input is connected directly into the directional amplifier, resulting in a series connection, while the output provides a feedback to the differential amplifier, resulting in a shunt connection.

Q7. The beta network consists of R_1 and R_2 , and the value of β is $\frac{R_1}{R_1+R_2} = 0.5$. The

feedback components R_{11} and R_{22} are simply $R_{11} = R_1 = 100 \text{ k}\Omega$ and $R_{22} = R_2 = 100 \text{ k}\Omega$.

- Q8.** The series-shunt amplifier can be represented as a two port network with h parameters. The voltage gain is equal to $\frac{1}{h_{12}}$ where $h_{12} = \beta$. Therefore the voltage gain, A_v , is $\frac{1}{0.5} = 2$. This voltage gain matches with the voltage gain, A_v , of 2 (or 6 dB) determined in the simulation done in Step 1.7. The input impedance R_{in} is equal to $h_{11} = R_1 \parallel R_2 = 50 \text{ k}\Omega$, and the output impedance R_o is equal to $\frac{1}{h_{22}} = R_1 + R_2 = 200 \text{ k}\Omega$.

Part 2

Q9. $C = C_1 = C_2$ and $R = R_3 = R_4$

$$\begin{aligned}
 V_o &= V_+ \left(1 + \frac{1}{sCR} \right) + RV_+ \left[\frac{1}{R} + sC \left(1 + \frac{1}{sCR} \right) \right] \\
 &= V_+ \left(1 + \frac{1}{sCR} \right) + V_+ (2 + sCR) \\
 &= V_+ \left(3 + \frac{1}{sCR} + sCR \right) \\
 \Rightarrow \frac{V_+}{V_o} &= \frac{s/CR}{s^2 + s(\frac{3}{CR}) + (\frac{1}{CR})^2} \\
 L(s) &= \left(1 + \frac{R2}{R1} \right) \frac{s/CR}{s^2 + s\frac{3}{CR} + (\frac{1}{CR})^2}
 \end{aligned}$$

The zero loop phase frequency ω_0 is $\omega_0 = \frac{1}{CR}$. At the zero loop phase frequency, $|L(j\omega)| = \frac{1}{3} \left(1 + \frac{R2}{R1} \right)$, therefore for oscillation we require $\frac{1}{3} \left(1 + \frac{R2}{R1} \right) \geq 1$ which occurs when $\frac{R2}{R1} \geq 2$.

Q10. The characteristic equation of the system is $1 - L(s) = 1 - \left(1 + \frac{R2}{R1} \right) \frac{s/CR}{s^2 + s\frac{3}{CR} + (\frac{1}{CR})^2} = 0$.

To find the pole Q , we can convert $L(s)$ into the frequency domain, can find that $L(j\omega) = \frac{j\omega \left[\frac{1+R2/R1}{CR} \right]}{\left[\left(\frac{1}{CR} \right)^2 - \omega^2 \right] + j\frac{3\omega}{CR}}$. From this equation, we see that the value of $R2/R1 = 2$ will give us $j\frac{3\omega}{RC}$ in both the numerator and denominator, leaving us with $-\omega^2 - (\frac{1}{CR})^2$ or a pole Q at $(\frac{1}{CR})^2$ due to the Barkhausen Criterion.

Q11. The settling times for $R2 = 220$ k Ω , 240 k Ω and 280 k Ω are approximately 3.75 ms, 1.25 ms and 0.6 ms. The settling time decreases as the value of $R2$ increases. This behaviour is due to the loop gain $L(s)$ (derived in Q9) increasing as the value of $R2$ increases, decreasing the amount of time the oscillator circuit requires to reach saturation ($|5$ V| for this circuit).

Q12. 1. The plots for V_o found in Steps 2.4, 2.6, 2.9, and 2.10 are shown in Figure 5. The plots for 2.9 and 2.10 continue from after the oscillations have settled, but show the same behaviour as the simulated plots after settling, including sharing the same frequencies.

2. The frequencies in Step 2.4 (simulated) and 2.9 (measured) were found to be approximately 17.5 kHz, while the frequencies in Step 2.6 (simulated) and 2.10 (measured) were found to be approximately 33 kHz. This matches the expected results from theory, as the frequency is inversely proportional to the values of R and C ($\omega \propto \frac{1}{RC}$), which was explored in Q9. Therefore, decreasing the value of R to almost half its value (8.25 k Ω to 4.02 k Ω) nearly doubles the frequency of the oscillations (17.5 kHz to 33 kHz).

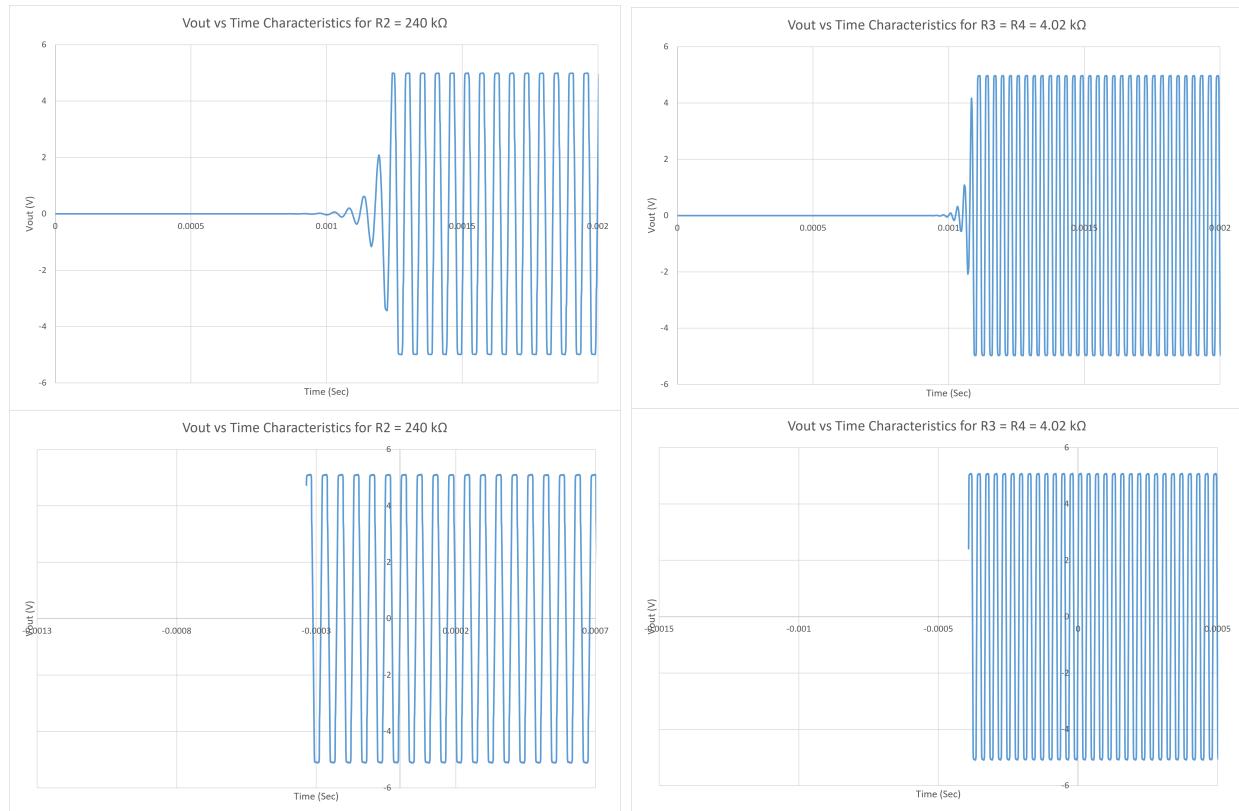


Figure 5: Output voltage V_o

Appendix

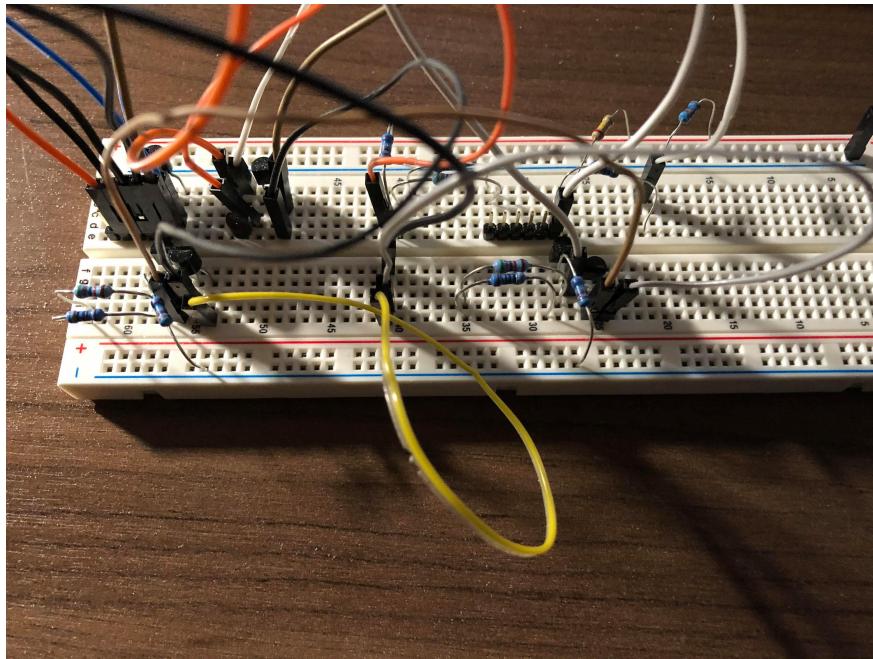


Figure 6: Circuit for Part 1

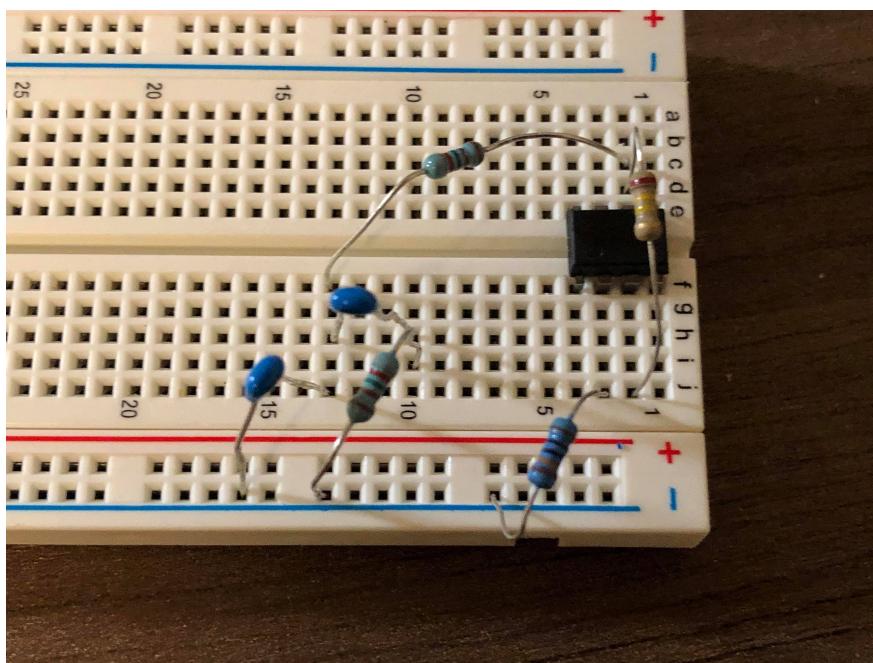


Figure 7: Circuit for Part 2