

# ELECENG 3EJ4 Lab 2

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## Part 1

- Q1.** The  $V_{o,min}$  and  $I_o$  of the current sink determined from the simulation data in Step 1.2 are  $V_{o,min} = -3$  V and  $I_o = 0.185$  mA. The simulation data is shown in Figure 1a. The  $V_{o,min}$  and  $I_o$  of the current sink determined from the measurement data were  $V_{o,min} = -3$  V and  $I_o = 0.199$  mA. The measurement data is shown in Figure 1b. The measured  $V_{o,min}$  value was the same as the simulated value, and the measured  $I_o$  value was similar to the simulated value.

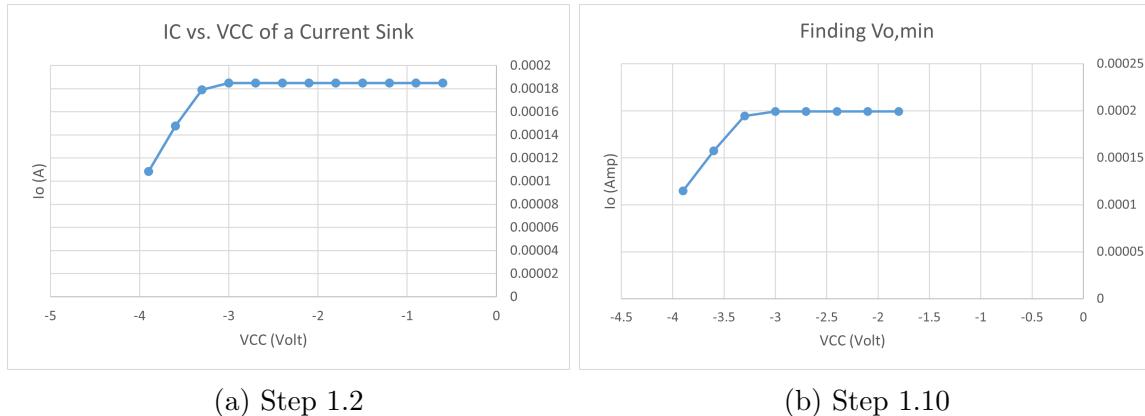


Figure 1: Determination of  $V_{o,min}$  and  $I_o$  of current sink

- Q2.** The values determined in Step 1.5 were  $V_{o1} = 4.94$  V and  $V_{o2} = -3.58$  V. These values are close to the maximum and minimum output voltages due to the value of  $V_{sig}$  at  $V_{o1}$  and  $V_{o2}$  being outside of the range the circuit works as an amplifier.

- Q3.** 1. The simulated DC  $V_o$  vs  $V_{sig}$  characteristics plot is shown in Figure 2.

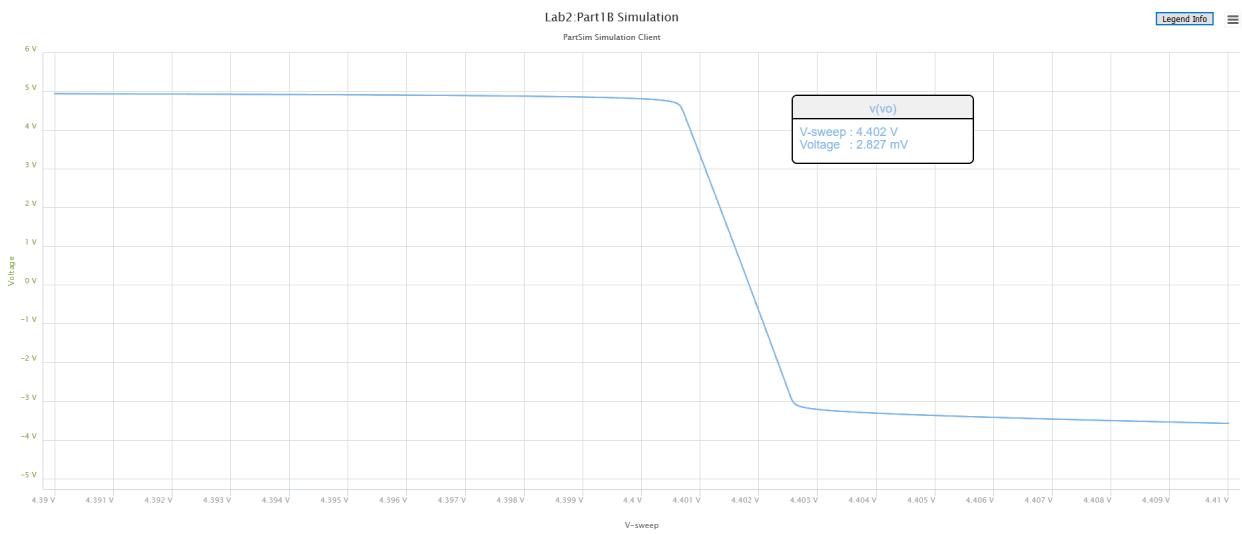


Figure 2: Simulated DC  $V_o$  vs.  $V_{sig}$  characteristics

2. For the circuit to work as an amplifier, the DC input range for  $V_{sig}$  is between 4.4005 V and 4.4025 V and the output voltage range for  $V_o$  is between 5 V and -3.6 V.
3. The value of  $V_{sig}$  for  $V_o \approx 0$  V is  $V_{sig} = 4.40183$  V, where the collector current  $I_{C2} = 185 \mu\text{A}$ .
4. The measured DC  $V_o$  vs  $V_{sig}$  characteristics plot is shown in Figure 3.

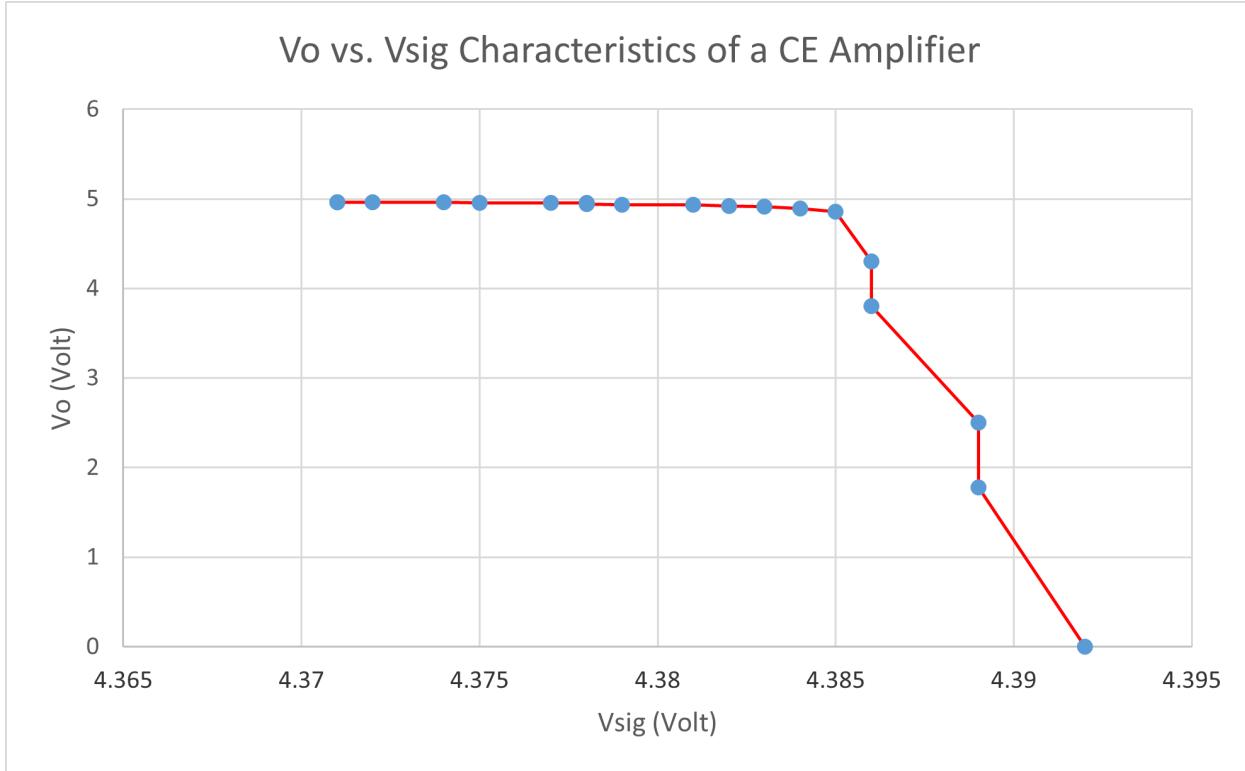


Figure 3: Measured DC  $V_o$  vs.  $V_{sig}$  characteristics

- Q4.**
1. The magnitude (in dB) and phase of the intrinsic voltage gain  $A_{vo}$  at low frequency (100 Hz) are 12.15 dB and 180°. The upper 3-dB frequency is approximately 14.4 KHz. The bode plots (with real magnitude and phase in degrees) are shown in Figure 4.
  2. The voltage gain  $A_{vo}$  calculated using the measured data in Steps 1.17 and 1.18 was 63.4 dB.
  3. The value of  $A_{vo}$  was 62.9 dB, very similar to the gain calculated at 100 Hz. However, the amplitudes of both signals were close to 0.707 of their original values ( $V_{QB2} = 0.7047$  V,  $V_o = 0.50683$  mW compared to  $V_{QB2} = 1$  V,  $V_o = 0.67577$  mW). The WaveForms screenshot can be seen in Figure 5.

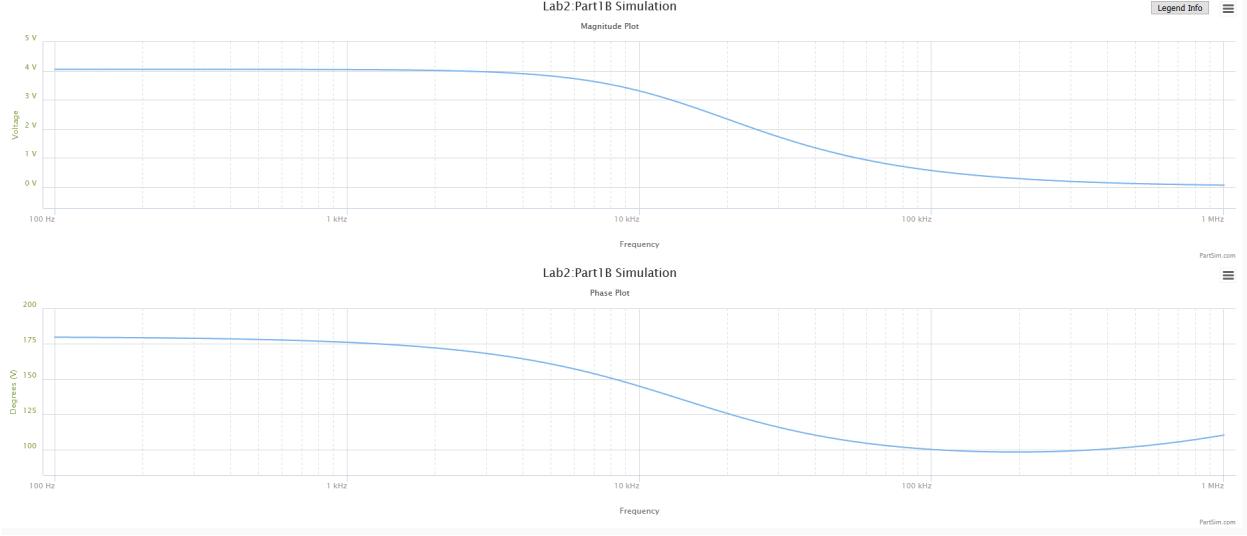


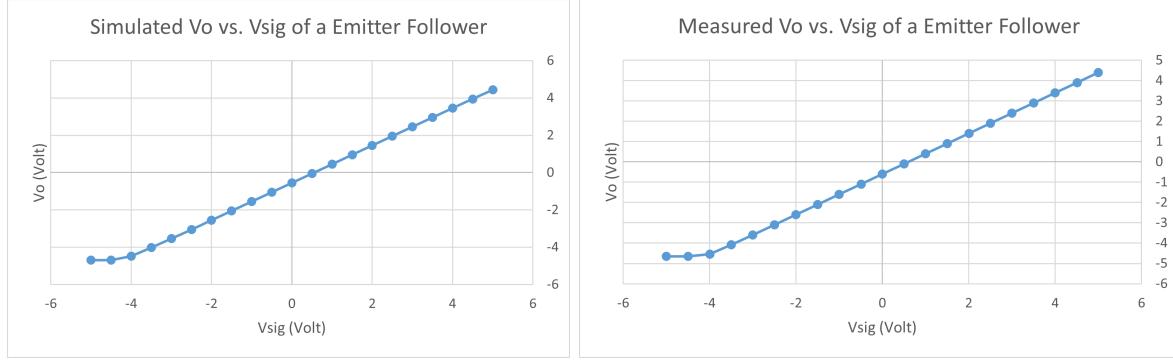
Figure 4: Bode plots of intrinsic voltage gain  $A_{vo}$  (real magnitude and phase in degrees)



Figure 5: WaveForms screenshot for Q4.3

## Part 2

- Q5.** 1. The simulated  $V_o$  vs  $V_{sig}$  characteristics are shown in Figure 6a. The measured  $V_o$  vs  $V_{sig}$  characteristics are shown in Figure 6b. The characteristics align with the expected characteristics of a common-collector amplifier, a near linear 1:1 voltage ratio due to the voltage gain being nearly zero.



(a) Step 2.2

(b) Step 2.6

Figure 6:  $V_o$  vs  $V_{sig}$  characteristics

2. The DC input range for  $V_{sig}$  was found to be  $V_{sig} > -4$  V and the voltage range for  $V_o$  was found to be around  $V_o > 4.5$  V.
3. The value of  $V_{sig}$  that results in  $V_o \approx 0$  V was found to be approximately 0.6 V.

**Q6.** Based on the simulation data obtained in Step 2.3, the magnitude and phase of the simulated intrinsic voltage gain  $A_{vo}$  at low frequency are  $-60$  dB and  $0^\circ$ . Based on the measurement data obtained in Step 2.8, the magnitude and phase of the measured intrinsic voltage gain  $A_{vo}$  at low frequency was determined to be  $0$  dB and  $0^\circ$ . The simulated bode plots for the intrinsic voltage gain  $A_{vo}$  (real magnitude and phase in degrees) is shown in Figure 7.

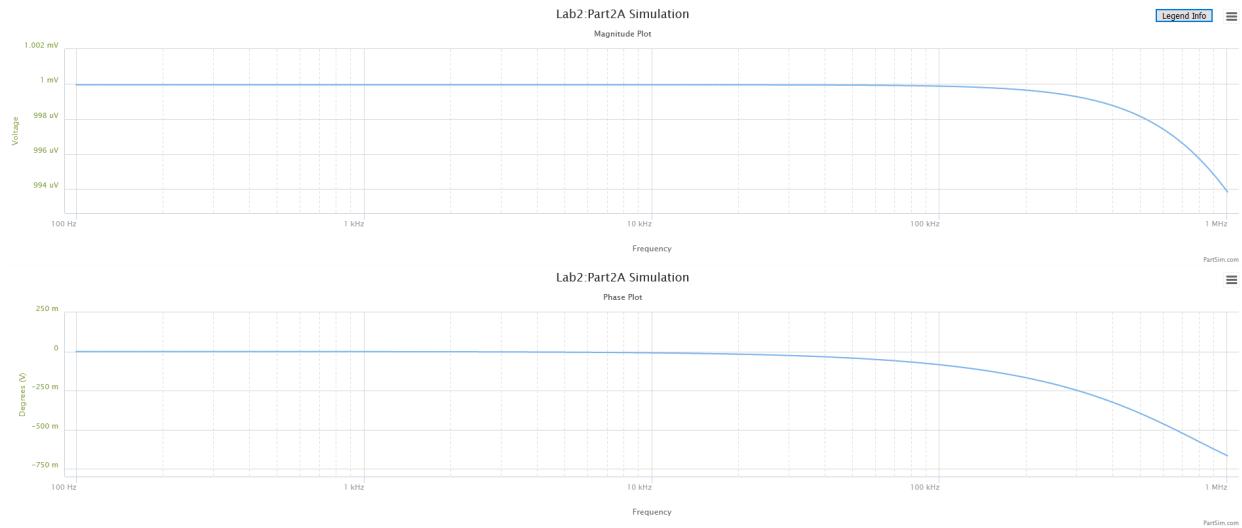


Figure 7: Bode plots for the intrinsic voltage gain  $A_{vo}$  (real magnitude and phase in degrees)

## Part 3

- Q7.** 1.  $V_o = 4.25 \text{ V}$ ,  $V_e = -0.525\text{V}$ ,  $I_{C2} = 90.91\mu\text{A}$ . A plot of the simulated data is shown in Figure 8.

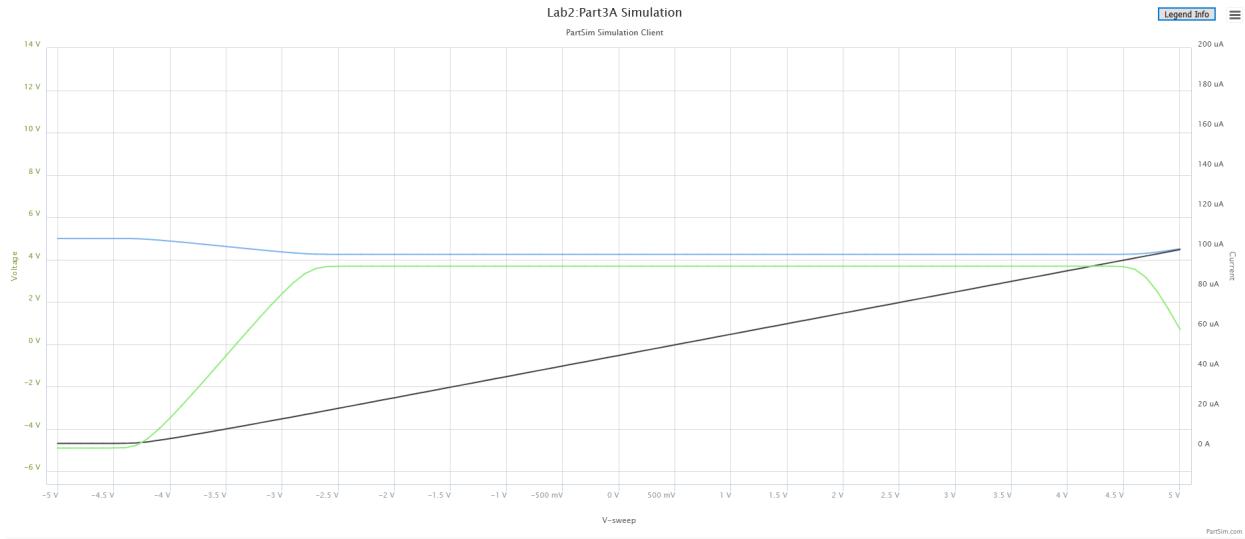
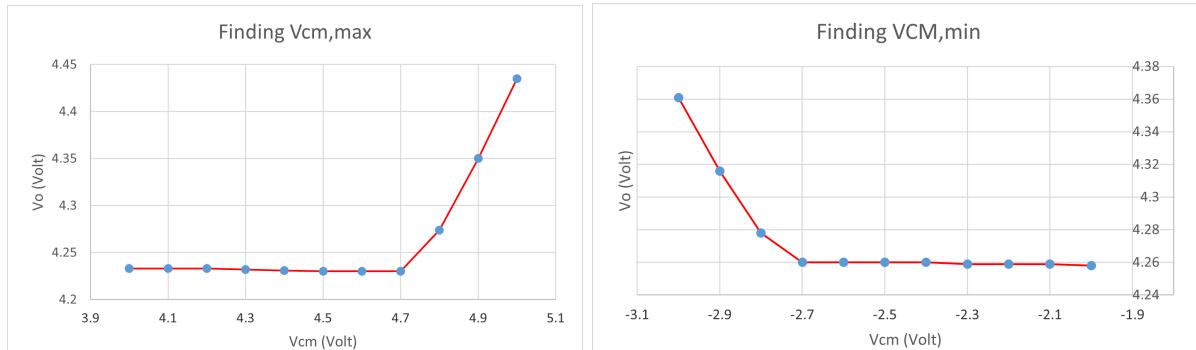


Figure 8: Step 3.2

2. The input common-mode range is  $-2.7 \text{ V} < V_{CM} < 4.7 \text{ V}$
3. The upper and lower bounds of the input common-mode range are determined by the regions where the BJT's collector current and output voltage are constant.
5. The input common-mode range determined using the measured data was  $-2.7 \text{ V} < V_{CM} < 4.7 \text{ V}$ , the same as the range determined in simulation. The plots of the measured data are shown in Figure 9.



(a) Step 3.10

(b) Step 3.11

Figure 9: Input common-mode range

- Q8.** The low-frequency voltage gain  $A_{cm}$  in dB for the common-mode signal was determined to be approximately -147 dB. The bode plots of voltage gain  $A_{cm}$  with real magnitude and phase in degrees are shown in Figure 10.

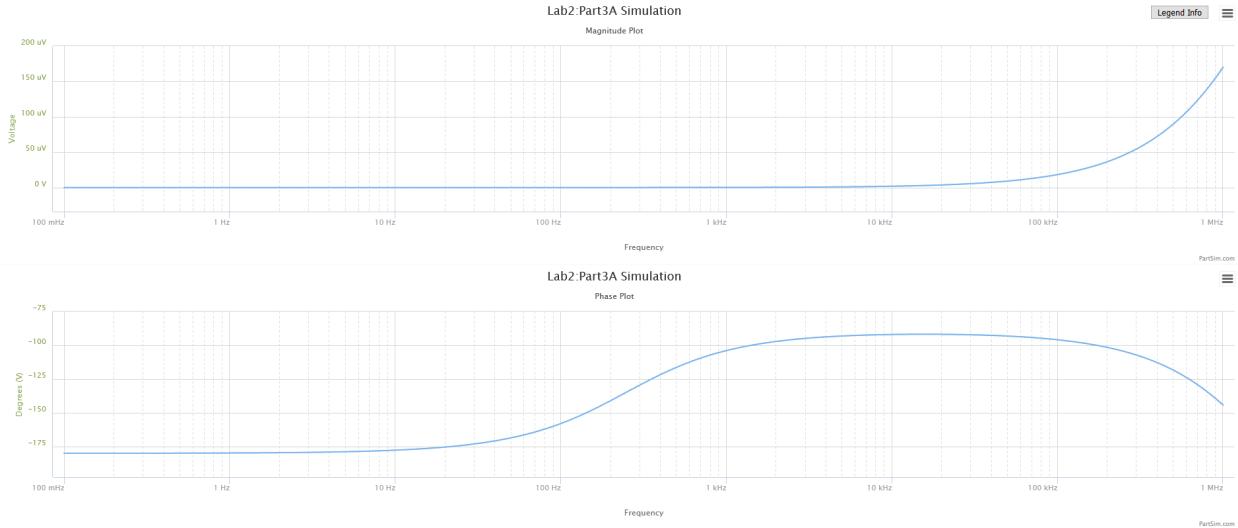


Figure 10: Bode plots for the voltage gain  $A_{cm}$  (real magnitude and phase in degrees)

- Q9.** The simulation data for Step 3.5 is shown in Figure 11.

1. The input differential-mode range was determined to be approximately  $-0.06 \text{ V} < V_{id} < 0.06 \text{ V}$ .
2. The upper and lower bounds are determined by finding the value of  $V_{id}$  that causes most of the current to flow through a single BJT (approximately 0.12 V), and dividing this value by 2.

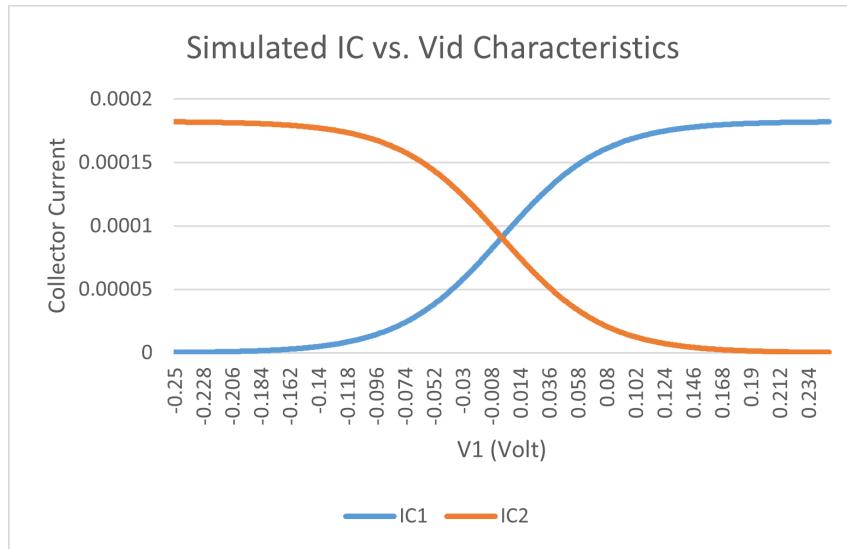


Figure 11: Step 3.5

- Q10.** 1. The voltage gain  $A_d$  in dB is -34.352 dB. The bode plots of voltage gain  $A_d$  with real magnitude and phase in degrees are shown in Figure 12.

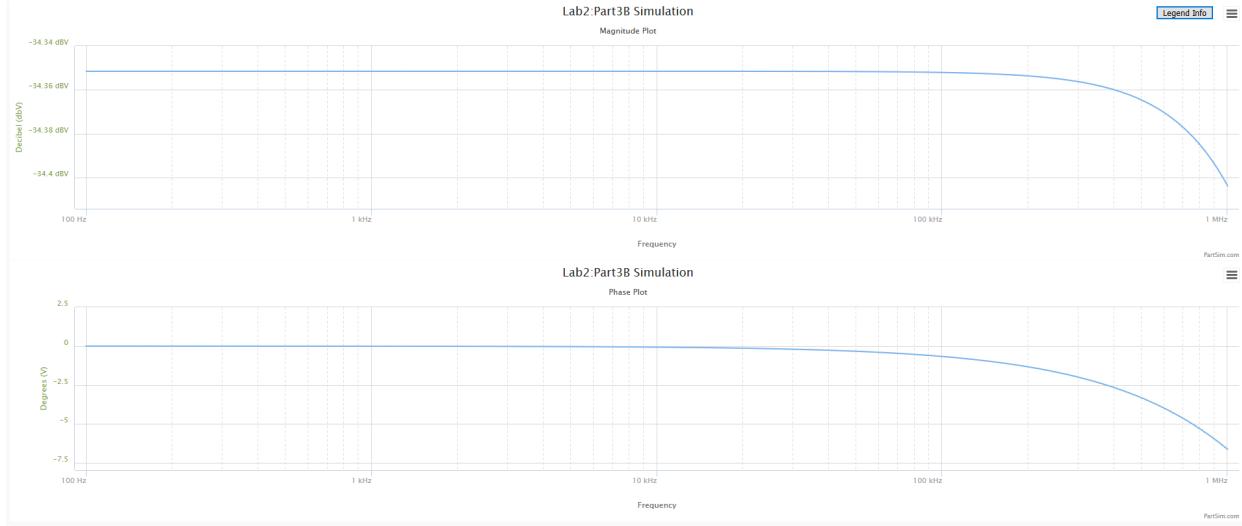
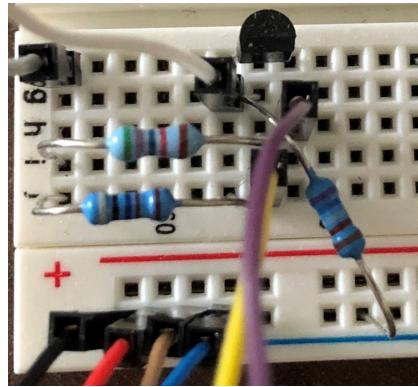


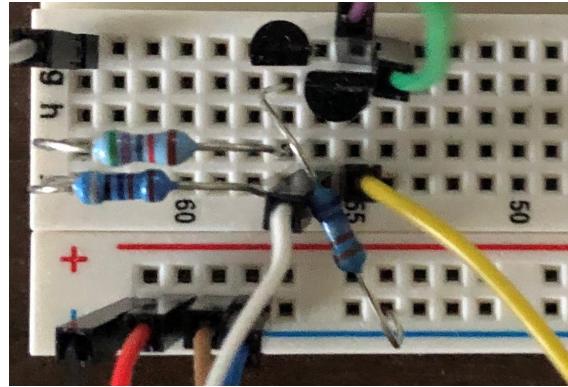
Figure 12: Bode plots for the voltage gain  $A_d$  (real magnitude and phase in degrees)

2. The DC analysis was extended to stop at a frequency of 10 MHz, and the upper 3-dB frequency was found to be approximately 8.4 MHz.
  3. The upper 3-dB frequency of this differential amplifier is extremely large (3 magnitudes greater) in comparison to the upper 3-dB frequency of the CE amplifier obtained in Q4 (8.4 MHz vs 14 KHz).
  4. The measured low-frequency differential voltage gain  $A_d$  was determined in Step 3.14 to be 20.5 dB.
- Q11.** The common-mode rejection ratio (CMRR),  $\frac{|A_d|}{|A_{CM}|}$ , was calculated to be approximately 112.5 dB.

# Appendix



(a) Part 1: C Circuit



(b) Part 1: D Circuit

Figure 13: Circuits for Part 1

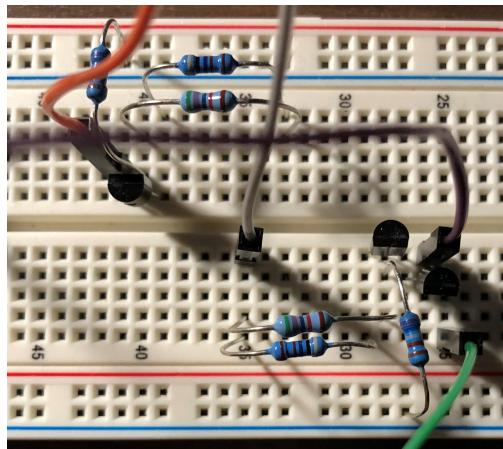
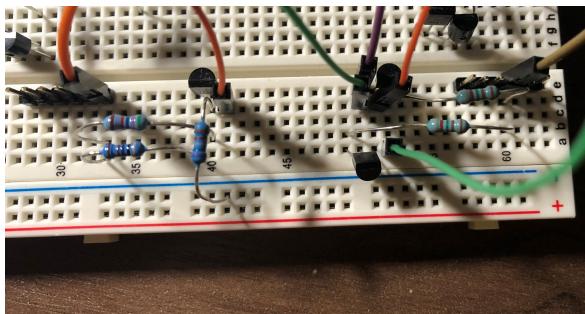
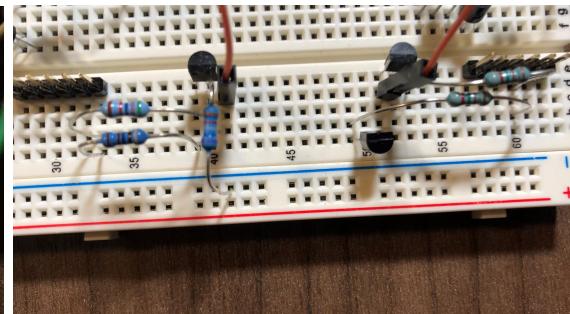


Figure 14: Part 2: B Circuit



(a) Part 3: C Circuit



(b) Part 3: D Circuit

Figure 15: Circuits for Part 3