The Hardware/Software Interface



Chapter 3

Subword parallelism

(This set contains adaptations of ten slides from MK Publishers' originals and 25 new, complementary slides by Luiz Santos)

Streaming SIMD Extension 2 (SSE2)

- Adds 8 × 128-bit registers
 - Extended to 16 registers in AMD64/EM64T
- Can be used for multiple FP operands
 - 2 × 64-bit double precision (double in C)
 - 4 × 32-bit single precision (float in C)
 - Instructions operate on them simultaneously
 - Single-Instruction Multiple-Data

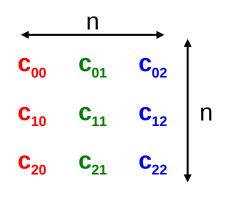
Example: Matrix Multiplication

- C = C + A × B (DGEMM)
 - Double precision General Matrix Multiply
- Hypothesis:
 - All 32 × 32 matrices, 64-bit double-precision elements
- C code:



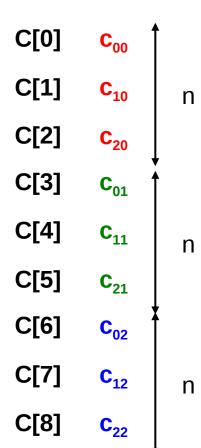
Matrix: vectorial representation

- For higher performance:
 - Single-dimensional representation of a matrix
 - Column-major transformation



Address arithmetic

Example: $c_{12} = C[1+2*3] = C[7]$



Unoptimized code:

```
1. void dgemm (int n, double* A, double* B, double* C)
2. {
3. for (int i = 0; i < n; ++i)
4.  for (int j = 0; j < n; ++j)
5.  {
6.  double cij = C[i+j*n]; /* cij = C[i][j] */
7.  for(int k = 0; k < n; k++ )
8.  cij += A[i+k*n] * B[k+j*n]; /* cij += A[i][k]*B[k][j] */
9.  C[i+j*n] = cij; /* C[i][j] = cij */
10. }
11. }</pre>
```



```
1. vmovsd (%r10),%xmm0 # Load 1 element of C into %xmm0
2. mov %rsi,%rcx # register %rcx = %rsi
3. xor %eax, %eax # register %eax = 0
4. vmovsd (%rcx), %xmm1 # Load 1 element of B into %xmm1
5. add %r9, %rcx # register %rcx = %rcx + %r9
6. vmulsd (%r8,%rax,8),%xmm1,%xmm1 # Multiply %xmm1,
  element of A
7. add $0x1, %rax # register %rax = %rax + 1
8. cmp %eax,%edi # compare %eax to %edi
9. vaddsd %xmm1,%xmm0,%xmm0 # Add %xmm1, %xmm0
10. jg 30 <dgemm+0x30> # jump if %eax > %edi
11. add $0x1, %r11d # register %r11 = %r11 + 1
12. vmovsd %xmm0,(%r10) # Store %xmm0 into C element
  (Inner loop only, i.e. it corresponds to lines 6 to 9 from source code)
```

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  (Inner loop only, i.e. it corresponds to lines 6 to 9 from source code)
```

- X86 assembly code: (generated with gcc, 2014 version) 1. vmovsd (%r10),%xmm0 # Load 1 element of C into %xmm0
- 2. mov %rsi,%rcx Cij (right) # register %rcx = %rsi
- 3. xor %eax,%eax # register %eax = 0
- 4. vmovsd (%rcx),%xmm1 # Load 1 element of B into %xmm1
- 5. add %r9, %rcx # register %rcx = %rcx + %r9
- 6. vmulsd (%r8,%rax,8),%xmm1,%xmm1 # Multiply %xmm1, element of A **a**ik **b**kj product
- 7. add \$0x1,%rax # register %rax = %rax + 1
- 8. cmp %eax,%edi # compare %eax to %edi
- 9. vaddsd %xmm1, %xmm0, %xmm0 # Add %xmm1, %xmm0 sum-of-products
- accumulator 10. jg 30 <dgemm+0x30> # jump if %eax > %edi
- 11. add \$0x1, %r11d # register %r11 = %r11 + 1
- 12. vmovsd %xmm0, (%r10) # Store %xmm0 into C element (Inner loop only, i.e. it corresponds to lines 6 to 9 from source code)



How to fully exploit AVX?

- Can be used for multiple FP operands
 - 4 × 64-bit double precision (double in C)
 - 8 × 32-bit single precision (float in C)
- How to exploit vector operations?
 - Cannot compute scalar times scalar
 - Classic (scalar) matrix traversal inadequate...

$$i = 0,1,2,3$$
 $j = 0$ $k = 0$

$$i = 0,1,2,3$$
 $j = 0$ $k = 1$

$$i = 0,1,2,3$$
 $j = 0$ $k = 2$

$$i = 0,1,2,3$$
 $j = 0$ $k = 3$

$$i = 0,1,2,3$$
 $j = 0$ $k = 4$

$$i = 0,1,2,3$$
 $j = 0$ $k = 5$

$$i = 0,1,2,3$$
 $j = 1$ $k = 0$

$$i = 0,1,2,3$$
 $j = 1$ $k = 1$

$$i = 0,1,2,3$$
 $j = 1$ $k = 2$

$$i = 0,1,2,3$$
 $j = 1$ $k = 3$

$$i = 0,1,2,3$$
 $j = 1$ $k = 4$

$$i = 0,1,2,3$$
 $j = 1$ $k = 5$

$$i = 0,1,2,3$$
 $j = 31$ $k = 31$

$$i = 4,5,6,7$$
 $j = 0$ $k = 0$

```
1. #include <x86intrin.h>

    void dgemm (int n, double* A, double* B, double* C)

3. {
4. for (int i = 0; i < n; i+=4)
5. for (int j = 0; j < n; j++) {
    __m256d c0 = _mm256_load_pd(C+i+j*n); /* c0 = C[i]
  [j] */
7. for( int k = 0; k < n; k++)
8.
     c0 = _{mm256} add_{pd}(c0, /* c0 += A[i][k]*B[k][j] */
9.
                _{mm256} _{mul} _{pd} (_{mm256} _{load} _{pd} (A+i+k*n),
10.
                _mm256_broadcast_sd(B+k+j*n)));
     _{mm256\_store\_pd(C+i+j*n, c0); /* C[i][j] = c0 */
11.
12. }
13. }
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  [j] */
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     c0 = _mm256_add_pd(c0, /* c0 += A[i][k]*B[k][j] */
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  [j] */
7. for( int k = 0; k < n; k++)
8. c0 = \underline{mm256}_{add}\underline{pd}(c0, /* c0 += A[i][k]*B[k][j] */
9.
                 _{mm256}mu1_{pd}(_{mm256}load_{pd}(A+i+k*n),
10.
                 _mm256_broadcast_sd(B+k+j*n)));
     _{mm256\_store\_pd(C+i+j*n, c0); /* C[i][j] = c0 */
11.
12. }
13. }
```



Optimized x86 assembly code:

```
# Load 4 elements of C into %ymm0
1. vmovapd (%r11),%ymm0
2. mov %rbx,%rcx
                       # register %rcx = %rbx
3. xor %eax, %eax
                        # register %eax = 0
4. vbroadcastsd (%rax,%r8,1),%ymm1 # Make 4 copies of B element
5. add $0x8,%rax
                 # register %rax = %rax + 8
6. vmulpd (%rcx),%ymm1,%ymm1 # Parallel mul %ymm1,4 A elements
7. add %r9,%rcx
                     # register %rcx = %rcx + %r9
8. cmp %r10, %rax
                       # compare %r10 to %rax
9. vaddpd %ymm1,%ymm0,%ymm0 # Parallel add %ymm1, %ymm0
10. jne 50 <dgemm+0x50> # jump if not %r10 != %rax
11. add $0x1,%esi
                   # register % esi = % esi + 1
12. vmovapd %ymm0, (%r11) # Store %ymm0 into 4 C elements
```

[Generated with gcc (2014 version) when using C Intrinsics to induce full AVX exploitation]

(Inner loop only, i.e. it corresponds to lines 6 to 11 from source code)



Impact of subword parallelism

- Experiment: 32 x 32 matrices
 - 2.6GHz Intel Core i7 (Sandy Bridge)
 - Using a single core
- Unoptimized DGEMM
 - 1.7 GigaFLOPS
- Optimized DGEMM
 - 6.4 GigaFLOPS
- Speed up: 3.85 times as fast!