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```
`timescale 1ns / 1ps
// Company:
// Engineer:
//
// Create Date:
                12:54:44 02/27/12
// Design Name:
// Module Name:
                piggy
// Project Name:
// Target Device:
// Tool versions:
// Description:
//
// Dependencies:
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
module piggy(clk, reset, b1_in, b5_in, b10_in, segment1, segment0, full_led);
   input clk, reset;
   input b1_in, b5_in, b10_in;
   output [6:0]segment1;
   output [6:0]segment0;
   output full_led;
   reg [6:0]segment1;
   reg [6:0]segment0;
   reg full led;
   reg [3:0]n;
   reg [3:0]s;
   reg [3:0]nn;
   reg [3:0]ns;
// Add code here
always @ (posedge clk)
  if (reset)
     begin
       s<=#1 0;
       n < = #1 0;
     end
  else
     begin
       s<=#1 ns;
       n<=#1 nn;
always @ (n or s or b1_in or b5_in or b10_in)
  begin
     case({b10_in, b5_in, b1_in})
        3'b000:
               begin
                  nn=n;
                  ns=s;
                end
        3'b001:
               if (n<9)
                  begin
                     nn=n+1;
                     ns=s;
                  end
                else if ((n==9) && (s==9))
                  begin
                     nn=n;
                     full_led = 1;
                  end
               else
```

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```
begin
                                nn=0;
71
                                ns=s+1;
72
                             end
73
                3'b010:
                         if (n<5)
                             begin
                                nn=n+5;
                                ns=s;
                             end
                          else if ((s==9) \&\& (n>4))
                             begin
                                nn=9;
80
                                ns=9;
                                full_led = 1;
                             end
84
                         else
85
                             begin
                                nn=n-5;
                                ns=s+1;
                             end
                3'b011:
                         if (n<5)
                             begin
                                nn=n+5;
92
93
                                ns=s;
                             end
                         else if ((s==9) && (n>4))
                             begin
                                nn=9;
98
                                ns=9;
99
                                full led = 1;
100
                             end
101
                         else
102
                             begin
103
                                nn=n-5;
104
                                ns=s+1;
105
                             end
                3'b100: if (s==9)
106
107
                             begin
108
                                nn=9;
109
                                ns=9;
110
                                full_led = 1;
111
                             end
112
                         else
113
                             begin
114
                                nn=n;
115
                                ns=s+1;
116
                             end
117
                3 b101: if (s==9)
118
                             begin
119
                                nn=9;
120
                                ns=9;
                                full_led = 1;
121
122
                             end
123
                         else
124
                             begin
125
                                nn=n;
126
                                ns=s+1;
127
                             end
128
                3'b110:
                         if (s==9)
129
                             begin
                                nn=9;
130
131
                                ns=9;
132
                                full_led = 1;
133
                             end
134
                         else
135
                             begin
136
                                nn=n;
```

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```
ns=s+1;
                      end
         3'b111:
                  if (s==9)
                     begin
                        nn=9;
                        ns=9;
                         full_led = 1;
                      end
                  else
                     begin
                         nn=n;
                        ns=s+1;
                      end
      endcase
   end
always @ (n or s)
   if ((n==9) && (s==9))
      full_led = 1;
   else
      full_led = 0;
always @ (n)
   case (n)
      0: segment0 = 7'b1111110;
      1: segment0 = 7'b0110000;
      2: segment0 = 7'b1101101;
      3: segment0 = 7'b1111001;
      4: segment0 = 7'b0110011;
      5: segment0 = 7'b1011011;
      6: segment0 = 7'b0011111;
      7: segment0 = 7'b1110000;
      8: segment0 = 7'b1111111;
      9: segment0 = 7'b1111011;
      default: segment0 = 7'bx;
   endcase
always @ (s)
   case (s)
      0: segment1 = 7'b1111110;
      1: segment1 = 7'b0110000;
      2: segment1 = 7'b1101101;
      3: segment1 = 7'b1111001;
      4: segment1 = 7'b0110011;
      5: segment1 = 7'b1011011;
      6: segment1 = 7'b0011111;
      7: segment1 = 7'b1110000;
      8: segment1 = 7'b11111111;
      9: segment1 = 7'b1111011;
      default: segment1 = 7'bx;
   endcase
```

endmodule