OpenFPGA: An Open-Source Framework for Agile Prototyping Customizable FPGAs

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***Abstract*—Demanded by ever-evolving data processing algorithms, field-programmable gate arrays (FPGAs) have become essential components of modern computing systems, thanks to their reconfigurable and distributed computing capabilities. However, FPGAs are among the very few integrated chips that still require long development cycles and high human efforts, even for industrial vendors. In this article, we introduce OpenFPGA, an open-source framework that can automate and significantly accelerate the development cycle of customizable FPGA architectures. OpenFPGA allows users to customize their FPGA architectures down to circuit-level details using a high-level architecture description language and autogenerate associated Verilog netlists which can be used in a backend flow to generate production-ready layouts. A generic Verilog-to-Bitstream generator is also provided, allowing end-users to implement practical applications on any FPGAs that OpenFPGA can support. Using OpenFPGA, we demonstrate less than 24-h layout generation of two FPGA fabrics, which are based on a Stratix-like architecture built with a commercial 12-nm standard cell library and 40-nm custom cells, respectively.**

Heterogeneous computing has become the mainstream solution to executing high-performance data processing applications. Field-programmable gate arrays (FPGAs) are ubiquitous components in modern heterogeneous computing systems, playing an enabling role for programmable accelerators.[1] To maximize their execution efficiency, FPGA fabrics have to be tailored for domain-specific applications so that they can cooperate seamlessly with other

Digital Object Identifier 10.1109/MM.2020.2995854
Date of publication 21 May 2020; date of current version 30 June 2020.

Published by the IEEE Computer Society

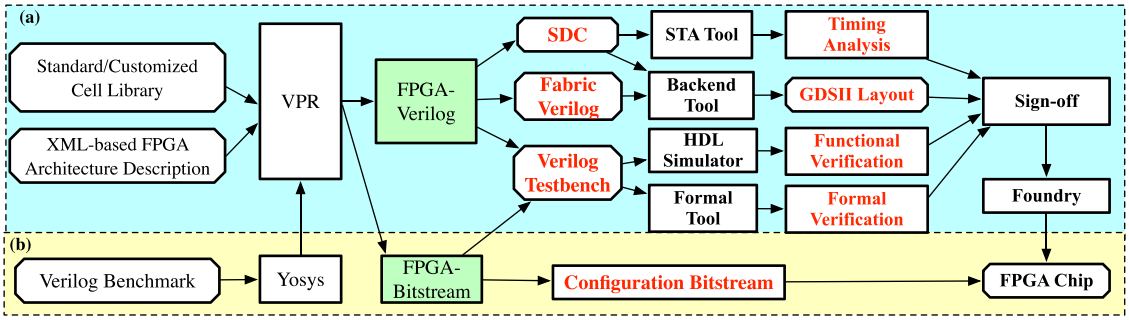

Figure 1. OpenFPGA design flow. (a) Production flow. (b) End-user flow.

computing resources.[2] For example, existing FPGA products cannot all offer the large number of memory blocks and multipliers required by AI accelerators. However, FPGAs are among the last few digital integrated circuits that require significant full-custom optimizations and long development cycles, even for industrial leaders. The major barrier for chip designers is the strong expertise required on both the hardware and software components, which may take years to acquire. From a hardware perspective, manual layouts are still widely used in FPGA fabrics, imposing significant manual efforts when porting to a new technology node. From a software perspective, associated electronic design automation (EDA) tools, e.g., bitstream generation, have to be tuned for each FPGA architecture. Due to such high development costs, commercial products widely adopt general-purpose but not domain-specific FPGA architectures, which may miss the peak efficiency required by modern data science applications. Driven by these applications, embedded FPGA (eFPGA) industrial players and academic researchers have developed automated methodologies,[3–8] where FPGA fabrics are described with Verilog netlists and implemented using a semicustom design tool suite. However, these pioneering works are still in their infancy, and their tools are closed-source as they often contain proprietary information.

In this article, we introduce OpenFPGA, an open-source framework that enables agile prototyping for modern and customizable FPGA architectures. As illustrated in Figure 1, OpenFPGA framework consists of two design flows. (a) The production flow, which can translate an XML-based FPGA architecture description to gate-level Verilog netlists of the whole FPGA fabric that can be fed into a physical design backend flow to obtain a complete GDSII layout. Besides, the production flow can autogenerate testbenches to perform pre- and post-layout verification. Synopsys design constraint (SDC) files are also autogenerated to enable timing-driven backend flows and to conduct post-layout timing analysis. Once the signoff is completed, the GDSII layout is ready for tapeout. (b) The end-user flow, that allows FPGA developers to transcript applications written in Verilog to configuration bitstream and implement them on the FPGA fabric. This is similar to standard vendor tools, e.g., Xilinx Vivado. We demonstrate the capability of OpenFPGA by prototyping a medium-size heterogeneous FPGA fabric whose architecture is similar to Stratix IV. Both layout generations are completed within 24 h. Using OpenFPGA, standard cell FPGAs can be ported to advanced technology nodes with few manual efforts and benefit significant performance improvement. As for custom FPGAs, OpenFPGA can produce an initial layout with a 60%/20% area/performance gap when compared to a commercial state-of-the-art.

RELATED WORKS

Previous works have proven the feasibility of agile production for customized FPGA fabrics by exploiting semicustom design flows.[3–8] These works share the same principle with the production flow of the OpenFPGA framework, as depicted in Figure 1(a), where complete layout generation is achieved in two steps: 1) describe an FPGA architecture as Verilog netlists and 2) use commercial ASIC design tools to synthesize RTL designs into standard cell libraries. Early attempts rely on manually crafted RTL netlists for FPGA architectures

as well as transistor-level circuit designs.[3,4] However, such methodology is inefficient to support a wide range of FPGA architectures necessary to enable domain-specific applications. Early works focus only on developing fabric generators while neglecting associated bitstream generators.[3,4] Recent works typically build Verilog and bitstream generation backends on the popular VTR framework,[9] so that customizable FPGAs and overlays can be easily supported by leveraging the rich VTR's XML-based architecture description language.[5–8,10] Note that previous works all show that semicustom designed FPGAs have a considerable performance gap when compared to commercial products. This is mainly due to missing many pragmatic features of modern FPGAs.

We propose a novel OpenFPGA framework, providing a complete toolchain to prototype customizable FPGA fabrics and implement applications on the FPGAs.

1) Multimode logic blocks, which can effectively improve resource utilization rate, are only supported in recent works.[5,6]
2) Heterogeneous blocks, which are ubiquitous in commercial FPGAs. However, only Grady *et al.*[6] has investigated this.
3) Tile-based architecture, an essential feature to develop million-of-LUT FPGAs, while only an early work covered this.[3]
4) Bitstream generation, a fundamental EDA support for FPGAs, which is missing in a few works.[3,4,7]
5) Custom cell support, a key to high-performance FPGAs. For instance, commercial FPGAs use transmission gates to build routing multiplexers rather than standard cells. This has not been supported in any previous works.

Besides, lack of verification techniques and backend codesign techniques are common problems, which may limit the usability of these tools. OpenFPGA is so far the only tool that supports all of these features.

OpenFPGA FRAMEWORK

We propose a novel OpenFPGA framework, providing a complete toolchain to prototype customizable FPGA fabrics and implement applications on the FPGAs. To achieve these purposes, we developed two backends, FPGA-Verilog and FPGA-bitstream generators, on top of the VPR tool suite, as highlighted in green in Figure 1. We also extend the XML-based FPGA architecture language to support detailed circuit-level description and binding to standard/customized cell libraries. As a result, OpenFPGA can support any FPGA architecture that VPR can model as well as a versatile circuit implementation of primitive blocks, such as routing multiplexers and lookup tables (LUTs). Note that FPGA-Verilog and FPGA-bitstream generators are the core engines of the OpenFPGA framework, driving two types of design flows: (a) the production flow, which aims at achieving production-ready GDSII from an XML-based FPGA architecture description file; (b) the end-user flow, which provides Verilog-to-Bitstream compilation for user applications.

FPGA-Verilog Generator: FPGA-Verilog converts an XML-based FPGA architecture description to technology-mapped full-fabric Verilog netlists. The autogenerated fabric netlists include both a programmable fabric with configuration-chain circuits embedded. As shown in Figure 2(a), the programmable fabric consists of an array of tiles where a few columns may be replaced by heterogeneous blocks. Note that FPGA-Verilog generates highly hierarchical fabrics, where large FPGAs can be built with a small number of repeatable tiles. This can significantly simplify the backend process, where only a few unique tiles are P&Red and then are assembled in a final layout. FPGA-Verilog can support flexible routing architectures even inside each tile, which can be customized by the VPR architecture description language. The configuration-chain circuits consist of configurable memory elements, i.e., configuration-chain flip-flops (CCFFs), connected to a configuration chain, where configuration bitstreams are loaded serially. Currently, OpenFPGA adopts a configuration chain because it is straightforward to implement and easy to debug. In the future, OpenFPGA will support more versatile configuration circuitry, e.g., frame-based, which can efficiently enable partial reconfiguration during FPGA runtime. Moreover, FPGA-Verilog can autogenerate netlists that are mapped to a standard cell library and even

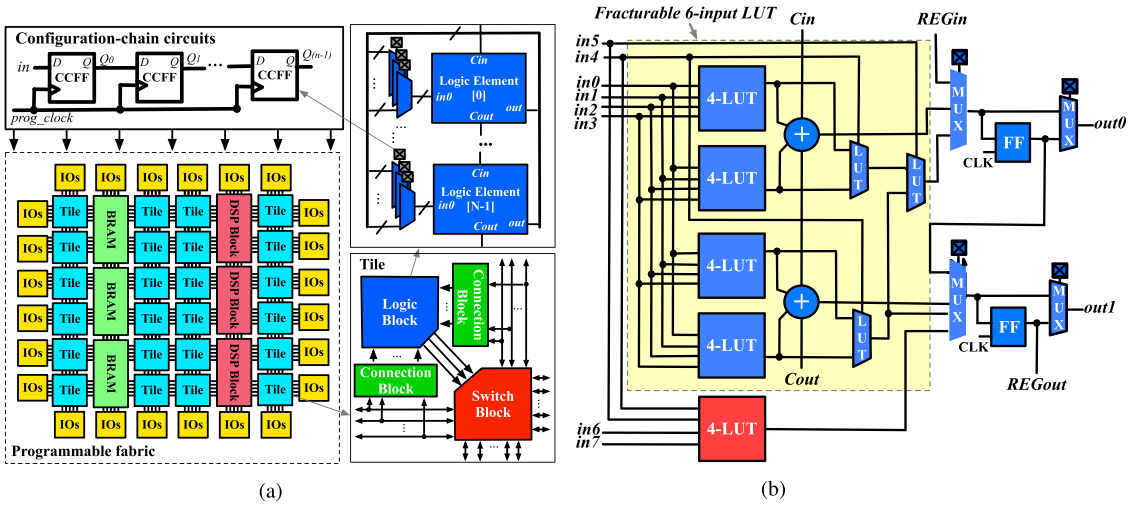

Figure 2. Tile-based heterogeneous FPGA architecture. (a) Tile organization and configuration circuits. (b) LE architecture considered in the showcased fabrics in Figure 4.

customized logic cells, approaching current state-of-the-art FPGA technologies. For instance, one-level and multilevel routing multiplexers, as well as fracturable LUTs, are commonly used in commercial FPGAs while being unavailable in standard cell libraries. We refer interested readers to[11,12] for more details.

Verilog Testbench Generator: FPGA-Verilog can autogenerate two types of Verilog testbenches to validate the correctness of the fabric before tapeout: full and formal-oriented. Both testbenches share the same organization, as depicted in Figure 3(a). To enable self-testing, the FPGA and user's RTL design (simulated using an HDL simulator) are driven by the same input stimuli, and any mismatch on their outputs will raise an error flag. Full testbench aims at simulating an entire FPGA operating period, consisting of two phases: 1) the configuration phase, where the synthesized design bitstream is loaded to the programmable fabric, as highlighted by the green rectangle of Figure 3(b); 2) the operating phase, where random input vectors are autogenerated to drive both devices under test (DUTs), as highlighted by the red rectangle of Figure 3(b). Using the full testbench, users can validate both the configuration circuits and programming fabric of an FPGA. However, the testing vectors used in the full testbench may lead to only a small set of functional coverage. To guarantee a higher coverage, we developed the formal-oriented testbench, where a programmed FPGA is instantiated with the user's bitstream. The module of the programmed FPGA is encapsulated with the same port mapping as the user's RTL design and thus can be fed to a formal tool for a 100% coverage formal verification. Compared to the full testbench, this skips the time-consuming configuration phase, reducing the simulation time, potentially also significantly accelerating the functional verification, especially for large FPGAs. As the size of the bitstream increases quadratically with the FPGA size, the number of clock cycles required to load the bitstream becomes a dominating factor in the verification runtime. In summary, OpenFPGA allows designers and test engineers to customize the testbenches by applying a different combination of benchmarks and

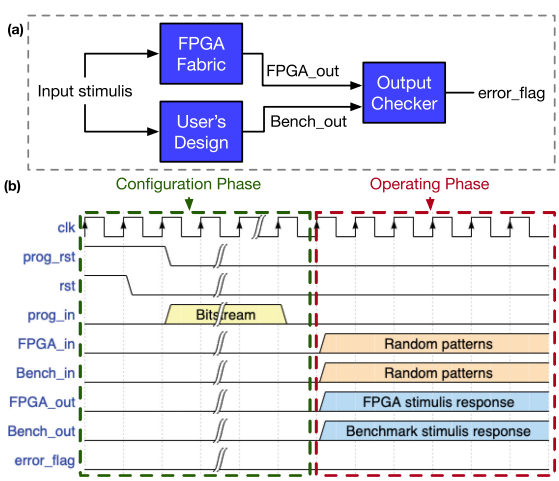

Figure 3. Principles of testbenches organization. (a) Block diagram. (b) Waveforms.

testing vectors. We believe that with proper use of the self-testing testbenches, the verification process for FPGAs can be significantly simplified or even automated.

SDC Generator: FPGA-Verilog can also generate two sets of SDC files. The first set of SDCs is intended for backend tools, which constrains pin-to-pin timing for all the resources in the FPGA to obtain homogeneous delays across the fabric. Each pin-to-pin timing can be specified by users in the XML-based architecture language. The SDCs also break all the combinational loops, which do legally exist across an FPGA fabric. Note that this is an exclusive challenge in the backend strategy for FPGAs, as combinational loops are considered illegal in the ASIC backend flow. The second set of SDCs is designed for STA tools, which disable unused resources in the mapped FPGA fabric, to perform timing analysis of a specific benchmark at the post layout stage. More details are available in the OpenFPGA online documentation.[11]

Bitstream Generator: FPGA-Bitstream generates a configuration bitstream, which can be directly loaded into the configuration circuit of the FPGA fabric [see Figure 2(a)]. FPGA-Bitstream is a generic bitstream generator, natively supporting any FPGA architecture that can be modeled by VPR as well as various circuit designs, such as fracturable LUTs, one/multilevel multiplexers, etc. This indicates that instant EDA support for the FPGA fabric is ready for users once the XML-based architecture description is finalized. More details are available in the work by Tang *et al.*[11]

EXPERIMENTAL RESULTS

We demonstrate OpenFPGA's capabilities by implementing two FPGA fabrics: 1) a 20×20 homogeneous FPGA using a commercial 40-nm technology; 2) a 32×32 heterogeneous FPGA using a commercial 12-nm technology. In both FPGAs, each tile includes ten logic elements (LEs) and a local routing architecture with 50% connectivity. To showcase the customization level that OpenFPGA can offer, we consider a multimode LE architecture for the homogeneous FPGA, as shown in Figure 2(b), with a similar logic capacity as the Stratix-IV. The LE consists of a 6-input fracturable LUT, a 4-input LUT, two 1-bit adders, and two flip-flops, which can operate in six different modes. The heterogeneous FPGA employs a similar LE without the 4-input LUT, as highlighted red in Figure 2(b). A column of 512-kb block RAMs (BRAMs), generated by a foundry memory compiler, is located in the center of the heterogeneous fabric. Note that even though our FPGA fabric is smaller than the Stratix IV, it has a similar LUT/RAM density, guaranteeing a high utilization of both resources. Full details about the showcased FPGA fabrics are listed in Table 1.

Table 1. Comparison on the FPGAs in Figure 4.

Resource/Capacity	Homogeneous	Heterogeneous
Array size	20×20	32×32
Tileable routing	$\times$	✓
Fracturable 6-input LUTs	4k	9.92k
4-input LUTs	8k	N/A
1-bit full adder	8k	19.84k
Flip-flops	8k	19.84k
Block RAM	N/A	512kbits
I/Os	480	124
Routing channel width	300	200
Routing wires	87% L4 13% L16	L4
Fc_{in}	0.055	0.15
Routing Multiplexer	one/two-level	tree-like
Backend details	**Homogeneous**	**Heterogeneous**
Tool	Cadence Innovus 19.1	Synopsys ICC2 2019.03
Layout area	$7mm^2$	$9mm^2$
Flow type	Two-step flatten	Hierarchical
Runtime	24 hr	12 hr
Peak Memory	60 GB	215 GB

Fabric Implementation: To showcase the agility of OpenFPGA, the two FPGA architectures are implemented using two different PnR strategies. The homogeneous FPGA was implemented using a two-step backend flow where configurable logic blocks (CLBs) are P&Red first and then instantiated at the top-level as hard macros. To leverage the symmetry of an FPGA fabric, the heterogeneous FPGA adopted a more hierarchical backend flow, where a first library of hard macros for CLBs, connection blocks, and switch blocks is built and then assembled in the final layout. The hierarchical backend flow allows us to optimize each hard macro with respect to the timing constraints generated by our tool with few combinational loops to be broken. Therefore, the heterogeneous FPGA is larger in array size, while its backend is $2\times$ faster than the homogeneous. The runtime and memory usage are well within our server's capability,

Table 2. Area and delay comparison between previous works,[6] OpenFPGA, and Stratix IV.

Generality Delay	Baseline [6]	Homo-FPGA	Stratix IV	Hetero-FPGA
Technology	40nm	40 nm	40nm	12nm
Cell Library	Standard	Custom[1]	Custom	Standard
Tile Area (μm^2)	30,625 (100%)	17,648 (-42%)	11,050 (-63%)	8,373 (-72%)
Path Delay (ns)	**Baseline [6]**	**Homo-FPGA**	**Stratix IV**	**Hetero-FPGA**
Process Corner	TT	SS	SS[2]	TT
6-LUT	0.5 (100%)	0.27 (-46%)	0.28 (-44%)	0.23 (-54%)
20-bit Adder[3]	1.63 (100%)	2.12 (+30%)	1.23 (-25%)	1.13 (-31%)
Local Routing[4]	0.27 (100%)	0.17 (-37%)	0.23 (-15%)	0.15 (-44%)
L4 track[5]	2.53 (100%)	0.82 (-67%)	0.59 (-76%)	0.75 (-70%)
Average	100%	-30%	-40%	(-50%)

[1] Use custom cells only in routing multiplexers and configuration chains. The rest are standard cells. See details in [11]
[2] Consider the slow model in Quartus STA.
[4] Local routing path starts from a BLE output and ends at a BLE input.
[5] LX track: FF→length-X wire→Local Routing→LUT→FF.

which operates a 64-bit RedHat Linux on 64 Intel Xeon Processors clocked at 2.6 GHz and 512-GB memory. Note that the statistics are shown to demonstrate the capability of OpenFPGA to accommodate different backend strategies, rather than discussing the differences between both backend tools. Commercial signoff tools are then used to ensure that both fabrics are DRC-clean.

Custom FPGA Evaluation: For a comprehensive analysis, we consider the area, pin-to-pin delays as well as the delays of the implemented benchmarks when evaluating the FPGA fabrics. In Table 2, the homogeneous FPGA is compared to two baselines, a commercial Stratix-IV FPGA and a resembled academic counterpart.[6] We believe it is a fair comparison since these FPGAs are similar in architecture and also implemented using 40-nm technologies. Our results prove the high value of using one-level and two-level multiplexing structures as well as an optimized cell library, which can improve the area by 42% and path delay by 30% when compared to a standard cell FPGA. Indeed, our fabric is 60% larger in area and 20% slower in path delays than the well-optimized commercial FPGA. We believe that the performance gap can be reduced through a careful codesign between backend strategies and custom cell implementations.

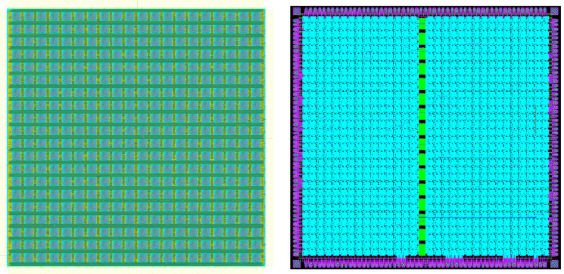

Figure 4. Complete layout of FPGA fabrics. (a) Homogeneous (40 nm). (b) Heterogeneous (12 nm).

For performance benchmarking, we selected eight MCNC circuits that fit all the 40-nm FPGAs. Each benchmark is verified through the self-testing Verilog testbenches in Figure 3, using Mentor ModelSim and Synopsys Formality. Quartus 18.1.0 is used to implement the same benchmark set as the industry baseline, and the device model is set to the Stratix IV EP4S40G2F40C2. Figure 5(a) shows that our custom cell FPGA is $2\times$ slower on average than the Stratix IV. The gap comes from the hardware lags in performance, with an average of 20%. When critical paths consist of multiple routing paths listed in Table 2, the delay difference will aggregate.

Standard Cell FPGA Evaluation: We compare the heterogeneous FPGA in Figure 4(b) to a

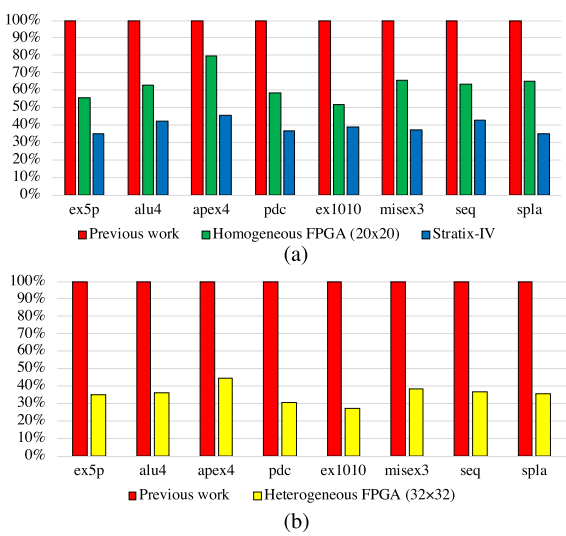

Figure 5. Delay comparison between OpenFPGA and previous works[6] using selected MCNC benchmarks. (a) Impact of custom cells and multiplexers on FPGAs at 40 nm. (b) Standard cell FPGAs scaling from 40 to 12 nm.

previous work,[6] using the same methodology as for the 40-nm FPGAs. Note that both FPGAs are implemented by standard cells and also similar in architecture while using different technologies. Our results show that using OpenFPGA, FPGA architectures can be portable between different technology nodes and benefit significant performance improvements. In Table 2, the 12-nm FPGA is 72% smaller in area and 50% faster in path than the 40-nm baseline. In Figure 5 (b), the heterogeneous FPGA is $3\times$ faster on average in benchmark delays than the 40-nm baseline.

CONCLUSION

In this article, we introduced OpenFPGA, an open-source framework that enables rapid prototyping of customizable FPGA architectures through a semicustom design approach. We proposed an XML-to-Prototype design flow, where the Verilog netlists of a full FPGA fabric can be autogenerated and then fed into a backend flow. We also developed a Verilog-to-Bitstream design flow for the associated CAD tools, especially a generic bitstream generator supporting *any* FPGA architectures that can be described by the XML language. To demonstrate OpenFPGA's capabilities, we implemented a 20×20 homogeneous and a 32×32 heterogeneous FPGA fabric whose architectures are similar to the Stratix IV, using commercial 40-nm and 12-nm technologies, respectively. Both layout generations are completed within 24 h. Using OpenFPGA, standard cell FPGAs can be ported to advanced technology nodes with few manual efforts and benefit significant performance improvements. As for custom FPGAs, OpenFPGA can produce an initial layout with a 60%/20% area/performance gap when compared to a commercial state-of-the-art FPGA. OpenFPGA, including source codes, documentation, and architectures shown in this article, is publicly available.[11]

In this article, we introduced OpenFPGA, an open-source framework that enables rapid prototyping of customizable FPGA architectures through a semicustom design approach.

ACKNOWLEDGMENTS

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