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Microprocessadores e Projetos Digitais

Trabalho Final

# ISA do RISC-V

| Tipo/Bits | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | | | | | RS2 | | | | RS1 | | | | RD | | | FUNC3 | | | OPCODE | | | | | |
| I | | IMM | | | | | | | RS1 | | | | RD | | | FUNC3 | | | OPCODE | | | | | |
| S & B | | IMM | | | | | | | RS1 | | | | RS2 | | | FUNC3 | | | OPCODE | | | | | |
| J | | IMM | | | | | | | | | | | RD | | | IMM | | | OPCODE | | | | | |

| Tipo | Instrução | Nome | FUNC3 | OPCODE | Descrição |
|---|---|---|---|---|---|
| R | ADD | Addition | 000 | 0000 | add rd, rs1, rs2 |
| | SUB | Subtraction | 001 | | sub rd, rs1, rs2 |
| | MUL | Multiplication | 010 | | mul rd, rs1, rs2 |
| | DIV | Division | 011 | | div rd, rs1, rs2 |
| | SLL | Shift Left Logical | 100 | | sll rd, rs1, rs2 |
| | SLT | Shift Right Logical | 101 | | slt rd, rs1, rs2 |
| I | ADDI | ADD Immediate | 000 | 0001 | addi rd, rs1, imm |
| | SLLI | Shift Left Logical Imm | 001 | | slli rd, rs1, imm |
| | SLTI | Shift Right Logical Imm | 010 | | slti rd, rs1, imm |
| | LW | Load Word | 000 | 0011 | slti rd, rs1, imm |
| | JALR | Jump And Link Reg | 000 | 0110 | jalr rd, rs1, imm |
| B | BEQ | Branch Equal | 000 | 0010 | beq rs1, rs2, imm |
| | BNE | Branch Not Equal | 001 | | bne rs1, rs2, imm |
| | BLT | Branch Less Than | 010 | | blt rs1, rs2, imm |
| | BGE | Branch Greater or Equal | 011 | | bge rs1, rs2, imm |
| S | SW | Store Word | 000 | 0100 | sw rs1, rs2, imm |
| J | JAL | Jump And Link | | 0101 | jal ra, imm |