

Another question that arises is whether the algorithm removes all the redundant edges. This is true for the following reasons: 1) the rows $I + 1$ to N do not have any redundant entries, and 2) row I can have 1's only in columns greater than $I + 1$.

Thus the theorem is established. Indirectly, the algorithm makes use of the fact that the nonredundant graph of a precedence graph is unique (see [2] for a proof).

IV. ANALYSIS OF THE ALGORITHM

A. Time Complexity

The analysis is made assuming that step 4 can be performed in unit time. In fact, this is the assumption for analyzing Warshall's algorithm. Though in practice step 4 is not totally independent of N , the growth of time with respect to N of step 4 is very low. Hence we can assume without loss of generality that step 4 is independent of N .

It can be easily observed that the time required in the worst case (when all the elements above the diagonal are 1's) is proportional to $[(N - 1)N]/2$, whereas Yelowitz's algorithm [2] requires time of the order N^3 .

B. Paging Complexity

In the case of Yelowitz's algorithm [2], the number of times the entire matrix is paged in (i.e., swapping N rows from the auxiliary storage to main memory) is always N ; this follows from the fact that the whole matrix has to be swapped in to the main memory for each column scan.

In our case, it can be easily observed that the number of times the entire matrix is paged in is $(N - 1)/2$ in the worst case.

V. FINAL REMARKS

In this section, we briefly discuss the relationship of our algorithm with the interpretive structural modeling process [4].

The term interpretive structural modeling [4] refers to the systematic applications of some elementary notions of graph theory in such a way that theoretical, conceptual, and computational leverage is exploited to efficiently construct a directed graph, or network representation, of the complex pattern of a contextual relationship among a set of elements. The interpretive structural modeling (ISM) is based upon the one-to-one correspondence between a binary matrix and a graphical representation of a directed network. In the realm of ISM, Warfield [5] deals with one of the important problems of synthesizing hierarchies of a complex system. It must be noted that this problem is sometimes essential and often desirable in the study of complex systems, in developing plans, in managing organizations, and in various other kinds of human endeavors. In [5], Warfield describes a) procedures for constructing a binary matrix from the given set of subordination relations, and b) procedures for constructing hierarchical graph from the matrix.

The algorithm (Table I) discussed in this paper gives a neat solution to the problem b) both from a computational point of view and a conceptual point of view.

Further, from the analysis in the previous sections it can be observed that our algorithm is more efficient than that described in [2] by an order N . Also, the algorithm has better paging characteristics than that of [2]. The paging complexity of [2] is N in all cases whereas the worst case paging complexity of the algorithm described is $(N - 1)/2$. Further, in the algorithm of Table I it is

possible to use sparse matrix techniques [3] for storing M , without difficulties.

To conclude, the algorithm of Table I is superior to that of the existing algorithms.

ACKNOWLEDGMENT

The author thanks Dr. P. V. Sankar for invaluable discussions. The author is indebted to the referee for his constructive remarks in revising the paper.

REFERENCES

- [1] R. K. Shyamasundar and E. V. Krishnamurthy, "Algorithms for constructing hierarchical graphs," *IEEE Trans. Syst., Man, Cybern.*, vol. SMC-4, pp. 459-461, Sept. 1974.
- [2] L. Yelowitz, "An efficient algorithm for constructing hierarchical graphs," *IEEE Trans. Syst., Man, Cybern.*, vol. SMC-6, pp. 327-329, Apr. 1976.
- [3] D. E. Knuth, *The Art of Computer Programming*, Vol. I: *Fundamental Algorithms*. Reading, MA: Addison-Wesley, 1968.
- [4] J. N. Warfield, *Structuring Complex Systems*. Battelle Monograph, Battelle Memorial Inst., Columbus, OH, Apr. 1974.
- [5] ———, "On arranging elements of a hierarchy in graphic form," *IEEE Trans. Syst., Man, Cybern.*, vol. SMC-3, pp. 121-133, Mar. 1973.

SIGHT-I: A COMPUTER VISION SYSTEM FOR AUTOMATED IC CHIP MANUFACTURE

MICHAEL L. BAIRD

Abstract—A computer vision system was developed for locating and inspecting integrated circuit chips for their automatic alignment during various manufacturing processes at the General Motors Delco Electronics Division. This system, called SIGHT-I, is currently in production use. The application, vision strategy, system components, and performance are described.

I. INTRODUCTION

In 1972, General Motors Research Laboratories and Manufacturing Development Staff demonstrated the technical feasibility and potential usefulness of computer vision applied to complex industrial parts, in an experiment to automatically mount automobile wheels onto hubs [23], [24]. This experimental system was not intended for production operation.

In 1974, a laboratory facility for machine perception research became operational. This laboratory is based on computer network concepts, with a DEC PDP 11/45 process control computer acting as the interface between the specialized equipment of the laboratory (cameras, picture display device, positioning tables, robot arm) and an IBM 370/168 host computer supporting graphic consoles [6].

Also in 1974, an extensive survey of potential computer vision applications within the Corporation was conducted with the objective of identifying a "nontrivial" pilot production task, or class of tasks, to which applied computer vision research and development could be best directed. (By "nontrivial" we mean to exclude those applications that can and are being automated through the use of binary imaging and very simple analysis.) The

Manuscript received July 19, 1976; revised August 15, 1977.

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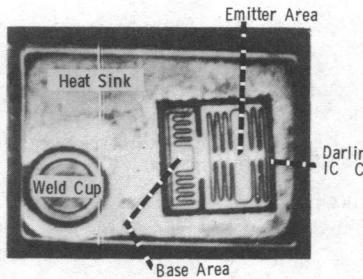


Fig. 1. Darlington assembly.

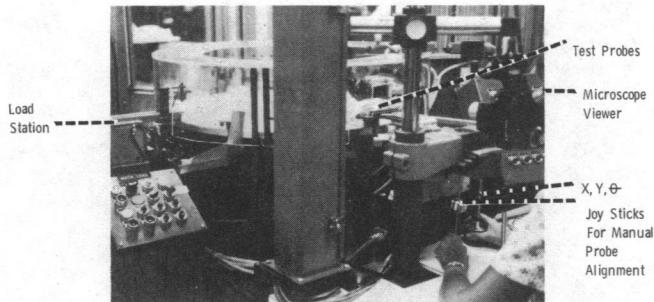


Fig. 2. Manually operated Darlington electrical test probe station.

pilot task identified was the automatic alignment and inspection of electronic components at Delco Electronics.

In 1975 the pilot computer vision system was demonstrated in the laboratory and by 1977 the system, called SIGHT-I, was fully integrated into production.

II. THE APPLICATION

A. The Part

The part subject to visual recognition (for location determination) and inspection (for size, placement, and integrity) is shown in Fig. 1. (The photograph is a mirror image and is taken from a TV monitor.) This assembly consists of 1) a large (8.89 mm × 12.70 mm) heat sink mounted firmly in a fixture (fixture not visible), 2) a weld cup on a corner of the heat sink, and 3) the object of interest, a Darlington power transistor-pair IC chip (5.26 mm × 5.26 mm) which is bonded to the surface of the heat sink. This assembly is a component in the high-energy ignition system installed in all new General Motors automobiles [19].

B. The Process

Before the development of SIGHT-I, these assemblies were automatically fed into the rotating table shown in Fig. 2, where human operators 1) visually (through a microscope or on a TV monitor) determined the location (position and orientation) of the IC chip on the heat sink, 2) inspected for any gross defects in the chip (e.g., cracked, missing, undersized, off the edge of the heat sink, rotated too much, or displaced too close to the weld cup), and 3) manually manipulated a set of electrical test probes over the base and emitter areas of the chip (as shown in Fig. 1) via the joy sticks shown. One stick translates and the other rotates the probe assembly. Depression of a foot pedal then lowered the probes onto the chip and initiated the automatic electrical test process which within one second brought a new assembly into view and the cycle repeated.

In order to increase product quality and increase throughput

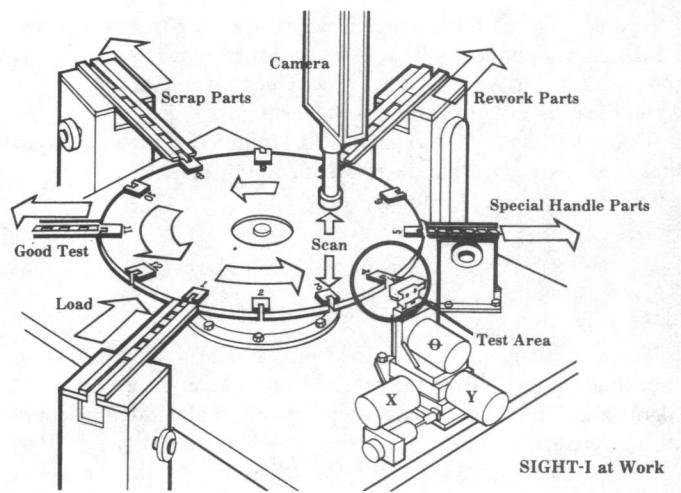


Fig. 3. Automated Darlington electrical test probe station.

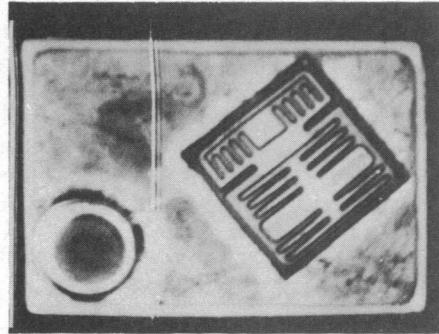


Fig. 4. Darlington chip tilted greater than ±30 degrees.

(the operator cannot perform the recognition, inspection, and manipulation tasks as fast as the machine can cycle), this type of machine was fully automated through the use of computer vision technology. Fig. 3 is an artist's rendition of the automated Darlington electrical test probe station. The operator, microscope viewer, and joy sticks have been replaced by a solid-state instrumentation camera, interfaced to a mini-computer for sensing the assembly at the stage before electrical test. Computer controlled alignment tables then manipulate the test probes into position over the chip at the next stage.

III. VISION OBJECTIVES AND STRATEGY

A. Objectives

It was determined that the required positional accuracy of the chip could be attained from a 50 × 50 digitized image of the assembly.

The recognition programs must 1) determine the location of the chip (e.g., by determining the coordinates of its four corners), and 2) inspect for defective assemblies where chips are a) rotated too much for the automatic test equipment (as illustrated in Fig. 4), b) off the edge of the heat sink (as illustrated in Fig. 5), c) too close to the weld cup for the automatic test equipment (as illustrated in Fig. 6), d) partial, missing corner, or fractured (as illustrated in Fig. 7), e) cut to undersize (as illustrated in Fig. 8), or f) completely missing (as illustrated in Fig. 9).

A "relational template matching" approach, as exemplified in [5], [8], and [12], was followed for location determination, and a

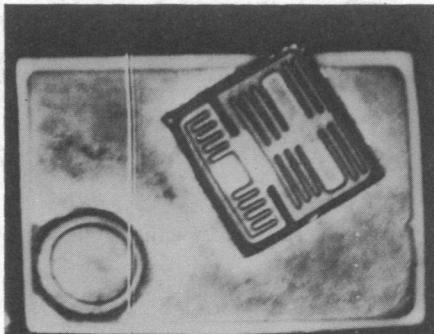


Fig. 5. Darlington chip too close to heat sink edge.

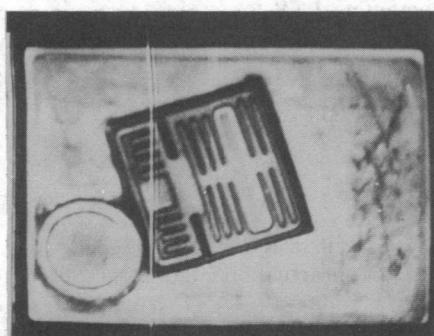


Fig. 6. Darlington chip too close to weld cup.

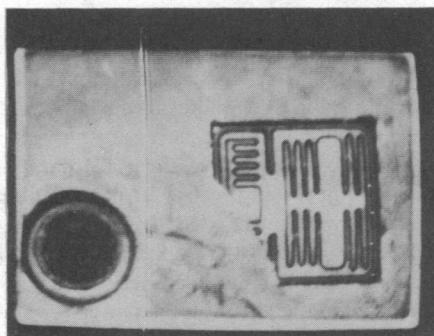


Fig. 7. Defective Darlington chip.

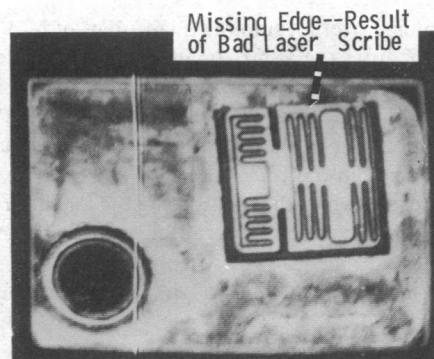


Fig. 8. Darlington with edge cut off.

contrast detection scheme performed the inspection tasks which did not occur as part of the location determination process. The reader interested in the theory and motivation for using "relational descriptions" (or exploitation of contextual constraints) is referred to [2]-[4], [7], and [16].

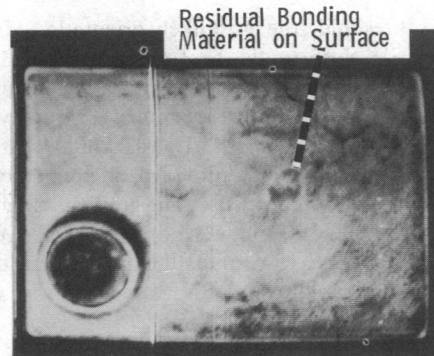


Fig. 9. Missing Darlington chip.

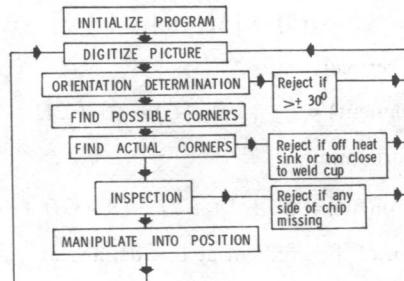


Fig. 10. Program logic flow chart.

The time available to recognize and inspect an assembly was less than one second. In addition, the production line target for the system demanded a very high reliability.

B. Strategy

A set of computer programs performs the vision task through the following sequence of five steps.

- 1) Digitize to obtain a 50×50 image of the assembly.
- 2) Determine the approximate orientation (rotation or tilt) of the chip on the heat sink (through gradient direction analysis). At this point, inspection for a chip rotated too much can be made.
- 3) Locate possible corners of the chip in the image (through small local template matching).
- 4) Determine the actual four corners of the chip (by selecting the four most likely possible corners). The four corners defined are constrained to be in a rectangular spatial configuration of known size, and must exhibit the approximate orientation established in step 2). At this point, inspection for chips off the edge of the heat sink or too close to the weld cup can be made.
- 5) Inspect for chip integrity (cracked, fractured, undersized, missing corner(s), partial, or completely missing) by looking for uniform contrast around the chip boundary.

This sequence is depicted in the flow chart shown in Fig. 10. Steps 2-5 are described in more detail in the following paragraphs.

- 1) *Determining Approximate Orientation of the IC Chip on the Heat Sink:* The approximate orientation of the chip on the heat sink is computed by taking advantage of the fact that the chip boundary and most of its internal details exhibit "edges" having directions parallel or perpendicular to each other. Thus each picture element (pixel) is examined (by application of a "gradient" operator) to determine whether or not it constitutes an edge point. By examining the relative frequency of occurrence of all the directions of the edge points (i.e., those points whose gradient magni-

tudes exceed a threshold), the most likely orientation of the chip is determined. Pixels close to the heat sink edges are ignored in order to avoid introduction of a strong zero-degree component.

Several gradient operators were examined for quality of results and execution time requirements. It was found that a simple approximation to the gradient provided adequate results at a minimum of computational expense. The gradient magnitude and direction were computed as follows. For each pixel E of interest, let A, B, C, D, F, G, H, I denote (the light intensities of) its immediate neighbors as shown:

$$\begin{array}{ccc} A & B & C \\ D & E & F \\ G & H & I \end{array}$$

Then the magnitude of the gradient at E is defined as

$$G(E) = |\Delta I| + |\Delta J|$$

where ΔI (the vertical

$$\text{component}) = (A + 2B + C) - (G + 2H + I),$$

and ΔJ (the horizontal

$$\text{component}) = (C + 2F + I) - (A + 2D + G).$$

The direction of the gradient at E is defined as

$$D(E) = \arctan(\Delta I / \Delta J).$$

It is known that the chip is rotated no more than $\pm 45^\circ$. Each $D(E)$ is therefore mapped into this range, if necessary (since we are interested in the overall orientation of the chip, not of each internal feature or individual side) by merely adding or subtracting 90° degrees.

In order to determine the dominant edge direction, an array of accumulators (one for each degree) is used to keep a count of the weighted frequency of occurrence of edge directions. By weighting an edge direction directly proportional to its magnitude, more emphasis is given to significant edges in the image [25].

The final step in determining the chip orientation was to smooth the data in the accumulators with a simple nonweighted, low-pass filter (of width 15 pulses or degrees) to eliminate any spurious peaks in the distribution. The approximate orientation of the chip, then, is taken to be that degree value for which the corresponding accumulator value is maximum. At this point, chips rotated too much for the automatic test equipment can be so identified.

2) Locating Possible Corners of the IC Chip: The system now knows that a chip of width α and height β exists at some approximate orientation θ in the digitized image. The recognition strategy at this point becomes one of finding the four corners of the chip which would establish its exact position. In order to do this, the entire picture matrix is first scanned, assigning to each pixel a probability that it centers on a corner of the chip. This measure is achieved by the application of small local templates.

Local templates (LT's) are functions which assign to picture elements a weak local probability that such an element is the center of a corner (a black region surrounded by a white region). The field of view is such that one can assume that each of the four different types of corners (northeast, northwest, southwest, and southeast) occupy quadrants 1, 2, 3, and 4 of the picture, respectively. Thus four different LT's are applied in a manner which partitions the picture.

The LT used is given below for a northwest corner, which

would be a black region ($A B C D E$) surrounded to the left and top by a white region ($F G H M N P Q$):

$$\begin{array}{cccc} M & N & P & Q \\ H & C & B & A \\ G & D & & \\ F & E & & \end{array}$$

The local template value (LTV) for picture point (X, Y) is defined as

$$\begin{aligned} \text{LTV}(X, Y) = & F + 2G + 2H + M + 2N + 2P + Q \\ & - 3A - 2B - C - 2D - 3E. \end{aligned}$$

The figure below thus indicates the relative weight of each picture element in computing LTV for a northwest corner point. This weighting proved to be particularly effective for parts whose corners were rounded off.

$$\begin{array}{cccc} 1 & 2 & 2 & 1 \\ 2 & -1 & -2 & -3 \\ 2 & -2 & & \\ 1 & -3 & & \end{array}$$

Because of the small sizes of the LT's, good values were obtained regardless of the actual orientation of the chip, and thus no effort was made to "rotate" the LT's to compensate for the known approximate orientation. The result of processing a picture P with the four LT's is a new picture P' in which corners are enhanced. It is through P' that the search will continue. This leads to the definition of the global template for determining the actual four corner points of the part.

3) Determining the Actual Four Corners of the IC Chip: The four actual corner points of the chip are selected by applying a "relational mask" or "global template" to the LTV data described above. A global template (GT) measures, for any specified location in the picture, to what degree the LTV data support the hypothesis that the object (chip) exists at that location. Thus, for example, if a location were specified as "corner i is at picture point (X_i, Y_i) , $i = 1, 2, 3, 4$ (such that the points form a rectangle of the required size, and within some tolerance of the approximate orientation calculated above)," the global template value (GTV) is computed as

$$\text{GTV} = \sum_{i=1}^4 \text{LTV}(X_i, Y_i).$$

The GT is applied over all suitable quadruples of LTV points (in the range $\pm 15^\circ$ from the approximate orientation calculated) to assure finding the optimal embedding. Fig. 11 graphically illustrates this step where a rectangle is superimposed over the original picture corresponding to the location where the global template value is maximized in the LTV data.

The reader can observe that computing the maximum GTV is a special case of maximizing a generalized embedding metric [12]:

$$M = \sum_{i=1}^p \sum_{j=1}^i G_{ij}(C_i, C_j)$$

where $G_{ij}(C_i, C_j)$ is a local measure of the "goodness of fit" exhibited by the relation G between components C_i and C_j .

At this point, chips found to be off the edge of the heat sink, too close to the weld cup, or rotated too much, can be so identified as part of the inspection task. We note that since the field of view includes part of the fixture, the chip can usually be located even if several of its corners are off the heat sink.

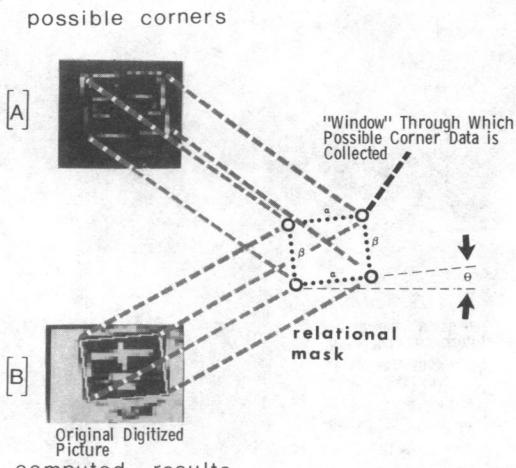


Fig. 11. Relational template matching.

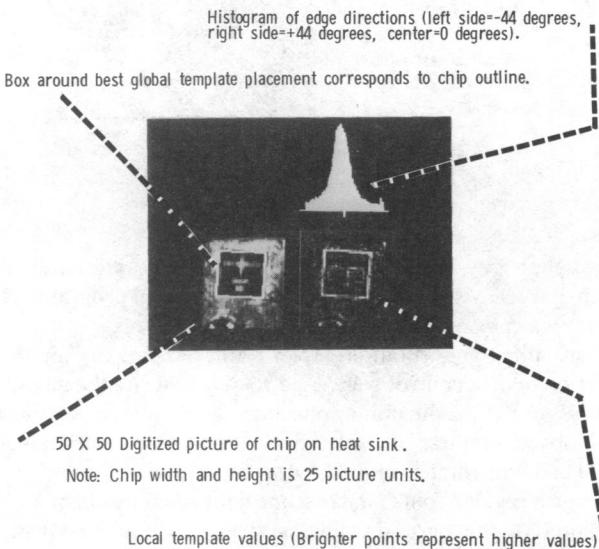


Fig. 12. Contents of graphic display.

4) Inspecting for IC Chip Integrity: In order to complete the remaining inspection objectives (identify broken, cracked, undersized, fractured, missing chips), a simple contrast detection scheme is utilized. This step involves measuring the contrast across each of the four sides and corners of the chip. Contrast is computed as the difference between the average light intensity of the background and the edge of the chip. If the contrast falls below a specified threshold anywhere along the boundary of the chip, the system identifies that assembly as being defective. An algorithm for efficiently summing diagonal lines in an array was developed for this task.

C. Some Recognition Results

Fig. 12 illustrates a typical graphic display depicting the recognition of the position and orientation of a chip on a heat sink. Captions in the illustration summarize the salient contents of the display. Shown are 1) the original 50×50 gray-level picture (lower left), 2) the histogram of relative frequency of occurrence of weighted gradient directions in the picture (upper right), 3) a "corner-enhanced" picture in the lower right. (Because of the implementation, this picture, unfortunately, does not reflect the true LTV data, as it is the result of smaller 4 point corner func-

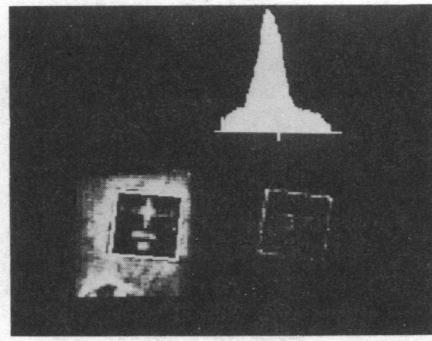


Fig. 13. Graphic displays for OK2.PIC.

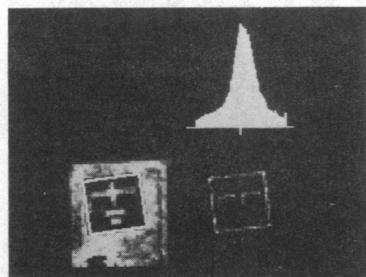
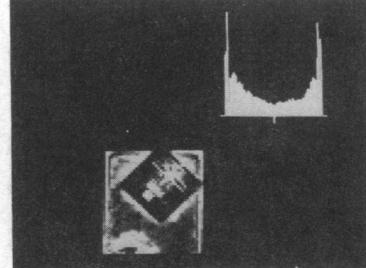


Fig. 14. Graphic displays for OK6.PIC.

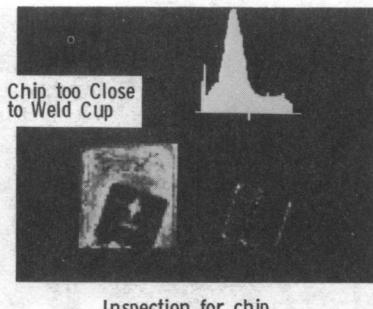
Inspection for chip orientation rejected part
Fig. 15. Graphic displays for TILT3.PIC.

tions as opposed to the 12 point LT functions described above.), and 4) a rectangle superimposed over the original digitized picture corresponding to the location of the optimal embedding of the GT in the LTV data. During execution of the program this rectangle is redisplayed each time a better fit of the GT is found. The visual result is a convergence of the rectangle into its correct recognition location. The absence of a rectangle indicates the part was rejected due to improper location on the heat sink. Figs. 13-19 illustrate similar displays associated with recognition of a variety of other chips.

IV. MAJOR SYSTEM COMPONENTS

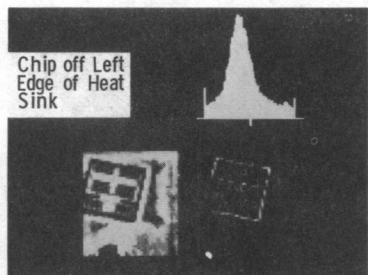
Several of the major components of the pilot system are illustrated in Fig. 20.

We chose to use a commercially available solid-state diode array camera providing 16 levels of gray with a spatial resolution of 50×50 .



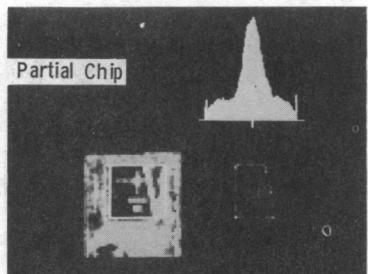
Inspection for chip location rejected part

Fig. 16. Graphic displays for WC3.PIC.



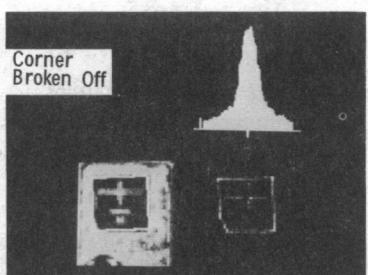
Inspection for chip location rejected part

Fig. 17. Graphic displays for EDGE5.PIC.



Inspection for chip integrity rejected part

Fig. 18. Graphic displays for CK1.PIC.



Inspection for chip integrity rejected part

Fig. 19. Graphic displays for CK4.PIC.

The computer utilized for development was a DEC PDP 11/45 with large core memory, floating point hardware, and peripheral disks and tape drive. This permitted easy program development and debugging. For demonstrations, however, the machine would simulate the smaller production minicomputer requiring only 8K of core and having no floating point hardware.

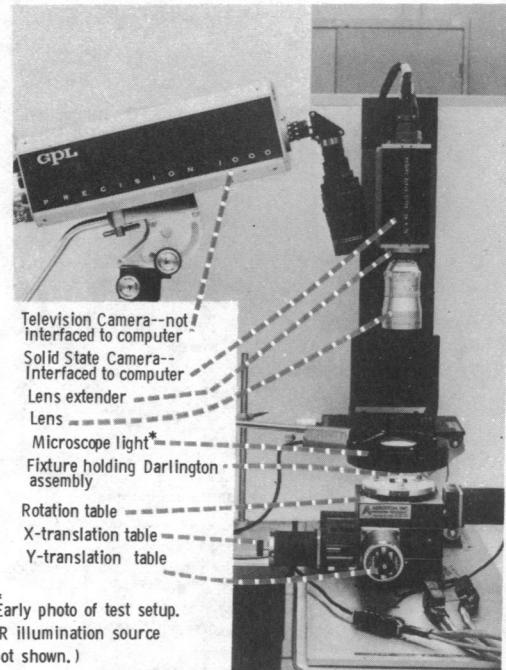


Fig. 20. Cameras, optics, and tables.

A digital gray-level display device provided optional displays which gave a visual "trace" of the recognition programs. This feature was not required in the production system.

Translation and rotation tables with stepping motor drives under computer control were used to demonstrate the alignment process. In the production application the chip assembly itself is not moved, rather, the electrical test probe mechanism is translated and rotated into the proper position.

While a regular "pink" microscope light provides adequate illumination of the part, the final system was equipped with an infrared illumination source consisting of several LED's. This configuration has a longer operating life and produces high contrast images.

Focusing an optional standard TV camera onto the assembly (as shown in Fig. 20) enables people to see the small part being manipulated into position by viewing it on a TV monitor.

V. SYSTEM PERFORMANCE CHARACTERISTICS

A. Accuracy of Recognition

The system recognizes the position of each of the four corners of the chip with a maximum error of $\pm 1/2$ pixel. In a field of view equal to twice the width of the chip ($2 \times 5.26 \text{ mm} = 10.52 \text{ mm}$), and a spatial resolution of 50×50 pixels, this corresponds to $\pm 1/2 \text{ pixel} \times 10.52 \text{ mm}/50 \text{ pixels} = \pm 0.105 \text{ mm}$. Thus $\pm 0.105 \text{ mm}$ also represents the maximum positional accuracy in the recognition of any feature in the interior of the chip. This positional accuracy exceeded the production requirement.

The maximum error in rotation or orientation determination is defined by an error vector (corresponding to, for example, the top edge of the chip) whose horizontal component is the chip width (25 pixels) and whose vertical component is the relative positional error (in the vertical direction) of the upper left and right corners of the chip. This error is $\pm 1/2$ pixel since translation errors are not cumulative due to the topology of the model. Thus rotation

error is the arctangent of $\pm 1/2$ pixel/25 pixels, or ± 1.15 degrees. Rotational accuracy of ± 1.15 degrees exceeded the required production accuracy of ± 3.5 degrees.

B. Reliability

Three sample sets of Darlington assemblies were provided to test the reliability of the pilot system.

The first set consisted of 270 nondefective units, all of which were properly recognized and manipulated into a reference position within the time and accuracy requirements.

The second set consisted of 33 defective assemblies in which the Darlington chip was either off the edge of the heat sink, too close to the weld cup, or rotated more than ± 30 degrees. The system was able to reject all of these defective units.

The third set consisted of 39 defective assemblies in which the Darlington chip was either missing, broken, cracked, or partial. Such units are automatically rejected by the electrical test. An effort was made, however, to visually reject these units by detecting nonuniform contrast at the sides and corners of the chip. The system was able to reject all (16) of these units for which the defect was visible to the human eye in the digitized image.

The costs required to achieve the above performance were maintained within the limits predicted by Horn [17] for such a system.

VI. STATE OF THE ART

At the time of writing (late 1975) Hitachi Central Research Laboratories in Japan had just announced [1], [9], [15], [20], [21] the development of a production (partially hardwired) machine which performs the function of automatically aligning transistor circuit chips for wire bonding. This machine is the first true production "robot" extensively employing visual image processing functions. This system appears to be very similar in approach and objectives to the system described in this correspondence; however, it appears that their application was amenable to "binary" image processing, thus simplifying the vision task considerably. In addition, the Hitachi system evidently does not perform inspection tasks.

At the time of revision of this correspondence (mid 1977) commercially available "chip alignment" systems had become available. Based on image dissector technology, however, their cost effectiveness and durability have yet to be established. IC chip manufacture indeed appears to be a natural first application for computer vision technology, since it is a highly automated, computer oriented, aggressive industry.

Other recent articles and research papers [10], [11], [13], [14], [17], [18], and [22] have also focused on electronic component manufacture as a fertile domain for computer vision technology.

ACKNOWLEDGMENT

The author is indebted to L. Rossol for many useful discussions during the course of this work, for suggesting the method for determining chip orientation, and for directing this project. The interest and encouragement of G. G. Dodd is deeply appreciated. The programming assistance of M. R. Ward, A. L. Martin, and W. A. Perkins is also appreciated. E. M. Kavetsky and R. Dewar of General Motors Manufacturing Development Staff produced the production version of SIGHT-I from the laboratory pilot system. G. Voorhis and others at Delco Electronics Division of General Motors were especially helpful in bringing this project to its successful completion.

REFERENCES

- [1] "Images processed to control transistor assembly machine," *Automation*, p. 8, July 1975.
- [2] M. L. Baird, "A paradigm for semantic picture recognition," Ph.D. dissertation, Georgia Inst. of Technology, Atlanta, June 1973 (available from University Microfilms, Ann Arbor, MI, 48106).
- [3] M. L. Baird and M. D. Kelly, "A paradigm for semantic picture recognition," *Pattern Recognition*, vol. 6, pp. 61-74, 1974.
- [4] —, "Recognizing objects by rules of inference on sequentially thresholded gray-level pictures," *Comput. Graphics Image Processing*, vol. 3, pp. 1-22, Mar. 1974.
- [5] M. L. Baird, "Relational models for object location," *ACM SIGART*, vol. 55, Dec. 1975.
- [6] M. L. Baird, J. T. Olszyn, W. A. Perkins, and L. Rossol, "The GM research laboratories' machine perception project," *ACM SIGART*, vol. 55, Dec. 1975.
- [7] D. I. Barnea and H. F. Silverman, "A class of algorithms for fast digital image registration," *IEEE Trans. Comput.*, vol. C-21, pp. 179-186, Feb. 1972.
- [8] Y. P. Chien and K. S. Fu, "Recognition of x-ray picture patterns," *IEEE Trans. Syst., Man, Cybern.*, vol. SMC-4, pp. 145-156, Mar. 1974.
- [9] "Pattern recognition capability lets robot operate unattended," *Comput. Design*, p. 54, Nov. 1975.
- [10] M. G. Dreyfus, "Visual robots," *Industrial Robot*, pp. 260-264, Dec. 1974.
- [11] M. Ejiri, T. Uno, M. Mese, and S. Ikeda, "A process for detecting defects in complicated patterns," *Comput. Graphics Image Processing*, vol. 2, pp. 326-339, 1973.
- [12] M. A. Fischler and R. A. Elschlager, "The representation and matching of pictorial structures," *IEEE Trans. Comput.*, vol. C-22, pp. 67-92, Jan. 1973.
- [13] J. A. G. Hale and P. Saraga, "Control of a PCB drilling machine by visual feedback," in *Proc. Fourth Int. Joint Conf. on Artificial Intelligence*, pp. 775-781, 1975.
- [14] C. A. Harlow, S. E. Henderson, D. A. Rayfield, R. J. Johnston, and S. J. Dwyer, III, "Automatic inspection of electronic assemblies," *IEEE Trans. Comput.*, vol. C-8, pp. 36-45, Apr. 1975.
- [15] "Fully automated transistor assembly system," *CRL NEWS*, Central Research Labs., Hitachi, Ltd., Japan, July 25, 1975.
- [16] S. W. Holland, "A programmable computer vision system based on spatial relationships," Digital Systems Laboratory, Stanford Univ., Stanford, CA, Tech. Rep. 104, Dec. 4, 1975. (Also GM Research Publication 2078 available from the author.)
- [17] B. K. P. Horn, "Orienting silicon integrated circuit chips for lead bonding," *Comput. Graphics Image Processing*, vol. 4, pp. 294-303, Sept. 1975.
- [18] J. F. Jarvis, "Automatic visual inspection of Western Electric series 700 connectors," in *Proc. IEEE Comput. Soc. Conf. on Pattern Recognition and Image Processing*, pp. 153-159, June 1977.
- [19] R. K. Jurgen, "Ignition systems go solid state," *IEEE Spectrum*, pp. 49-51, Sept. 1975.
- [20] S. Kashioka, M. Ejiri, and Y. Sakamoto, "A transistor wire-bonding system utilizing multiple local pattern matching techniques," *IEEE Trans. Syst., Man, Cybern.*, vol. SMC-6, pp. 562-570, Aug. 1976.
- [21] S. Kashioka, M. Ejiri, and Y. Sakamoto, "A transistor assembly system utilizing time shared visual image processing techniques," *Elec. Eng. in Japan*, vol. 96, pp. 118-124, 1976.
- [22] E. S. McVey, G. L. Jarvis, II, and E. A. Parrish, "An example of advanced automation: printed circuit board drilling," *IEEE Trans. Ind. Electron. Contr. Instrum.*, vol. IECl-22, pp. 10-15.
- [23] J. T. Olszyn, L. Rossol, R. Dewar, and N. R. Lewis, "An application of computer vision to a simulated assembly task," in *Proc. First Int. Joint Conf. on Pattern Recognition*, pp. 505-513, 1973.
- [24] "Research in computer vision systems," *SEARCH*, vol. 8, Nov.-Dec. 1973. (GM Research Publication available from the author).
- [25] H. Yoda, J. Motoike, and M. Ejiri, "Direction coding method and its application to scene analysis," in *Proc. Fourth Int. Joint Conf. on Artificial Intelligence*, pp. 620-627, 1975.

On the Sequential Approach to Medial Line Transformation

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Abstract—An iterative procedure to obtain the medial line of a binary digital figure is presented. At every iteration step, local sequential operations are employed to delete the contour elements which are neither end points nor are necessary to preserve the order of

Manuscript received June 7, 1977; revised September 14, 1977.

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