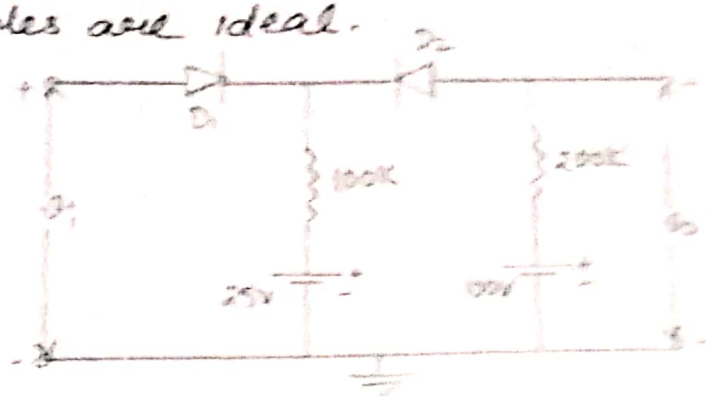
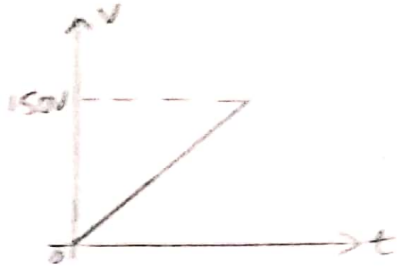
PART-B

Q11(a) Sketch the output response for following clipper circuit when input is linearly varying from 0 to 150V. Assume diodes are ideal.



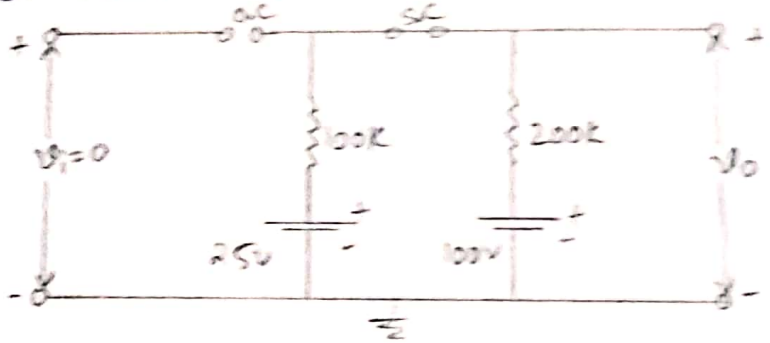
Sol Given Input is linearly varying from 0 to 150V then



i) $V_i = 0V$

D_1 - R.B, off / open ckt

D_2 - F.B, on / short ckt



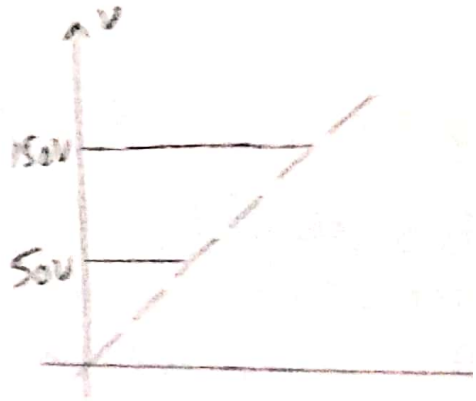
$$V_o = \frac{25 \times 200}{200+100} + 100 \times \frac{100}{200+100}$$

$$V_o = 50V$$

ii) $V_i < 50V$

D_1 - R.B, D_2 - F.B

Hence: $V_o = 50V$.



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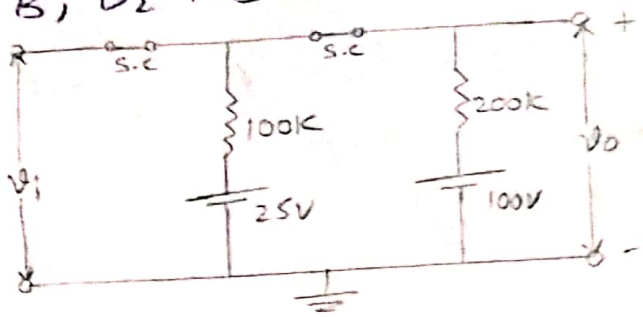
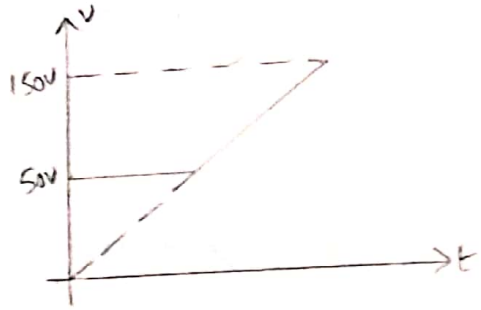
iii) $50 < v_i < 100$

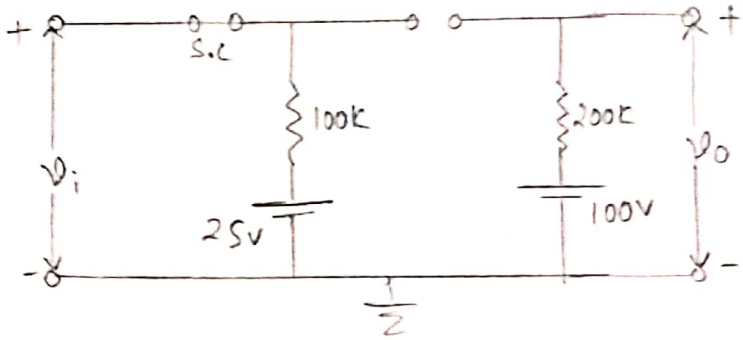
D_1 - F.B, D_2 - F.B



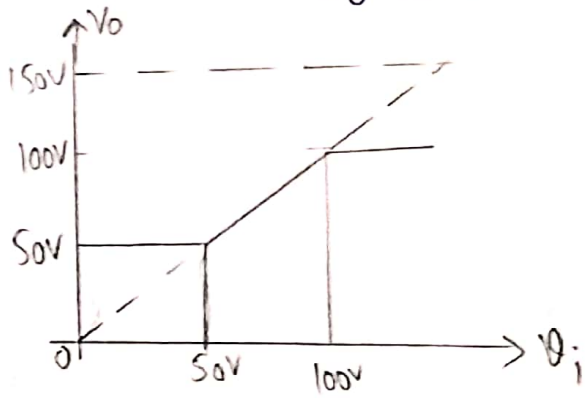


iv) $v_i > 100V$,

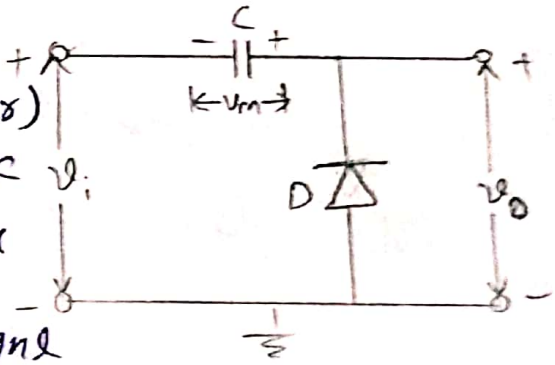
D_1 - F.B, D_2 - R.B



$v_o = 100V$



b) Explain positive clamper



A: Positive clamper (-ve peak clamper)

This ckt clamps the -ve peak of a signal the -ve peak clamper introduces a +ve DC value. i/p sgnl

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$v_i = v_m \sin \omega t$

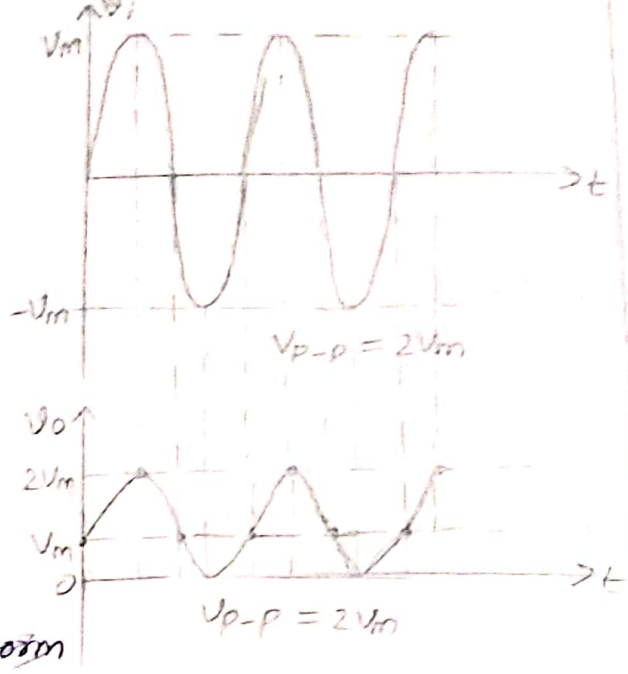
when v_i goes -ve the diode gets forward bias & conducts. capacitors changes to v_m

$$v_0 = v_i - (-v_m) = v_i + v_m$$

$$v_i = 0 \Rightarrow v_0 = 0 + v_m = v_m$$

$$v_i = v_m \Rightarrow v_0 = v_m + v_m = 2v_m$$

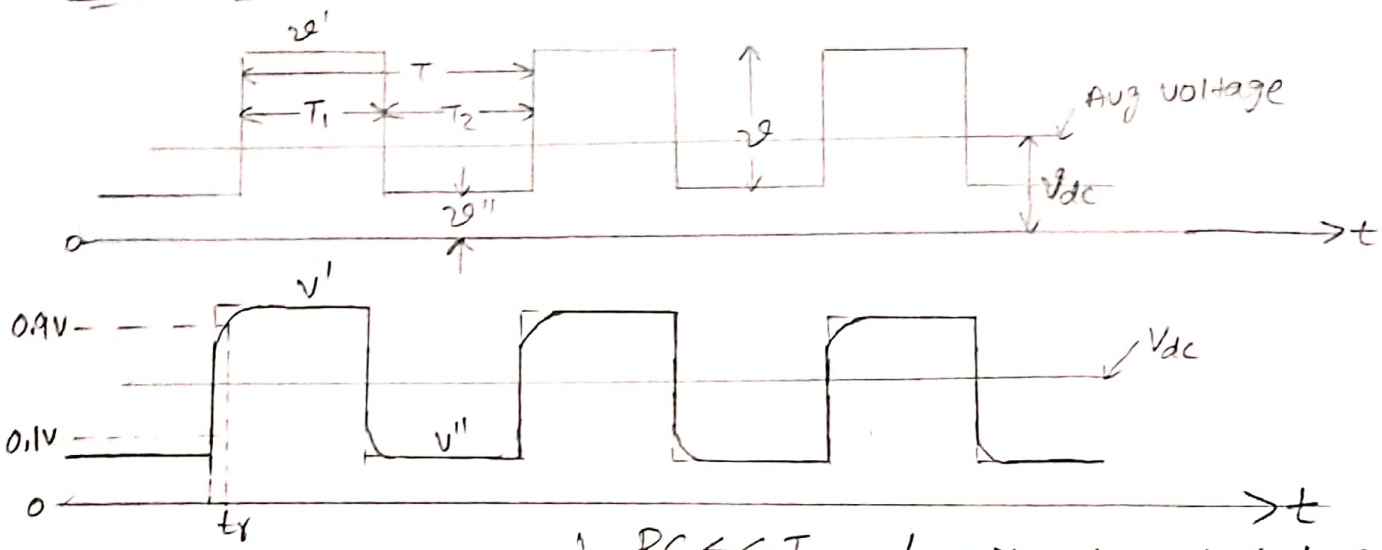
$$v_i = -v_m \Rightarrow v_0 = -v_m + v_m = 0$$



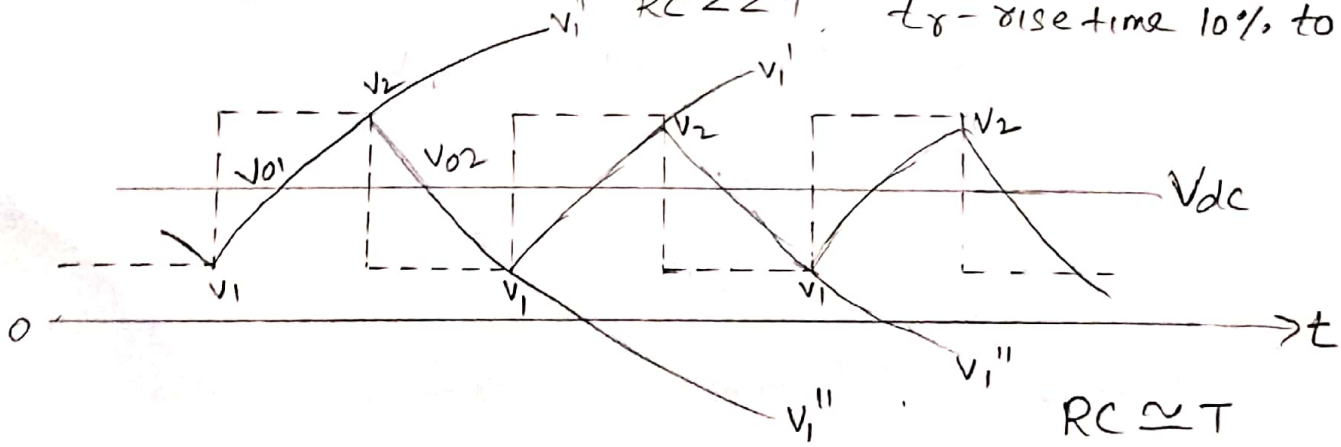
~~Effect of R_f & R_s on output waveform~~

Q12) ⓐ Explain the response of low pass RC circuit for square wave input.

A: Response of Low pass RC circuit for square wave input.



$RC << T$. t_r - rise time 10% to 90%.



$RC \simeq T$

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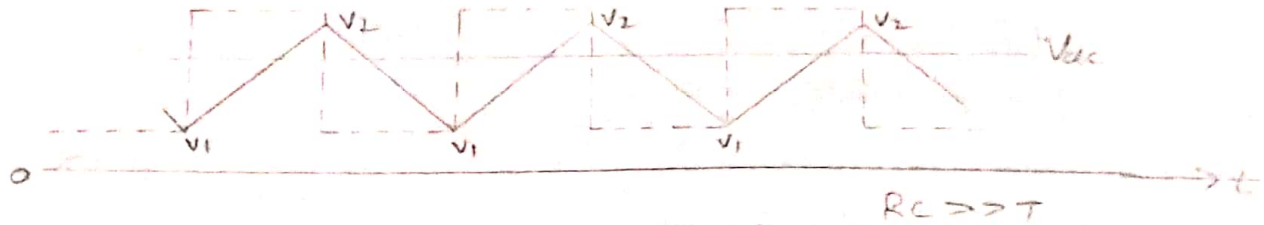

consider a periodic waveform whose instantaneous value is constant at v' w.r.t ground for time T_1 & then changes abruptly (suddenly) to v'' for a time T_2

A resonable reproduction of the input is obtained if $t_r << t_p$

If V_1 is the initial value of the o/p voltage

$$v_0 = V_F + (v_i - V_F)e^{-t/\tau} \qquad (\because \tau = RC)$$

let $v_i = V_1$ & $V_F = v_1'$, $v_0 = v_{01}$, $\tau = RC$

$$v_{01} = v_1' + (v_1 - v_1')e^{-t/RC} \rightarrow (1)$$

$$v_{02} = v_1'' + (v_2 - v_1'')e^{-(t-T_1)/RC} \rightarrow (2)$$

$$\left.\begin{matrix} v_F = v_1'' \\ v_i = v_2 \end{matrix}\right\} \text{ at } \left.\begin{matrix} t = T_1, \ v_{01} = v_2 \\ t = T_1 + T_2, \ v_{02} = V_1 \end{matrix}\right\} - (3)$$

consider a symmentrical square wave with zero Avgerage value. So, that $T_1 = T_2 = T/2$ & $v' = -v'' = \frac{V}{2}$

$$\begin{bmatrix} V_1' = v' \\ V_1'' = v'' \end{bmatrix}$$

$$V_1 = -V_2$$

$$V_1 = -V_2$$

$$v_{01} = v' + (V_1 - V')e^{-t/RC} \rightarrow (2) \qquad t = T/2$$

$$(2) \Rightarrow v_2 = \frac{V}{2} + \left(V_1 - \frac{V}{2}\right)e^{-\frac{T}{2RC}}$$

$$\because V_1 = -V_2$$

$$V_2 = \frac{V}{2} + \left(-V_2 - \frac{V}{2}\right)e^{-\frac{T}{2RC}}$$

$$V_2 = \frac{V}{2}\left[1 - e^{-\frac{T}{2RC}}\right] - V_2 e^{-\frac{T}{2RC}}$$

$$V_2\left(1 + e^{-\frac{T}{2RC}}\right) = \frac{V}{2}\left(1 - e^{-\frac{T}{2RC}}\right)$$

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$$V_2 = \frac{V}{2}\,\frac{(1-e^{-T/2RC})}{(1+e^{-T/2RC})}$$

multiplying numerator & denominator with $e^{T/2RC}$

$$V_2 = \frac{V}{2}\,\frac{(e^{T/2RC}-1)}{e^{T/2RC}+1} \qquad \text{let } x = \frac{T}{4RC}$$

$$V_2 = \frac{V}{2}\,\frac{(e^{2x}-1)}{e^{2x}+1} = \frac{V}{2}\,\frac{(e^{x}-e^{-x})}{e^{x}+e^{-x}}$$

$$V_2 = \frac{V}{2}\,\frac{(e^{x}-e^{-x})/2}{(e^{x}+e^{-x})/2}$$

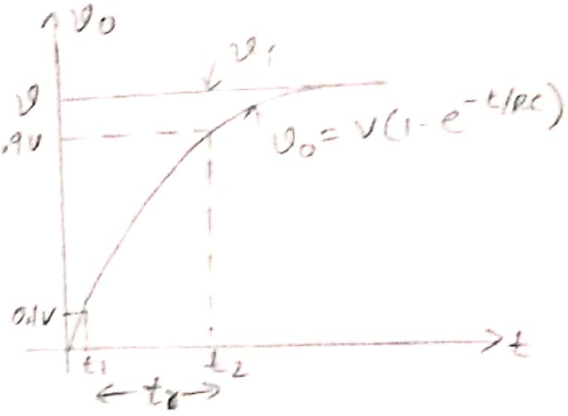
$$V_2 = \frac{V}{2}\,\frac{\sinh x}{\cosh x}$$

$$V_2 = \frac{V}{2}\tanh x$$

12(b) Obtain the expression for Rise time.

A: Rise time (t_r):

The time required for the voltage to rise time 10% to 90% of the final steady value is termed as rise time it is denoted as t_r



$$\boxed{t_r = 2.2RC}$$

Proof: Put $t = t_1$, $V_o = 0.1V$

$$v_o = v(1-e^{-t_1/RC})$$

$$0.1V = V(1-e^{-t_1/RC})$$

$$e^{-t_1/RC} = 1-0.1 = 0.9$$

$$-t_1/RC = \log_e(0.9)$$

$$t_1 = -RC\log_e(0.9) \quad \text{— (1)}$$

at $t = t_2$ $v_o = 0.9V$

$$v_o = V(1-e^{-t_2/RC})$$

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$$0.9V = V(1 - e^{-t_2/RC})$$

$$e^{-t_2/RC} = 1 - 0.9 = 0.1$$

$$-t_2/RC = \log_e(0.1)$$

$$t_2 = -RC \log_e(0.1) \rightarrow (2)$$

Rise time $t_r = t_2 - t_1$

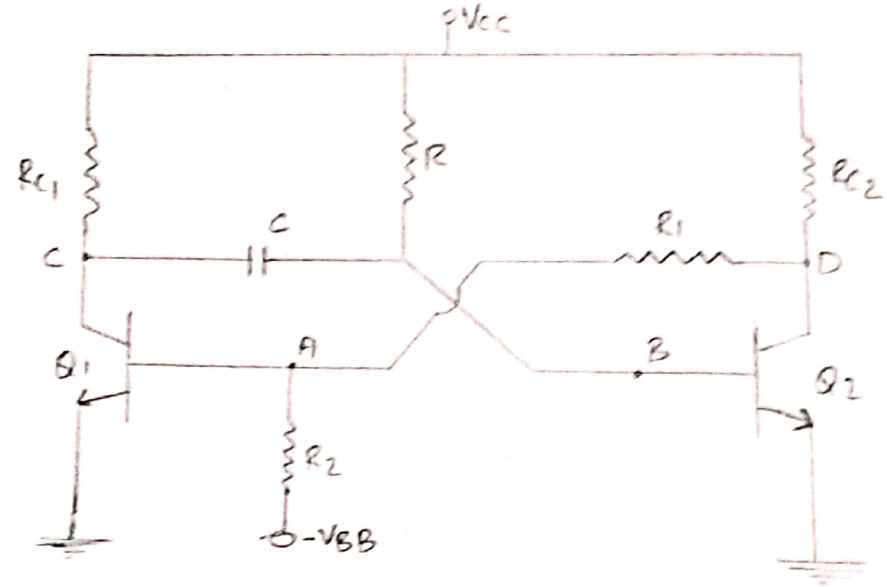
$$t_r = -RC[\log_e(0.1) + \log_e(0.9)]$$

$$t_r = 2.2RC$$

Hence the rise time is 2.2 times of the time constant.

Q13) (a) Draw the circuit of monostable multivibrator & derive the expression for pulse width.

A:



Other names of monostable mv

- one shot, univibrator, pulse generator, Gating ckt, Delay ckt.

Expression for pulse width or Delay time (T)

Initial value of V_B at $t=0$

$$V_{in} = -V_{CC}$$

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- As the Capacitor discharges V_B rises exponentially & attain a value $+V_{cc}$ but at $t=T$ Q_2 becomes ON
- V_B takes the value $V_B = V_\gamma$, the cut-in-vol of Q_2 which is very small taking it as zero.

Final value of V_B $(t=\infty)$

$$V_F = +V_{cc} \;\&$$

at $t=T$, $V_B = V_\gamma = 0$

$$V_B = V_F - (V_F - V_i)e^{-t/RC}$$

$$V_B = V_{cc} - [V_{cc} - (-V_{cc})]\, e^{-t/RC}$$

at $t=T$, $V_B = V_\gamma = 0$

$$0 = V_{cc} - 2V_{cc}\, e^{-T/RC}$$

$$e^{-T/RC} = 2$$

$$T/RC = \log_e(2) = 0.69$$

$$\boxed{T = 0.69RC}$$ pulse width

If I_{CBO} taken into consideration

$$T = RC\log_e\left[\frac{2V_{cc} + I_{CBO}R}{V_{cc} + I_{CBO}R}\right]$$

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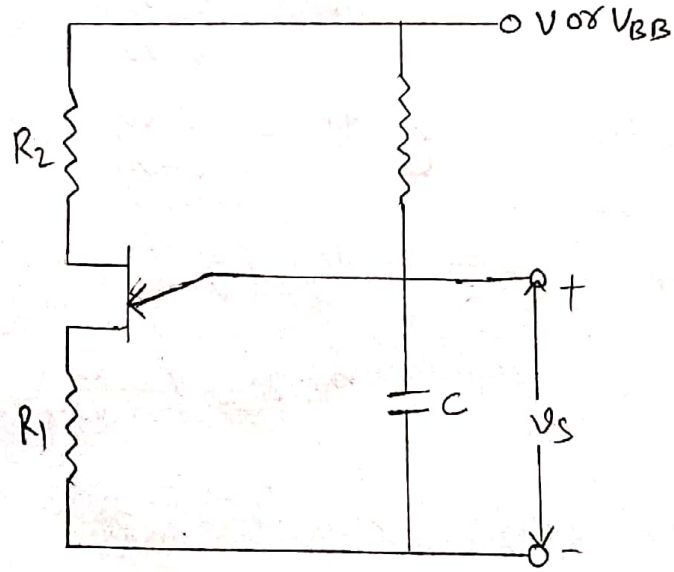
13. (b) Design & analyse sweep circuit using UJT.

A: Sweep circuit using UJT:-



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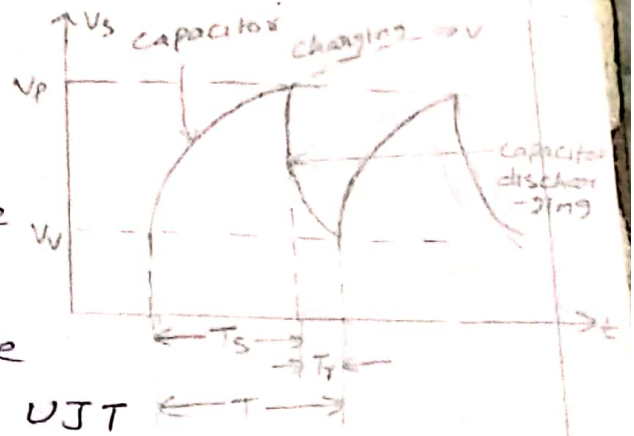
Working Principle:



UJT is off as long as $V_v < V_P$ when UJT is off capacitor charges through the resistance R form the supply voltage V. V_s is equal capactor voltage when V_s rises to the value V_P UJT ready conducts. when UJT ON capacitor discharges & its voltage falls. when the voltage falls vary Pt V_B. UJT OFF & capacitor charges again to V_P. this cycle of charging & discharging of the capacitor repeats a saw tooth waveform is generated.

Expression for frequency:

V_{in} is the initial value, V_F is the final value

$V_{in} = V_V$, $V_F = V$

when UJT off $\rightarrow V_S = V_F - (V_F - V_{in})e^{-t/RC}$

$$V_S = V - (V - V_V)e^{t/RC}$$

at $t = T_S$, $V_S = V_P$

$$V_P = V - (V - V_V)e^{-T_S/RC}$$

$$(V - V_V)e^{-T_S/RC} = V - V_P$$

$$e^{-T_S/RC} = \frac{V - V_P}{V - V_V}$$

$$e^{T_S/RC} = \frac{V - V_V}{V - V_P}$$

$$\frac{T_S}{RC} = \log_e\left(\frac{V - V_V}{V - V_P}\right)$$

$$T_S = RC \log_e\left(\frac{V - V_V}{V - V_P}\right)$$

$$f = \frac{1}{T}, \quad T = T_S + T_r \quad (T_r << T_S)$$

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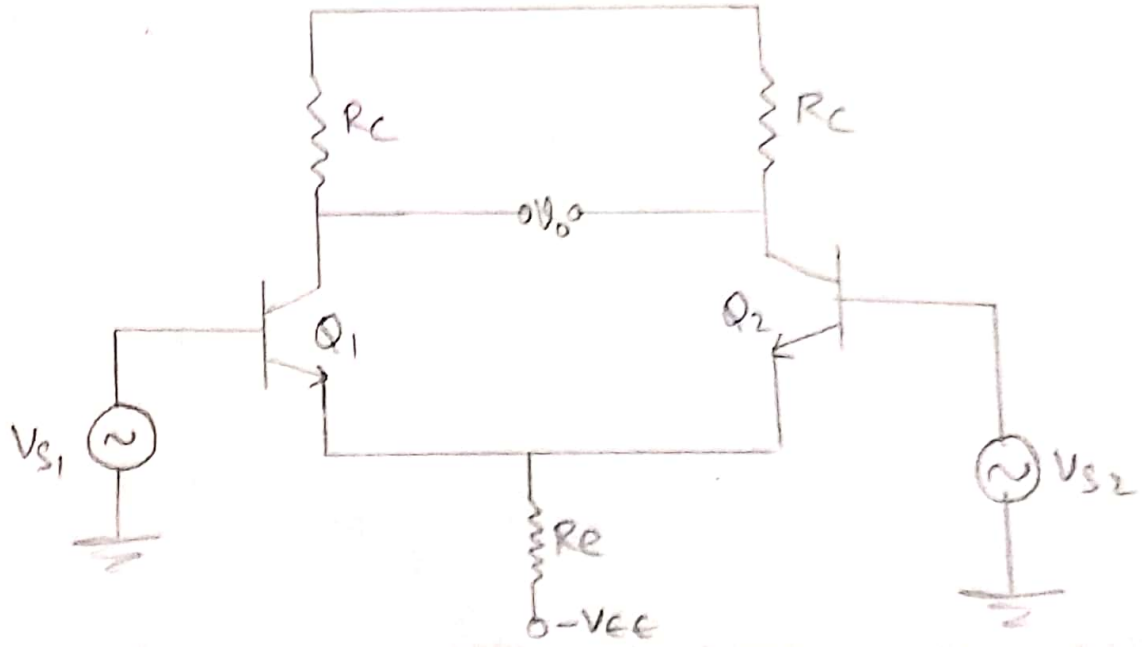
Q14) a) Explain DC & AC analysis of dual input & balance output differential amplifier.

A: AC analysis of differential amplifiers

Dual input balanced output:



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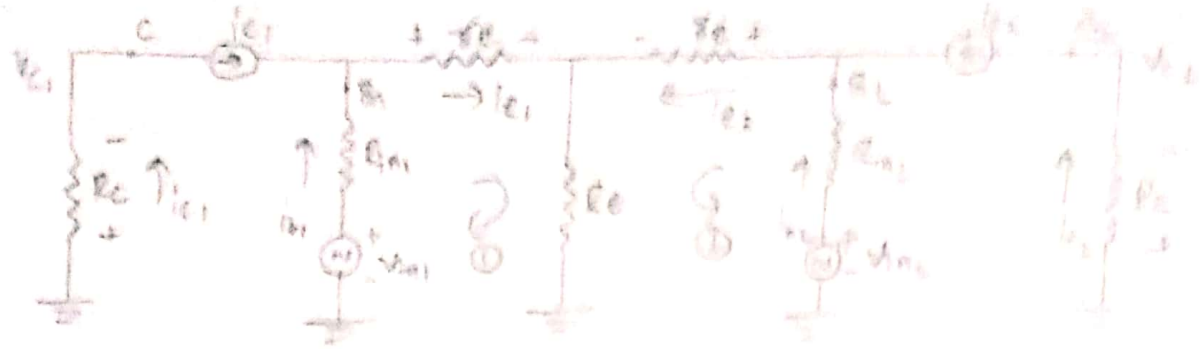

Voltage Gain :

KVL for loop ① & loop ②

$$V_{in_1} - R_{in_1} i_{b_1} - r_e i_{e_1} - R_e (i_{e_1} + i_{e_2}) = 0 \rightarrow ①$$

$$V_{in_2} - R_{in_2} i_{b_2} - r_e i_{e_2} - R_e (i_{e_1} + i_{e_2}) = 0 \rightarrow ②$$

Since $i_{b_1} = \frac{i_{e_1}}{\beta_{ac}}$ & $i_{b_2} = \frac{i_{e_2}}{\beta_{ac}}$

$$① \Rightarrow V_{in_1} - R_{in_1} \frac{i_{e_1}}{\beta_{ac}} - r_e i_{e_1} - R_e (i_{e_1} + i_{e_2}) = 0 \rightarrow ③$$

$$② \Rightarrow V_{in_2} - R_{in_2} \frac{i_{e_2}}{\beta_{ac}} - r_e i_{e_2} - R_e (i_{e_1} + i_{e_2}) = 0 \rightarrow ④$$

$\frac{R_{in_1}}{\beta_{ac}}$ & $\frac{R_{in_2}}{\beta_{ac}}$ are very small, so neglected

$$③ \Rightarrow i_{e_1}(r_e + R_e) + R_e i_{e_2} = V_{in_1} \rightarrow ⑤$$

$$④ \Rightarrow R_e (i_{e_1}) + (r_e + R_e) i_{e_2} = V_{in_1} \rightarrow ⑥$$

$$i_{e_1} = \frac{\begin{vmatrix} V_{in_1} & R_e \\ V_{in_2} & R_e + r_e \end{vmatrix}}{\begin{vmatrix} r_e + R_e & R_e \\ R_e & r_e + R_e \end{vmatrix}} = \frac{(r_e + R_e) V_{in_1} - R_e (V_{in_1})}{(r_e + R_e)^2 - (R_e)^2}$$

$$i_{e_2} = \frac{\begin{vmatrix} r_e + R_e & V_{in_1} \\ R_e & V_{in_2} \end{vmatrix}}{\begin{vmatrix} r_e + R_e & R_e \\ R_e & r_e + R_e \end{vmatrix}} = \frac{(r_e + R_e) V_{in_2} - R_e (V_{in_1})}{(r_e + R_e)^2 - (R_e)^2}$$

output voltage $V_o = V_{c_2} - V_{c_1} = -i_{c_2} R_c - (-i_{c_1} R_c)$

$$= -R_c (i_{c_2} - i_{c_1})$$

$$V_o = R_c (i_{e_1} - i_{e_2}) \quad (i_e \cong i_c)$$

$$V_o = \frac{R_c}{r_e} (V_{in_1} - V_{in_2})$$

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$$\frac{V_o}{V_{in_1} - V_{in_2}} = \frac{V_o}{V_{id}} \Rightarrow A_v = \frac{R_c}{r_e}$$

Input resistance

$$R_{in_1} = \frac{V_{in1}}{i_{b1}} \Big|_{V_{in_2}=0}$$

$$R_{in_1} = \frac{V_{in1}}{i_{e1}/\beta_{ac}} \Big|_{V_{in_2}=0} \Rightarrow R_{in_1} = \frac{V_{in_1}\beta_{ac}}{i_{e_1}} \Big|_{V_{in_2}=0}$$

$$R_{in_1} = \frac{V_{in_1}\beta_{ac}}{\frac{(r_e + R_e)V_{in_1} - R_e(0)}{(r_e+R_e)^2 - (R_e)^2}}$$

$$R_{in_1} = \frac{V_{in}\,\beta_{ac}\,(r_e^2 + 2R_e r_e)}{(r_e + R_e)V_{in_1}}$$

$$R_{in_1} = \frac{\beta_{ac} r_e (r_e + 2R_e)}{(r_e + R_e)}$$

$$(r_e + 2R_e) \simeq 2R_e \qquad R_e >> r_e$$

$$(r_e + R_e) \simeq R_e$$

$$R_{in} = \frac{\beta_{ac}\, r_e (2R_e)}{R_e} = 2\beta_{ac} r_e$$

$$R_{in} = \frac{V_{in2}}{i_{b2}} \Big|_{V_{in_1}=0} = 2\beta_{ac} r_e$$

Output resistance

It is defined as the equalent Resistance that would be measured at either o/p terminal w.r.t ground. $R_{c_1} = R_{c_2} = R_c$

DC analysis of differential amplifiers:

It explains the concept of plotting the operating point (Q) on a dc load line plotted b/w V_{CE} & I_C

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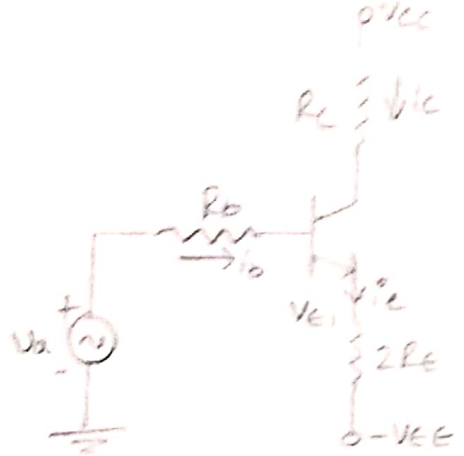
Q-pt for common mode (Q-operating pt) the diff i/p vol $V_{id} = 0$ & two input signals are equal $v_{b1} = v_{b2}$.

but $v_{ic} = \frac{v_{b1} + v_{b2}}{2} = \frac{2v_{b1}}{2}$

$$v_{ic} = v_{b1} = v_a \text{ (say)}$$

With the above assumption the diff amp is simplified with a sign. single transistor.

In common mode to maintain constant current in emitter terminal R_E is replaced by $2R_E$



Apply KVL at emitter terminal

$$V_{E1} - i_e R_E + V_{EE} = 0$$

$$i_e = \frac{V_{E1} + V_{EE}}{R_E}$$

$$i_{e1} + i_{e2} = \frac{V_{E1} + V_{EE}}{R_E}$$

But $i_{e1} = i_{e2} = i_e/2$

equivalent ckt has $2R_E$ in its emitter terminal apply KVL at Collector loop

$$V_{CC} - i_c R_C - V_{CE} - i_e(2R_E) + V_{EE} = 0$$

If Q_1-on $\Rightarrow i_e = i_c$

$$V_{CC} - i_c(R_C + 2R_E) - V_{CE} + V_{EE} = 0$$

$$V_{CC} - V_{CE} + V_{EE} = i_c(R_C + 2R_E) \rightarrow (I)$$

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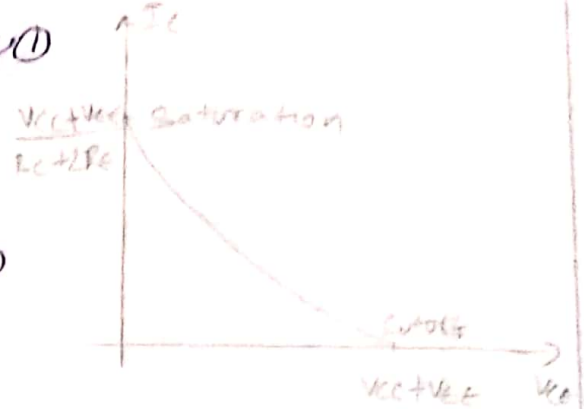
from (I) $\Rightarrow i_C = \dfrac{V_{CC} - V_{CE} + V_{EE}}{R_C + 2R_E} \rightarrow (1)$

from (I) $\Rightarrow V_{CE} = V_{CC} + V_{EE} - i_C(R_C + 2R_E) \rightarrow (2)$

To get the extrem pts of load line i.e., V_{CE} on axis (cut-off region) & on i_C axis (saturation region)

For Saturation Region $V_{CE} = 0$ in equ (1)

$$i_C = \frac{V_{CC} + V_{EE}}{R_C + 2R_E}$$



For cut off region $I_C = 0$ in equ (2)

$$V_{CE} = V_{CC} + V_{EE}$$

To mark the Q operating pt

Apply the KVL to the base emitter loop by sitting $V_a = 0$

$$0 - i_b R_b - V_{BE} - i_e(2R_E) + V_{EE} = 0 \rightarrow (3)$$

$$i_e = i_b + i_c$$

$$i_e = i_b + \beta i_b = (1+\beta) i_b$$

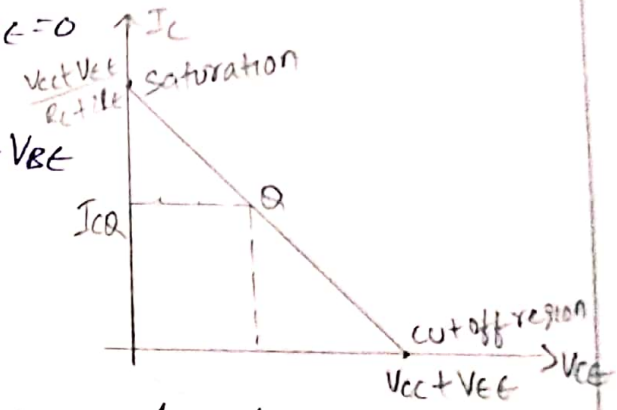
$$i_b = \frac{i_e}{1+\beta} \simeq \frac{i_c}{1+\beta}$$

Substituting i_b value in equ (3)

$$0 - \frac{i_c R_b}{1+\beta} - V_{BE} - i_c(2R_E) + V_{EE} = 0$$

$$i_c\left(\frac{R_b}{1+\beta} + 2R_E\right) = V_{EE} - V_{BE}$$

$$i_{CQ} = \frac{V_{EE} - 0.7}{\frac{R_b}{1+\beta} + 2R_E}$$



The Q_{max} & Q_{min} varies from $V_{a(max)}$ to $V_{a(min)}$ with $V_{id} = 0$

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14(b) Define the following OPAMP parameters i) input bias current ii) input offset current iii) ~~output~~ Input Offset ~~Voltage~~ Current iv) output offset voltage.

A: i) Input bias Current:

The input bias current is the DC current required by the inputs of the amplifier to properly operate the first stage. By definition, the input bias current is the average of bothe input current.

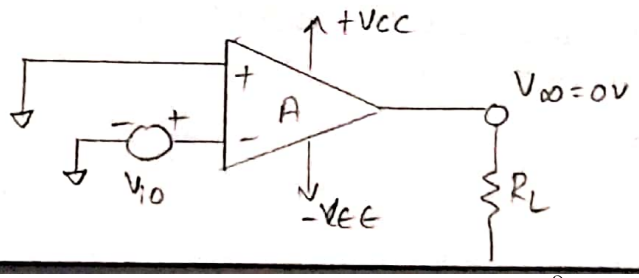
$$I_B = \frac{I_B^+ + I_B^-}{2}$$

ii) Input offset current:

The difference b/w the bias current at the i/p terminals of the op-amp is called as i/p offset current. The i/p terminals conduct a small value of dc current to bias the i/p transistors. Since the i/p transistors cannot be made identical, there exists a difference in bias currents.

iii) Input offset voltage:

Input offset vol V_{io} is the differential i/p vol that exists b/w two i/p terminals of an op-amp without any external i/p's applied. In other words, it is the amount of the i/p vol that should be applied b/w two i/p terminals in order to force the o/p vol to zero. Since this vol could be +ve or -ve its absolute value is listed on this data sheet. for 741C, the maximum value is 6mV.



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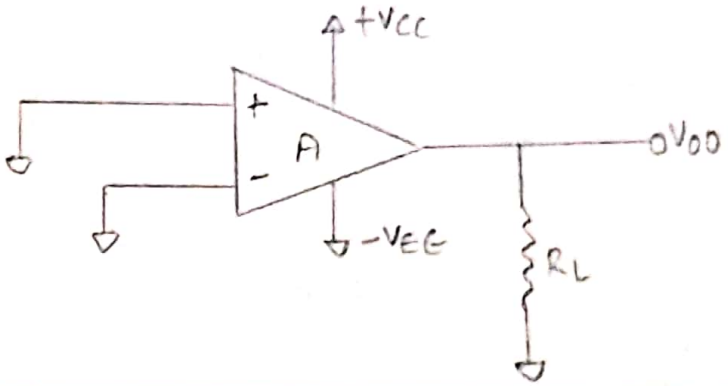
iv) output offset voltage.

- The o/p offset vol V_{oo} is caused by mismatching b/w two i/p terminals. Even though all the components are integrated on the same chip, it is not possible to have two transistors in the i/p differential amp stage with exactly the same characteristics.
- This means that the collector current in these two transistors are not equal which causes a differtial o/p vol from the first stage.
- The o/p of first stage is amplified by following stages & possibly aggravated by more mismatching in them. Thus o/p vol caused by mismatching b/w two i/p terminals is the o/p offset V_{oo}.
- The o/p offset vol is a dc voltage; it may be +ve or -ve in polarity depending on whether the potential depending on whether the potential difference b/w two i/p terminals is +ve or -ve



Q15) (a) Draw & explain the operation of second order low pass active filter & derive the expression for its cut off frequency.

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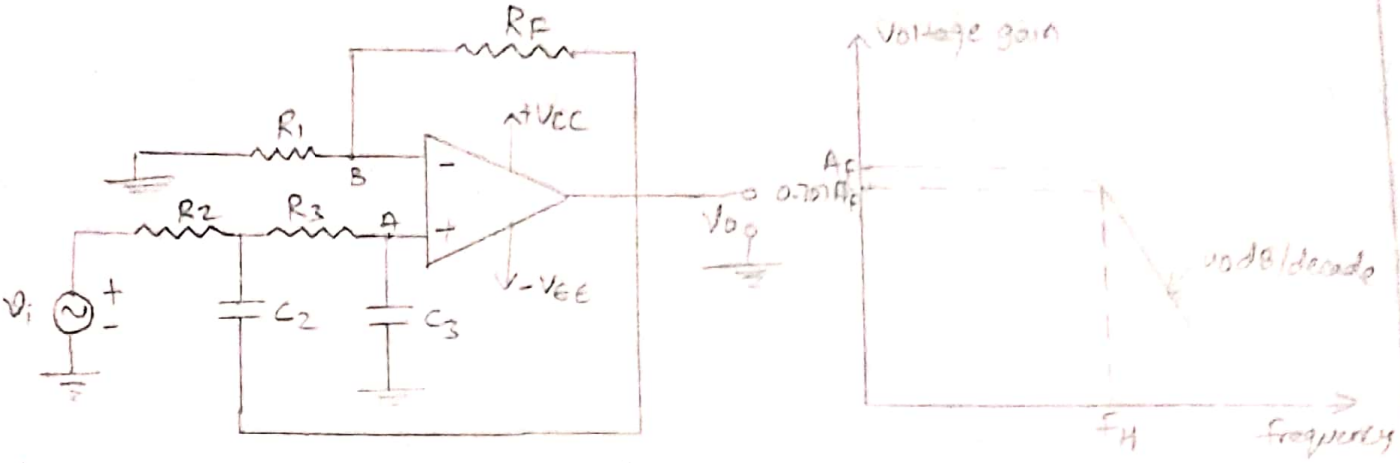
Second order low pass Butterworth Active filter:

A stop band response having a 40-dB/decade roll off is obtained with the second order LPF. A first order LPF can be converted into a second order type simply by using an additional RC Network.



the gain of the second order filter is set by R_1 & R_F. while the high cut off frequency f_H is determined by R_2, C_2, R_3, C_3.

$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

the voltage gain of the second order filter in magnitude

as
$$\left|\frac{V_o}{V_i}\right| = \frac{A_F}{\sqrt{1+\left(\frac{f}{f_H}\right)^4}}$$

$A_F = 1 + \frac{R_F}{R_1}$ = passband gain of the filter

f = frequency of i/p sgnl

$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

Design of the Filter:

- The cut off freq f_H is suitably selected
- set $R_2 = R_3 = R$ & $C_2 = C_3 = C$, then $f_H = \frac{1}{2\pi\sqrt{R^2C^2}}$

  choose a value of $C \leq 1\mu F$
- calculate the value of R using $R = \frac{1}{2\pi f_H C}$

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Finally because of the equal resistor ($R_2 = R_3$). & capacitor [$C_2 = C_3$] values, $A_F = (1 + \frac{R_F}{R_1})$ of the second order LPF has to equal to 1.586.

$$1.586 = 1 + \frac{R_F}{R_1}$$

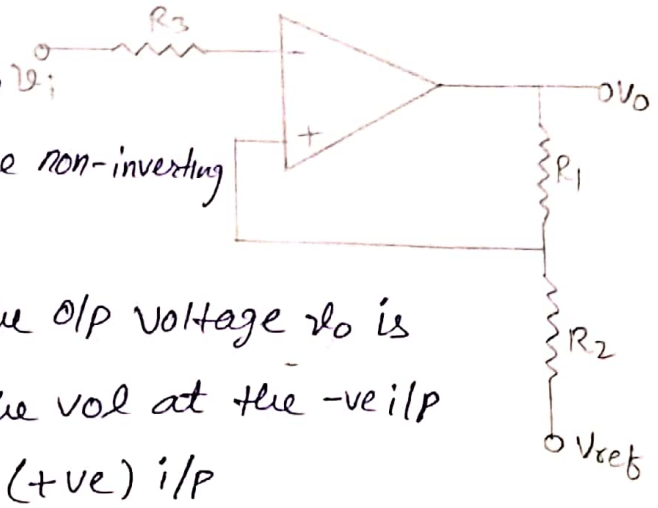
$$0.586 = \frac{R_F}{R_1} \Rightarrow R_F = 0.586 R_1$$

The gain is necessary to guarante active response choose $R_1 \leq 100 k\Omega$ & calculate R_F.

15(b). Explain the operation of Schmitt trigger using OPAMP.

A: Schmitt trigger using op-amp

Schmitt trigger is a +ve f/b comparator ckt. It is also called as a sine wave to a square wave generator



the i/p vol is applied to the inverting terminal of the op-amp & the f/b vol is applied to the non-inverting terminal of the op-amp.

When V_{in} is less than V_{ref}, the o/p voltage v_o is at $-V_{sat}$ ($\simeq -V_{EE}$) because the vol at the -ve i/p is higher than that at (+ve) i/p

When V_{in} is greater than V_{ref}, the +ve i/p becomes +ve w.r.t the -ve i/p. & v_o goes to $+V_{sat}$ ($\simeq +V_{CC}$)

thus v_o changes from one saturation level to another whenever $V_{in} \simeq V_{ref}$

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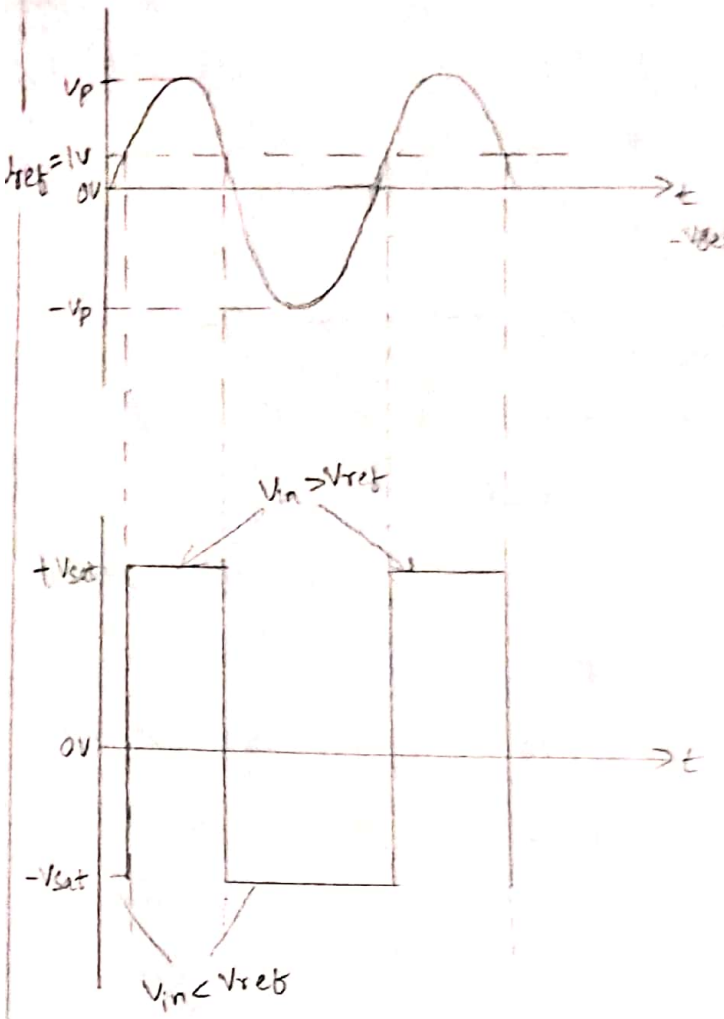
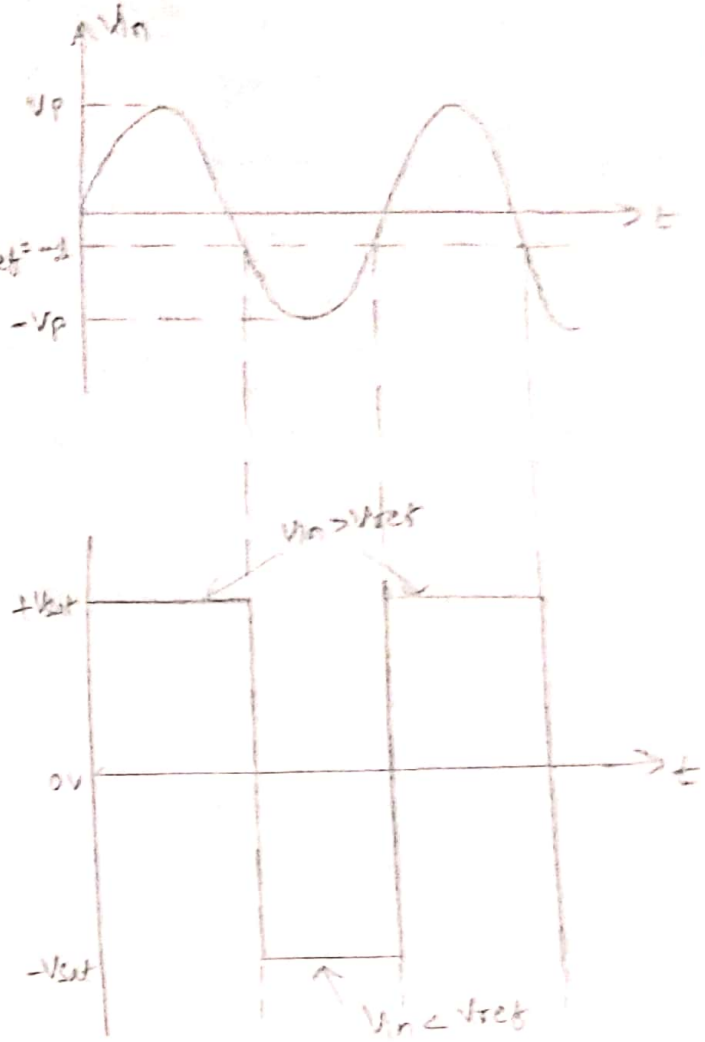


If Vref is positive



If Vref in negative

The i/p vol V_{in} trigger the o/p V_o every time it exceeds certain vol levels. these vol levels are called upper threshold vol (V_{UT}) & lower threshold vol (V_{LT})

the hysteresis width is the difference b/w these two threshold vol i.e., $V_{UT} - V_{LT}$

$$V_H = V_{UT} - V_{LT}$$

Suppose the o/p $V_o = +V_{sat}$ using superposition theorem

$$V_{UT} = \frac{V_{ref} \cdot R_1}{R_1 + R_2} + \frac{R_2 V_{sat}}{R_1 + R_2}$$

when the o/p $V_o = -V_{sat}$

$$V_{LT} = \frac{V_{ref} R_1}{R_1 + R_2} - \frac{R_2 V_{sat}}{R_1 + R_2}$$

$$V_H = V_{UT} - V_{LT}$$

$$V_H = 2 V_{sat} \frac{R_2}{R_1 + R_2}$$

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As long as V_{in} is less than UTP pt the o/p remains constant at $+V_{sat}$.

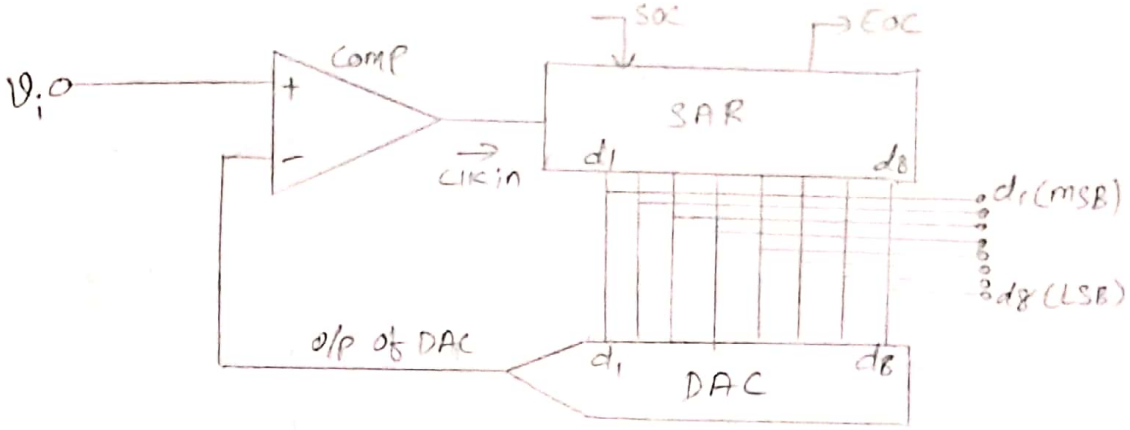
When V_{in} > than UTP pt, the o/p switches to $-V_{sat}$.

Q16) (a) Explain the working of successive approximation ckt type ADC ckt.

A: Successive approximation ADC ckt:

A successive approximation A to D convertor is based on a very efficient code searching strategy called binary search. The searching process is very fast, a n-bit conversion being completed in only n clock periods. The strategy consists in adjusting the i/p code of a DAC such that i/p o/p is within = ± ½ LSB of the analog i/p signal which is to be converted into equivalent digital signal.

It is a trial & error process & that particular code which comes nearest is the required ADC o/p.



The ckt uses a successive approximation register a DAC & a comparator.

The external ckt i/p sets the internal timing parameter. The SOC signal starts the process of conversion & the activated EOC signal announces the end of the conversion process

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Operation:

→ The SOC signal initiates the process of search the SAR sets the MSB $d_1 = 1$ & soon as the START signal arrives. & all other bits are set to 0. If the converter is a 8-bit convertor, the initial setting would be 10000000 the o/p V_d of the DAC for this trial code is compared with the analog i/p V_i.

If the $V_i > V_d$. It implies that the trial code 10000000 is less than the correct digital representation of V_i. the MSB d_1 is left at 1 & the next lower significant bit is set at 1, & the process is repeated

If $V_i < V_d$, it implies that the trial code 10000000 is greater than the current digital rep of V_i then the MSB is set to 0, & the next LSB is set to 1, & the process is repeated.

The comparator changes state whenever the DAC o/p crosses V_i & thus activates the EOC command.

With the successive comparision of the bits of the DAC o/p the o/p vol of the ADC becomes more & more close to the actual i/p voltage.

Whatever the value of the analog i/p only 8 pulses are required to establish the accurate o/p.

In practice, however an additional pulse is needed to load the o/p register & reinitialize the ckt.

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Correct digital representation	SAR o/p at different stages	Comparator o/p
10110010	>1000 0000	1
	<1100 0000	0
	1010 0000	1
	1011 0000	1
	1011 1000	0
	1011 0100	0
	1011 0010	1
	1011 0011	0

The time required for one conversion from analog to digital depends on both the CKT Period T & the no of bits n.

$T_C \rightarrow$ denotes conversion time

$$T_C = T(n+1)$$

16) (b) Design an Astable multivibrator using 555 timer with a frequency of 1KHz for the duty cycle of 40%.

Sol Given: $F = 1KHz$ & $D = 40\% = 0.4$

W.K.T

$$T_{ON} = 0.693 R_A C \rightarrow (1)$$

$$T_{OFF} = 0.693 R_B C \rightarrow (2)$$

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

$$D = \frac{0.693 R_A C}{0.693 R_A C + 0.693 R_B C}$$

$$D = \frac{R_A}{R_A + R_B}$$

$$0.4 = \frac{R_A}{R_A + R_B}$$

$$R_A = 0.4 R_A + 0.4 R_B$$

$$R_B = \frac{0.6}{0.4} R_A$$

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$$R_B = 1.5 R_A \rightarrow (3)$$

$$f = \frac{1}{0.693C(R_A + R_B)}$$ assume $C = 0.1\mu F$

$$1K = \frac{1}{0.693 \times 0.1 \times 10^{-6}(R_A + R_B)}$$

$$R_A + R_B = \frac{1}{0.693 \times 0.1 \times 10^{-6} \times 10^{3}}$$

$$R_A + R_B = 14400$$

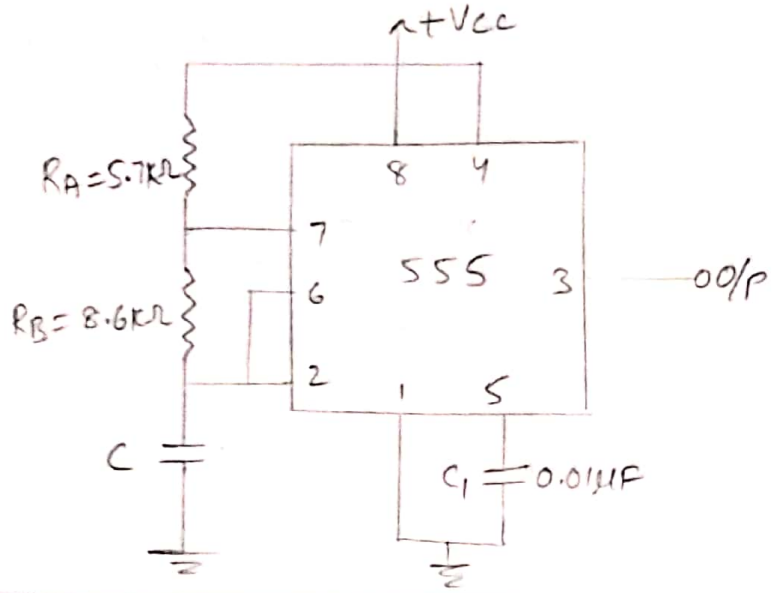
from (3) $\Rightarrow$ $R_A + 1.5R_A = 14400$

$$2.5R_A = 14400$$

$$R_A = 5760 = 5.7K\Omega$$

$$5760 + R_B = 14400$$

$$R_B = 8640 = 8.6K\Omega$$



Q17. Write short notes on following

a) Phase locked loop b) Precision rectifier using opAmp

c) Difference b/w bootsrap & miller circuit.

A: a) Phase locked loop:

PLL is a closed loop system which is designed to lock the o/p freq & phase to the freq & phase of the i/p sgnl.

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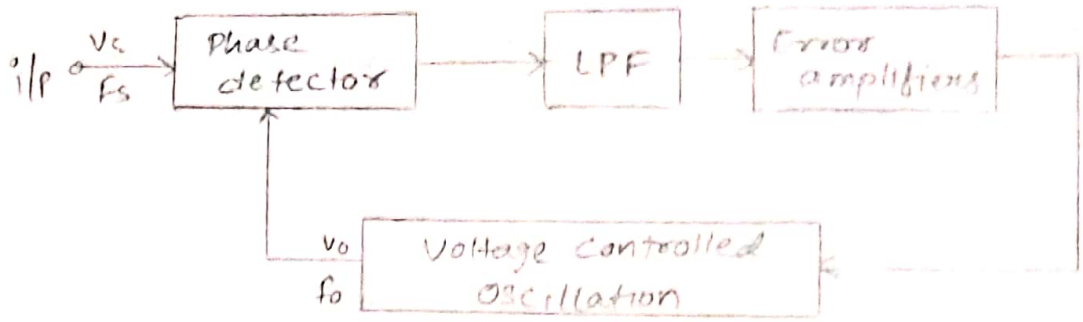
PLL's are available in monolithic IC form & hence they are inexpensive & are extensively used in modern communication system.

Operating principle of PLL:



The main features of PLL are a phase detector, a LPF an error amp & a vol controlled oscillator

b) Precision rectifier using op-amp:

Ordinary diodes cannot rectify voltages below V_γ (0.6V) this is main defect in silicon rectifier. This is overcomed by precision rectifiers by using op-amp rectifier, where the voltage is the mV range be obtained.

Two types 1) Precision Halfwave rectifier
2) Precision fullwave rectifier

c) Difference b/w boothsrap & miller circuit:

Boothsrap	Millar
- It employees +ve feedback	- It employees -ve feedback
- It generates +ve goining ramp	- It generates -ve goining ramp
- It employess an emitter follower whose gain nearly unity	- It employess high gain amplifier (gain is ideally infinite)
- Amplifier must have infinite resistance	- Not very essential.

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