Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
			T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
		Fetch	T ₂	MDR←RAM[MAR]	R,	44 00 00 00 00
				PC←PC+1	C _p	
1)	ACC ← Memory		T ₃	IR←MDR	E _{MDR} , L _{IR1} , CTR _L	00 C0 00 00 80
LDA Address	[Address]		T ₄	MAR←PC	E_PC , L_MAR	18 00 00 00 00
		Execution	T ₅	MDR←RAM[MAR] PC←PC+1	R, Cp	44 00 00 00 00
			T ₆	MAR←MDR	E _{MDR} , L _{MAR}	08 80 00 00 00
			T ₇	MDR←RAM[MAR]	R	04 00 00 00 00
			T ₈	ACC←MDR	E_{MDR} , L_{A} , CTR_{R}	00 84 00 00 40
			T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
		Fetch	T ₂	MDR←RAM[MAR]	R,	44 00 00 00 00
2)	• •			PC←PC+1	C _p	
2)	Memory [Address]		T ₃	IR←MDR	E _{MDR} , L _{IR1,} CTR _L	00 C0 00 00 80
STA Address	\leftarrow ACC		T ₄	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
		Execution	T ₅	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
			T ₆	MAR←MDR	E _{MDR} , L _{MAR}	08 80 00 00 00
			T ₇	MDR←ACC	E _A , L _{MDR}	01 02 00 00 00
			T ₈	RAM[MAR]←MDR	W, CTR _R	02 00 00 00 40
			T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
3) MOV ACC, B	ACC←B	Fetch	T ₂	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
, -			T ₃	IR←MDR	E _{MDR} , L _{IR1,} CTR _L	00 CO 00 00 80
		Execution	T ₄	ACC←B	L _A , E _{B,} CTR _R	00 04 00 80 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
			T_1	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
4)		Fetch	T_2	MDR←RAM[MAR]	R,	44 00 00 00 00
MOV B, ACC	B←ACC			PC←PC+1	Cp	
			T ₃	IR←MDR	E _{MDR} , L _{IR1,} CTR _L	00 C0 00 00 80
		Execution	T_4	B←ACC	L_B , E_{A_r} CTR _R	
						00 02 01 00 40
			T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
5)		Fetch	T ₂	MDR←RAM[MAR]	R,	44 00 00 00 00
				PC←PC+1	C _p	
MOV ACC, immediate	ACC ← immediate		T ₃	IR←MDR	E _{MDR} , L _{IR1} CTR _L	00 C0 00 00 80
			T ₄	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
			T ₅	MDR←RAM[MAR]	R,	44 00 00 00 00
		Execution		PC←PC+1	Cp	
			T ₆	ACC←MDR	L _A , E _{MDR,}	00 84 00 00 40
					CTR _R	
			T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
6)		Fetch	T ₂	MDR←RAM[MAR]	R,	44 00 00 00 00
	ACC ← input			PC←PC+1	C _p	
IN			T ₃	IR←MDR	E _{MDR} , L _{IR1}	00 C0 00 00 80
		Execution	T ₄	ACC←IN	L_A , E_{IN} , CTR_R	80 04 00 00 40
			T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
7)		Fetch	T ₂	MDR←RAM[MAR]	R,	44 00 00 00 00
•	output←ACC		_	PC←PC+1	C _p	
OUT	·		T ₃	IR←MDR	E _{MDR} , L _{IR1}	00 C0 00 00 80
		Execution	T ₄	OUT←ACC	L _O , E _{A,} CTR _R	00 02 00 01 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
			T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
8)		Fetch	T ₂	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
ADD B	B ACC ← ACC+B		T ₃	IR←MDR	E _{MDR} , L _{IR1}	00 C0 00 00 80
		Execution	T ₄	TEMP←B	L _{TEMP} , E _{B,} E _{ADD}	00 00 44 80 00
			T ₅	ACC←ACC+TEMP FLAGS←C,Z	E _{ALU} , L _{A,} L _{FLAG} CTR _R	00 04 80 08 40
			T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
9)	ACC ←	Fetch	T ₂	MDR←RAM[MAR] PC←PC+1	R, Cp	44 00 00 00 00
ADC B	ACC+B+C		T ₃	IR←MDR	E _{MDR} , L _{IR1}	00 C0 00 00 80
			T ₄	IR←FLAGS	L _{IR2} , E _{FLAGS}	00 20 00 02 00
		Execution	T ₅	TEMP←B C _{IN} ←IR _C	L _{TEMP} , E _B SADD, E _{ADD}	00 00 44 80 08
			T ₆	ACC←ACC+TEMP+C FLAGS←C,Z	E _{ALU,} L _{A,} L _{FLAGS,} CTR _R	00 04 80 08 40
			T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
10)		Fetch	T ₂	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
SUB B	ACC ←ACC-B		T ₃	IR←MDR	E _{MDR} , L _{IR1}	00 C0 00 00 80
		Execution	T ₄	TEMP←B	L _{TEMP} , E _B ,	00 00 24 80 00
			T ₅	ACC←ACC-TEMP FLAGS←C,Z	E _{ALU} , L _{A,} L _{FLAG} CTR _R	00 04 80 08 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
			T_1	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
11)	ACC ←ACC-	Fetch	T ₂	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
SBB B	B-C		T ₃	IR←MDR	E _{MDR} , L _{IR1}	00 C0 00 00 80
			T ₄	IR←FLAGS	L _{IR2} , E _{FLAGS}	00 20 00 02 00
		Execution	T ₅	TEMP←B C _{IN} ←IR _C	L _{TEMP} , E _B SADD,	00 00 24 80 08
			T ₆	ACC←ACC-TEMP-C FLAGS←C,Z	E _{SUB} E _{ALU} , L _A , L _{FLAGS} CTR _R	00 04 80 08 40
			T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
		Fetch	T ₂	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
12)	ACC←ACC + immediate +		T ₃	IR←MDR	E _{MDR} , L _{IR1}	00 C0 00 00 80
ADC	С		T ₄	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
immediate		Execution	T ₅	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
			T ₆	IR←FLAGS	L _{IR2} , E _{FLAGS}	00 20 00 02 00
			T ₇	TEMP←MDR C _{IN} ←IR _C	E _{MDR} , L _{TEMP} SADD, E _{ADD}	00 80 44 00 08
			T ₈	ACC←ACC+ TEMP+C FLAGS←C,Z	E _{ALU} , L _A , L _{FLAGS} CTR _R	00 04 80 08 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
			T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
13)		Fetch	T ₂	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
SBB	ACC←ACC - immediate -		T ₃	IR←MDR	E _{MDR} , L _{IR1}	00 C0 00 00 80
immediate	С		T ₄	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
		Execution	T ₅	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
			T ₆	IR←FLAGS	L _{IR2} , E _{FLAGS}	00 20 00 02 00
			T ₇	TEMP←MDR C _{IN} ←IR _C	E _{MDR} , L _{TEMP} SADD,	00 80 24 00 08
			T ₈	ACC←ACC –TEMP-C FLAGS←C,Z	E _{SUB} E _{ALU,} L _{A,} L _{FLAGS} CTR _R	00 04 80 08 40
	ACC		T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
14)	Unchanged; FLAGS	Fetch	T ₂	MDR←RAM[MAR] PC←PC+1	R,	44 00 00 00 00
CMP B	changed accordingly		T ₃	IR←MDR	E _{MDR} , L _{IR1}	00 C0 00 00 80
		Execution	T ₄	TEMP←B	L _{TEMP} , E _{B,} E _{SUB}	00 00 24 80 00
			T ₅	FLAGS←ALU	L _{FLAGS} , E _{ALU} CTR _R	00 00 80 08 40
			T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
15)		Fetch	T ₂	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
XCHG	ACC←→B		T ₃	IR←MDR	E _{MDR} , L _{IR1}	00 C0 00 00 80
			T ₄	TEMP←B	L _{TEMP} , E _B	00 00 04 80 00
		Execution	T ₅	B←ACC	L _B , E _A	00 02 01 00 00
			T ₆	ACC←TEMP	L_A , E_{TEMP}	00 04 02 00 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
			T_1	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
16)		Fetch	T ₂	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
JC address	Jumps if C=1		T ₃	IR←MDR	E _{MDR} , L _{IR1}	00 C0 00 00 80
			T ₄	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
		Execution	T ₅	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
			T ₆	IR(6,7)←FLAGS	E _{FLAGS} , L _{IR2}	00 20 00 02 00
			T ₇	MUX C determine	CTR _C	00 00 00 00 20
			T ₈	PC ← MDR	E _{MDR,} L _{PC} CTR _R	20 80 00 00 40
44		Fetch	T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
17)						
JE address	Jumps if Z=1		T ₂	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
			T ₃	IR←MDR	E _{MDR} , L _{IR1}	00 C0 00 00 80
		Execution	T ₄	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
			T ₅	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
			T ₆	IR(6,7)←FLAGS	E _{FLAGS} , L _{IR2}	00 20 00 02 00
			T ₇	MUX Z determine	CTR _z	00 00 00 00 10
			T ₈	PC ← MDR	E _{MDR,} L _{PC} CTR _R	20 80 00 00 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
		Fetch	T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
18)	STACK←ACC		T ₂	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
PUSH			T ₃	IR←MDR	E _{MDR} , L _{IR1} CTR _L	00 C0 00 00 80
		Execution	T ₄	MDR←ACC SP←SP-1	L _{MDR} , E _A D _{SP}	01 02 00 10 00
			T ₅	MAR←SP	L _{MAR} , E _{SP}	08 00 00 40 00
			T ₆	RAM[MAR]←MDR	W CTR _R	02 00 00 00 40
		Fetch	T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00
19)	ACC←STACK		T ₂	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
POP			T ₃	IR←MDR	E _{MDR} , L _{IR1} CTR _L	00 C0 00 00 80
		Execution	T ₄	MAR←SP	L _{MAR} , E _{SP}	08 00 00 40 00
			T ₅	MDR←RAM[MAR] SP←SP+1	R, U _{SP}	04 00 00 20 00
			T ₆	ACC←MDR	L _A , E _{MDR} CTR _R	00 84 00 00 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
		Fetch	T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
20)	Calls		T ₂	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
CALL Address	subroutine		T ₃	IR←MDR	E _{MDR} , L _{IR1} CTR _L	00 C0 00 00 80
		Execution	T ₄	MDR(0-4)←ACC MDR(6-7)←FLAG SP←SP-1	L _{MDR} , E _A , E _{FLAGS}	01 02 00 12 00
		Execution	T ₅	MAR←SP	D_{SP} L_{MAR} , E_{SP}	08 00 00 40 00
			T ₆	RAM[MAR]←MDR	W	02 00 00 00 00
			T ₇	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
			T ₈	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
			T ₉	TEMP←MDR SP←SP-1	L _{TEMP} , E _{MDR} , DSP	00 80 04 10 00
			T ₁₀	MDR←PC	L _{MDR} , E _{PC}	11 00 00 00 00
			T ₁₁	MAR←SP	L _{MAR} , E _{SP}	08 00 00 40 00
			T ₁₂	RAM[MAR]←MDR	W	02 00 00 00 00
			T ₁₃	PC←TEMP	L _{PC} , E _{TEMP} CTR _R	20 00 02 00 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
			T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
		Fetch	T ₂	MDR←RAM[MAR]	R,	44 00 00 00 00
21)				PC←PC+1	C_p	
RET	Returns to caller from		T ₃	IR←MDR	E _{MDR} , L _{IR1} CTR _L	00 C0 00 00 80
	current		T_4	MAR←SP	L _{MAR} , E _{SP}	08 00 00 40 00
	subroutine	Execution	T ₅	MDR←RAM[MAR] SP←SP+1	R U _{SP}	04 00 00 20 00
			T ₆	PC←MDR	L _{PC} , E _{MDR}	20 80 00 00 00
			T ₇	MAR←SP	L _{MAR} , E _{SP}	08 00 00 40 00
			T ₈	MDR←RAM[MAR] SP←SP+1	R, U _{SP}	04 00 00 20 00
			T ₉	ACC←MDR(0-4) FLAGS←MDR(6-7)	L _A , E _{MDR} , L _{FLAGS} CTR _R	00 84 00 08 40
			T ₁	MAR ← PC	E _{PC} , L _{MAR}	18 00 00 00 00
		Fetch	T ₂	MDR←RAM[MAR]	R,	44 00 00 00 00
22)			٠,٧	PC←PC+1	C _p	
JMP address	Jumps to address		T ₃	IR←MDR	E _{MDR} , L _{IR1}	00 C0 00 00 80
			T ₄	MAR←PC	L _{MAR} , E _{PC}	18 00 00 00 00
		Execution	T ₅	MDR←RAM[MAR]	R	04 00 00 00 00
			T ₆	PC←MDR	L_{PC} , E_{MDR} CTR_{R}	20 80 00 00 40
			T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
23) HLT	Halts		T ₂	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
	execution		T ₃	IR←MDR	E _{MDR} , L _{IR1}	00 C0 00 00 80
		Execution	T ₄	Stops clock	HLT, CTR _R	00 00 00 044

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
24)		Fetch	T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
NOP	No operation		T ₂	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
			T ₃	IR←MDR	E _{MDR} , L _{IR1} CTR _L	00 C0 00 00 80
		Execution	T_4	Do nothing	CTR _R	00 00 00 00 40
25)		Fetch	T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
STZ	Z ← 1		T ₂	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
			T ₃	IR←MDR	E _{MDR} , L _{IR1}	00 CO 00 00 80
		Execution	T ₄	FLAGS←SET_ZF_BUF (1)	SET_ZF, E_SET_ZF, L_FLAG_Z CTR _R	00 18 00 04 40
26) CLZ	z ← 0	Fetch	T ₁	MAR←PC	E _{PC} , L _{MAR}	18 00 00 00 00
			T ₂	MDR←RAM[MAR] PC←PC+1	R, C _p	44 00 00 00 00
			T ₃	IR←MDR	E _{MDR} , L _{IR1}	00 CO 00 00 80
		Execution	T ₄	FLAGS←SET_ZF_BUF (0)	E_SET_ZF, L_FLAG_Z CTR _R	00 08 00 04 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
			T ₁	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
		Fetch	T_2	MDR←RAM[MAR]	R,	44 00 00 00 00
				PC←PC+1	C_p	
27)	ACC ← ACC		T_3	IR←MDR	E_{MDR} , L_{IR1}	00 CO 00 00 80
AND	& immediate				CTR _L	
immediate			T ₄	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_{5}	MDR←RAM[MAR]	R,	44 00 00 00 00
		Execution		PC←PC+1	C_p	
			T_6	TEMP←MDR	L _{TEMP} , E _{MDR} ,	00 80 14 00 00
					E _{AND}	
			T_7	ACC←ACC & TEMP	E_{ALU}, L_{A}	00 04 80 08 40
				FLAGS←C,Z	L _{FLAGS}	
					CTR _R	
			T ₁	MAR←PC	E_PC , L_MAR	18 00 00 00 00
		Fetch	T ₂	MDR←RAM[MAR]	R,	44 00 00 00 00
				PC←PC+1	C _p	
28)	ACC ← ACC		T ₃	IR←MDR	E_{MDR} , L_{IR1}	00 C0 00 00 80
	Memory				CTR _L	
OR[address]	[address]		T ₄	MAR←PC	E_PC , L_MAR	18 00 00 00 00
			T ₅	MDR←RAM[MAR]	R,	44 00 00 00 00
		Execution		PC←PC+1	C _p	
			T_6	MAR←MDR	L_{MAR} , E_{MDR}	08 80 00 00 00
			T ₇	MDR←RAM[MAR]	R	04 00 00 00 00
			T ₈	TEMP←MDR	L _{TEMP} , E _{MDR} ,	00 80 0C 00 00
					E _{OR}	
			T ₉	ACC←ACC TEMP	E_{ALU}, L_{A}	00 04 80 08 40
				FLAGS←C,Z	L_{FLAGS}	
					CTR _R	