Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
1) LDA Address	ACC ← Memory [Address]	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1}, CTR_L	00 C0 00 00 80
		Execution	T_4	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_5	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_6	MAR←MDR	E_{MDR} , L_{MAR}	08 80 00 00 00
			T_7	MDR←RAM[MAR]	R	04 00 00 00 00
			T_8	ACC←MDR	E_{MDR} ,$L_{A,}CTR_R$	00 84 00 00 40
2) STA Address	Memory [Address] ← ACC	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , $L_{IR1,}$ CTR_L	00 C0 00 00 80
		Execution	T_4	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_5	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_6	MAR←MDR	E_{MDR} , L_{MAR}	08 80 00 00 00
			T_7	MDR←ACC	E_A , L_{MDR}	01 02 00 00 00
			T_8	RAM[MAR]←MDR	W, CTR_R	02 00 00 00 40
3) MOV ACC, B	ACC←B	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , $L_{IR1,}$ CTR_L	00 C0 00 00 80
		Execution	T_4	ACC←B	L_A , $E_{B,}$ CTR_R	00 04 00 80 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
4) MOV B, ACC	B←ACC	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , $L_{IR1,}$ CTR_L	00 C0 00 00 80
		Execution	T_4	B←ACC	L_B , $E_{A,}$ CTR_R	00 02 01 00 40
5) MOV ACC, immediate	ACC ← immediate	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_5	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_6	ACC←MDR	L_A , $E_{MDR,}$ CTR_R	00 84 00 00 40
6) IN	ACC←input	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	ACC←IN	L_A , $E_{IN,}$ CTR_R	80 04 00 00 40
7) OUT	output←ACC	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	OUT←ACC	L_O , $E_{A,}$ CTR_R	00 02 00 01 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
8) ADD B	ACC ← ACC+B	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	TEMP←B	L_{TEMP} , E_B, E_{ADD}	00 00 44 80 00
			T_5	ACC←ACC+TEMP FLAGS←C,Z	E_{ALU}, L_A, L_{FLAG} CTR_R	00 04 80 08 40
9) ADC B	ACC ← ACC+B+C	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	IR←FLAGS	L_{IR2}, E_{FLAGS}	00 20 00 02 00
			T_5	TEMP←B C_{IN}←IR_C	L_{TEMP} , E_B SADD, E_{ADD}	00 00 44 80 08
			T_6	ACC←ACC+TEMP+C FLAGS←C,Z	E_{ALU}, L_A, L_{FLAGS}, CTR_R	00 04 80 08 40
10) SUB B	ACC ←ACC-B	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	TEMP←B	L_{TEMP} , E_B, E_{SUB}	00 00 24 80 00
			T_5	ACC←ACC-TEMP FLAGS←C,Z	E_{ALU}, L_A, L_{FLAG} CTR_R	00 04 80 08 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
11) SBB B	ACC ←ACC-B-C	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	IR←FLAGS	L_{IR2}, E_{FLAGS}	00 20 00 02 00
			T_5	TEMP←B C_{IN}←IR_C	L_{TEMP} , E_B SADD, E_{SUB}	00 00 24 80 08
			T_6	ACC←ACC-TEMP-C FLAGS←C,Z	$E_{ALU,}$ $L_{A,}$ L_{FLAGS} CTR_R	00 04 80 08 40
12) ADC immediate	ACC←ACC + immediate + C	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_5	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_6	IR←FLAGS	L_{IR2}, E_{FLAGS}	00 20 00 02 00
			T_7	TEMP←MDR C_{IN}←IR_C	E_{MDR} , L_{TEMP} SADD, E_{ADD}	00 80 44 00 08
			T_8	ACC←ACC + TEMP+C FLAGS←C,Z	$E_{ALU,}$ $L_{A,}$ L_{FLAGS} CTR_R	00 04 80 08 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
13) SBB immediate	ACC←ACC - immediate - C	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_5	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_6	IR←FLAGS	L_{IR2}, E_{FLAGS}	00 20 00 02 00
			T_7	TEMP←MDR C_{IN}←IR_C	E_{MDR} , L_{TEMP} SADD, E_{SUB}	00 80 24 00 08
			T_8	ACC←ACC –TEMP-C FLAGS←C,Z	$E_{ALU,}$ $L_{A,}$ L_{FLAGS} CTR_R	00 04 80 08 40
14) CMP B	ACC Unchanged; FLAGS changed accordingly	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	TEMP←B	L_{TEMP} , $E_{B,}$ E_{SUB}	00 00 24 80 00
			T_5	FLAGS←ALU	$L_{FLAGS,}$ E_{ALU} CTR_R	00 00 80 08 40
15) XCHG	ACC←→B	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	TEMP←B	L_{TEMP} , E_B	00 00 04 80 00
			T_5	B←ACC	L_B , E_A	00 02 01 00 00
			T_6	ACC←TEMP	L_A , E_{TEMP} CTR_R	00 04 02 00 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
16) JC address	Jumps if C=1	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_5	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_6	IR(6,7)←FLAGS	E_{FLAGS} , L_{IR2}	00 20 00 02 00
			T_7	MUX C determine	CTR_C	00 00 00 00 20
			T_8	PC ← MDR	$E_{MDR,}L_{PC}$ CTR_R	20 80 00 00 40
44 17) JE address	Jumps if Z=1	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_5	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_6	IR(6,7)←FLAGS	E_{FLAGS} , L_{IR2}	00 20 00 02 00
			T_7	MUX Z determine	CTR_Z	00 00 00 00 10
			T_8	PC ← MDR	$E_{MDR,}L_{PC}$ CTR_R	20 80 00 00 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
18) PUSH	STACK←ACC	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	MDR←ACC SP←SP-1	L_{MDR} , E_A D_{SP}	01 02 00 10 00
			T_5	MAR←SP	L_{MAR} , E_{SP}	08 00 00 40 00
			T_6	RAM[MAR]←MDR	W CTR_R	02 00 00 00 40
19) POP	ACC←STACK	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	MAR←SP	L_{MAR} , E_{SP}	08 00 00 40 00
			T_5	MDR←RAM[MAR] SP←SP+1	R, U_{SP}	04 00 00 20 00
			T_6	ACC←MDR	L_A , E_{MDR} CTR_R	00 84 00 00 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
20) CALL Address	Calls subroutine	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	MDR(0-4)←ACC MDR(6-7)←FLAG SP←SP-1	L_{MDR},E_A,E_{FLAGS} D_{SP}	01 02 00 12 00
			T_5	MAR←SP	L_{MAR} , E_{SP}	08 00 00 40 00
			T_6	RAM[MAR]←MDR	W	02 00 00 00 00
			T_7	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_8	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_9	TEMP←MDR SP←SP-1	L_{TEMP} , E_{MDR} , DSP	00 80 04 10 00
			T_{10}	MDR←PC	L_{MDR} , E_{PC}	11 00 00 00 00
			T_{11}	MAR←SP	L_{MAR} , E_{SP}	08 00 00 40 00
			T_{12}	RAM[MAR]←MDR	W	02 00 00 00 00
			T_{13}	PC←TEMP	L_{PC} , E_{TEMP} CTR_R	20 00 02 00 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
21) RET	Returns to caller from current subroutine	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	MAR←SP	L_{MAR} , E_{SP}	08 00 00 40 00
			T_5	MDR←RAM[MAR] SP←SP+1	R U_{SP}	04 00 00 20 00
			T_6	PC←MDR	L_{PC} , E_{MDR}	20 80 00 00 00
			T_7	MAR←SP	L_{MAR} , E_{SP}	08 00 00 40 00
			T_8	MDR←RAM[MAR] SP←SP+1	R, U_{SP}	04 00 00 20 00
			T_9	ACC←MDR(0-4) FLAGS←MDR(6-7)	L_A , E_{MDR} , L_{FLAGS} CTR_R	00 84 00 08 40
22) JMP address	Jumps to address	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	MAR←PC	L_{MAR} , E_{PC}	18 00 00 00 00
			T_5	MDR←RAM[MAR]	R	04 00 00 00 00
			T_6	PC←MDR	L_{PC} , E_{MDR} CTR_R	20 80 00 00 40
23) HLT	Halts execution	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	Stops clock	HLT, CTR_R	00 00 00 00 44

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
24) NOP	No operation	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	Do nothing	CTR_R	00 00 00 00 40
25) STZ	Z ← 1	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	FLAGS←SET_ZF_BUF (1)	SET_ZF, E_SET_ZF, L_FLAG_Z CTR_R	00 18 00 04 40
26) CLZ	Z ←0	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	FLAGS←SET_ZF_BUF (0)	E_SET_ZF, L_FLAG_Z CTR_R	00 08 00 04 40

Instruction	Macro Instruction	Cycle	T-States	Micro Instructions	Active Bits	CON
27) AND immediate	ACC ← ACC & immediate	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_5	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_6	TEMP←MDR	L_{TEMP} , $E_{MDR,}$ E_{AND}	00 80 14 00 00
			T_7	ACC←ACC & TEMP FLAGS←C,Z	$E_{ALU,}$ $L_{A,}$ L_{FLAGS} CTR_R	00 04 80 08 40
28) OR[address]	ACC ← ACC | Memory [address]	Fetch	T_1	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_2	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_3	IR←MDR	E_{MDR} , L_{IR1} CTR_L	00 C0 00 00 80
		Execution	T_4	MAR←PC	E_{PC} , L_{MAR}	18 00 00 00 00
			T_5	MDR←RAM[MAR] PC←PC+1	R, C_p	44 00 00 00 00
			T_6	MAR←MDR	L_{MAR} , E_{MDR}	08 80 00 00 00
			T_7	MDR←RAM[MAR]	R	04 00 00 00 00
			T_8	TEMP←MDR	L_{TEMP} , $E_{MDR,}$ E_{OR}	00 80 0C 00 00
			T_9	ACC←ACC | TEMP FLAGS←C,Z	$E_{ALU,}$ $L_{A,}$ L_{FLAGS} CTR_R	00 04 80 08 40