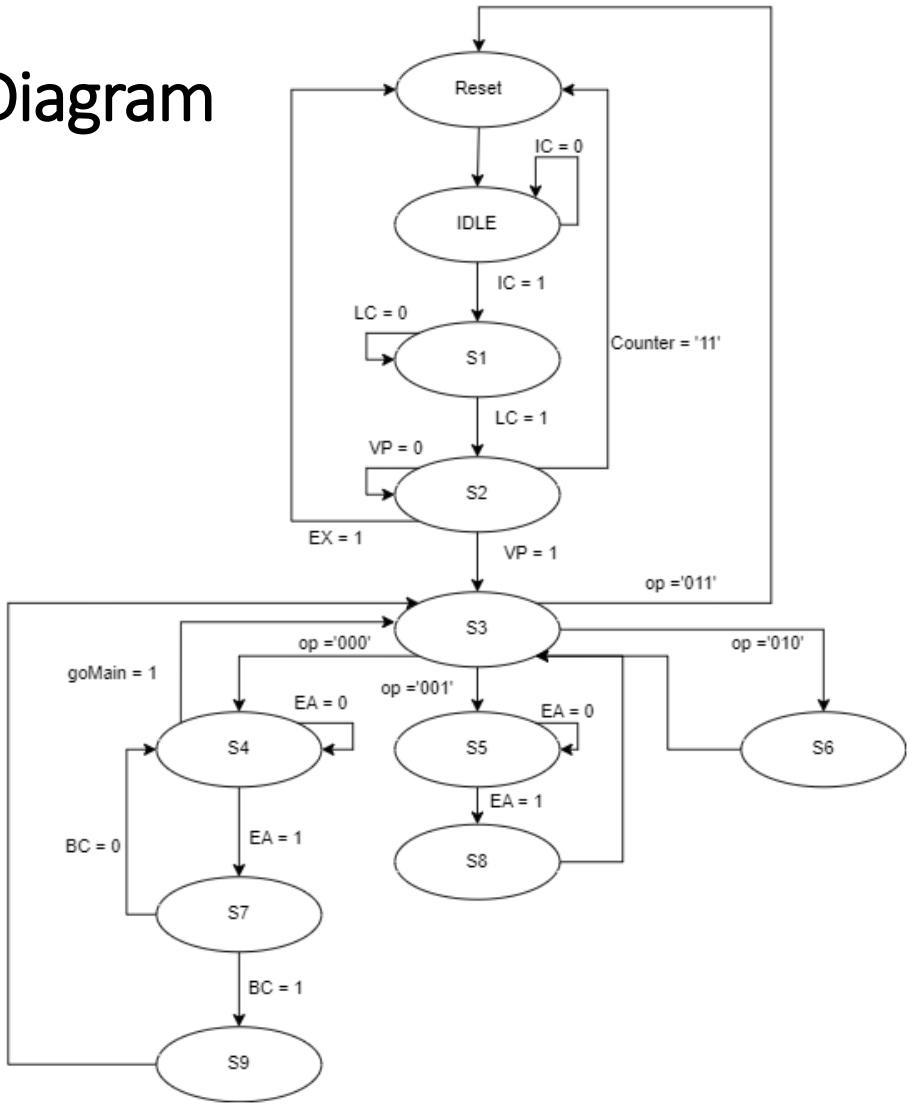
State Diagram



Input	Description
IC	Insert Card
LC	Language Chosen
VP	Valid Password
BC	Balance Check
Counter	Invalid Pass Counter
Ex	Exit
goMain	Go to Main Menu
op	Operations (Withdraw/Deposit/Balance Check)

State	Description
IDLE	IDLE State
S1	Language
S2	Password
S3	Main Menu
S4	Withdraw
S5	Deposit
S6	Balance
S7	Check Balance
S8	Adding Balance
S9	Subtracting Balance

Implementing the core of the bank ATM design

Reset:

This state returns all input to the initial state then continues to IDLE.

IDLE:

Default State that transitions to the next state when User enters his *Card.*

S1:" Language":

This state ensures that user inputs *language* for the ATM machine to transition to next state

S2:" Password":

This state ensures that user inputs *Correct Password* for the ATM machine to transition to next state.

If the *Password* is incorrect after 3 failed attempts the *Counter* will be set to '11' and ATM is reset.

If User wants to exit, he can input *Ex* and ATM is reset.

S3:" Main Menu":

This state has four main points:

1- If User wants to exit, he can input *op = '011'* and ATM is reset.
2- If User wants to check his balance, he can input *op = '010'* which transitions to **S6.**

3- If User wants to *Deposit* to his balance, he can input *op = '001'* which transitions to **S5.**

4- If User wants to *Withdraw* from his balance, he can input *op = '000'* which transitions to **S4.**

S4:" Withdraw":

This state ensures that user inputs *EA (Entered Amount)* for the ATM machine to transition to **S7**.

User can input *goMain* if he wants to go to *Main Menu.*

S5:" Deposit":

This state ensures that user inputs *EA (Entered Amount)* for the ATM machine to transition to **S8**.

User can input *goMain* if he wants to go to *Main Menu.*

S6:" Balance":

This state shows user his balance and return to **S3** *Main Menu.*

S7:" Check Balance":

This state checks if *Withdraw Amount* is less than User's balance and raise the *BC (Balance Check)* flag then continues to **S9.**

If User's balance is not sufficient returns to **S4**.

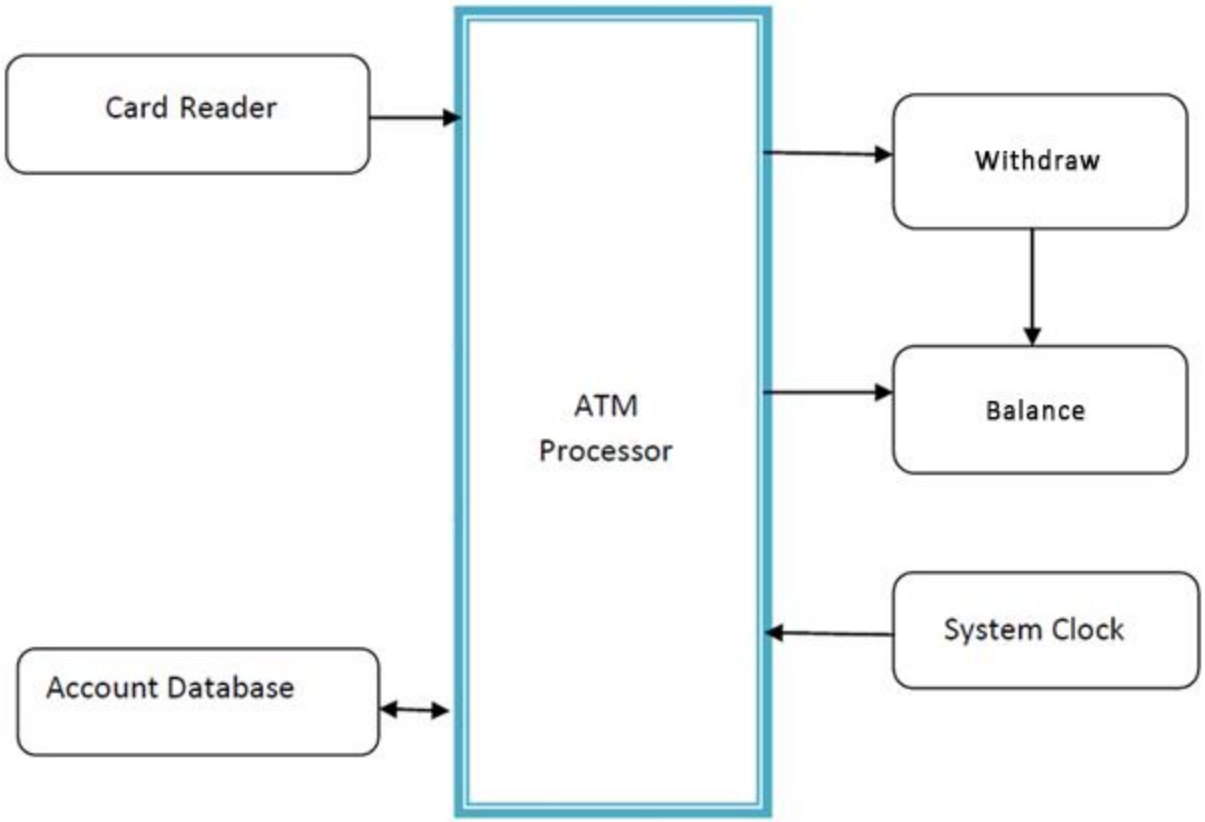
S8:" Adding Balance":

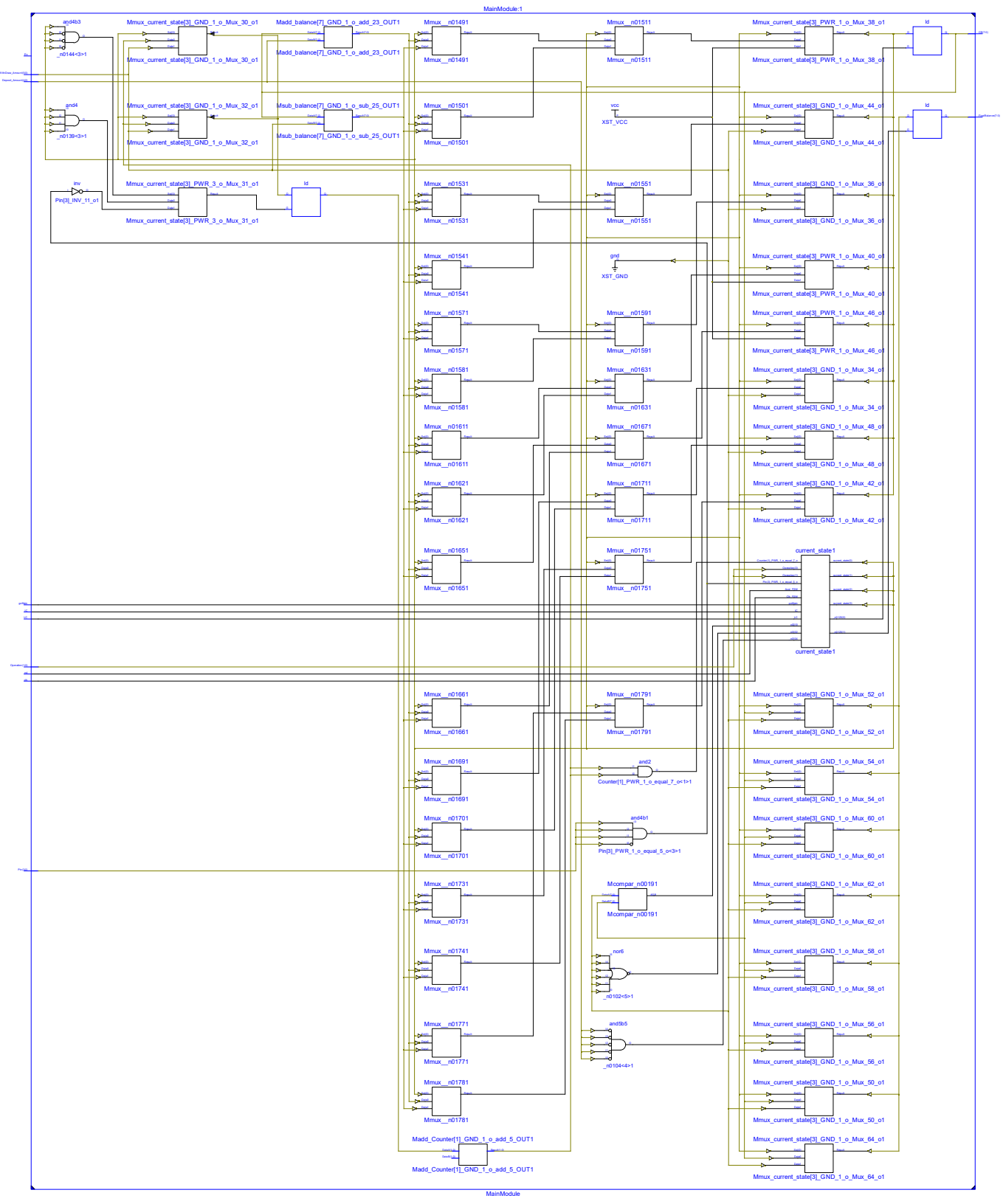
This state adds the deposited money into User's balance then returns to **S3** *Main Menu.*

S9:" Subtracting Balance":

This state subtracts the *Withdraw* money from User's balance then returns to **S3** *Main Menu.*

Model:




MainModule:1
and4b3
_n0144<3>1
Mmux_current_state[3]_GND_1_o_Mux_30_o1
Mmux_current_state[3]_GND_1_o_Mux_30_o1
Madd_balance[7]_GND_1_o_add_23_OUT1
Madd_balance[7]_GND_1_o_add_23_OUT1
Mmux__n01491
Mmux__n01491
Mmux__n01511
Mmux__n01511
Mmux_current_state[3]_PWR_1_o_Mux_38_o1
Mmux_current_state[3]_PWR_1_o_Mux_38_o1
ld
and4
_n0139<3>1
Mmux_current_state[3]_GND_1_o_Mux_32_o1
Mmux_current_state[3]_GND_1_o_Mux_32_o1
Msub_balance[7]_GND_1_o_sub_25_OUT1
Msub_balance[7]_GND_1_o_sub_25_OUT1
Mmux__n01501
Mmux__n01501
vcc
XST_VCC
Mmux_current_state[3]_GND_1_o_Mux_44_o1
Mmux_current_state[3]_GND_1_o_Mux_44_o1
ld
inv
Pin[3]_INV_11_o1
Mmux_current_state[3]_PWR_3_o_Mux_31_o1
Mmux_current_state[3]_PWR_3_o_Mux_31_o1
ld
Mmux__n01531
Mmux__n01531
Mmux__n01551
Mmux__n01551
Mmux_current_state[3]_GND_1_o_Mux_36_o1
Mmux_current_state[3]_GND_1_o_Mux_36_o1
Mmux__n01541
Mmux__n01541
gnd
XST_GND
Mmux_current_state[3]_PWR_1_o_Mux_40_o1
Mmux_current_state[3]_PWR_1_o_Mux_40_o1
Mmux__n01571
Mmux__n01571
Mmux__n01591
Mmux__n01591
Mmux_current_state[3]_PWR_1_o_Mux_46_o1
Mmux_current_state[3]_PWR_1_o_Mux_46_o1
Mmux__n01581
Mmux__n01581
Mmux__n01631
Mmux__n01631
Mmux_current_state[3]_GND_1_o_Mux_34_o1
Mmux_current_state[3]_GND_1_o_Mux_34_o1
Mmux__n01611
Mmux__n01611
Mmux__n01671
Mmux__n01671
Mmux_current_state[3]_GND_1_o_Mux_48_o1
Mmux_current_state[3]_GND_1_o_Mux_48_o1
Mmux__n01621
Mmux__n01621
Mmux__n01711
Mmux__n01711
Mmux_current_state[3]_GND_1_o_Mux_42_o1
Mmux_current_state[3]_GND_1_o_Mux_42_o1
Mmux__n01651
Mmux__n01651
Mmux__n01751
Mmux__n01751
current_state1
current_state1
Mmux__n01661
Mmux__n01661
Mmux__n01791
Mmux__n01791
Mmux_current_state[3]_GND_1_o_Mux_52_o1
Mmux_current_state[3]_GND_1_o_Mux_52_o1
Mmux__n01691
Mmux__n01691
and2
Counter[1]_PWR_1_o_equal_7_o<1>1
Mmux_current_state[3]_GND_1_o_Mux_54_o1
Mmux_current_state[3]_GND_1_o_Mux_54_o1
Mmux__n01701
Mmux__n01701
and4b1
Pin[3]_PWR_1_o_equal_5_o<3>1
Mmux_current_state[3]_GND_1_o_Mux_60_o1
Mmux_current_state[3]_GND_1_o_Mux_60_o1
Mmux__n01731
Mmux__n01731
Mcompar_n00191
Mcompar_n00191
Mmux_current_state[3]_GND_1_o_Mux_62_o1
Mmux_current_state[3]_GND_1_o_Mux_62_o1
Mmux__n01741
Mmux__n01741
nor6
_n0102<5>1
Mmux_current_state[3]_GND_1_o_Mux_58_o1
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Mmux__n01771
Mmux__n01771
and5b5
_n0104<4>1
Mmux_current_state[3]_GND_1_o_Mux_56_o1
Mmux_current_state[3]_GND_1_o_Mux_56_o1
Mmux__n01781
Mmux__n01781
Mmux_current_state[3]_GND_1_o_Mux_50_o1
Mmux_current_state[3]_GND_1_o_Mux_50_o1
Madd_Counter[1]_GND_1_o_add_5_OUT1
Madd_Counter[1]_GND_1_o_add_5_OUT1
Mmux_current_state[3]_GND_1_o_Mux_64_o1
Mmux_current_state[3]_GND_1_o_Mux_64_o1
MainModule