Department Of Electronics and Communication Engineering
National Institute Of Technology, Hazratbal
Major Examination, Regular - Autumn 2018

Course: B.Tech – CSE
Subject: Basic Electronics
Max Marks: 60

Semester: III
Duration: 3 Hours

Note: Attempt any four questions. Draw diagrams wherever necessary.

Q1. (a) Draw the common emitter circuit and sketch its input output characteristics. Also explain the operating regions by indicating them on the curve.

(b) Explain hall effect? [10, 5]

Q2. (a) With a neat circuit diagram explain the working of bridge rectifier. Show that its efficiency is 81.2%.
Also derive the expression for I_{dc} and I_{RMS}
(b) Design a fixed biased circuit using a silicon transistor having $\beta = 100$.
V_{cc} is 100 V and dc biased conditions are to be $V_{ce} = 5$ V and $I_c = 5$mA

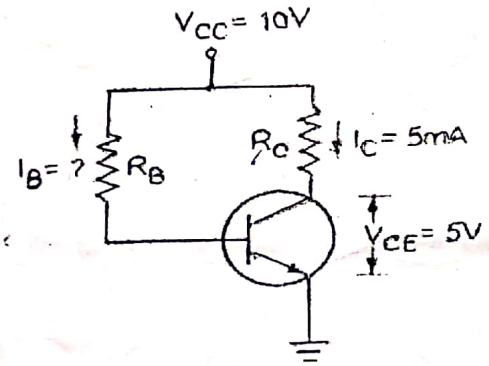

Fig .1

[10, 5]

Q3. (a) Explain the operation and characteristics of P-channel JFET in detail.
(b) What are clippers? Explain parallel clippers using additional voltage sources. [8, 7]

Q4. (a) Explain the fixed biased circuit and derive the various stability factors.
(b) Calculate the collector current and emitter current of a transistor with $\alpha = 0.99$ and $I_{ceo} = 100\mu A$ when the base current is 10 μA. [10, 5]

Q5. Explain briefly:
(a) H -- parameter transistor model for CE configuration
(b) Concept of load line and operating point
(c) Early effect [5, 5, 5]