Deptt. of ECE

N.I.T Sgr.

B.Tech. 4th CSE Major Session: Supplementary Dec. 2014

Subject: Digital Electronics Time Allowed: 2 hrs.

Max.Marks : 50

Note: Attempt any four questions. All questions carry equal marks.

Q1. a) Design a 2X4 decoder. How will you convert it to a demultiplexer?

b) Design a BCD-to-Excess-3 code converter. (6.5,6)

Q2. a) Implement the following function with only AND & NOT gates

$$F = XY + X'Y' + Y'Z$$

b) Use map method to obtain simplified POS expression of the given function

$$F(A,B,C,D) = \sum (0,1,2,5,8,9,10)$$ (6,6.5)

Q3. a) Obtain characteristics table, characteristics equation and logic diagram of a jk flip flop.

b) Design a counter with the following binary sequence using JK flip flops
0,4,2,1,6 & repeat. (5,7.5)

Q4. a) Differentiate between 1's & 2's complement.

b) Find the 2's complement of the following number
1101.001 - 100.11

Find the 8's complement of $(162)_8$ (5,7.5)

Q5. a) Design a combinational circuit with four input lines that represent a decimal digit in BCD & four output lines that generate the 9's complement of the input digit.

b) A seven -bit Hamming code is received as 1 1 1 1 1 0 1. Check if it is correct, if not, find the correct code. (7, 5)

Q6. a) The content of a 4-bit shift register is initially 1101. The register is shifted six times to right ,with the serial input being 101101. What is the content of the register after each shift.

b) Draw a block diagram of serial adder. In what respect it is different than parallel adder. (6.5,6)

162
80

2+48