DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, SRINAGAR

Examination: Major

Subject: Digital Electronics & Logic Design — *B.Tech : 4TH IT*

Max Marks: 60 — *Time allotted: 2 Hrs*

Note: Attempt any 4 questions. All questions carry equal marks. — *Date: 15-07-2017*

Q.1) a) Define the following signal types :

i)Analog signal ii)Discrete time signal iii)Digital signal iv)Binary signal.

Enumerate the advantages & disadvantages of digital systems over analog signals. (5)

b) Perform the following conversions:

i)$(11.825)_{10} = (\ )_2$ ii) $(80)_{10} = (\ )_8$ iii) $(1101011010110101111)_2 = (\ )_{16}$

iv)$(1110101100010)_2 = (\ )_8$ v) $(5A7C)_{16} = (\ )_8$ vi) $(3257)_8 = (\ )_2$ (6)

c) Calculate the values of x & y in the expression:

$$(235)_x = (565)_{10} = (865)_y$$ (4)

Q.2) a) Consider 0010001 is received at the receiver's end. The receiver doesn't know what was transmitted. Find any error that occurred during transmission if even parity is used. (7.5)

b)Reduce the following expression using K-Map

f(A,B,C,D,E)=∑m(0,1,2,3,10,12,13,14,20,21,22,23,26,27,28,29,30,31) (7.5)

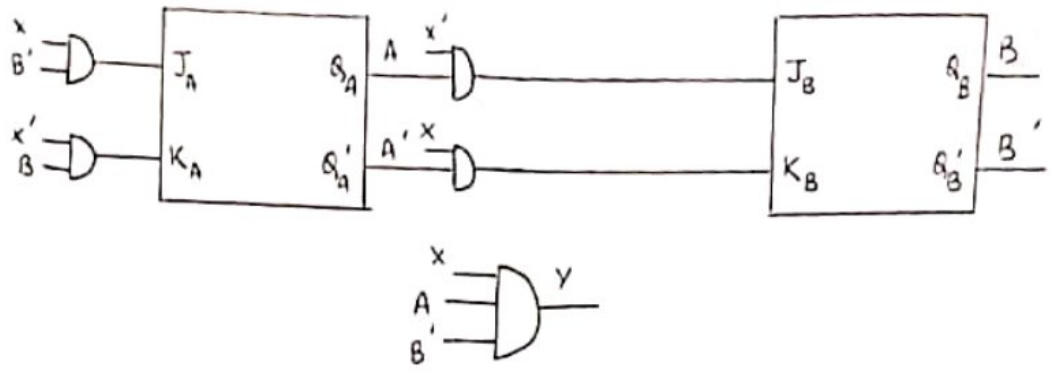
Q.3)a)Reduce the following expression using Tabular method:

F(A,B,C,D) =∑m(0,1,3,7,8,9,11,15) (7.5)

b)NAND & NOR are called as universal gates .Justify (7.5)

Q.4) a) Convert SR Flip flop to T Flip flop. (7.5)

b) Analyze and draw the state diagram for the given circuit :



(7.5)

Q.5) Write short notes on:

a) SISO Shift register

b) 3 bit up/down synchronous counter (7.5, 7.5)