## Department of Electronics and Communication Engineering

## National Institute of Technology, Srinagar

Examination: Major
Subject: Digital Electronics
Date: 23rd – June 2016

Semester: 4th (IT)
Max Marks: 50
Time allotted: 2hrs

***Note: Attempt any four questions.***

Q1.i) Minimize using Boolean algebra:

$$Y = (A + B)(A + \overline{AB})C + \overline{A}(B+\overline{C}) + \overline{A}B + ABC$$ (4)

ii) Minimize using K-map:

$$f(A,B,C,D) = \sum m(0, 3, 4, 5, 7) + d(8, 9, 10, 11, 12, 13, 14, 15)$$ (4)

iii) Consider 0010001 is received at receiver end. The receiver does not know what was transmitted. Find any error that occurred during transmission if even parity is used. (4.5)

Q2. i) Define and explain with example the following:

a) Canonical and Standard Expression
b) Maxterm and Minterm (6)

ii) Draw and explain logic diagram of look- ahead carry generator. (6.5)

Q3.) i) Differentiate between Combinational and Sequential circuits. (4)

ii) Draw the schematic diagram of J-K flip flop. Obtain the characteristics, excitation tables and write down its truth table. (5)

iii) State the disadvantage of SR flip flop. How can they be avoided? (3.5)

Q4. i) What is VHDL? What are the three main parts of VHDL code? (4.5)

ii) Implement the following function with a multiplexer (Use selector BCD)

$$f(A,B,C,D) = \sum m (0, 2, 3, 6, 8, 9, 11, 12, 14)$$ (5)

iii) Implement the following function using a 4 to 16 line decoder:

$$f = \sum m (1, 2, 4, 7, 8, 11, 12, 13)$$ (3)

Q5. i) What is a Counter? Explain the working of a Ring Counter. (4.5)

ii) Design a Sequential circuit whose state diagram is given (Use JK-FF) (8)