NATIONAL INSTITUTE OF TECHNOLOGY SRINAGAR

Department of Computer Science and Engineering

Major Exam (Autumn 2019)

Course: **COA**	Course Code: **CSE 501**	Max marks: **90**
Semester: **5th(CSE)**	Time Allotted: **3 hours**	Dated:-**Feb 2020**

Course Outcomes (CO)

CO1	Understanding basic computer organization and various addressing modes and instructions.
CO2	Understanding basic processing unit and organization of simple processor.
CO3	Exposing different ways of communicating with I/O devices and standard I/O interfaces.
CO4	Understanding memory hierarchy with emphasis on different cache mapping techniques.
CO5	Understanding arithmetic and logical operation and circuit with integer and floating point data representation.

This Question Paper Consists of 6 Questions. (Attempt only five)

Q1. a) An instruction is stored at location 300 with its address field at location 301. The address field has value 400. A processor register R1 contains number 200. Evaluate the effective address if the addressing mode of instruction is a) Direct; B) Immediate; c) Relative; d) Register Indirect; e) Index, Index with R1 as the index register. **[CO1][5]**

b) For each of the following categories explain any two instruction in detail.
b.1) Arithmetic instruction.
b.2) Program control instruction.
b.3) Logical instruction.
b.4) Data transfer instruction. **[CO1][8]**

c) Starting from an initial value of R = 11011101, determine the sequence of binary values in R after each operation in the sequence: (1) a logical shift-left, (2) followed by an arithmetic shift-right, (3) followed by another arithmetic shift-right, and (4) followed, finally, by a circular shift-left. Show all your work. **[CO1][5]**

Q2.a) Define instruction cycle? Explain with proper timing diagram execution of fetch and decode instruction. **[CO2][8]**

b) Give difference between hardwired and microprogrammed control unit? For an embedded system which of these architectures are suitable and why? **[CO2][5]**

c) Consider the following possibilities for saving the return address of a subroutine:
i) In a processor register
ii) In a memory location associated with the call, so that a different location is used when the subroutine is called from different places
iii) on a stack

Which of these possibilities supports subroutine nesting and which supports Subroutine recursion? [CO2][3]

d) A computer supports one address and two address instructions. All the Addresses are the memory addresses. Memory size is 1Mbyte. How many one address instructions are possible if it has 240 two addresses instructions? (Assume binary instructions code has 48 bits) [CO3][2]

Q3.a) Draw a block diagram of DMA controller. Explain in detail DMA transfer operation with help of a neat diagram. [CO3][9]

b) Explain the terms interrupt break point and DMA break point. Also specify the significance of both. [CO3][2]

c) Discuss the significance of strobe and handshaking in asynchronous data transfer. Which one is advantageous and why? [CO3][3]

d) What are priority based interrupts? Explain Daisy chain priority (hardware implementation) with a help of block diagram. [CO3][4]

Q4.a) Memory access time is 5ns for a read operation with a hit in cache, 10ns for a read operation with a miss in cache, 4ns for a write operation with a hit in cache and 20ns for a write operation with a miss in cache. Execution of a sequence of instructions involve 100 instruction fetch operation, 80 memory read operation and 40 memory write operation. The cache hit ratio is 0.9. Calculate the average memory access time (in ns) in executing the sequence of instruction. [CO4][6]

b) What is direct mapping? With the help of example explain limitation of this mapping scheme. [CO4][4]

c) A memory system consisting of two levels L_1 and L_2. The required access times of those are 5 ns and 120 ns respectively. Another memory system has also two levels L_3 and L_4 whose access time are 10 ns and 150 ns respectively. The hit ratio of second system is 0.8 and average access time is twice than that of first system. What is the hit ratio of first system? [CO4][5]

d) A direct mapped cache is of size 64 KB with block size 32 B. Logical address generated is 32 bit. What is the bits required for tag and block field? [CO4][3]

Q5.a) Consider the addition of two numbers 10001110 and 1000000 in a 8 bit ALU. What will be the status of (Z) Zero, (S) Sin, (C) Carry, (O) Overflow Flags? Assume numbers represented in 2's Compliment format and that S=1 if result is negative. [CO5][2]

b) Perform the following operation on four-bit input with an adder circuit:
b.1) Subtraction and subtraction with borrow.
b.2) Increment and Decrement [CO5][4]

c) Differentiate between the following with example. (Give at least five differences)

c.1) Subroutine Call and Interrupt.

c.2) RISC and CISC

c.3) Von Neumann architecture and Harvard Architecture. **[CO5][9]**

d) Represent the number $(117)_{10}$ in IEEE single and double precision formats. **[CO5][3]**

Q6.a) Explain following CPU organisations with an example **[CO2][6]**

a.1) Single Accumulator organisation.

a.2) General register organisation.

a.3) Stack organisation.

b) What is an effective address? Which addressing mode is preferred for program relocation at run time? **[CO2][5]**

c) What is the difference between isolated I/O and memory mapped I/O? What are the advantages and disadvantages of each? **[CO3][5]**

d) How big is a four-way set associative cache memory with a block size of 64 Bytes and containing 1024 sets? **[CO4][2]**

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