Figure 120. Pad Configuration Registers 0–107 (PCR[0:107])

Base + 0x0040 (PCR0)

Address: ... Access: User read/write

Base + 0x0116 (PCR107) 108 registers

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	SMC	APC	0	PA[1:0]		OBE	IBE	0	0	ODE	0	0	SRC	WPE	WPS
W																
Reset(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1. See *Table 111*.

Note: 16/32-bit access is supported for the PCR[0:107] registers.

Table 110. PCR[0:107] field descriptions

Field	Description
SMC	Safe Mode Control This bit supports the overriding of the automatic deactivation of the output buffer of the associated pad upon entering Safe mode of the device. 0: In Safe mode, output buffer of the pad disabled 1: In Safe mode, output buffer remains functional
APC	Analog Pad Control This bit enables the usage of the pad as analog input. 0: Analog input path from the pad is gated and cannot be used. 1: Analog input path switch can be enabled by the ADC.
PA[1:0]	Pad Output Assignment This field selects the function that is allowed to drive the output of a multiplexed pad. The PA field size can vary from 0 to 2 bits, depending on the number of output functions associated with this pad. 00: Alternative mode 0: GPIO 01: Alternative mode 1 (see *Chapter 2 Signal Description*) 10: Alternative mode 2 (see *Chapter 2 Signal Description*) 11: Alternative mode 3 (see *Chapter 2 Signal Description*) *Note: The number of bits in the PA bitfield depends of the number of actual alternate functions provided for each pad. Please see the SPC560Pxx Datasheet (SPC560Pxx).*
OBE	Output Buffer Enable This bit enables the output buffer of the pad in case the pad is in GPIO mode. 0: Output buffer of the pad disabled when PA = 00 1: Output buffer of the pad enabled when PA = 00
IBE	Input Buffer Enable This bit enables the input buffer of the pad. 0: Input buffer of the pad disabled 1: Input buffer of the pad enabled
ODE	Open Drain Output Enable This bit controls output driver configuration for the pads connected to this signal. Either open drain or push/pull driver configurations can be selected. This feature applies to output pads only. 0: Open drain enable signal negated for the pad 1: Open drain enable signal asserted for the pad

Table 110. PCR[0:107] field descriptions (continued)

Field	Description
SRC	Slew Rate Control 0: Slowest configuration 1: Fastest configuration
WPE	Weak Pull Up/Down Enable This bit controls whether the weak pull up/down devices are enabled/disabled for the pad connected to this signal. 0: Weak pull device enable signal negated for the pad 1: Weak pull device enable signal asserted for the pad
WPS	Weak Pull Up/Down Select This bit controls whether weak pull up or weak pull down devices are used for the pads connected to this signal when weak pull up/down devices are enabled. 0: Pull down enabled 1: Pull up enabled

Table 111. PCR[*n*] reset value exceptions

Field	Description
PCR[2] PCR[3] PCR[4]	These registers correspond to the ABS[0], ABS[1], and FAB boot pins, respectively. Their default state is input, pull enabled. Their reset value is 0x0102.
PCR[20]	This register corresponds to the TDO pin. Its default state is ALT1, slew rate = 1. Its reset value is 0x0604.
PCR[21]	This register corresponds to the TDI pin. Its default state is input, pull enabled, pull selected, slew enabled. So its reset value is 0x0107.
PCR[*n*]	For other PCR[*n*] registers, the reset value is 0x0000.

Pad Selection for Multiplexed Inputs registers (PSMI[0_3:32_35])

The purpose of the PSMI[0_3:32_35] registers is to allow connecting a single input pad to one of several peripheral inputs. Thus, it is possible to define different pads to be possible inputs for a certain peripheral function.