8.6 Functional description

The functional description involves the areas of interrupt request sources, priority management, and handshaking with the processor.

Note: The INTC has no spurious vector support. Therefore, if an asserted peripheral or software settable interrupt request, whose PRIn value in INTC_PSR0–INTC_PSR221 is higher than the PRI value in INTC_CPR, negates before the interrupt request to the processor for that peripheral or software settable interrupt request is acknowledged, the interrupt request to the processor still can assert or will remain asserted for that peripheral or software settable interrupt request. In this case, the interrupt vector will correspond to that peripheral or software settable interrupt request. Also, the PRI value in the INTC_CPR will be updated with the corresponding PRIn value in INTC_PSRn. Furthermore, clearing the peripheral interrupt request's enable bit in the peripheral or, alternatively, setting its mask bit has the same consequences as clearing its flag bit. Setting its enable bit or clearing its mask bit while its flag bit is asserted has the same effect on the INTC as an interrupt event setting the flag bit.

Table 87. Interrupt vector table

IRQ #	Offset	Interrupt	Module
On-Platform Peripherals			
Software Interrupts			
0	0x0800	Software configurable flag 0	Software
1	0x0804	Software configurable flag 1	Software
2	0x0808	Software configurable flag 2	Software
3	0x080C	Software configurable flag 3	Software
4	0x0810	Software configurable flag 4	Software
5	0x0814	Software configurable flag 5	Software
6	0x0818	Software configurable flag 6	Software
7	0x081C	Software configurable flag 7	Software
8	0x0820	Reserved	
ECSM			
9	0x0824	Platform Flash Bank 0 Abort | Platform Flash Bank 0 Stall | Platform Flash Bank 1 Abort | Platform Flash Bank 1 Stall | Platform Flash Bank 2 Abort | Platform Flash Bank 2 Stall | Platform Flash Bank 3 Abort | Platform Flash Bank 3 Stall	ECSM
DMA2x			
10	0x0828	Combined Error	DMA2x
11	0x082C	Channel 0	DMA2x

Table 87. Interrupt vector table (continued)

IRQ #	Offset	Interrupt	Module
12	0x0830	Channel 1	DMA2x
13	0x0834	Channel 2	DMA2x
14	0x0838	Channel 3	DMA2x
15	0x083C	Channel 4	DMA2x
16	0x0840	Channel 5	DMA2x
17	0x0844	Channel 6	DMA2x
18	0x0848	Channel 7	DMA2x
19	0x084C	Channel 8	DMA2x
20	0x0850	Channel 9	DMA2x
21	0x0854	Channel 10	DMA2x
22	0x0858	Channel 11	DMA2x
23	0x085C	Channel 12	DMA2x
24	0x0860	Channel 13	DMA2x
25	0x0864	Channel 14	DMA2x
26	0x0868	Channel 15	DMA2x
27	0x086C	Reserved	
SWT			
28	0x0870	Timeout	Software Watchdog (SWT)
29	0x0874	Reserved	
STM			
30	0x0878	Match on channel 0	STM
31	0x087C	Match on channel 1	STM
32	0x0880	Match on channel 2	STM
33	0x0884	Match on channel 3	STM
34	0x0888	Reserved	
ECSM			
35	0x088C	ECC_DBD_PlatformFlash | ECC_DBD_PlatformRAM	ECSM
36	0x0890	ECC_SBC_PlatformFlash | ECC_SBC_PlatformRAM	ECSM
37	0x0894	Reserved	
38	0x0898	Reserved	
39	0x089C	Reserved	
40	0x08A0	Reserved	

Table 87. Interrupt vector table (continued)

IRQ #	Offset	Interrupt	Module
SIUL			
41	0x08A4	SIU External IRQ_0	System Integration Unit Lite (SIUL)
42	0x08A8	SIU External IRQ_1	System Integration Unit Lite (SIUL)
43	0x08AC	SIU External IRQ_2	System Integration Unit Lite (SIUL)
44	0x08B0	SIU External IRQ_3	System Integration Unit Lite (SIUL)
45	0x08B4	Reserved	
46	0x08B8	Reserved	
47	0x08BC	Reserved	
48	0x08C0	Reserved	
49	0x08C4	Reserved	
50	0x08C8	Reserved	
ME			
51	0x08CC	Safe Mode Interrupt	Mode Entry module (ME)
52	0x08D0	Mode Transition Interrupt	Mode Entry module (ME)
53	0x08D4	Invalid Mode Interrupt	Mode Entry module (ME)
54	0x08D8	Invalid Mode Configuration	Mode Entry module (ME)
55	0x08DC	Reserved	
56	0x08E0	Functional and destructive reset alternate event interrupt	Reset Generation Module (RGM)
XOSC			
57	0x08E4	XOSC counter expired	XOSC
58	0x08E8	Reserved	
PIT			
59	0x08EC	PITimer Channel 0	Periodic Interrupt Timer (PIT)
60	0x08F0	PITimer Channel 1	Periodic Interrupt Timer (PIT)
61	0x08F4	PITimer Channel 2	Periodic Interrupt Timer (PIT)
ADC0			
62	0x08F8	ADC_EOC	Analog to Digital Converter 0 (ADC0)
63	0x08FC	ADC_ER	Analog to Digital Converter 0 (ADC0)
64	0x0900	ADC_WD	Analog to Digital Converter 0 (ADC0)
FlexCAN0			
65	0x0904	FLEXCAN_ESR[ERR_INT]	FlexCAN 0 (CAN0)

Table 87. Interrupt vector table (continued)

IRQ #	Offset	Interrupt	Module
66	0x0908	FLEXCAN_ESR_BOFF | FLEXCAN_Transmit_Warning | FLEXCAN_Receive_Warning	FlexCAN 0 (CAN0)
67	0x090C	FLEXCAN_ESR_WAK	FlexCAN 0 (CAN0)
68	0x0910	FLEXCAN_BUF_00_03	FlexCAN 0 (CAN0)
69	0x0914	FLEXCAN_BUF_04_07	FlexCAN 0 (CAN0)
70	0x0918	FLEXCAN_BUF_08_11	FlexCAN 0 (CAN0)
71	0x091C	FLEXCAN_BUF_12_15	FlexCAN 0 (CAN0)
72	0x0920	FLEXCAN_BUF_16_31	FlexCAN 0 (CAN0)
73	0x0924	Reserved	
DSPI0			
74	0x0928	DSPI_SR[TFUF] DSPI_SR[RFOF]	DSPI 0
75	0x092C	DSPI_SR[EOQF]	DSPI 0
76	0x0930	DSPI_SR[TFFF]	DSPI 0
77	0x0934	DSPI_SR[TCF]	DSPI 0
78	0x0938	DSPI_SR[RFDF]	DSPI 0
LINFlex0			
79	0x093C	LINFlex_RXI	LINFlex 0
80	0x0940	LINFlex_TXI	LINFlex 0
81	0x0944	LINFlex_ERR	LINFlex 0
ADC1			
82	0x0948	ADC_EOC	Analog to Digital Converter 1 (ADC1)
83	0x094C	ADC_ER	Analog to Digital Converter 1 (ADC1)
84	0x0950	ADC_WD	Analog to Digital Converter 1 (ADC1)
85	0x0954	Reserved	
86	0x0958	Reserved	
87	0x095C	Reserved	
88	0x0960	Reserved	
89	0x0964	Reserved	
90	0x0968	Reserved	
91	0x096C	Reserved	
92	0x0970	Reserved	
93	0x0974	Reserved	

Table 87. Interrupt vector table (continued)

IRQ #	Offset	Interrupt	Module
DSPI1			
94	0x0978	DSPI_SR[TFUF] DSPI_SR[RFOF]	DSPI 1
95	0x097C	DSPI_SR[EOQF]	DSPI 1
96	0x0980	DSPI_SR[TFFF]	DSPI 1
97	0x0984	DSPI_SR[TCF]	DSPI 1
98	0x0988	DSPI_SR[RFDF]	DSPI 1
LINFlex1			
99	0x098C	LINFlex_RXI	LINFlex 1
100	0x0990	LINFlex_TXI	LINFlex 1
101	0x0994	LINFlex_ERR	LINFlex 1
102	0x0998	Reserved	
103	0x099C	Reserved	
104	0x09A0	Reserved	
105	0x09A4	Reserved	
106	0x09A8	Reserved	
107	0x09AC	Reserved	
108	0x09B0	Reserved	
109	0x09B4	Reserved	
110	0x09B8	Reserved	
111	0x09BC	Reserved	
112	0x09C0	Reserved	
113	0x09C4	Reserved	
DSPI2			
114	0x09C8	DSPI_SR[TFUF] DSPI_SR[RFOF]	DSPI 2
115	0x09CC	DSPI_SR[EOQF]	DSPI 2
116	0x09D0	DSPI_SR[TFFF]	DSPI 2
117	0x09D4	DSPI_SR[TCF]	DSPI 2
118	0x09D8	DSPI_SR[RFDF]	DSPI 2
119	0x09DC	Reserved	
120	0x09E0	Reserved	
121	0x09E4	Reserved	
122	0x09E8	Reserved	

Table 87. Interrupt vector table (continued)

IRQ #	Offset	Interrupt	Module
123	0x09EC	Reserved	
124	0x09F0	Reserved	
125	0x09F4	Reserved	
126	0x09F8	Reserved	
PIT			
127	0x09FC	PITimer Channel 3	Periodic Interrupt Timer (PIT)
128	0x0A00	Reserved	
129	0x0A04	Reserved	
130	0x0A08	Reserved	
131	0x0A0C	Reserved	
132	0x0A10	Reserved	
FlexRay			
133	0x0A14	CIFRR.FNEAIF	FlexRay Controller (FlexRay)
134	0x0A18	CIFRR.FNEBIF	FlexRay Controller (FlexRay)
135	0x0A1C	CIFRR.WUPIF	FlexRay Controller (FlexRay)
136	0x0A20	CIFRR.PRIF	FlexRay Controller (FlexRay)
137	0x0A24	CIFRR.CHIF	FlexRay Controller (FlexRay)
138	0x0A28	CIFRR.TBIF	FlexRay Controller (FlexRay)
139	0x0A2C	CIFRR.RBIF	FlexRay Controller (FlexRay)
140	0x0A30	CIFRR.MIF	FlexRay Controller (FlexRay)
141	0x0A34	Reserved	
142	0x0A38	Reserved	
143	0x0A3C	Reserved	
144	0x0A40	Reserved	
145	0x0A44	Reserved	
146	0x0A48	Reserved	
147	0x0A4C	Reserved	
148	0x0A50	Reserved	
149	0x0A54	Reserved	
150	0x0A58	Reserved	
151	0x0A5C	Reserved	
152	0x0A60	Reserved	
153	0x0A64	Reserved	
154	0x0A68	Reserved	