For Masking with CAN, two registers need to be configured, namely „Mask Register (MR)“ and “Acceptance Register (AR)”.

The MR and AR should be of the same bit length. The bits contained and configured in mask register are checked against the bits configured in acceptance register with a one to one bit correspondence. Hence a 1 in the 0^{th} bit of this register claims a check on the 0^{th} bit of acceptance register for equivalence with the received 0^{th} bit in the message ID.

To configure these registers, one should consider the Message IDs to be received. The acceptance register must be configured with one of the allowed message IDs. Mask register bits must configured such that the bits from allowed message IDs which are constant should only be checked.

Example with a bit length of 4:

Message IDs to be received: 0x0A, 0x0B, 0x01, 0x00

Bit number	**3**	**2**	**1**	**0**
0x0A	1	0	1	0
0x0B	1	0	1	1
0x03	0	0	1	1
0x02	0	0	1	0
Acceptance value	x	0	1	x
Mask Value	0	1	1	0