Laboratory Work – Part 2

Project A: Flip-flops

Experiment 1: RS NAND Latch

Project Name Lab Work – Part ***2*** | Project ***A1*** |***u3191010***

Objective To explore the functions of an RS NAND Latch.

Hypothesis A simple flip-flop is able to store one bit of data, which can be binary 1 or binary 0. We should obtain outputs from the circuit that signify this. Pulser switches will be able to alter the outputs we obtain, such as causing a transition from 0 to 1, or 1 to 0.

Materials

- ETS-5000 Logic Trainer
- TTL IC 7400: Quad 2-input NAND gate

Procedure

1. Assemble the circuit as show in Figure 1.
2. Connect pin 14 of the IC to +5V and pin 7 to ground. On applying power to the latch, you will notice that the latch will either be set to 0 (reset) or 1 (set). You can represent this state as the variable X.
3. Momentarily depress A (high) and B (high) as shown in Table 1 and note down the states of the logic monitors L_1 and L_2.
4. Comment on your observations.

Figure 1:

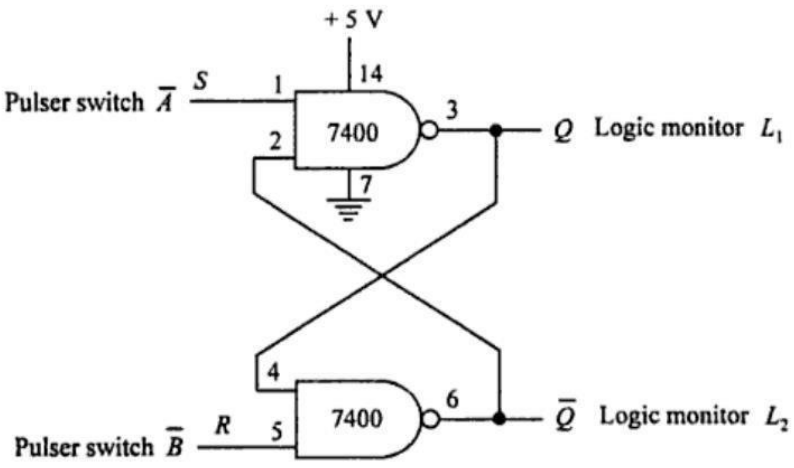


Table 1:

Inputs	
S	**R**
1	1
0	1

1	0
0	0

Tabulated Data

Results:

Inputs		**Outputs**		**Comments**
S	**R**	**Q (L_1)**	**Q- (L_2)**	
1	1	X = 0	~X = 1	Either sets or resets L_1 and L_2. The values of L_1 and L_2 are negations of each other.
0	1	1	0	Sets L_1. Resets L_2.
1	0	0	1	Sets L_2. Resets L_1.
0	0	1	1	Sets and clears the latch at the same time, which produces an invalid output (L_1 = L_2).

Analysis

Initially, the values of A (high) and B (high) are both 1. When the pulser switch for A is depressed, A (high) = 0. When the pulser switch for B is depressed, B (high) = 0. When S and R equal 1 (neither switches are pressed), it keeps the previous outputs, which in our case was L_1 = 0 (green light) and L_2 = 1 (red light). When the A switch was depressed, aka S = 0 and R = 1, L_1 lit up red (1) and L_2 lit up green (0). When the B switch was depressed, aka S = 1 and R = 0, the L_1 lit up green (0) and L_2 lit up red (1). When both the A and B switches were depressed, aka S = 0 and R = 0, both LED's lit up red (L_1 = L_2 = 1). This however is a contradiction according to Boolean algebra, as in this scenario, L_1 = ~L_2 and L_2 = ~L_1. This produces an invalid output.

Conclusion

In this lab, we observed the functions of an RS NAND latch. We used the ETS-5000 Logic Trainer and TTL IC 7400: Quad 2-input NAND gate to build a circuit that used pulser switches for inputs, and then tested different inputs to see what outputs we get. We recorded our results onto a table and added our own commentary to explain what we understood out of the results. Our data shows that the latch was, like we hypothesised, able to store data. The pulser switches, when depressed, were able to alter that stored data to give a different result. When an invalid output was obtained, the latch reset itself. From this lab, I learned how NAND gates operate and

how a NAND latch can store data, which can then be altered by sending pulses through the circuit.

Experiment 2: JK Flip-flops

Project Name Lab Work – Part ***2*** | Project ***A2*** |***u3191010***

Objective To explore the operations of the JK Flip-flop IC 7476.

Hypothesis A JK flip-flop has two main operations: asynchronous and synchronous. The asynchronous operations (pre-set and clear) will toggle our main output either 1 (pre-set) or 0 (clear). The synchronous operations will basically set or reset our main output using the pulser switch (our clock), depending on the switch, when both asynchronous operations are set to 1.

Materials

- ETS-5000 Logic Trainer
- TTL IC 7476 Dual J-K Flip-flop

Procedure

1. The IC contains two independent JK flip-flops. Only one of the flip-flops will be used. Connect the flip-flop as shown in Figure 2. The J, K, PR, and CLR inputs are connected to logic switches SW1 to SW4 respectively. The clock input is connected to pulser switch socket A, which is normally low. Outputs Q and Q- are connected to L_1 and L_2. Connect pin 5 of the IC to +5V and pin 13 to ground.
2. Now we consider the asynchronous operation of the Flip-Flop. As J and K inputs have no effect on the asynchronous operation, the position of switches SW1 and SW2 does not matter. With switches SW3 and SW4, apply logic levels to PR and CLR inputs as indicated in the first three rows of Table 2 and record your observations of the output.
3. For the remaining four rows of Table 2 (synchronous operations) the PR and CLR inputs are held high. Apply logic levels to J and K inputs as shown in the table. No clock pulse is applied in the fourth row. In the last three rows, after you have applied logic levels to J and K inputs, follow that up with low to high and high to low transitions with pulser switch A.

Figure 2:

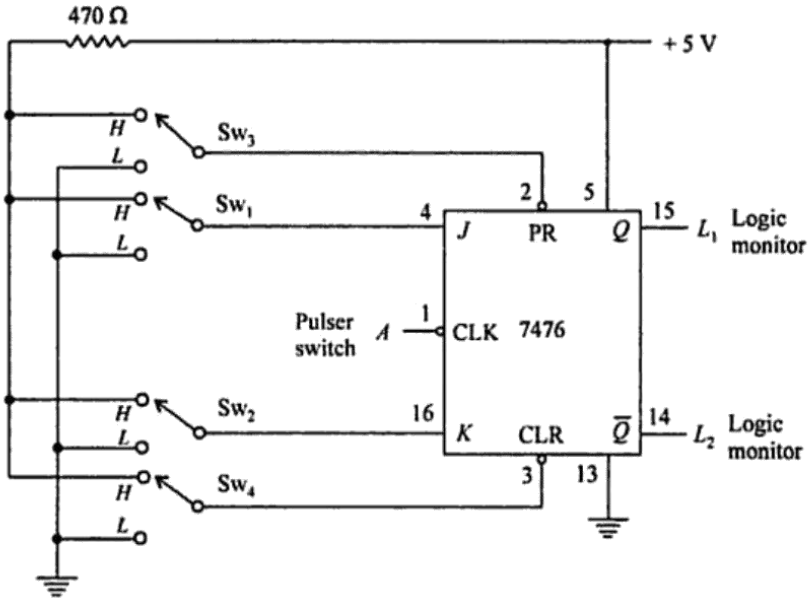


Table 2:

	Inputs				
	Asynchronous		Synchronous		
	PR (Sw3)	CLR (Sw4)	CLK (pulser)	J (Sw1)	K (Sw2)
1	0	0	X	X	X
2	0	1	X	X	X
3	1	0	X	X	X
4	1	1	X	0	0
5	1	1	1	0	1
6	1	1	1	1	0
7	1	1	1	1	1

Tabulated Data

Results:

	Inputs					Outputs
	Asynchronous		Synchronous			
	PR	CLR	CLK	J	K	Q
1	0	0	0	0	0	1 (Does not change.)
2	0	1	0	0	0	0 (Does not change.)
3	1	0	0	0	0	1 (Does not change.)
4	1	1	0	0	0	$Q_o = 1$ (Invalid.)
5	1	1	1	0	1	1 (Does not change)

6	1	1	1	1	0	0 (Does not change.)
7	1	1	1	1	1	1 (Toggle.)

Analysis

From the tabulated data, we can observe the effects of the asynchronous operations and the synchronous operations on the main output Q (L_1). The PR operation causes a transition from 0 to 1. The CLR operation causes a transition from 1 to 0. When both PR and CLR are set to 1, we get an output that is actually from the memory. In our case it was 1. However, should the previous output have been 0, if PR and CLR were set to 1, the output we would've gotten out of that would've been 0. As for the synchronous functions, these were tested with both asynchronous operations set to 1. CLK can set or reset Q depending on the states of J and K. When J is set to 1, CLK resets Q to 0. When K is set to 1, CLK sets Q to 1. When both J and K are set to 1, CLK can both set and reset Q.

Conclusion

In this lab, we explored the operations of the JK Flip-flop IC 7476. We built up a circuit using one JK flip-flop, and then tested the asynchronous operations, with the synchronous operations set to 0. Then we tested the synchronous operations with the asynchronous operations set to 1. We then recorded our results in a table. From our data, we can see how the asynchronous and synchronous operations of a JK flip-flop affect the output, as well as the reliance the asynchronous and synchronous operations have of each other. When everything but CLK is set to 1, we can use CLK to set the output according to our will. Overall, I learned how the JK flip-flop and its operations work, and can definitely see its mechanisms as a useful tool for future projects.

Experiment 3: Clocked JK Flip-flops

Project Name

Lab Work – Part ***2*** | Project ***A3*** |***u3191010***

Objective

To observe frequency division using clocked JK Flip-flops.

Hypothesis

No hypothesis was made.

Materials

- ETS-5000 Logic Trainer
- TTL IC 7476 Dual J-K Flip-flop

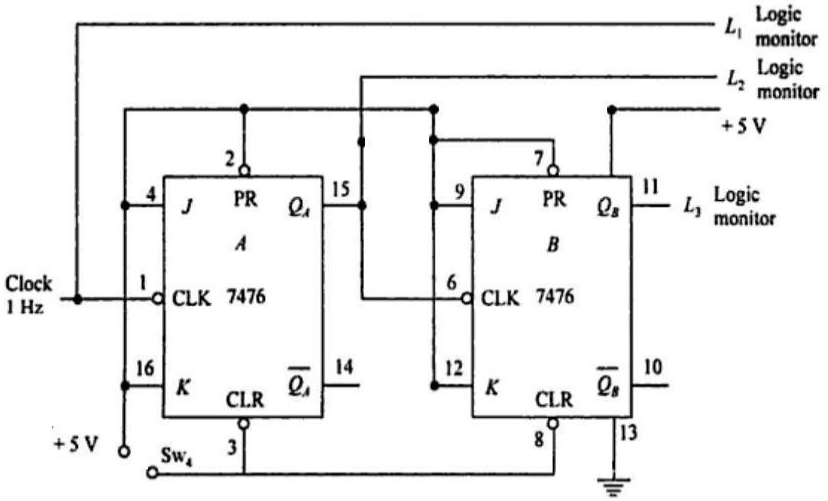
Procedure

1. Assemble the circuit as shown in Figure 3. Both Flip-Flops in the IC are to be used in this experiment. Power up the circuit by connecting pin 5 to +5V and pin 13 to ground.
2. From Figure 3, we can see that the flip-flop connected to L_2 and L_3 are dependent on the flip-flop connected to L_1 and CLK.
3. Use pulser switch A as the clock. Record each output into a table for every time you depress and every time you release the switch. Create a timing

diagram using the table that demonstrates the relationship of L_2 and L_3 with L_1.

4. Then connect the clock to the pulse generator, which automatically produces pulses according to the frequency you set. Adjust the knobs for max amplitude and a frequency of 10 Hz. Observe the speed of the high (red) outputs and the relationship of L_2 and L_3 with L_1.
5. Demonstrate proper operation of your circuit to the tutor. A dual trace oscilloscope will be used to observe the relationship derived in Step 3.

Figure 3:

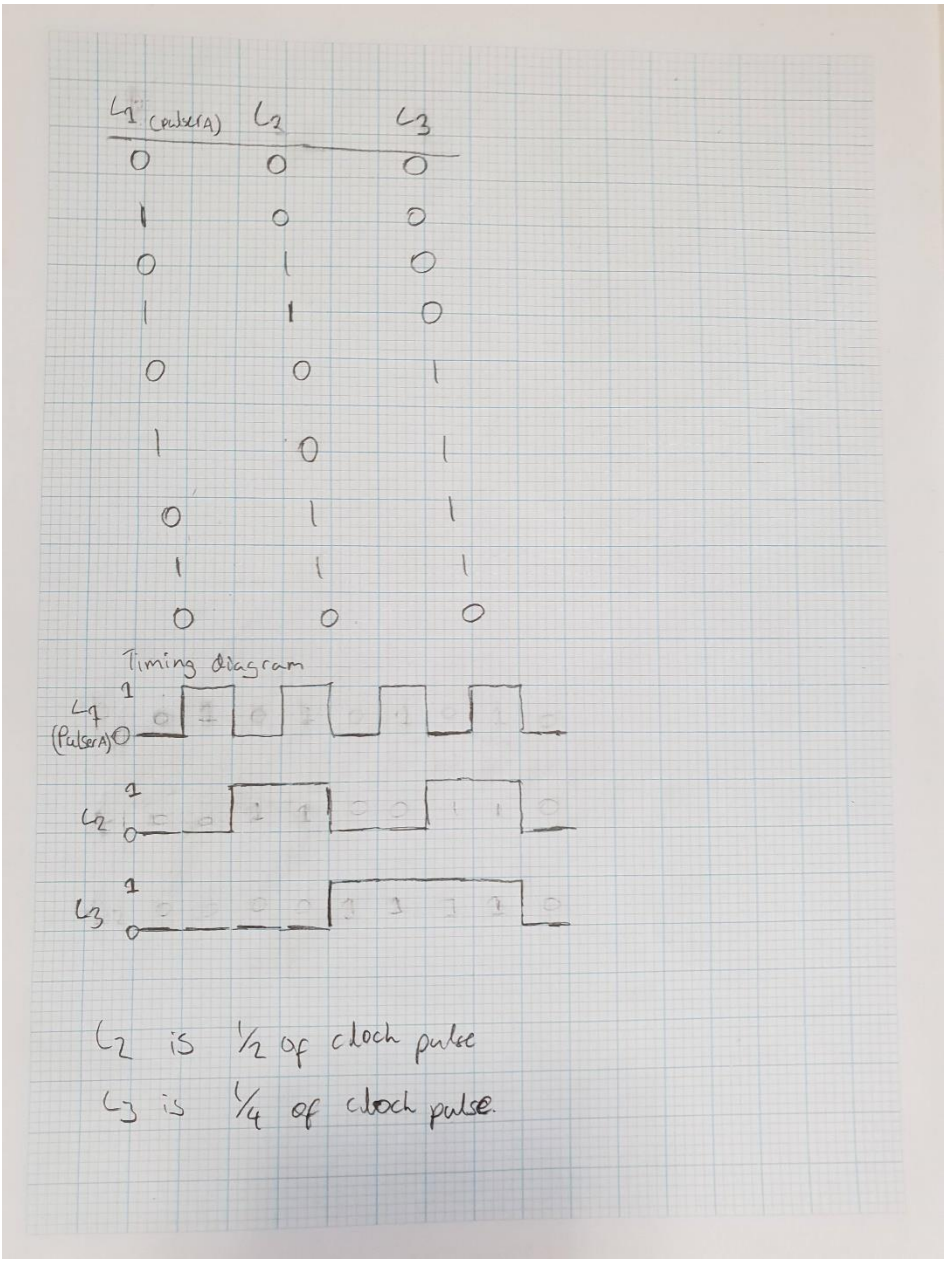


Tabulated Data

Results:

No. of Counts L_1	No. of Counts L_2	No. of Counts L_3
8	4	2

Analysis



The high output frequency of each LED varies. L_1's frequency is that of the clock, L_2's is half of L_1's, and L_3's is half of L_2's and a quarter of L_1's. When automated using the pulse generator, the LED's produce outputs at an interesting pattern.

Conclusion

The purpose of this lab was to further explore JK Flip-flops and to use them to observe frequency division. We built a circuit using two JK Flip-flops and connected it to two different clocks (one at a time) to observe the output speeds and the relationships between each output. We recorded our observations into tables and created a timing diagram out of our results. From our data, we can see that the output frequencies of each LED vary due to the way the circuit was built, and there is a clear dependency between L_2/L_3 (both connected to one flip-flop) and L_1 (connected to the other flip flop and the clock). Overall, I learned more about the mechanisms of JK flip-flops and how

they can be used in frequency division, and I also learned about other functionalities of the trainer board (the pulse generator).