**Manufacturing and Reliability Challenges of Advanced Packaging Technologies to Achieve Solutions Beyond Moore’s Rule**

Final Report

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**

Under Guidance of

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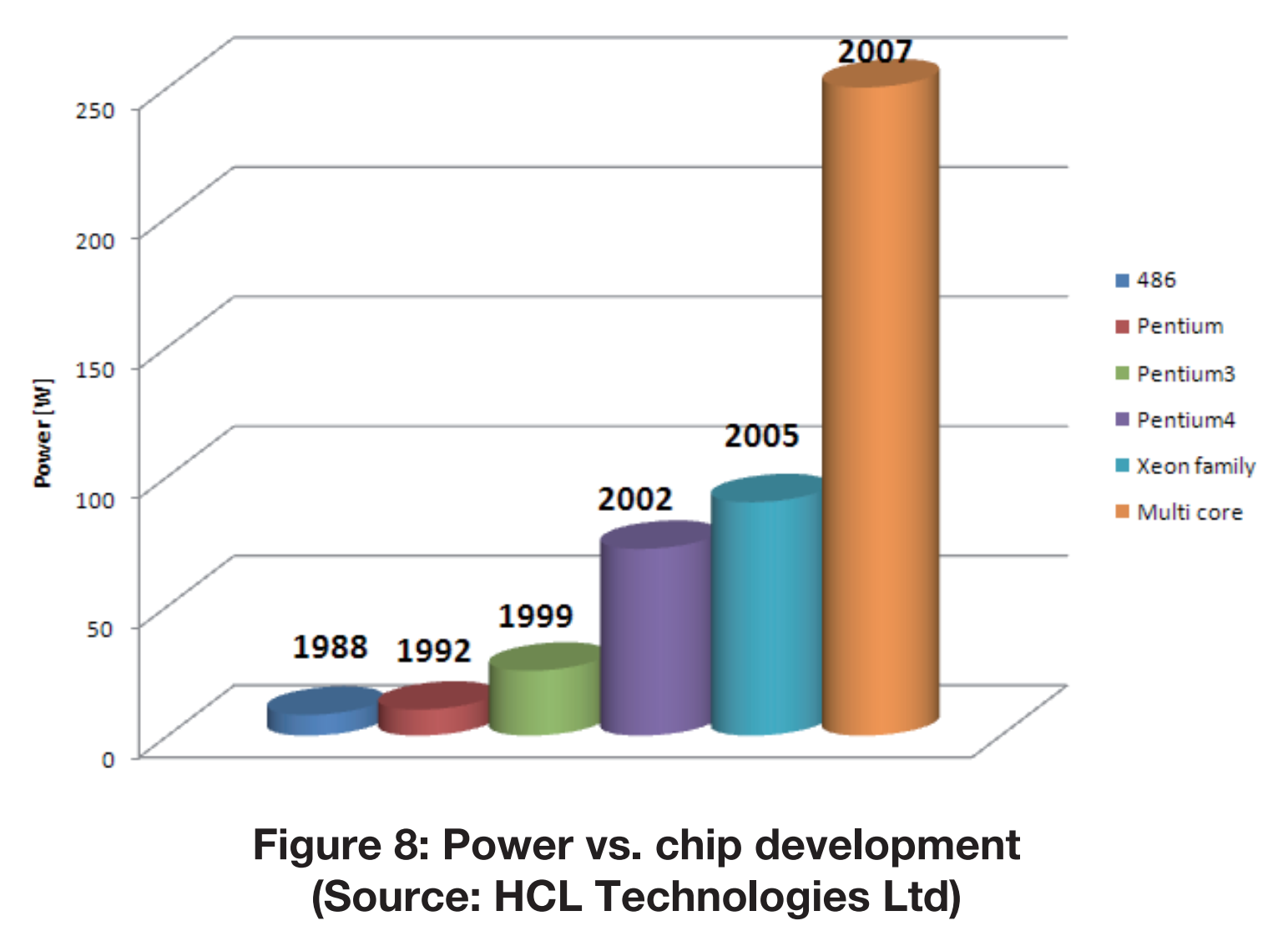
17 December 2020

*Manufacturing and Reliability Challenges of Advanced Packaging Technologies to Achieve Solutions Beyond Moore’s Rule*

# 1 Introduction

Annaporna Krishnaswamy, product marketing manager Ansys said, “Moore’s Law has served us extremely well so far, but there is a growing challenge of interconnect delays.”

The continual increasing performance of microelectronics products places a high demand on packaging technologies. Key drivers such as thermal management, power delivery, interconnect density, and integration require novel material development and new package architectures. This paper will talk about the package technology migrations for microprocessors and new package architecture. Moreover, material requirements for high thermal dissipation, high-speed signaling, and high-density interconnects will be discussed. Scaling of microprocessors for improved performance and reducing cost imposes significant challenges on power delivery, operating voltages and increasing power which can be seen in the figure below.



*Figure 1. Power vs. Chip Development*

Some of the factors that are tilting semiconductor industry towards advanced packaging technologies are as follows:

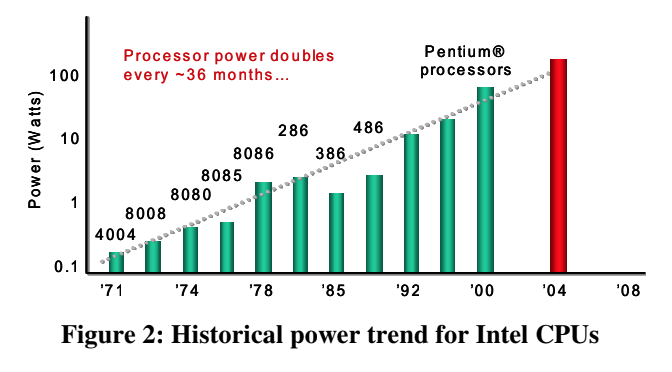
* Scaling rate of transistors is not the same as the scaling rate of a system on a chip interconnects and wires.
* Designing and manufacturing chips at new nodes is expensive.
* With an increasing number of transistors on chip, resistance and capacitance are increasing at each node, along with heat and noise.

Therefore, to meet these challenges , improvement in package substrate and advanced packaging solutions such as Bumpless Build Up Layer Technology and power delivery architectures such as On-Package Integrated Voltage Regulation used for increasing the power delivery capability of the packaging architecture should be implemented.

# 2 Power Delivery Considerations

Requirement of high end microprocessors to meet the demanded performance requires increased processor power. Scaling of microprocessors has resulted in increasing transistor density which places very stringent requirements on power integrity as the power density increases and the operating voltage decreases. The power integrity and product cost requirements cannot be met for high performance devices without chip/package/system co-design. Power delivery systems for processors such as Voltage Regulator Modules (VRMs) are used to supply power to chips to meet the increasing demand of electric currents. Power doubles approximately every 36 months which is half the pace of the increase in the number of transistors as forecasted by Moore’s Law[17] .This difference leads to greater amounts of memory content in microprocessors as they are scaled, leading to less overall capacitance contributing to power consumption and smaller die sizes. Sudden surges in current affects the power delivery system of a CPU in two principal ways:

1. Power consumption is lowered when the power saving feature of a CPU is activated. A sudden surge in current in a short duration is demanded when the state of the CPU changes to a fully operational mode.
2. Power loss occurs when large currents flow in the interconnect between VRMs and CPU.



*Figure 2: Power trend for Intel CPUs [17]*

## 2.1 Power Path Loop Inductance Scaling and Reduction

Series of supply voltage variations results in sudden surges of current or relaxation of current demanded by the CPU. These surges of current and relaxation of current are referred to as supply droops and overshoots[17]. The magnitude of these droops can be calculated as follows:

(1)

where and in equation (1) refer to the package

loop inductance and the die effective capacitance

Variation in refers to the droops and surges in voltage. The main challenge in minimizing these droops is imposed by scaling of package loop inductance to meet the demands of CPU scaling. This can be further written as :

(2)

and,

(3)

where is the package loop inductance in process-1 and is the same for the next-generation

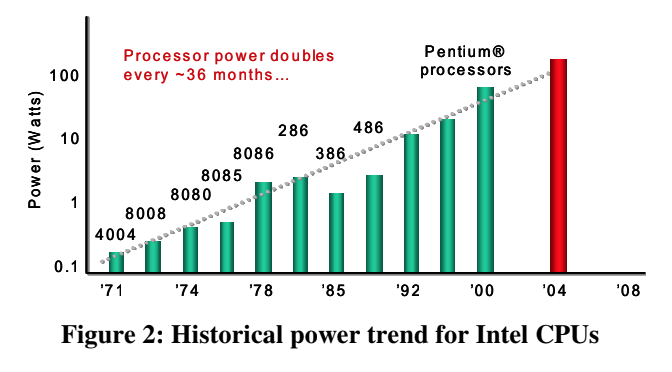
Process-2. Therefore , dividing the two equations, loop inductance scaling is obtained which is given as:

(4)

T hus, it can be concluded that the scaling factor for loop inductance directly depends upon capacitance scaling factor and operational frequency scaling factor .

## 2.2 Power Progression for CPUs

Figure 3 provides the historical data on increase in power requirements for modern microprocessors. From the figure, it can be seen that power doubles every 36 months which half the speed at which transistors are increasing. To meet the increasing power requirement for microprocessors, scaling is an available option and this results in less overall capacitance. From equation (1), it can be seen that droops depend on which are determined by the CPU architecture, circuit design and layout. But the droop in a damped resonant circuit is affected directly by effective loop inductancewhich is determined by components of assembly technology. Therefore, reducing the power loop inductance to control droop ratios as supply currents are increased is a key driver that leads to consideration of advanced packaging techniques such as Bumpless Build-Up Layer (BBUL) technique[17].



*Figure 3: Power trend for Intel CPUs [17]*

## 2.3 Power Series Resistance Scaling and reduction

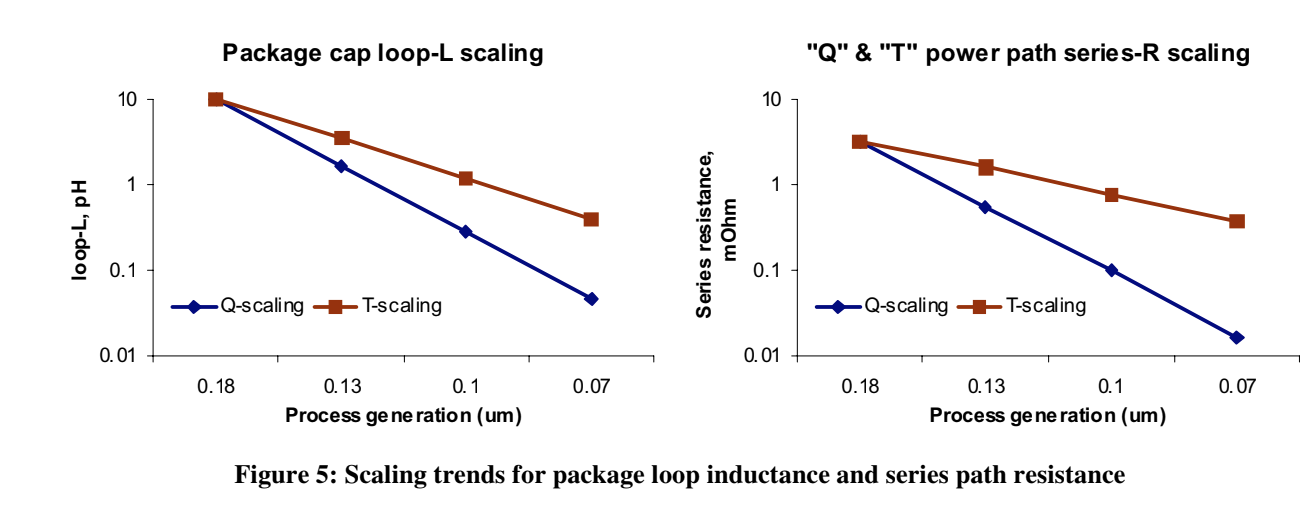
Power loss because of increased resistance leads to system inefficiency and heat generation within the microprocessor. Inorder to meet the demands of larger current values , microprocessors require greater number of pin counts in sockets and thicker copper wires. This results in greater challenges of arresting thickness reduction of metal layers within the substrate.

Therefore, to reduce the power loss because of increased resistance, the resistance is reduced by square of the current scaling factor. This scaling reduction of power decreases the heat generated in the interconnects[17].

(2)

where is the power interconnect resistance scaling

factor and is the current scaling factor.

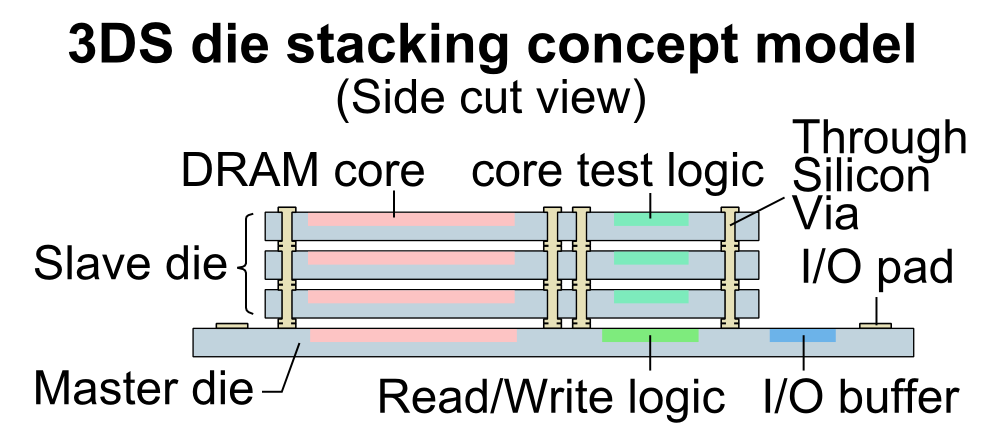


*Figure 4: Scaling trends for package loop inductance and series path resistance [17]*

Figure 4 demonstrates the challenge faced during scaling of assembly technology parameters as compared to microprocessor scaling . Thus, it is evident that new architectures satisfying increased power demands of the microprocessors are required.

## 2.4 3D Chip Stacking

Recently, 3D integration and packaging has been used successfully in order to increase logic density and reduce data-movement distances. Most memory devices involve some form of chip stacking, which will be critical in increasing the density of future devices. An example of chip stacking would be through the use of through-silicon vias (TSV). In this approach, holes are drilled through silicon chips to provide electrical connections between the stacked layers, and this allows for much higher bandwidth and energy efficiency than conventional chip packages such as ball grid arrays and other pin packages. The substantially reduced wire length decreases the wire resistance and capacitance. As a result, power as well as RC delay would drop proportionately, and this would result in a significant reduction in energy per operation [7]. This type of stacking technology provides substantial opportunity for deeper photolithographic layering and potentially orders of magnitude in improvement of component density in terms of increased functionality, memory capacity, as well as reduction in operating voltage. The following image is a model illustrating the architecture of 3D chip stacking with the use of through-silicon vias.



*Figure 5. 3D Die Stacking Model*

Although this technology does sound promising as a solution to the recent decline in the observation of Moore’s Law, they do come with their concerns and limitations. The primary challenges to scaling 3D photolithographic layering are improving defect tolerance, managing the thermal densities, and intrinsic resistance [8]. There is inevitably the risk of losing performance gain if the increased heat density leads to degraded performance. For circuits operating in saturation, the degradation of mobility with temperature tends to be the dominant effect, and each 10° C increase in operating temperature increases delay by almost 5%. This means that doubling the heat density without any improvement in cooling capacity will lead to more than a 30% degradation in performance [7]. Researchers are exploring applications, such as ones requiring large amounts of memory bandwidth like Automated Driving Systems. These types of applications tend to be very power hungry and the 3D chip stacking technology must demonstrate that the reduction in interconnect delay outweighs the increase in temperature delay.

# 3 Thermal Management

The continually increasing transistor density and voltage scaling caused by the power density of modern electronics to rise with each generation of innovative technology. This poses serious thermal management issues, especially for hand-held smartphones and wearable electronics because these types of devices are constrained by only passive convection. Therefore, the clock frequencies of the CPU’s in these types of devices are generally lower than that of larger electronics such as laptops and desktops where forced convection cooling is possible.

## 3.1 Current Trends

### 3.1.1 Heatsink with PCM Integration

Recently, the use of Phase Change Materials (PCM) has been emerging in various types of cooling applications aside from just the cooling of power electronics. These applications include the cooling of HVAC systems, spacecraft systems, missiles, battery cooling, and much more. Phase change materials are materials that store or release thermal energy by the phase change of the material because the latent heat from melting or freezing is at least one to two times the magnitude higher than the energy stored by the specific heat of the material. Currently, there is research being performed in order to find the most effective way to integrate Phase Change Materials to cooling systems for power electronics as well as to examine the potential thermal performance that Phase Change Materials may be able to bring in the electronics packaging industry.

A great potential for on-chip Phase Change Materials lies in the ability to reduce the peak chip temperature aside from just lowering the average chip temperature. Many existing and emerging mobile applications today, such as speech recognition and visual recognition, demand short bursts of intense computation separated by extended (at least tens of seconds) idle state waiting periods for user input [1]. This results in a CPU to run temporarily at a power density that is far beyond its sustainable thermal budget, and the chip would then be cooled down to its normal state. Phase Change Materials may be able to smooth out the thermal profile during these cases of pulsed operation, which would require a much less sophisticated cooling system for those types of power electronics.

There have been several prior experiments that were conducted in order to examine the thermal performance of a silicon thermal test-chip integrated with on-chip Phase Change Materials as a proxy for mobile chips. Many times, it was found that incorporating Phase Change Materials can either reduce peak and average chip temperatures, but the practical applicability of the measurement results is limited due the fact that the test chip is unable to perform any real computations. However, there was research performed by the University of Michigan that involved the use of realistic state-of-the-art accelerator test-chips (ATC) for deep learning [2]. Deep learning accelerator chips are generally used for intense applications such as the application of artificial intelligence and machine learning. These types of application depend heavily on the features of speed and facial recognition, which would result in frequent bursts of intense computation and temperature peaks as mentioned before. The accelerator test-chip designed by the University of Michigan actually outperformed the latest deep learning accelerators on other chips by using methods such as energy-efficient resonant clocking that optimizes area and power efficiency. Experiments with this accelerator test-chip design were performed for deeper investigation in the effectiveness of Phase Change Materials. When selected the Phase Chase Material to use, it was found that conventional Phase Change Materials such as paraffins and salt-hydrates were ineffective due to their inadequate thermal conductivities. The use of high thermal conductivity Phase Chase Materials such as metallic alloys were examined by placing them close to the heat source to attain a quick thermal response. The following figure illustrates experimental results by showing a graph of the temperature transient of the accelerate-test chip with and without the integration of the high thermal conductivity Phase Change Material. After creating simulations of temperature spikes that would occur in real world power electronics, temperatures were measured at the die, and the measurements suggested a promising 17% drop in die peak temperatures. These results show that the use of Phase Change Materials for CPU cooling can be explored and optimized further to manage heat-dissipation and improve the reliability.



*Figure 6: Temperature Transients With and Without PCM Integration [2]*

### 3.1.2 Thermoelectric Cooling

In power electronics, there are oftentimes areas, termed as “hotspots,” toward the center of CPU’s where the thermal density is significantly higher relative to the entire surface of the CPU. The heat flux at the hotspot location can be 2 to 5 times larger than the average heat flux [3]. Hotspots pose difficult challenges for thermal management because it forces electronic package designers to consider the inevitability of an uneven thermal profile. In other words, they need to consider the fact that heat transfer will not be the same at different points on the CPU. A technology that is currently being experimented with and has been growing popularity in the research scene is the thermoelectric cooler (TEC). Thermoelectric coolers work by using the heat flux and temperature differential created when a direct current is applied across two materials. This phenomenon allows heat to transfer from one side of the device to the opposite side. As shown in the following images, several P-N junctions are sandwiched between two thin ceramic wafers for rigidity and electrical insulation. Greater quantities of P-N junctions allows the thermoelectric cooler to have a greater cooling effect. Thermoelectric coolers can be useful in smaller applications such as power electronics, but are not very efficient for larger applications such as HVAC systems.

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*Figure 7. DC Current Applied to TEC*

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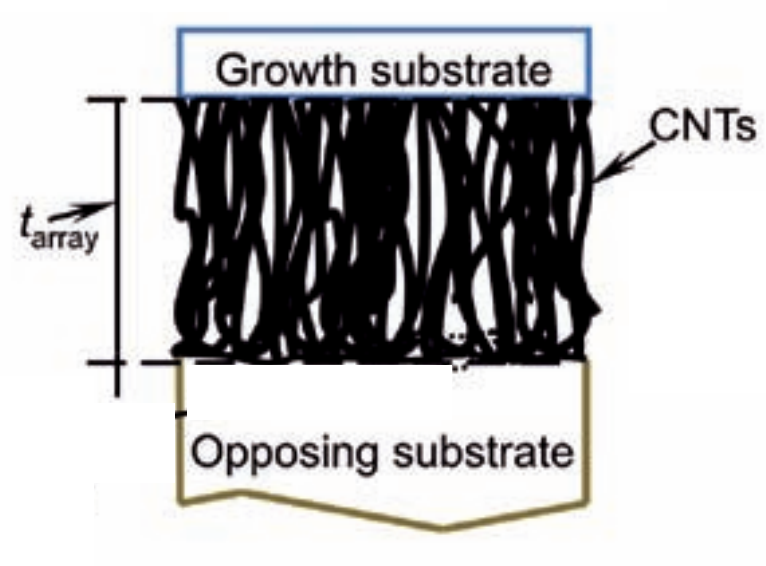
*Figure 8. Heat Transfer Path of TEC*

An experimental investigation of using thermoelectric cooling for hotspots in computer chips was performed at both low (10.8 W) and high (12.1 W) heat rates by the department of computer science and engineering at Jubail University College [4]. Their results showed that the hotspot temperature can be decreased for the low heat rate from 111.4 °C to 57.4 °C, which is a temperature reduction of 54.0 °C or 94%. For the high heat rate, the results showed that the hotspot temperature can be reduced from 138.8 °C to 77.7 °C, which is a reduction of 61.1 °C or 79%. The fact that there was a greater reduction for tests with lower initial heat rates is actually in agreement with other related studies. Furthermore, these results clearly suggest that investing in more time to experiment with thermoelectric cooling can be worthwhile for the development of a solution for CPU hotspots that may continue the trend of Moore’s Law and allow for continual innovation and performance increases in power electronics.

### 3.1.3 Carbon Nanotubes

One of the most significant problems with modern CPU’s is the efficient transfer of heat between the CPU cores and the heatsinks. This is because conventional thermal interface materials (TIM) are poor at conducting heat as well as spreading the heat across the surface of the computer chip. This essentially means that thermal energy is generally trapped at the top of CPU cores, and this creates hot spots on the die. However, carbon nanotubes (CNT) have recently been shown to possibly be very effective as a thermal interface material. Carbon Nanotubes are tubes made of carbon with diameters typically measured in nanometers. Single-wall carbon nanotubes are carbon nanotubes with a diameter in the range of a nanometer, and multi-wall carbon nanotubes consist of multiple nested single-wall carbon nanotubes. Carbon Nanotubes have been long known to have excellent electrical and thermal conductivity. They have continually been considered for applications ranging from electrical interconnects and field effect transistors to heat spreaders. It has been more than a decade since the experimental demonstration that the thermal conductivity of carbon nanotubes can exceed that of diamond, which has the highest thermal conductivity among naturally occurring materials [5].

To explain in more detail, carbon nanotubes are hexagonally shaped arrangements of carbon atoms that are constructed by rolling them into cylindrical tubes, and their diameters are as small as a few atoms wide. The most actively studied carbon nanotube array interface structure is the one-sided CNT array interface that consists of CNT’s directly grown on one substrate with the CNT free ends in contact with an opposing substrate. The following figures illustrate the construction of this type of carbon nanotube array interface. The numerous CNT contacts at both substrates form parallel heat flow paths within the framework of the thermal resistance network. Another type of configuration is the two-sided configuration, where CNT arrays are adhered to surfaces on both sides of the interface and are brought together like Velcro. The CNT’s are mechanically entangled and are attached to each other by van der Waals forces.



*Figure 9. One-Sided Carbon Nanotube Array Interface [6]*

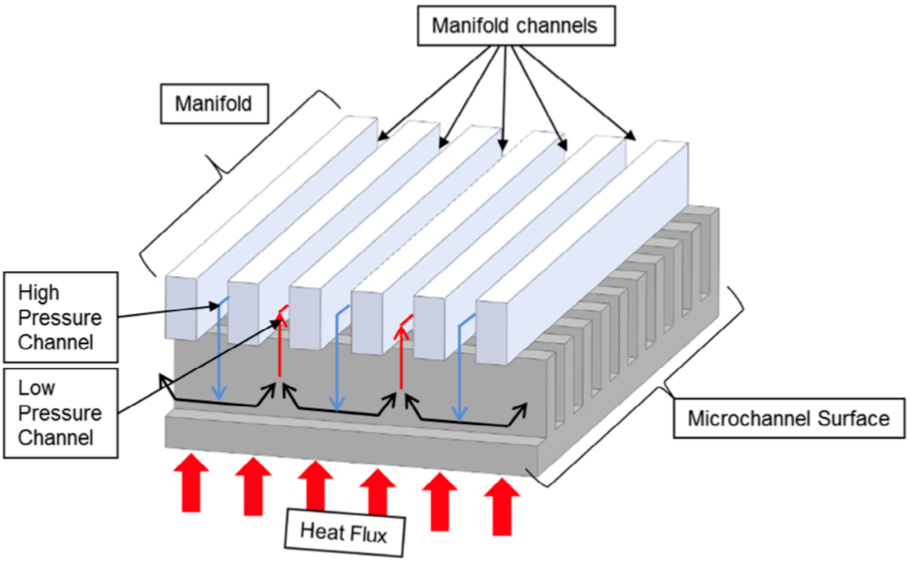


*Figure 10. Two-Sided Carbon Nanotube Array Interface [6]*

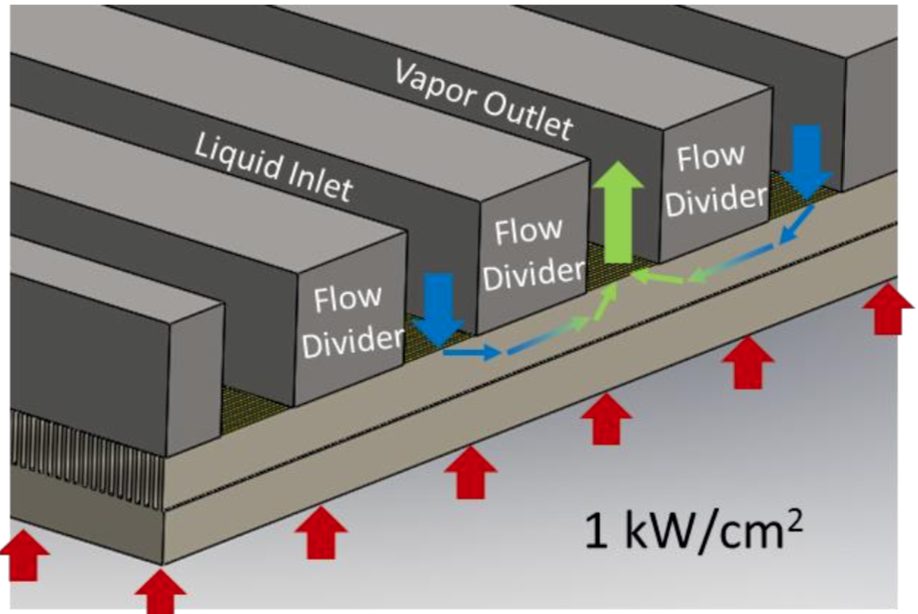
The experiments performed by Cola of the Georgia Institute of Technology showed that one-sided interfaces achieved thermal resistances as low as 7 mm2K/W and that two-sided interfaces achieved thermal resistances as low as 4 mm2K/W, which is comparable to the resistance of a soldered interface [6]. Further improvements can be achieved by optimizing the contact area of CNT arrays. Experimental data and theoretical predictions reveal that the resistances of CNT-substrate contacts severely limit the potential of CNT array thermal interface materials. Improvements in bonding and heat transfer at these contacts can lead to substantial reductions in thermal resistance, approaching estimated theoretical limits of ~0.1 mm2K/W.

### 3.1.4 Manifold Microchannel Heat Exchangers

Microchannels are channels for the movement and heat transfer of fluids. The width or diameter of a microchannel is below 1 mm, and microchannels are usually applied in micro-scaled heat exchangers. Manifold microchannels (MMC) are arrangements of flow channels so that the flow can be distributed with a high number of passes as well as maximize the total surface area of convection. At the same time, manifold microchannels also allow for the minimization of pressure drop across the heat exchanger. The following figure shows a three-dimensional image of an example of how manifold microchannels can be integrated to a CPU heat sink. The technology of manifold microchannels have been around for a while now and is currently still being researched and developed around the world with promises to bring innovation for high performance cooling of power electronics.



*Figure 11. Manifold Microchannel Heat Sink [9]*



*Figure 12. Flow Path of Manifold Microchannel*

The flow path of the particular manifold microchannel in the previous figure uses a novel flow distribution mechanism called fractal flow, which is essentially a tree-like branching of the flow. This is one to provide an effective flow distribution in microchannel heat sinks or heat exchangers [9]. Kim et al. compared a manifold microchannel heat sink with a traditional heat sink using air as the heat transfer fluid. The study reports a 35% decrease in thermal resistance for a manifold microchannel heat sink as compared to a traditional heat sink [10].

## 3.2 Reliability

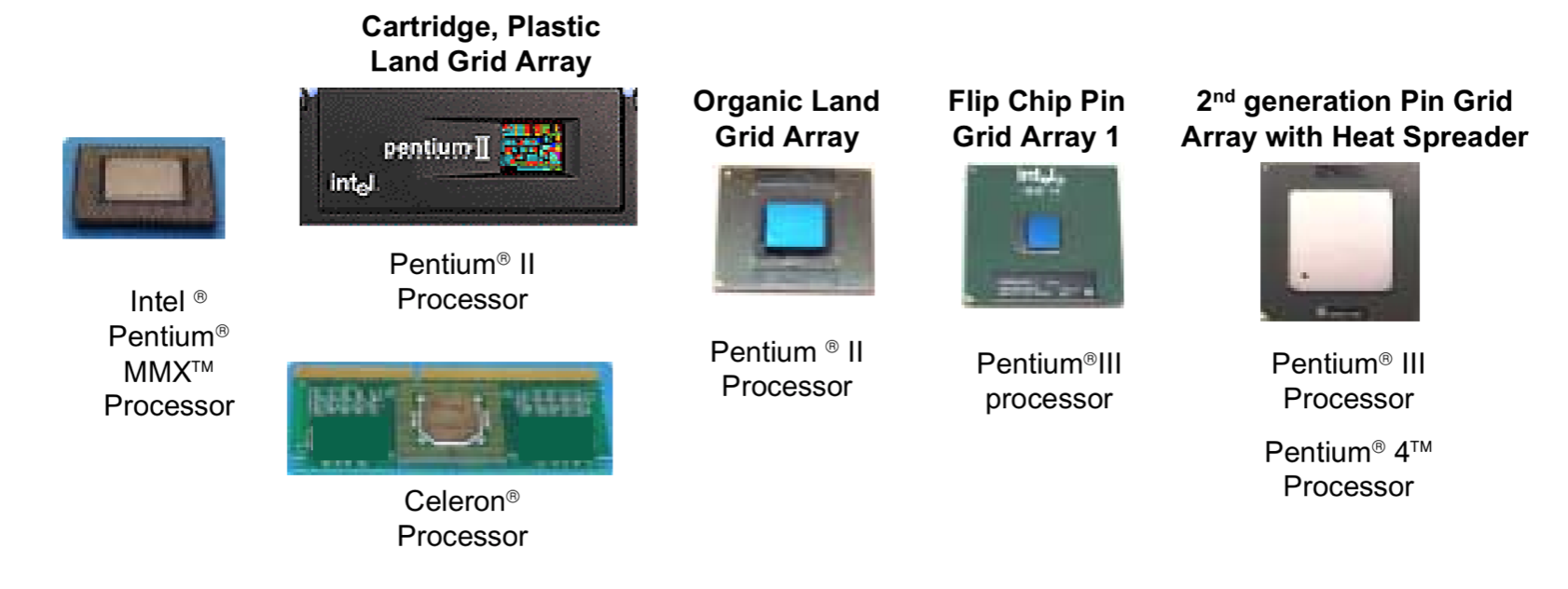
It is clear that the various emerging technologies regarding thermal management are bringing optimism to the continual growth of electronics performance, but there are also reliability concerns to be considered. For example, in the case of Phase Change Material integration to CPU coolers, the selection of the Phase Change Material is imperative. As previously mentioned, conventional Phase Change Materials, such as paraffins and salt-hydrates, become ineffective due to their low thermal conductivity [1]. A Phase Change Material with a sufficient thermal conductivity must be selected, but this poses its own challenge in that the cost of the Phase Change Material may become too great to be considered practical for the commercialization of a CPU cooler integrated with this Phase Change Material selection.

As for thermoelectric coolers, the main concern is achieving a reasonable efficiency. This can only be done for high heat load applications because efficiency decreases with lower heat load applications. Therefore, in order to implement thermoelectric coolers for CPU cooling, the designer must confirm and ensure that the thermoelectric cooler is integrated to a high-power CPU so that the application is a sensible one. Commercial thermoelectric coolers are typically designed to maximize the cooling of high-heat load (>1 W/cm2) conditions and for low thermally resistive environments [11]. If a reasonable efficiency is not met, then this results in efficient power consumption because a thermoelectric cooler works by inducing an electric current. This case would truly not be ideal and must be considered in order to be avoided.

It is important to note that not all carbon nanotube array thermal interface materials are not created equal. Therefore, performance can vary greatly depending on many factors such as array density, array height, tube diameter, quality, as well as the adhesion of the carbon nanotubes [6]. In particular, experimental data and theoretical predictions have revealed that the resistances of the contacts between the carbon nanotubes and the substrates can severely limit the potential of carbon nanotube array thermal interface materials. Therefore, there will have to be careful attention towards improving bonding and thermal transport at these contacts so that there can be substantial decrease in resistance.

# 4 Construction and Packaging

The last two decades witnessed significant changes in package substrate technology. Transitioning from ceramic to organic substrate occurred as ceramic substrates suffered greatly from disadvantages such as high dielectric constants, thick dielectric layer, poor conducting materials and limitations on feature size. Organic substrates on the other hand are cheaper and more efficient. With increasing number of microprocessors on a chip, several challenges are imposed on the performance of a substrate and are driven by the following technology drivers:



*Figure 13. Substrate Evolution[17]*

1. Feature size reduction to increase routing density: A reduction in feature size of the substrate requires new processes and process materials such as better photoresist and solder mask materials. Reduction in feature size results in reduction of interconnect width, micro via diameter, flip-chip bump pad pitch.
2. Increased Performance: New materials having low dielectric constant and low loss tangents are required by future high speed microprocessors. High speed signals are also driven by impedance matching and impedance control which are directly related to dielectric thickness of the material.
3. Increase in Mechanical Loading: Better performing microprocessors dissipate greater amounts of power and therefore, require larger and heavier heat sinks. Heat sinks are attached to the package by contact material known as Thermal Interface Material. These contact surfaces are clamped together with large static and dynamic loads on the package. Migration to Land Grid Array sockets and implementation of Inner Dielectric Layer imposes higher static loading on the substrate. Therefore, development of new class of next generation substrate materials are required to withstand the stresses while maintaining thermo-mechanical reliability of the system.
4. Lower Cost: Future substrate costs must be reduced to ensure competitiveness in the market. But the prices of substrates are increasing with an increased number of transistors on a chip providing higher performance to meet the future standards.

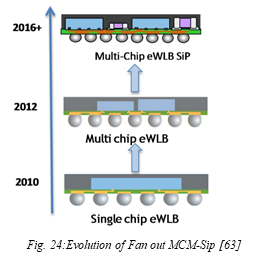
## 4.2 Current Trends

### 4.2.1 Silicon Interconnect Fabric

As time progresses, the demand for smaller and more portable electronics is increasing, which poses difficult challenges in design. A major barrier in decreasing size for electronic devices is associated with the printed circuit board (PCB), and researchers have been searching for a way to remove its necessity for a while now. Recently, research findings showed that printed circuit boards could potentially be replaced with the material that makes up the computer chips that are attached to it, which is silicon. This is known as silicon interconnect fabric, which is a technology that consists of only silicon, and this technology allows computer chips to connect directly to a wiring on a separate piece of silicon [12]. Unlike connections on a printed circuit board, the wiring between the chip and the fabric is as small as the wiring within a chip. With this, many more chip-to-chip connections are possible, and this also brings advantages of faster data transmission and less energy consumption. Silicon interconnect fabric also holds the potential of easier manufacturing because it would actually be more simpler in design than the conventional chip-to-PCB construction that is used for most applications today such as smartphones and supercomputers. This revolution is currently underway with research being performed by major semiconductor companies such as AMD, Intel, and NVIDIA.

### 4.2.2 Fan Out Packaging

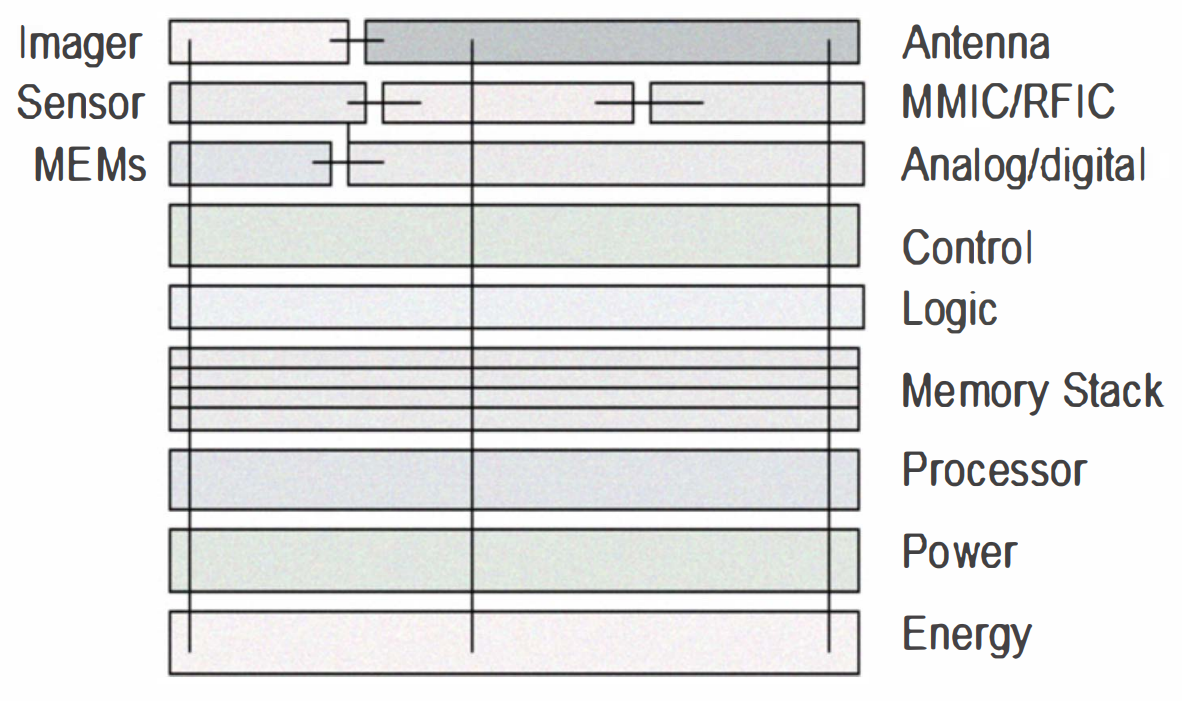
Another technology that calls for miniaturization is embedded die technology. This is different from most integrated circuit package types where the devices are situated on top of a substrate, and the substrate serves as a bridge between the device and the board of a system. Embedded die packaging involves embedding components inside the substrate using a multi-step manufacturing process [13]. One approach to embedded die technology is fan-out wafer level packaging (FOWLP), where dies are embedded into polymer encapsulants and 3D vertical integration. In other words, dies are embedded into the printed circuit boards. There are two methods to fabricating fan-out wafer level packages. First method is the “mold first” method where it starts with the die assembly on an intermediate carrier followed by overmolding and debonding the molded wafer from the carrier. Fan-out wafer level packaging involves dicing the wafer into chips and embedding these chips into a low cost material such as epoxy molding compound. The dicing of wafer is followed by application of a redistribution layer on the glass or silicon substrate, which provides more room to attach solder balls .The design flexibility of this method allows for integration of multiple dies and passives and is becoming an attractive solution for thinner profile and higher level of integration packages in a wide range of applications. Figure 14 shows the evolution for FOWLP. Also, Fan-Out Wafer Level Packaging has a high potential in significant package miniaturization concerning thickness. Main advantages of FOWLP include substrate-less packaging, lower thermal resistance, and higher performance due to shorter interconnects along with direct integrated circuit connection by thin film metallization instead of wire bonds or flip chip bumps. The inductance of the FOWLP is much lower compared to FC-BGA packages, making it ideally suited for radio frequency applications. Furthermore, it can be used for multi-chip packages for System in Package (SiP) and heterogeneous integration [13].



*Figure 14. Evolution of Fan-Out Wafer Level Packaging[22]*

### 4.2.3 3D Integration

Another term for electronic devices of smaller dimensions that are gaining in demand as time progresses is known as small form factor (SFF) microsystem technologies. At this point, it is an accepted view that the increased performance and functionality of these demands can only be achieved by using the third dimension. There are many approaches to 3D integration, including 3D-monolithic IC integration, 3D stacking of IC dies, and 3D integrated packaging [15]. These are all examples where the third dimension can be included in the electronics package design process for decreasing the package size while maintaining the performance demanded by electronic devices that are designed and manufactured today. Not only that, 3D integration holds the potential to improve cost and performance due to decreased connection lengths and decreased feature sizes [16]. A concept of a 3D microsystem integration is shown in the following figure.



*Figure 15. 3D Microsystem Integration Concept [15]*

## 4.3 Reliability Issues

### 4.3.1 Reliability Issues in Silicon Interconnect Fabric

1. Metal-Metal Interconnect: To achieve high-interconnect densities and small inter-dielet distances Chip-to-wafer metal-metal thermal compression bonding is selected as the main die attach technology[19]. Use of solder materials are eliminated which in turn inhibits formation of intermetallic compounds responsible for joint failures under thermal loading. To reduce failures due to loading, this technology uses similar materials at the interface. To prevent oxidation of Cu-Cu bond at elevated temperatures a pre-bonding cleaning process is implemented for reliable metal-metal bond[20].
2. Passivation: Conventional underfill materials cannot be used as Si-If approach requires tight pitches. Parylene known for its good moisture barrier is used for conformal coating in passivation[19].Therefore, to evaluate long term stability of Parylene coating on the substrate thermal cycling and high temperature storage tests should be performed.

### 4.3.2 Reliability Issues in Fan-Out Packaging

1. Molding Compound CTE mismatch and curing stress: Large CTE mismatch between semiconductor chip and molding compound results in generation of thermo mechanical stresses during the curing process[19].The CTE mismatch arises because of rigid molding compounds being used as base material. The stresses are reduced by increasing the ratio of filler particles to molding compounds. This increases Young’s modulus of the material while coefficient of thermal expansions decreases.
2. Die shift: Shrinking of rigid-molding compounds during the curing process results in several alignments issues giving rise to die shift. New materials with lower shrinking properties are being researched to replace the rigid-molding compounds[19]. Studies have shown that adaptive lithographic processes tend to reduce misalignment substantially.
3. Moisture ingression and salt intrusion: Medically graded silicon a flexible biocompatible substrate is known for its moisture ingression and salt intrusion properties which leads to reliability concerns for implantable electronics[19]. Therefore, poor adhesion between chips and Medically graded silicon can lead to delamination which causes corrosion in metal structures due to moisture ingression and salt intrusion.For biomedical applications, saline immersion tests are used for short or long-term qualification.

### 4.3.3 Reliability Issues in 3D Integration

1. Micro-bump technology: Copper pillars capped with a thin solder layer form the micro bumps used for interconnections between the stacked dies. Chips are mounted in a flip-chip fashion through a thermal compression bonding process[19]. This process exerts enough pressure to keep the die flat against the mounting substrate which is subjected to various reliability issues. Excess pressure can damage the solder at the joining interfaces and may result in fatigue cracks during thermal loading.
2. Passivation and moisture ingress: The package is passivated using an organic silicon based material. Medically graded silicon a flexible biocompatible substrate is known for its moisture ingression which leads to reliability concerns for implantable electronics[19]. If the passivation layer shows signs of poor adhesion, it might lead to water vapor condensing at the interface leading to corrosion of the underlying metal structures and severe reliability problems.
3. Electromigration: Electromigration a well-known reliability concern in the soldered contacts. Solder material may migrate due to high electrical current densities at the edge of the bumps leading to formation of voids. At elevated temperatures, voiding effect increases significantly as electromigration is further superimposed by thermo migration[21]. Using intermetallic to reduce electromigration is a viable solution but it comes with another drawback. Intermetallics are brittle in nature which enhances other failures modes such as cracking.

# 5 Conclusion

Although the challenges are growing to maintain a steady increase in advancements for electronics packaging, the numerous efforts being made to achieve technological breakthroughs look promising for the future. With efficient and high performing power delivery methods, careful considerations for thermal management, as well as novel packaging constructions, it seems that combinations of these can allow for the dimensional decrease as well as higher clock speeds in comparison to the convection integrated circuits that are being manufactured today. Heat sinks with PCM integration may be able to decrease thermal peak loads to allow the management of a more smooth and consistent thermal profile, while thermoelectric cooling may be able to mitigate the issues related to hotspots located at the core of central processing units. Material choices such as carbon nanotubes can also increase the performance of heat transfer, and the use of manifold microchannels is an example of how the mechanical aspects can be optimized for higher thermal efficiency. In this paper, current and emerging trends of the construction and packaging aspects were also examined. It was discovered that the use of Silicon Interconnect Fabric, an all-silicon material that can be used for removing the necessity of a printed circuit board, can allow for more chip-to-chip connections as well as faster data transmission and less energy consumption. Other packaging methods fan-out wafer level packaging hold the potential of significant packaging miniaturization with substrate-less packaging. The most promising may be the use of 3D integration, which may be one of best ways to improve cost and performance due to decreased connection lengths and feature sizes by utilizing the third dimension during the design process.

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